

### Features

- Frequency range : 1.25MHz to 170MHz
- SMD seam sealing ceramic package
- Supply voltage : 3.3V
- CMOS output
- Fundamental solution
- Low phase noise and phase jitter
- Tri-state function available
- External dimensions (mm)  
L : 7.0 x W : 5.0 x H : 1.4
- RoHS compliant & Pb free

### Applications

- Wireless communications, Smallcell, Base station
- Fibre channel, SONET, SDH, Ethernet
- Set-top box (STB)
- xDSL, VoIP, Cable modem
- Digital TV, Digital audio
- Phase-locked loop (PLL) circuits

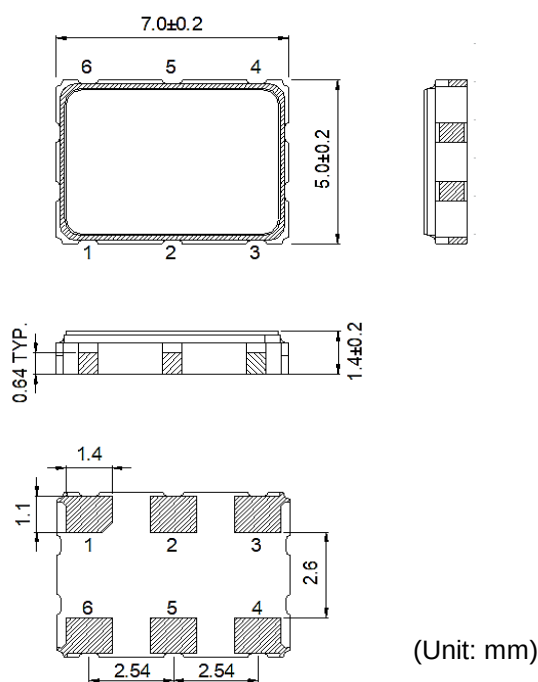
### Electrical Characteristics

| Item                                      | QTV750            | Conditions                |
|-------------------------------------------|-------------------|---------------------------|
| Frequency Range ( $F_0$ )                 | 1.25MHz ~ 170MHz  |                           |
| Operating Temperature Range ( $T_{OTR}$ ) | -40°C ~ +85°C     |                           |
|                                           | -40°C ~ +105°C    |                           |
| Supply Voltage ( $V_{DD}$ )               | 3.3 V             | $V_{DD} \pm 10\%$         |
| Current Consumption ( $I_{DD}$ )          | 30 mA Max.        |                           |
| Output Type                               | CMOS              |                           |
| Output Load ( $C_L$ )                     | 15 pF             |                           |
| Output Voltage High ( $V_{OH}$ )          | 90% $V_{DD}$ Min. |                           |
| Output Voltage Low ( $V_{OL}$ )           | 10% $V_{DD}$ Max. |                           |
| Rise & Fall Time ( $T_r / T_f$ )          | 5 ns Max.         | 10% ~ 90% of output swing |
| Duty Cycle                                | 45% ~ 55%         |                           |
| Start-up Time                             | 10 ms Max.        |                           |
| Enable Voltage High, Logic "1"            | 70% VDD Min.      | Input to Pin2<br>Note [1] |
| Enable Voltage Low, Logic "0"             | 30% VDD Max.      |                           |
| Absolute Pulling Range (APR)              | $\pm 50$ ppm Min. | Note [2]                  |
| Control Voltage Range                     | 0V ~ 3.3V         | Nominal 1.65V             |
| Linearity                                 | 10% Max.          |                           |
| Phase Noise ( $F_0 = 122.88$ MHz)         | -128 dBc/Hz Typ.  | at 1kHz offset            |
| Phase Jitter ( $F_0 = 122.88$ MHz)        | 50 fs Typ.        | 12kHz ~ 20MHz, RMS        |
| Storage Temperature Range ( $T_{STR}$ )   | -55°C ~ +125°C    |                           |

### Notes:

- [1] Output will be enabled if Pin2 is Logic "1" or open; Output will be disabled if Pin2 is Logic "0".
- [2] Absolute Pulling Range (APR) = Pulling Range - (Frequency tolerance at 25°C, variations over temperature, supply voltage, and aging).

### Dimensions

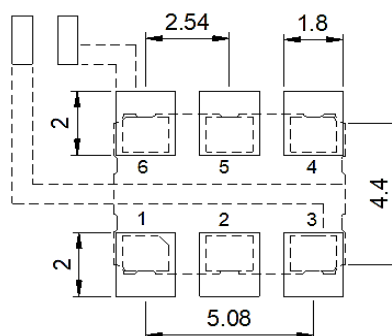


\* Pad dimension tolerance is  $\pm 0.2$ mm

### Pin function

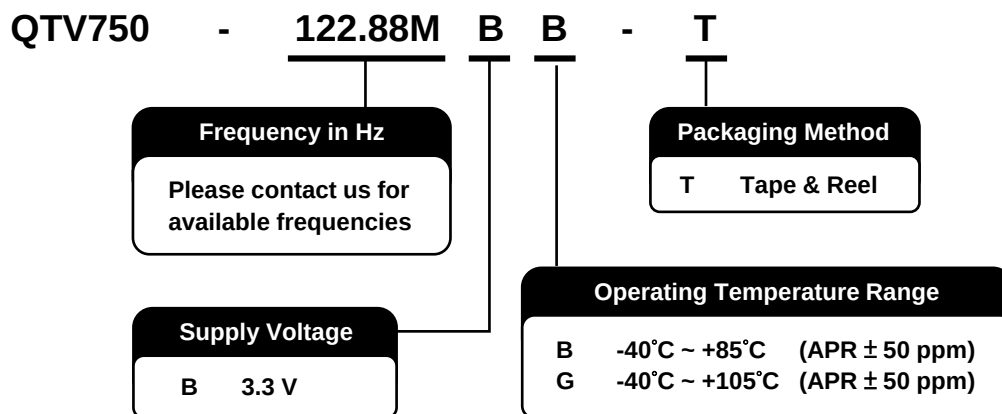
|       |                 |
|-------|-----------------|
| Pin 1 | VC              |
| Pin 2 | OE              |
| Pin 3 | GND             |
| Pin 4 | OUT             |
| Pin 5 | NC              |
| Pin 6 | V <sub>DD</sub> |

### Recommended pad layout

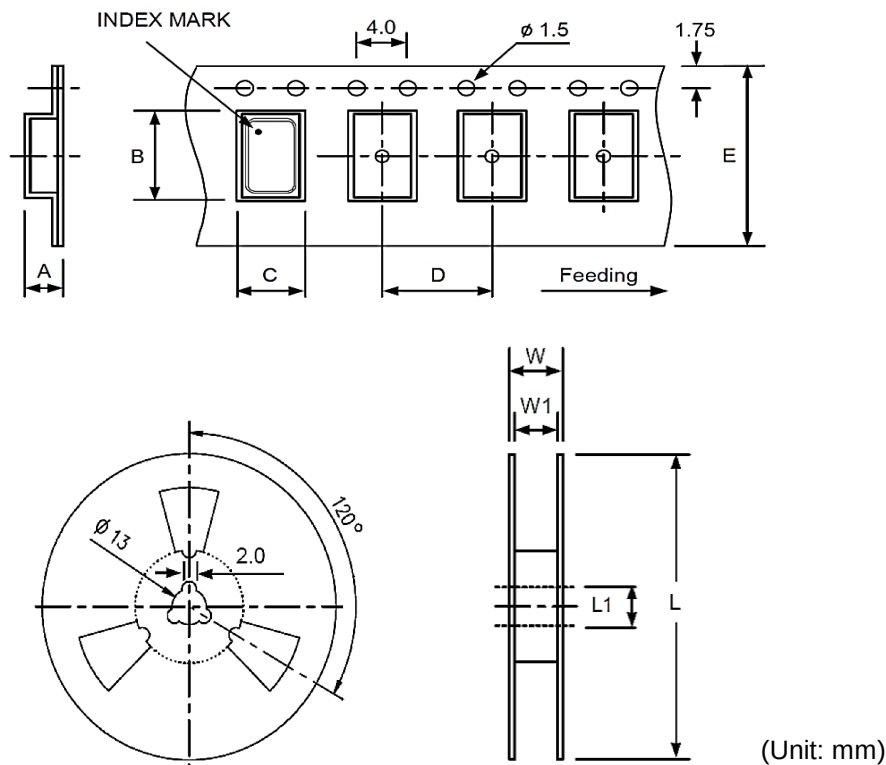


\* Power supply decoupling capacitor is required.

### Ordering Information



### Packing

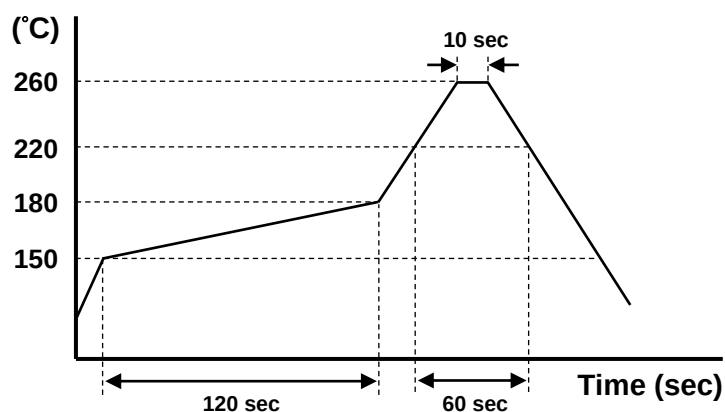


| DIMENSIONS | A    | B    | C    | D    | E    | L     | L1   | W    | W1   |
|------------|------|------|------|------|------|-------|------|------|------|
|            | 2.00 | 7.90 | 5.45 | 8.00 | 16.0 | 180.0 | 13.0 | 20.5 | 16.0 |

### Reflow Profile

Solder melting point :  $220^{\circ}\text{C} \pm 10^{\circ}\text{C}$ , 60 sec. Min., 200 sec. Max.

Peak temperature :  $260^{\circ}\text{C} \pm 10^{\circ}\text{C}$ , 10 sec. Min., 30 sec. Max.



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