RFMD2081
45MHz to 2.7GHz IQ MODULATOR with SYNTHESIZER & VCO

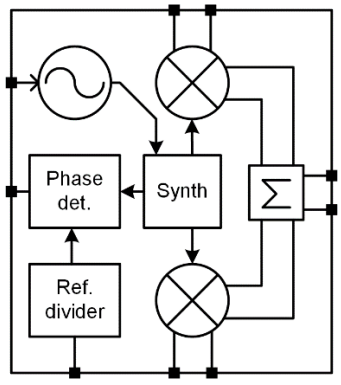
Product Overview

The RFMD2081 is a low power wideband IQ modulator with integrated Fractional-N synthesizer and voltage-controlled oscillator (VCO). The modulator features an input 3dB bandwidth of 100MHz and can generate output frequency between 45MHz and 2.7GHz. It is suitable for a wide range of applications.

The fractional-N synthesizer takes advantage of an advanced sigma-delta architecture that delivers ultra-fine step sizes and low spurious products. The synthesizer & VCO combined with an external loop filter allows the user to generate local oscillator (LO) signal from 90MHz to 5400MHz. The LO signal is buffered and routed to a high accuracy quadrature divider (/2) that drives the balanced I and Q mixers. The output of the mixers is summed and applied to a differential RF output stage. This device also features a differential input for an external VCO or LO source.

Device programming is achieved via a simple 3-wire serial interface. In addition, a unique programming mode allows up to four devices to be controlled from a common serial bus. This eliminates the need for separate chip-select control lines between each device and the host controller. The device provides up to six general purpose outputs, which can be used to access internal signals (the LOCK signal, for example) or to control front end components. The RFMD2081 is optimized for low power operation, consuming typically only 135mA from a 3V DC supply.

Functional Block Diagram



Functional Block Diagram – Simplified

Package: QFN, 32-Pin, 5mm x 5mm

Key Features

- 45 MHz to 2.7 GHz RF Output Frequency
- Very Low Spurious Fractional-N Synthesizer
- 1.5 Hz Resolution, Typical
- Fully Integrated Wideband VCOs and LO Buffers
- < 0.2° RMS Integrated Phase Noise at 1.0 GHz
- -40dBc Unadjusted Carrier Suppression
- -45dBc Unadjusted Sideband Suppression
- 100MHz 3dB Bandwidth of Baseband Input
- -162dBm/Hz Typical, Very Low Noise Floor
- +4dBm Output P1dB
- +17dBm Output IP3
- +2.7 V to +3.3 V DC Power Supply
- 135mA Typical Current Consumption
- Serial Programming Interface

Applications

- Satellite Communications
- QPSK/QAM Modulators
- Wireless Broadband
- Point-to-Point
- Software Defined Radios

Ordering Information

Part No.	Description
RFMD2081TR13	2,500 Pieces on a 13” reel
DKMD2081	Complete Design Kit in a box

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−65°C to +150°C
Supply Voltage (VDD)	−0.5V to +3.6V
Input Voltage (V_{IN}) on any pin	−0.3V to VDD +0.3V
LO Input Power	+15dBm

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Device Voltage (VDD)	+2.7	+3.0	+3.3	V
T_{CASE} (Bottom GND Paddle)	−40		+85	°C
Junction Temperature (T_J)			+125	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications (1)

Parameter	Condition	Min	Typ.	Max	Units
Logic Inputs/Outputs (VDD = Supply to DIG_VDD pin)					
Logic Low Input Voltage, V_{IL}		-0.3		+0.5	V
Logic High Input Voltage, V_{IH}		VDD / 1.5		VDD	V
Logic Low Input Current, I_{IL}	V_{IL} = 0 V	-10		+10	µA
Logic High Input Current, I_{IH}	V_{IH} = VDD	-10		+10	µA
Logic Low Output Voltage, V_{OL}		0		0.2*VDD	V
Logic High Output Voltage, V_{OH}		0.8*VDD		VDD	V
Logic Input Pin Resistance		10			kΩ
Logic Input Pin Capacitance				20	pF
GPO Drive Capability					
Sink Current	V_{OL} = +0.6 V		20		mA
Source Current	V_{OH} = +2.4 V		20		mA
Output Impedance			25		Ω
Static States					
Supply Current (IDD)	1.3V DC Bias on IQ Inputs		135		mA
Standby	Reference oscillator and bandgap only			2	mA
Power Down Current	ENBL = 0; REFSTBY = 0 (Register 03h bit 3)			300	µA
Module Thermal					
Thermal Resistance (R_{TH})	Junction to Case (Bottom Exposed Paddle)		30		°C/W
Modulator (output with 4:1 balun)					
I & Q Input 3dB Bandwidth			100		MHz
I & Q Modulation Input Voltage	Differential with 1.3V Input DC Bias		1		Vp-p
Output Power			-4		dBm
Output Noise Floor	At 10MHz offset with 1.3V Input DC Bias		-162		dBm/Hz
Output IP3	1.3V Input DC Bias		+17		dBm
Output P1dB			+4		dBm
Carrier Suppression	Unadjusted		-40		dBc
	Input DC Bias Offset Adjusted		-50		dBc
Sideband Suppression	Unadjusted		-40		dBc
Output Port Carrier Frequency		45		2700	MHz

Electrical Specifications (2)

Parameter	Condition	Min	Typ	Max	Units
Frequency Reference					
External Reference Frequency		10		104	MHz
Reference Divider Ratio		1		7	-
External Reference Input Level	AC coupled	500	800	1500	mV_{P-P}
Synthesizer (PLL Locked; 52 MHz reference)					
Synthesizer Output Frequency		90		5400	MHz
Phase Detector Frequency				52	MHz
Phase Noise (LO = 1 GHz)	10kHz offset		-108		dBc/Hz
	100kHz offset		-108		dBc/Hz
	1MHz offset		-135		dBc/Hz
	RMS integrated from 1KHz to 40MHz		0.19		Deg
Phase Noise (LO = 2 GHz)	10kHz offset		-102		dBc/Hz
	100kHz offset		-102		dBc/Hz
	1MHz offset		-130		dBc/Hz
	RMS integrated from 1KHz to 40MHz		0.32		Deg
Normalized Phase Noise Floor	Measured at 20KHz to 30KHz offset		-214		dBc/Hz
Voltage Controlled Oscillator					
Open Loop Phase Noise at 1MHz offset					
2.5GHz LO Frequency	VCO3, LO Divided by 2		-134		dBc/Hz
2.0GHz LO Frequency	VCO2, LO Divided by 2		-135		dBc/Hz
1.5GHz LO Frequency	VCO1, LO Divided by 2		-136		dBc/Hz
Open Loop Phase Noise at 10MHz offset					
2.5GHz LO Frequency	VCO3, LO Divided by 2		-149		dBc/Hz
2.0GHz LO Frequency	VCO2, LO Divided by 2		-150		dBc/Hz
1.5GHz LO Frequency	VCO1, LO Divided by 2		-151		dBc/Hz
External LO Input					
LO Input Frequency		90		5400	MHz
External LO Input Level	Driven from 50Ω Source via a 1:1 Balun		0		dBm

Theory of Operation

The RFMD2081 is a wideband IQ modulator with integrated fractional-N synthesizer and a low noise VCO core. It features a high accuracy LO quadrature divider followed by buffer circuits which drive the I and Q mixers of the modulator with the quadrature LO signals. The RFMD2081 has an integrated voltage reference and low drop out regulators supplying critical circuit blocks such as the VCOs and synthesizer. Synthesizer programming, device configuration and control are achieved through a mixture of hardware and software controls. All on-chip registers are programmable through a simple three-wire serial interface.

VCO

The VCO core in the RFMD2081 consists of three VCOs which, in conjunction with the integrated LO dividers of 1 to 32, cover the frequency range of 90MHz to 5400MHz. The modulator quadrature divider provides a further fixed divide by two to give the center frequency range at the modulator output of 45MHz to 2700MHz.

Each VCO has 128 overlapping bands which are used to achieve low VCO Gain and optimal phase noise performance across the whole tuning range. The chip automatically selects the correct VCO (VCO auto select) and the correct VCO band (VCO coarse tuning) to generate the desired LO frequency based on the values programmed into the PLL1 and PLL2 registers banks.

The VCO auto select and VCO coarse tuning are triggered every time ENBL is taken high, or if the PLL re-lock self-clearing bit is programmed high. Once the correct VCO and band have been selected the PLL will lock onto the correct frequency. During the band selection process, fixed capacitance elements are progressively connected to the VCO resonant circuit until the VCO is oscillating approximately at the correct frequency. The output of this band selection, CT_CAL, is made available in the readback register. A value of 127 or 0 in this register indicates that the coarse tuning was unsuccessful, and this will also be indicated by the CT_FAILED flag available in the read-back register. A CT_CAL value between 1 and 126 indicates a successful calibration, the actual value being dependent on the desired frequency as well as process variation for a particular device.

The band select process will center the VCO tuning voltage at about 0.8 V, compensating for manufacturing tolerances and process variation as well as environmental factors including temperature. In applications where the device is left enabled at the same LO frequency for some time it is recommended that automatic band selection be performed for every 30°C change in temperature. This assumes an active loop filter.

The RFMD2081 features a differential LO input to allow the mixer to be driven from an external LO source. The fractional-N PLL can be used with an external VCO driven into this LO input, which may be useful to reduce phase noise in some applications. This may also require an external Op-Amp, dependent on the tuning voltage required by the external VCO.

Fractional-N PLL (1)

The RFMD2081 contains a charge pump based fractional-N phase locked loop (PLL) for controlling the three VCOs. The PLL includes automatic calibration systems to counteract the effects of process and environmental variations, ensuring repeatable loop response and phase noise performance. As well as the VCO auto select and coarse tuning, there is a loop filter calibration mechanism which can be enabled if required. This operates by adjusting the charge pump current to maintain loop bandwidth. This can be useful for applications where the LO is tuned over a wide frequency range.

The PLL has been designed to use a reference frequency of between 10 MHz and 104 MHz from an external source, which is typically a temperature compensated crystal oscillator (TCXO). A reference divider (divided by 1 to 7) is supplied and should be programmed to limit the frequency at the phase detector to a maximum of 52MHz.

Two PLL programming banks are provided, the first bank is preceded by the label PLL1, and the second bank is preceded by the label PLL2. The active register bank is selected by the state of the MODE pin, low for PLL1 and high for PLL2.

Fractional-N PLL (2)

The VCO outputs are first divided down in a high frequency pre-scalar. The output of this high frequency pre-scalar then enters the N divider, which is a fractional divider containing a dual-modulus pre-scaler and a digitally spur-compensated fractional sequence generator. This allows very fine frequency steps and minimizes fractional spurs. The fractional energy is randomized and appears as fractional noise at frequency offsets above 100KHz which will be attenuated by the loop filter. An external loop filter is used, giving flexibility in setting loop bandwidth for optimizing phase noise and lock time, for example.

The synthesizer step size is typically 1.5Hz when using a 26MHz reference frequency. The exact step size for any reference and LO frequency can be calculated using the following formula:

$$(F_{REF} * P) / (R * 2^{24} * LO\_DIV*2)$$

Where F_{REF} is the reference frequency, R is the reference division ratio, P is the pre-scalar division ratio, and LO_DIV is the LO divider value.

Pin 26 (GPO4) can be configured as a lock detect pin. The lock status is also available in the read-back register. The lock detect function is a window detector on the VCO tuning voltage. The lock flag will be high to show PLL lock which corresponds to the VCO tuning voltage being within the specified range, typically 0.30V to 1.25V.

The lock time of the PLL will depend on a number of factors, including the loop bandwidth and the reference frequency at the phase detector. This clock frequency determines the speed at which the state machine and internal calibrations run. A 52MHz phase detector frequency will give shortest lock times, of typically <50μsecs when using the PLL re-lock bit.

Phase Detector and Charge Pump

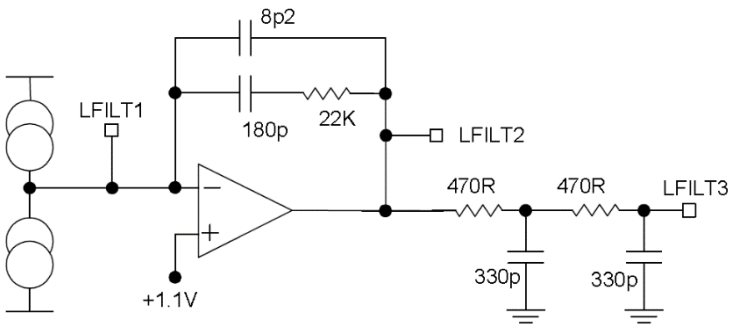
The phase detector provides a current output to drive an active loop filter. The charge pump output current is set by the value contained in the P1_CP_DEF and P2_CP_DEF fields in the loop filter configuration register. The charge pump current is given by approximately 3μA/bit, and the fields are 6 bits long. This gives default value (31) of 93μA and maximum value (63) of 189μA.

If the automatic loop bandwidth calibration is enabled the charge pump current is set by the calibration algorithm based upon the VCO gain.

The phase detector will operate with the maximum frequency of 52MHz.

Loop Filter

The active loop filter is implemented using the on-chip low noise op-amp with external resistors and capacitors. The op-amp gives a tuning voltage range typically +0.1V to +2.4V. The internal configuration of the chip is shown below with the recommended active loop filter. The loop filter shown is designed to give the lowest integrated phase noise for reference frequencies of between 26 MHz and 52MHz. The external loop filter components give the flexibility to optimize the loop response for any particular application and combination of reference and VCO frequencies.



External Frequency Reference

The RFMD2081 has been designed to use an external reference such as a TCXO. The typical input will be a 0.8Vp-p clipped sine wave, which should be AC-coupled into the reference input. When the PLL is not in use, it may be desirable to turn off the internal reference circuits, by setting the REFSTBY bit low, to minimize current draw while in standby mode.

On cold start, or if REFSTBY is programmed low, the reference circuits will need a warm-up period. This is set by the SU_WAIT bits. This will allow the clock to be stable and immediately available when the ENBL bit is asserted high, allowing the PLL to assume normal operation.

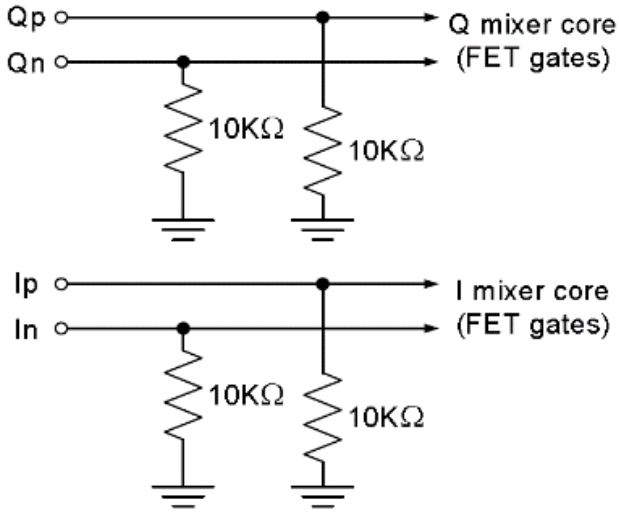
If the current consumption of the reference circuits in standby mode, typically 2mA, is not critical, then the REFSTBY bit can be set high. This allows the fastest startup and lock time after ENBL is taken high.

IQ Modulator (1)

The IQ modulator core of the RFMD2081 is wideband covering from 45MHz to 2700MHz. It has been designed to achieve exceptional linearity for the amount of DC power consumed.

The modulator mixer cores have four coarse gain/current settings. Each setting steps the gain and linearity by 6dB and can be used to optimize performance or reduce power consumption.

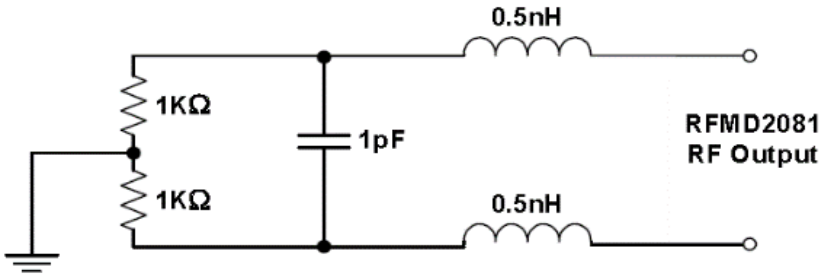
The differential I and Q baseband inputs have 3dB bandwidth of 100MHz, and their input impedance is dominated by 10KΩ pull down resistors on each pin, as shown in the diagram below, so presenting a 20KΩ differential impedance. A common mode DC bias voltage of around +1.3V is required to set the current through the mixer cores for optimal performance. The offset between the common mode voltages on the differential pins can be adjusted to minimize LO leakage at the modulator output. The baseband input signals will be typically of the order of 1Vp-p differential. If required, the phase and amplitude of the I and Q signals can be adjusted to reduce the level of the unwanted sideband signal at the modulator output.



IQ Modulator (2)

The modulator output is differential and requires a balun and simple matching circuit optimized to the specific application frequencies. The modulator output pins are also used to source current for the modulator mixer circuits, about 20mA on each pin. This is usually via a center-tapped balun or by RF chokes in the external matching circuitry from the DC supply. The modulator output is high impedance, consisting of approximately 2KΩ resistance in parallel with some capacitance, approximately 1pF. The modulator output does not require a conjugate matching network. It is a constant current output which will drive a real differential load of 200Ω typically. Since the mixer output is a constant current source, a higher resistance load will give higher output voltage and gain. A shunt inductor can be used to resonate with the output capacitance at the frequency of interest. This inductor may not be required at lower frequencies where the impedance of the output capacitance is less significant. At higher output frequencies the inductance of the bond wires (about 0.5nH on each pin) becomes more significant.

The following diagram is a simple model of the modulator output:



It is recommended to use a 4:1 balun on the modulator output, converting from single ended 50Ω system to the 200Ω differential load. The RFMD2081 evaluation board has an RFXF8553 wideband balun transformer.

Serial Interface

All on-chip registers in the RFMD2081 are programmed using a proprietary 3-wire serial bus which supports both write and read operations. Synthesizer programming, device configuration, and control are achieved through a mixture of hardware and software controls. Certain functions and operations require the use of hardware controls via the ENBL, MODE, and RESETX pins in addition to programming via the serial bus. Alternatively, there is the option to control the chip completely via the serial bus.

The serial data interface can be configured for 4-wire operation by setting the 4WIRE bit in the SDI_CTRL register high. Then pin 26 is used as the data out pin, and pin 32 is the serial data input pin.

Hardware Control

Three hardware control pins are provided: ENBL, MODE, and RESETX.

The ENBL pin has two functions: to enable the analog circuits in the chip and to trigger the VCO auto-selection and coarse tuning mechanisms. The VCO auto-selection and coarse tuning are initiated when the ENBL pin is taken high. Every time the frequency of the synthesizer is reprogrammed, ENBL must be asserted high to initiate these mechanisms and then to initiate the PLL locking. Alternatively following the programming of a new frequency, the PLL re-lock self-clearing bit could be used.

If the device is left in the enabled state for long periods, it is recommended that VCO auto-selection and coarse tuning (band selection) is performed for every 30°C change in temperature. The lock detect flag can be used to indicate when to perform the VCO calibration, it shows that the VCO tuning voltage has drifted significantly with changing temperature.

The RESETX pin is a hardware reset control that will reset all digital circuits to their startup state when asserted low. The device includes a power-on-reset function, so this pin should not normally be required, in which case it should be connected to the positive supply.

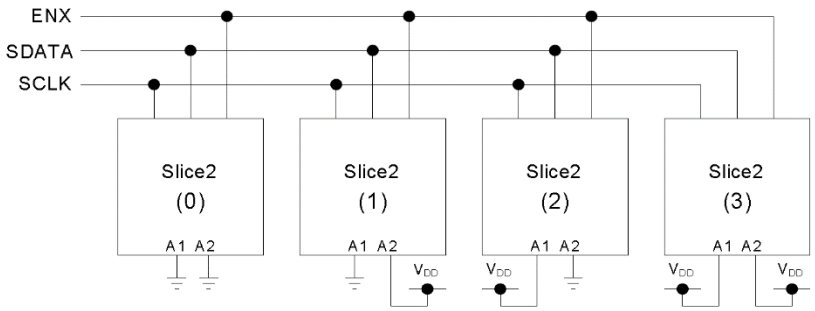
The MODE pin controls which PLL programming register bank is active.

Serial Data Interface Control

The normal mode of operation uses the 3-wire serial interface to program the device registers, and three extra hardware control lines: MODE, ENBL and RESETX.

When the device is under software control, achieved by setting the SIPIN bit in the SDI_CTRL register high, then the hardware can be controlled via the SDI_CTRL register. When this is the case, the three hardware control lines are not required. If the device is under software control, pins 1 and 9 can be configured as general-purpose outputs (GPO).

Multi-Slice Mode



The multi-slice mode of operation allows up to four devices to be controlled from a common serial bus. The device address pins (15 and 16) ADD1 and ADD2 are used to set the address of each part.

On power up, and after a reset, the devices ignore the address pins ADD1 and ADD2 and any data presented to the serial bus will be programmed into all the devices. However, once the ADDR bit in the SDI_CTRL register is set, each device then adopts an address according to the state of the address pins on the device.

General Purpose Outputs

The general-purpose outputs (GPOs) can be controlled via the GPO register and will depend on the state of MODE since they can be set in different states corresponding to either mixer path 1 or 2. For example, the GPOs can be used to drive LEDs or to control external circuitry such as switches or low power LNAs.

Each GPO pin can supply approximately 20mA load current. The output voltage of the GPO high state will drop with increased load current by approximately 20mV/mA. Similarly, the output voltage of the GPO low state will rise with increased current by approximately 25mV/mA.

Programming Information

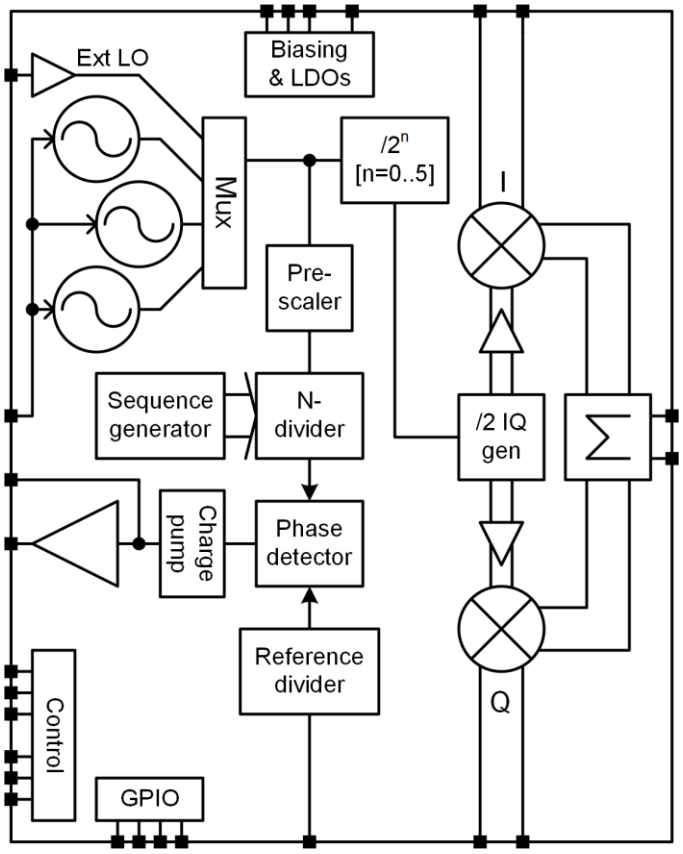
Please refer to the Register Maps and Programming Guide which are available for download from the links below:
https://www.qorvo.com/products/d/da000926
https://www.qorvo.com/products/d/da000927

Evaluation Boards

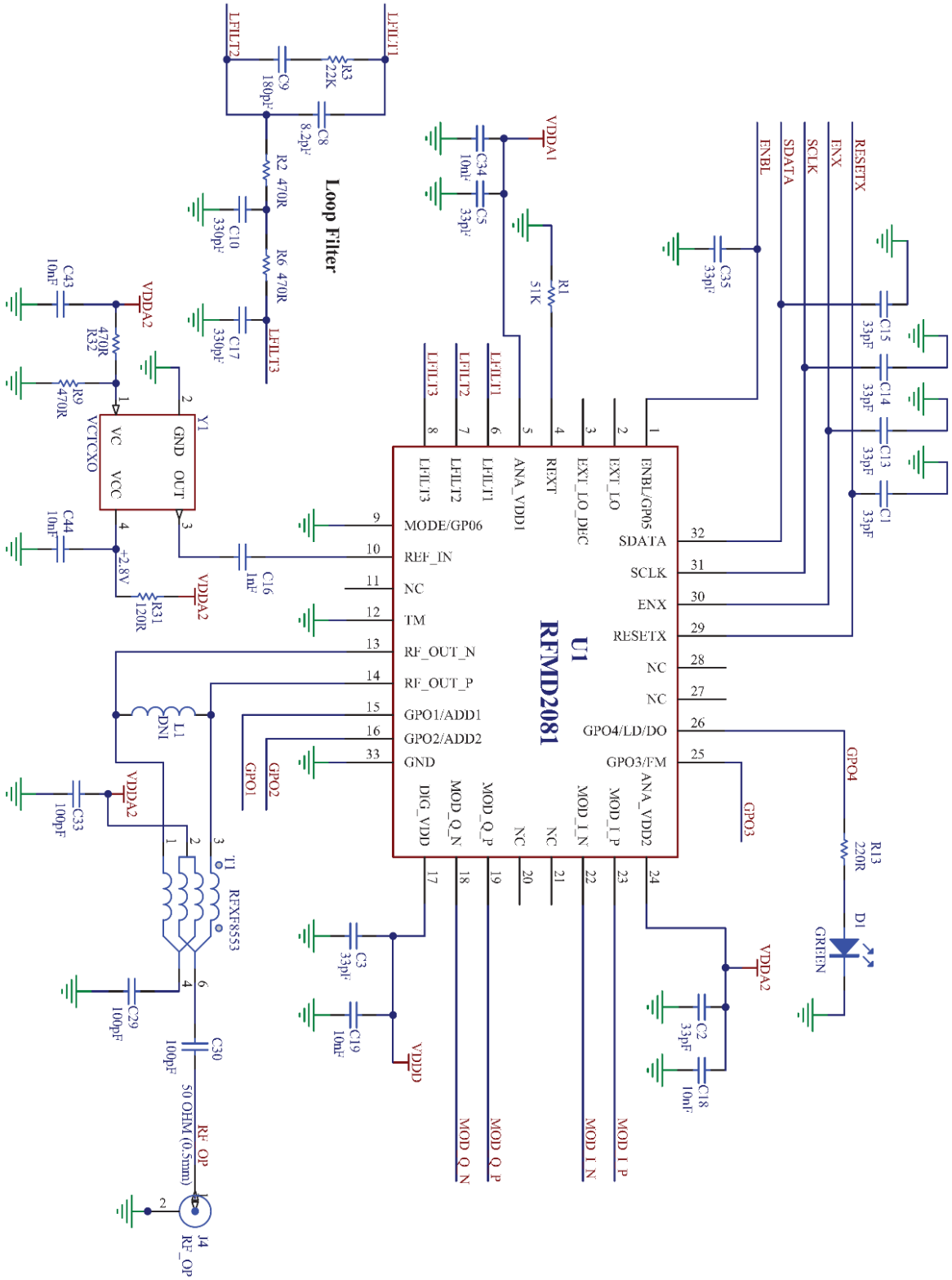
The evaluation board for RFMD2081 is provided as part of a design kit, along with the necessary cables and programming software tool to enable full evaluation of the device. The evaluation board has been configured for wideband operation. The modulator outputs are connected to wideband balun with a transmission line at the EVB RF output. Design kits can be ordered from www.qorvo.com or from local Qorvo sales offices and authorized sales channels. For ordering codes please see “Ordering Information” on page 1.

For further details on how to set up the design kits go to https://www.qorvo.com/products/d/da000924.

Detailed Functional Block Diagram

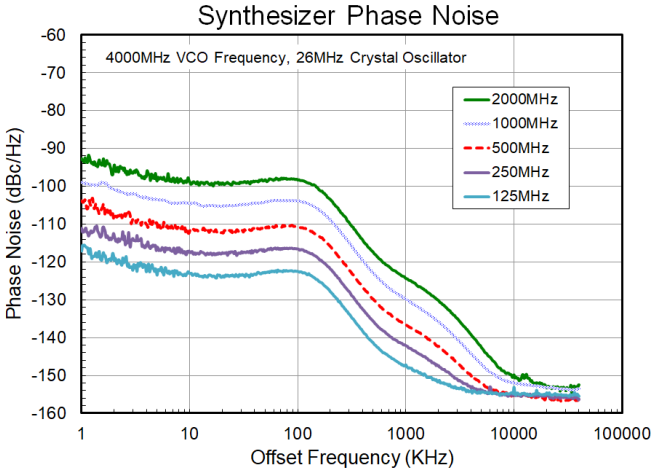


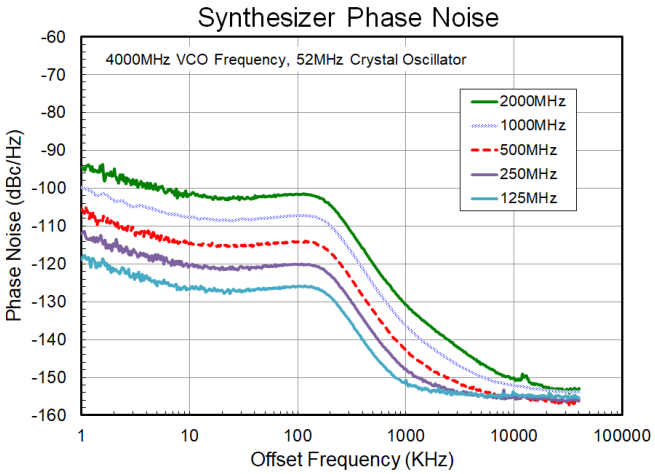
Application Schematic

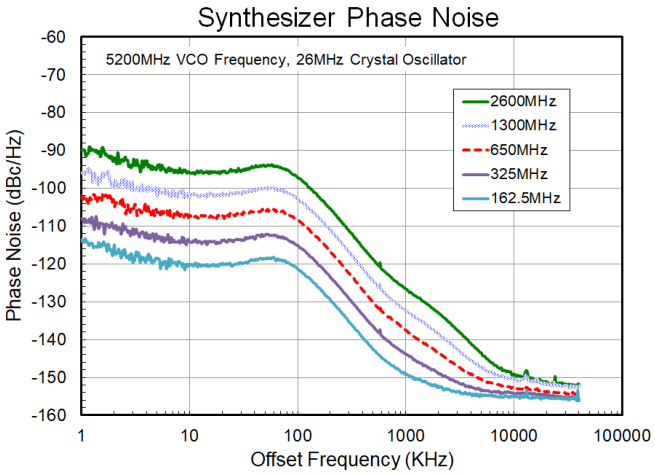


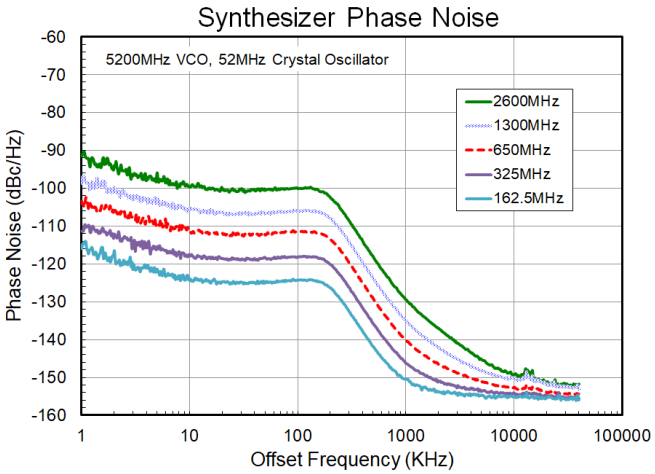
Typical Performance Characteristics – Synthesizer

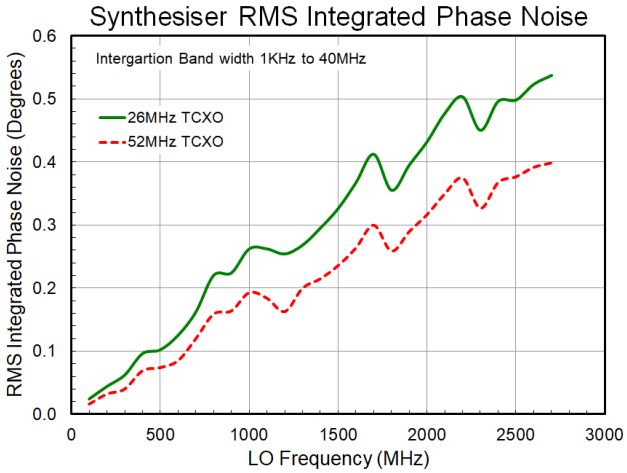
VDD = +3 V and T_C = +27 °C unless stated otherwise, on RFMD2081 EVB with active loop filter









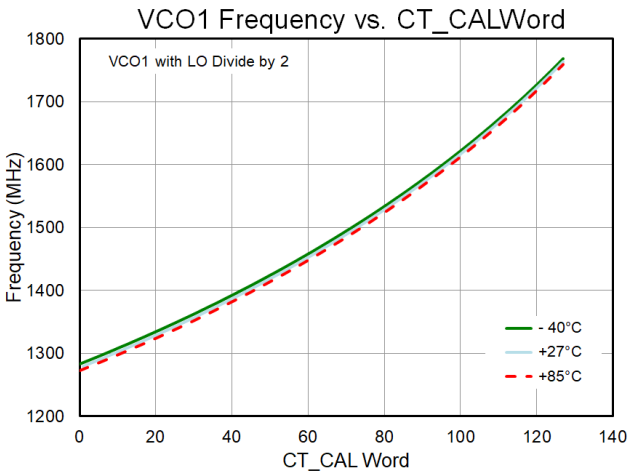


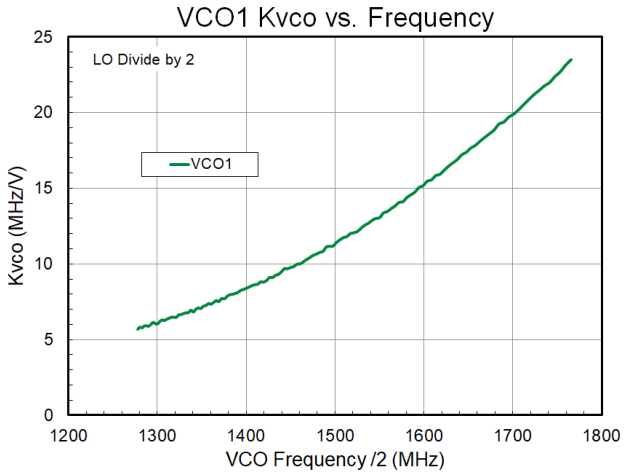
Notes:

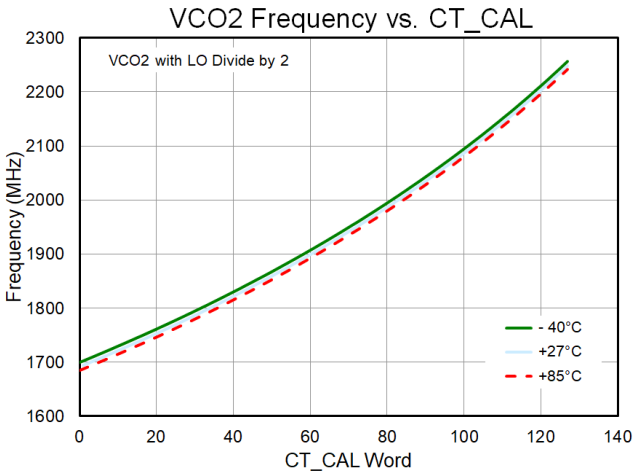
- 26MHz Crystal Oscillator: NDK ENA3523A
- 52MHz Crystal Oscillator: NDK ENA3560A

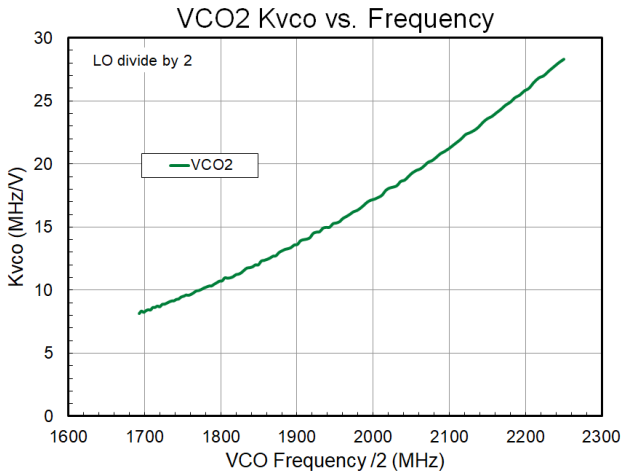
Typical Performance Characteristics – VCO (1)

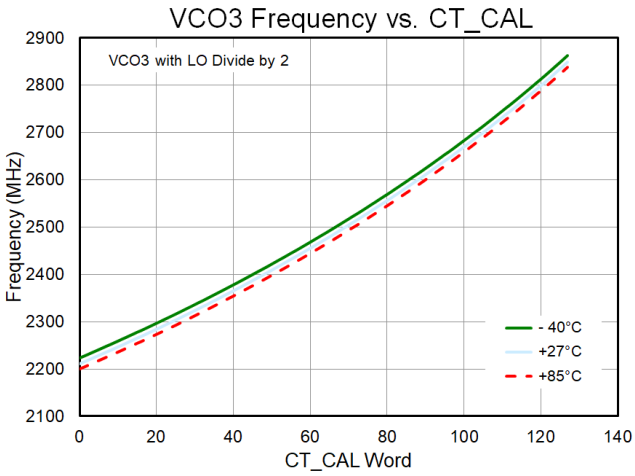
VDD = +3 V and T_C = +27 °C unless stated otherwise, on RFMD2081 EVB

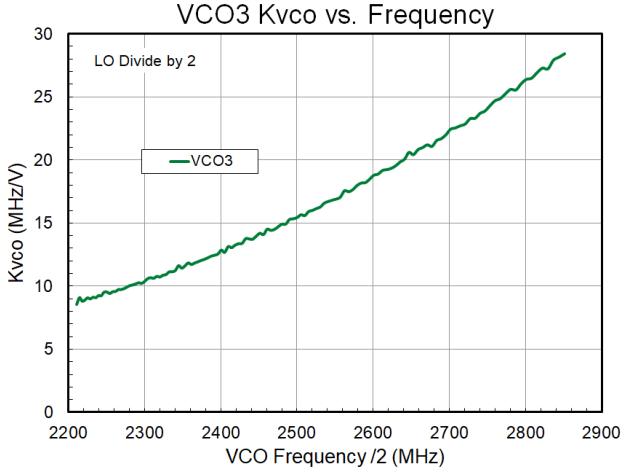












Typical Performance Characteristics – VCO (2)

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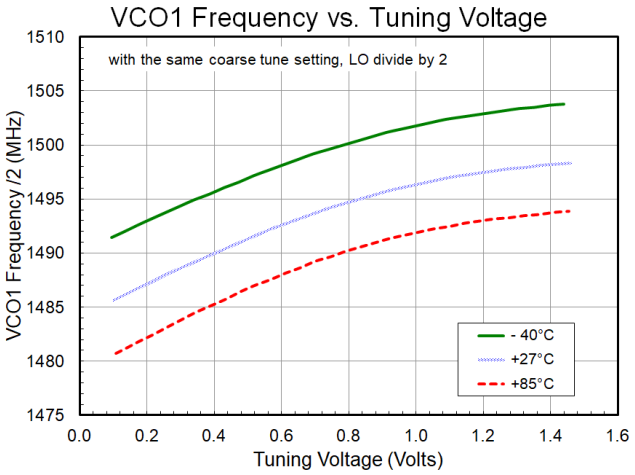
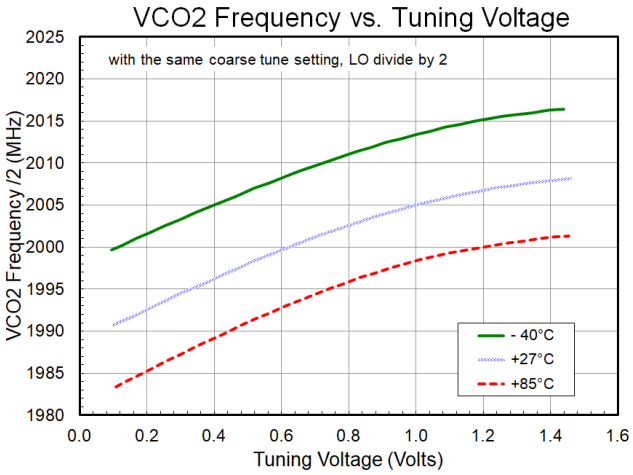
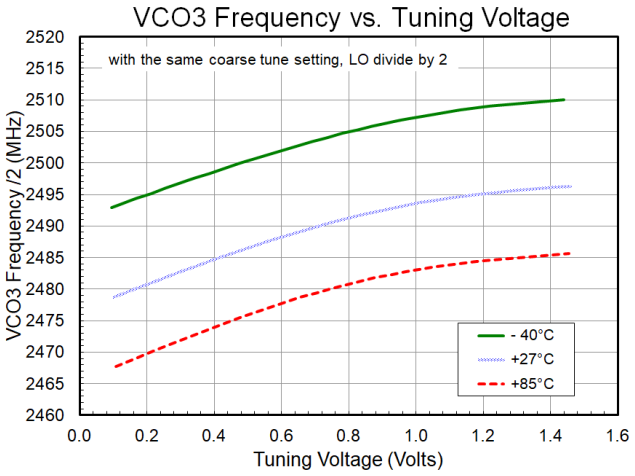
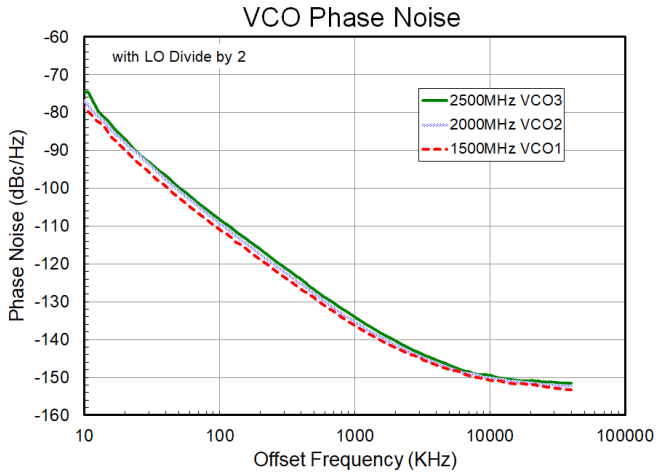


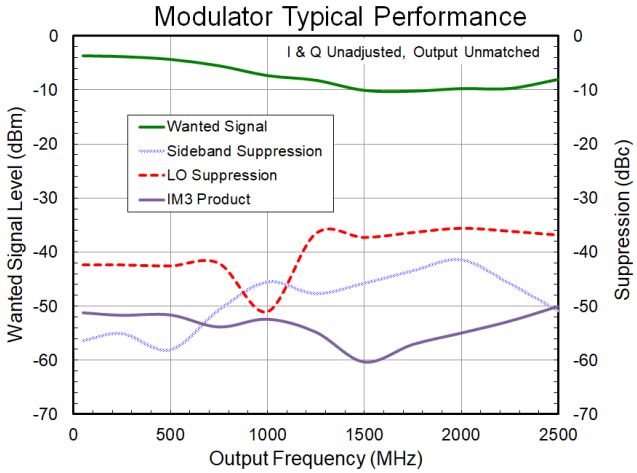


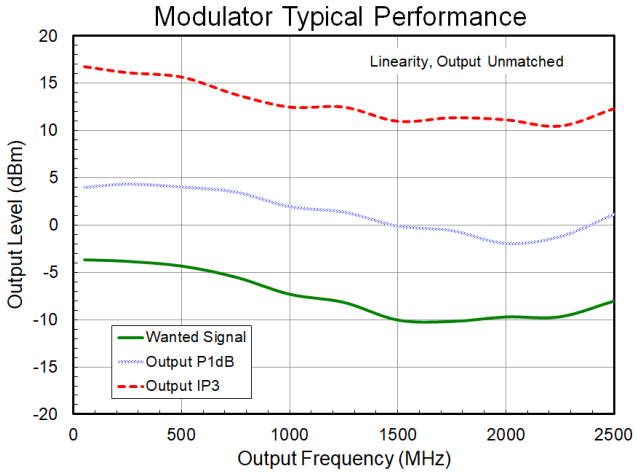


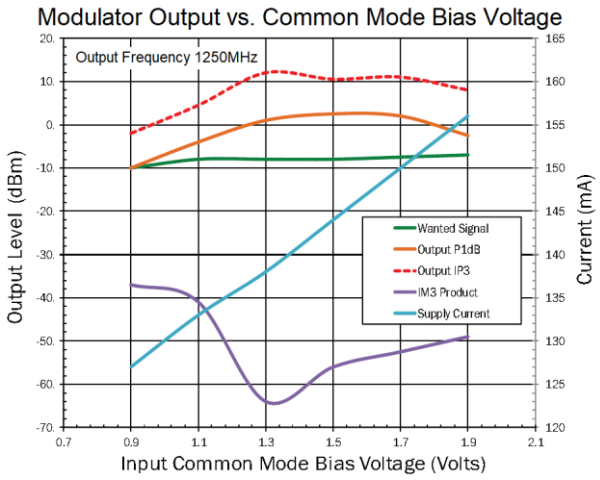


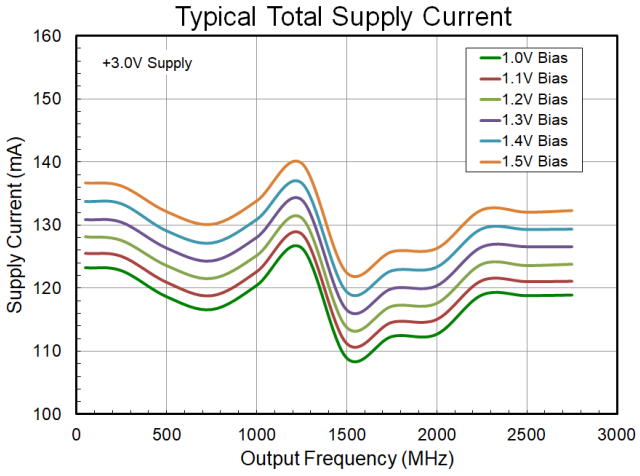
Typical Performance Characteristics – IQ Modulator (1)

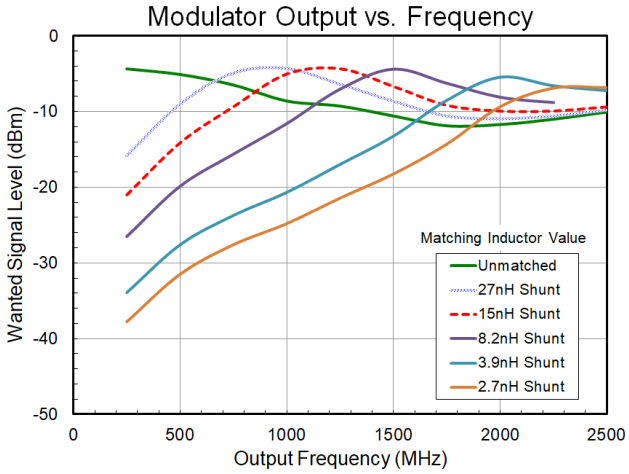
VDD = +3 V and T_C = +27 °C unless stated otherwise, on RFMD2081 EVB, I & Q input 1Vp-p differential with +1.3V DC Bias











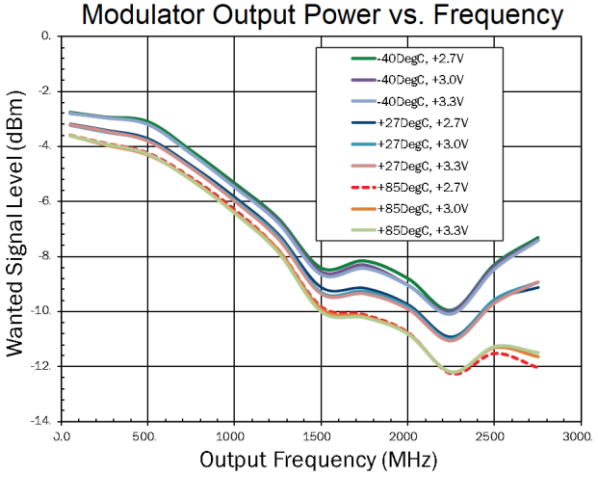
The modulator output power can be improved as output frequency increases by using a shunt inductor (L1 on Application Schematic) to resonate with the modulator output capacitance, typically 1 pF.

The output transformer used for characterization is the RFXF8553 (T1) which has 3 dB cut off point at 2500MHz.

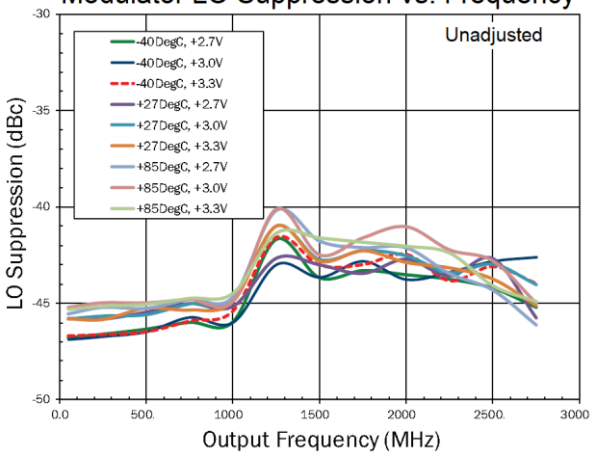
Typical Performance Characteristics – IQ Modulator (2)

VDD = +3 V and T_C = +27 °C unless stated otherwise, on RFMD2081 EVB, I & Q input 1Vp-p differential with +1.3V DC Bias

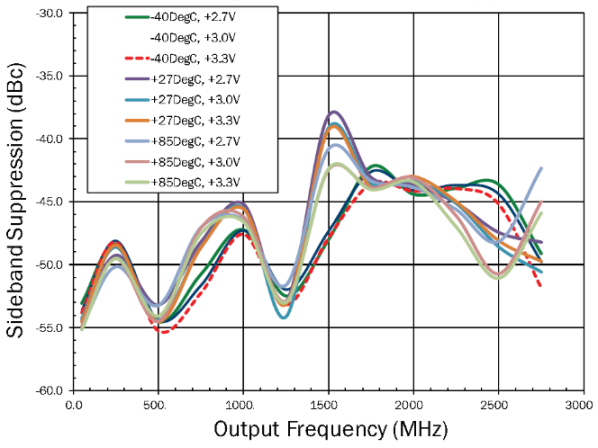
Modulator Output Power vs. Frequency



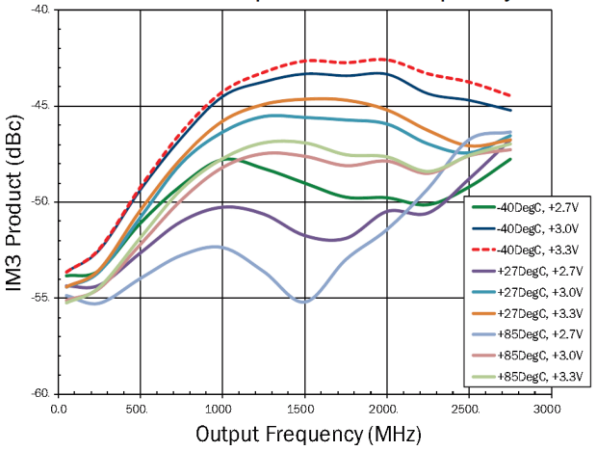
Modulator LO Suppression vs. Frequency



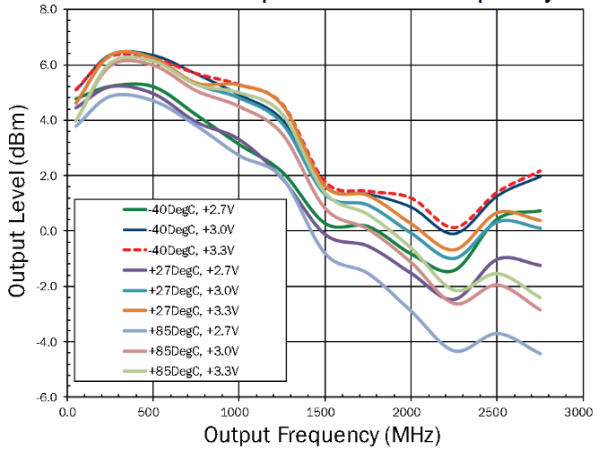
Modulator Unadjusted Sideband Suppression



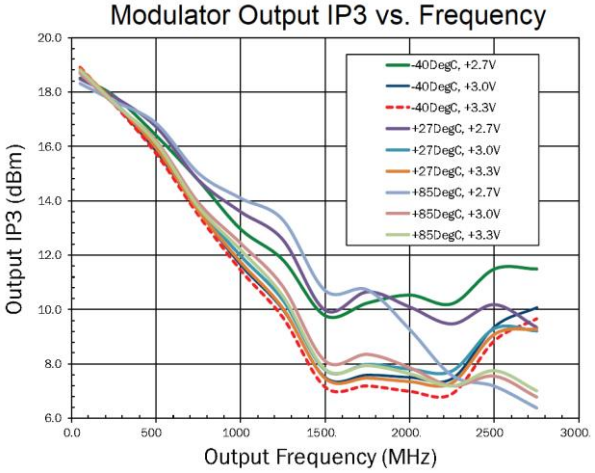
Modulator Output IM3 vs. Frequency



Modulator Output P1dB vs. Frequency

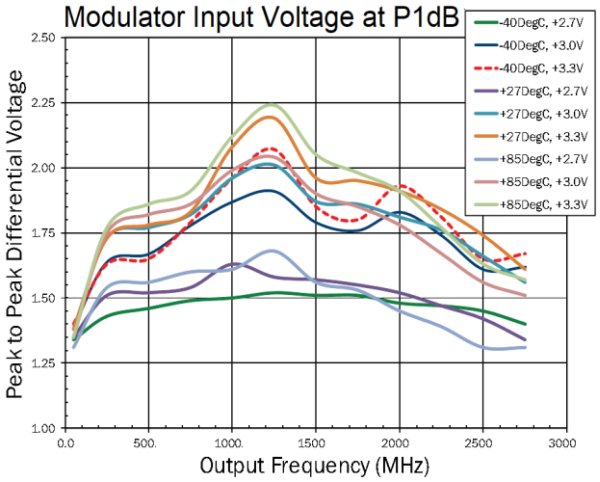


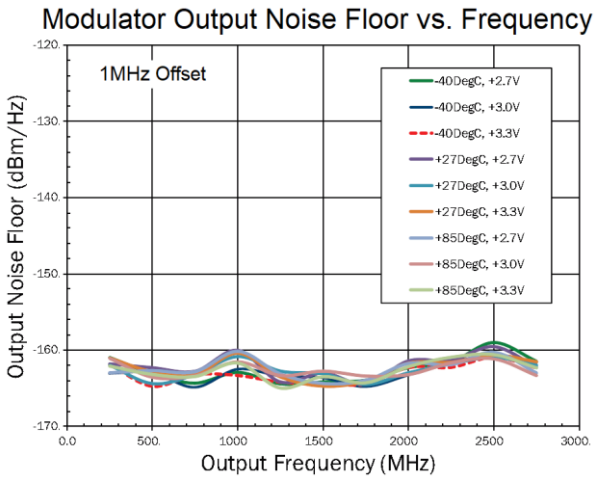
Modulator Output IP3 vs. Frequency

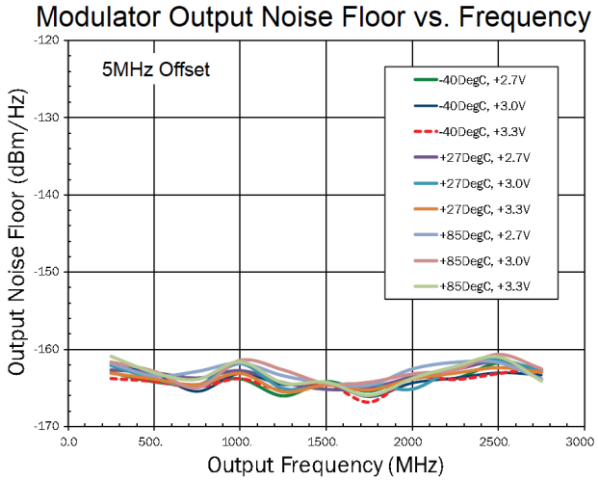


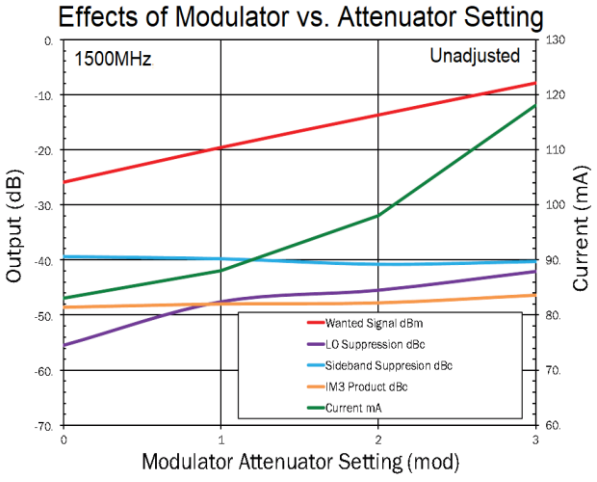
Typical Performance Characteristics – IQ Modulator (3)

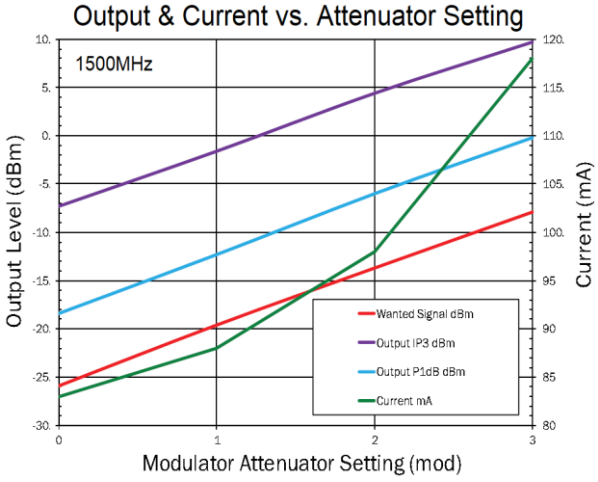
VDD = +3 V and T_C = +27 °C unless stated otherwise, on RFMD2081 EVB, I & Q input 1Vp-p differential with +1.3V DC Bias



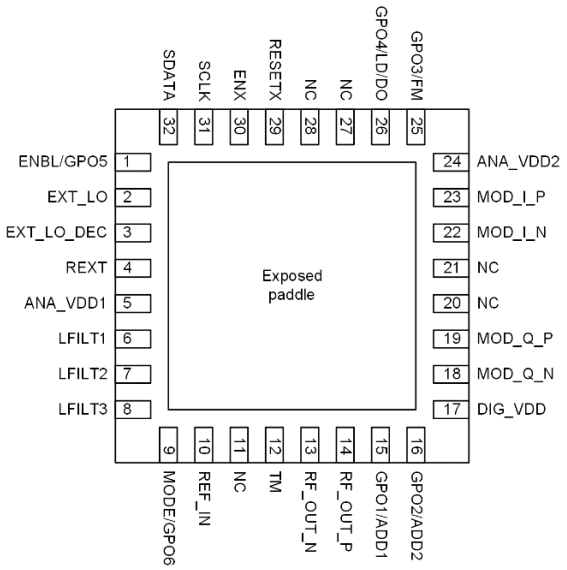








Pin Configuration and Descriptions

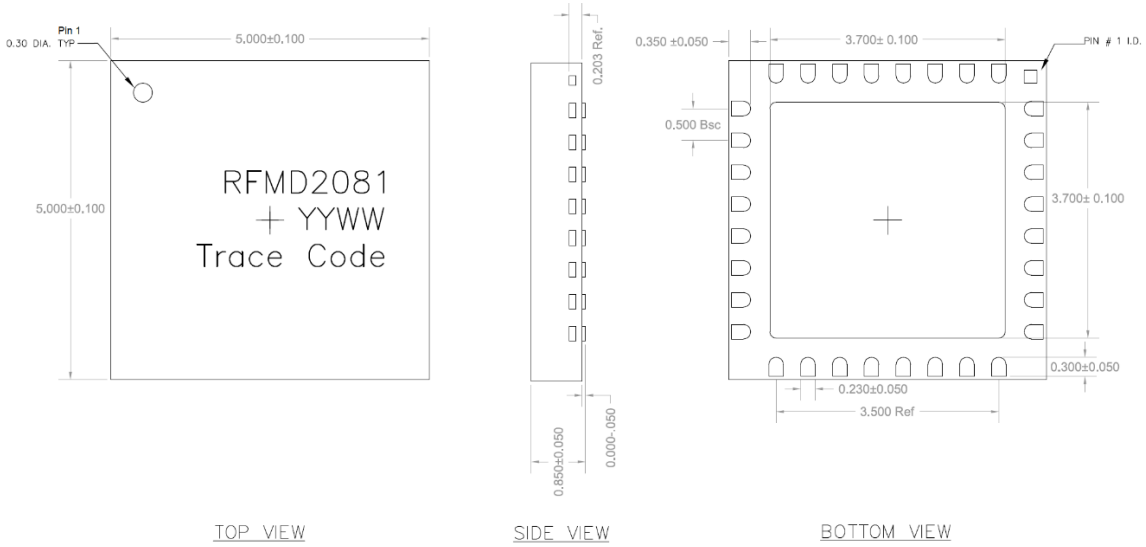


Pin No.	Label	Description
1	ENBL/GPO5	Device Enable pin (1) (2)
2	EXT_LO	External local oscillator input, AC coupling only
3	EXT_LO_DEC	Decoupling pin for external local oscillator with capacitors
4	REXT	External bandgap bias resistor (3)
5	ANA_VDD1	DC Voltage input 1 analog circuits. good RF decoupling required
6	LFILT1	Phase detector output. Low-frequency noise-sensitive node
7	LFILT2	Loop filter Op-Amp output. Low-frequency noise-sensitive node
8	LFILT3	VCO control input. Low-frequency noise-sensitive node
9	MODE/GPO6	Mode selecting input pin (1) (2)
10	REF_IN	Reference input. AC coupling only
11, 20, 21, 27, 28	NC	No internal connection
12	TM	Connect to ground.
13, 14	RF_OUT_N, RF_OUT_P	Differential Output (5)
15	GPO1/ADD1	General purpose output 1 / Multi-Slice address bit 1.
16	GPO2/ADD2	General purpose output 2 / Multi-Slice address bit 2.
17	DIG_VDD	Digital supply. Should be decoupled as close to the pin as possible
18, 19	MOD_Q_N, MOD_Q_P	Differential Input port of Q Modulator (4)
22, 23	MOD_I_N, MOD_I_P	Differential Input port of I Modulator (4)
24	ANA_VDD2	DC Voltage input 2 to analog circuits. good RF decoupling required
25	GPO3	General purpose output 3
26	GPO4/LD/DO	General purpose output 4 / Lock detect output / serial data output
29	RESETX	Chip reset (active low). Connect to DIG_VDD if asynchronous reset is not required.
30	ENX	Serial interface select (active low) (1)
31	SCLK	Serial interface clock (1)
32	SDATA	Serial interface data (1)
Exposed Paddle		Ground reference, should be connected to PCB ground through a low impedance

Notes:
1. An RC low-pass filter could be used on this line to reduce digital noise.
2. If the device is under software control this input can be configured as a general-purpose output (GPO).
3. Connect a 51 kΩ resistor from this pin to ground. This pin is sensitive to low frequency noise injection.
4. DC voltage and modulation signal should not be applied to this pin.
5. This pin must be connected to ANA_VDD2 using an RF choke or transformer (see application schematic).

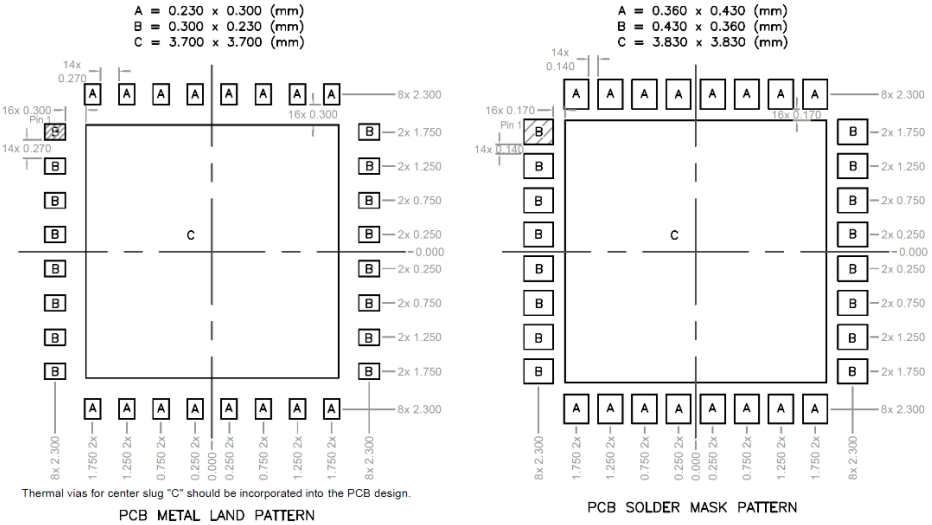
Package Marking and Dimensions

Marking: Part Number – RFMD2081
YYWW – Date Code, Two digits Year and Week
Trace Code – Assigned by subcontractor



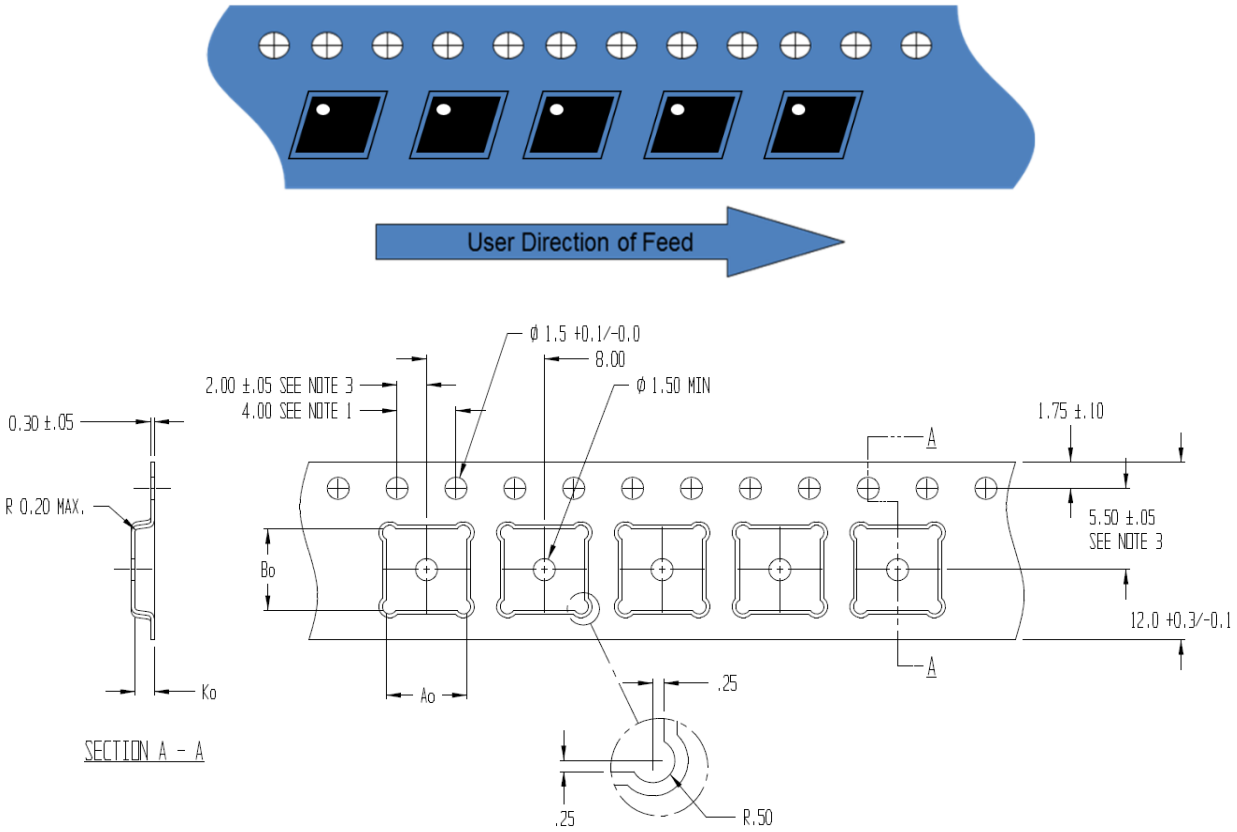
Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.
3. Contact plating: Matte Sn

PCB Mounting Pattern



Notes:
1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Via holes are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.01").
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

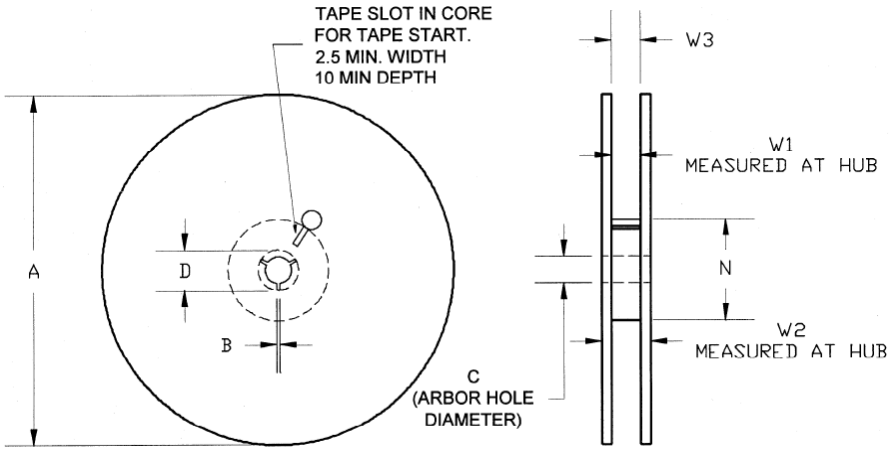
Tape and Reel Information – Carrier and Cover Tape Dimensions



Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.207	5.25
	Width	B0	0.207	5.25
	Depth	K0	0.051	1.30
	Pitch	P1	0.315	8.00
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.00
	Cavity to Perforation - Width Direction	F	0.217	5.50
Cover Tape	Width (Refence only)	C	0.362	9.20
Carrier Tape	Width	W	0.472	12.00

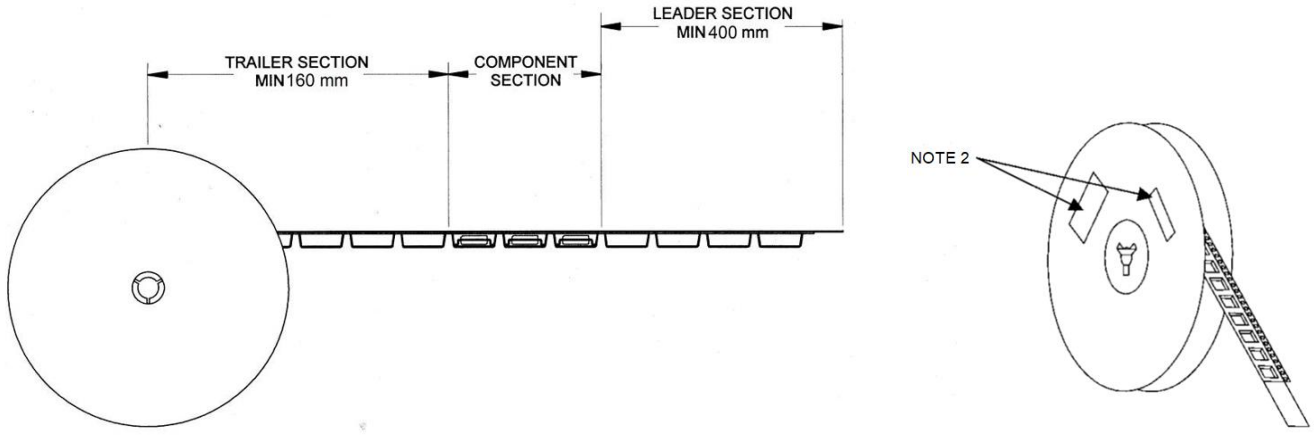
Tape and Reel Information – Reel Dimensions

Standard T/R size = 2,500 pieces on a 13” reel.



Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	12.992	330.0
	Thickness	W2	0.717	18.2
	Space Between Flange	W1	0.504	12.8
Hub	Outer Diameter	N	4.016	102.0
	Arbor Hole Diameter	C	0.512	13.0
	Key Slit Width	B	0.079	2.0
	Key Slit Diameter	D	0.787	20.0

Tape and Reel Information – Tape Length and Label Placement



Notes:
1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
2. Labels are placed on the flange opposite the sprockets in the carrier tape.

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1C	ESDA / JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	Class C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 2	IPC/JEDEC J-STD-020

Caution!
ESD-Sensitive Device

Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes.
Solder profiles available upon request.

Contact plating: Matte Sn *(Plating thickness 8~20 µm)*

RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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