USER'S GUIDE

# ACT43750EVK3 User's Guide

## Description

This document describes the characteristics and operation of the Qorvo ACT43750EVK3 evaluation kit (EVK). It provides setup and operation instructions, schematic, layout, BOM, GUI, and test data. This EVK ships as a standalone board that can be evaluated independently or with a GaN RF Power Amplifier.

The ACT43750 is an integrated power solution that controls GaN RF PA drain and gate:

- Generates negative gate voltage for the PA gate
- Properly sequenced turn on and turn off
- Automatic gate voltage / drain current calibration
- Drain voltage switching

It is an ideal solution for radio frequency (RF) power amplifiers (PAs) that demand fast transient, high current pulsed loads.

## Features

Qorvo recommends that the user evaluate the EVK functionality with an RF PA and with the EVK connected to a PC running the graphical user interface (GUI) software. The GUI allows the user to enable/disable the outputs and to customize the exact voltage and current requirements for the specific RF PA being tested. The user can use the ACT43750 GUI to set the RF PA Idq bias current target, and the EVK autonomously finds and stores the optimal gate voltage for the Idq bias current.


**Figure 1. ACT43750EVK3 Board**

## EVK Contents

The EVK ships with the following:

- ACT43750EVK3 PCB
- USB-TO-I2C Dongle and cables
- The EVK does not ship with an RF PA

## Appendix

Application Note 1: Safe Operation at High Drain Switching Frequency

Application Note 2: How to Configure Bias Current and Current Limit

Application Note 3: How to Configure Drain Switching Time

Application Note 4: How to Select Dongle and GUI

Application Note 5: Drain Capacitance for RFPA Drain Switching Operation

Application Note 6: Operation without I2C

## Hardware Setup

Required Equipment

- ACT43750EVK3
- DC power supply - 10~55V @ 10A for full power operation
- DC power supply – 12V
- Oscilloscope - 500MHz, 4 channels
- Function generator
- Current probe
- Digital Multi-meters (DMM)
- Windows compatible PC with spare USB port
- Qorvo USB-to-I$^2$C dongle
- Compatible GaN RF PA

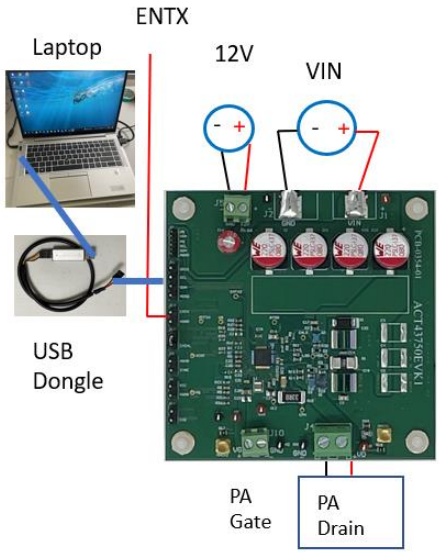



**Figure 2. ACT43750EVK3 SET-UP**

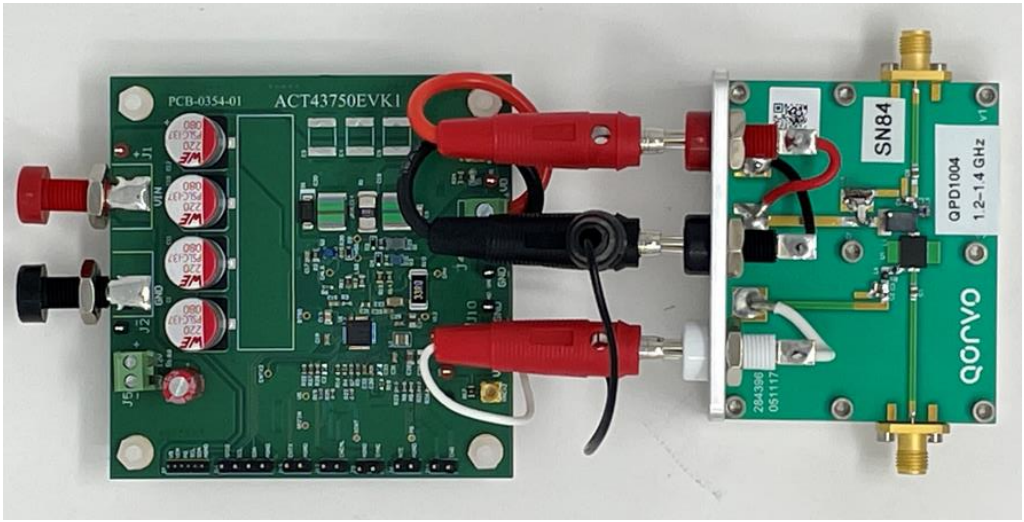



**Figure 3. ACT43750EVK3 + QPD1004EVK SET-UP**

## Hardware Connections

Refer to Figure 2 & 3 for hardware connections. Make all connections with power off.

1) Open J12 (ENCAL)
2) Open J6 (NTC)
3) Open J14 (ENG)
4) Connect the Qorvo USB-TO-I2C dongle cable to J11. The black wire connects to the AGND pin.
5) Optional: Connect a PWM generator to the J13 (ENTX) pin to AGND. ENTX supports 5V and 3.3V logic. Make sure the PWM generator is turned off. If an external PWM generator is not used, leave it open.
6) Connect a DC power supply between J1 (VIN) and J2 (GND). This is the voltage that is applied to the RF PA drain. Please use the required drain voltage for the RF PA.
7) Connect a 12VDC power supply between J5 (V12) Bias and J5 (GND).
8) If testing a dummy resistor load:
    a. Connect the resistor between VD and GND on J4.
9) If testing an RF PA:
    a. Connect the RF PA Drain between VD and GND on J4.
    b. Connect the RF PA Gate between VG and GND on J10.
10) The drain switch can be turned on/off by the ENTX pin or by the software GUI. For high-frequency operation, connect a function generator to ENTX.
11) If over-temperature protection is desired, an NTC can be placed on the RF PA and wired to the J6 NTC connector. The NTC along with R5 and R8 will set the over-temperature shutdown threshold.

## Recommended Operating Conditions

The ACT43750EVK3 operates with a 10V to 55V drain voltage and supports up to a 10A load.

| Parameter | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Vdrain | Drain voltage | 10 | - | 55 | V |
| Idrain | Drain current | 0 | - | 10 | A |
| V12V | 12V DC bias | 10.8 | 12 | 13.2 | V |
| ENTX On-Time | | 12 | - | - | µs |
| ENTX Off-Time | | 40 | - | - | µs |

**Table 1. Recommended Operating Conditions for ACT43750**

# ACT43750 Test Procedure

### Warning:

Devices may be damaged if the power up/power down procedure is not strictly followed.

Don't touch the high voltage potential: input voltage & output voltage terminals, test points, capacitors, and inductor.

### GUI Installation

- Get GUI files from the Qorvo website
- Plug the Qorvo dongle USB-TO-I2C cable into a free USB port.
- The USB driver will be automatically installed.
- Double click on the ACT43750 Customer GUI Rev0.5.exe to start the ACT43750EVK.

### Power up

1) Make sure the RF input signal is turned off.
2) Power on the 12V bias supply.
3) Power on the Vdrain supply (set voltage to appropriate value for the RF PA)
4) Open the GUI. Press "Read" button. Press "Enable Vgate" button.
    a. This sets the Vg voltage to -4.5V.
5) If testing with an RF PA, perform auto-calibration. The gate voltage will increase until the target IDQ is met. If testing with dummy load, auto-calibration is not necessary.
    a. Note1: Calibration resistor change is necessary for certain dc bias current. Please refer to App Note 2.
    b. Note 2: RFPA drain capacitor change is necessary. Please refer to App Note 5 for drain capacitance and drain switching operation.
6) Enable the drain switches with either ENTX pin or with the GUI. The pulse width on-time should be greater than 12µs. To limit the power dissipation in the load device (dummy resistor or RF PA), consider using a low duty cycle.
7) Measure the gate and drain voltage and drain current.

### Power down

1) If testing an RF PA with an RF input signal, disable the RF input.
2) Disable the drain switch by turning off the ENTX PWM pulses or using GUI
3) Power off 50V DC power supply.
    a. Note that the 50V DC supply must be turned off before the 12V bias supply
4) Power off 12V DC power supply

# ACT43750 GUI Operation

### GUI Operation

- Click on the "Read" icon and confirm the GUI returns "Success"
- Basic tab: easily enable gate and drain voltages
- Register tab: edit register settings
- Tool tab: read/write I2C commands

### OCP current sense resistor setting

- Default current sense resistor is 3mΩ for typical 12A overcurrent protection. Note: OCP threshold is set by the resistor on the EVK; the GUI cannot change the OCP threshold.

### Calibration current sense resistor setting

- Default calibration current sense resistor is 2Ω for 750mA bias current.
- By entering the value of the R2 resistor, the target bias current will display
- Note 1: Bias current can be adjusted +/- 31% digitally, Idq offset (%) button can do this function.
- Note 2: If the bias current adjustment is larger than +/-31%, the calibration resistor must be changed.
- Please refer to APP Note 2 for details.

### Gate voltage control

- Default gate voltage is –4.5V
- Default min gate voltage is –4.5V and max gate voltage is –1.5V
- Gate voltage can be changed by drop down menu in setting
- Note: Gate voltage can be changed when ENTX is low or PWM pulse operation. If ENTX is high, the gate voltage is not allowed to change.
- Auto calibration can be done after enabling Vgate

### Enable the ACT43750

- Push Enable Vgate button
- Confirm the gate voltage is -4.5V

### Enable the ACT43750 Autocalibration

- Push Enable Autocalibration button
- The gate voltage will rise until the target IDQ is met

### Enable/Disable the ACT43750 Drain Switch

- Push Enable Vdrain button
- Confirm the drain voltage is present
- Push this button again
- Confirm the drain voltage is zero
- Note: "Enable Vdrain" button is only for continuous operation. For pulse operation, Apply PWM pulse to ENTX pin.

# QPD1004EVB and ACT43750EVK3 System Test

Note 1: Calibration resistor change is necessary for certain RFPA dc bias current. Please refer to App Note 2.

Note 2: RFPA drain capacitor change is necessary. Please refer to App Note 5 for drain capacitance and drain switching operation.

Note 3: For the high-frequency operation of RFPA, it's necessary to estimate the power loss of charge pump resistor R10. Please refer to App Note 1 for details.

## Hardware connection

- Connecting ACT43750 J10, Vg to Vgate of QPD1004 EVB in the Figure 3 & 5.
- Connecting ACT43750 J4, VD to Vdrain of QPD1004 EVB in the Figure 3 & 5.
- Connecting ACT43750 J10, J4 (GND) to GND of QPD1004 EVB in the Figure 3 & 5.
- Make Vdrain cable as short and wide as possible.


Figure 5. QPD1004 EVB

## QPD1004 Bias up

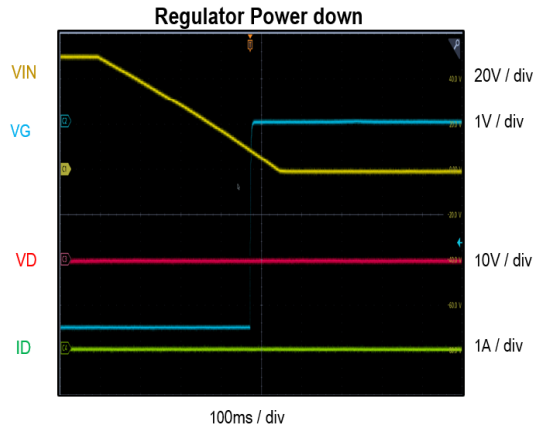
1) Make sure RF signal is off
2) Power up the ACT43750 12V bias supply
3) Power on 50V voltage source
4) Turn on VG to -4.5V by pushing Enable Vgate button
5) Do automatic calibration by pushing the Autocalibration button. The gate voltage should gradually rise to -2.5V.
6) Measure VG waveform to confirm VG change to -2.5V.
7) Turn on/off the drain switch by applying a PWM pulse to the ENTX pin
8) Measure VD & ID waveform to confirm drain voltage & current pulse amplitude and frequency
9) Turn on RF signal

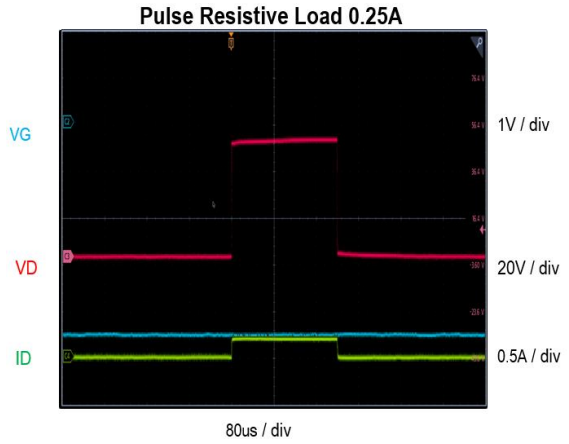
### QPD1004 Bias Down

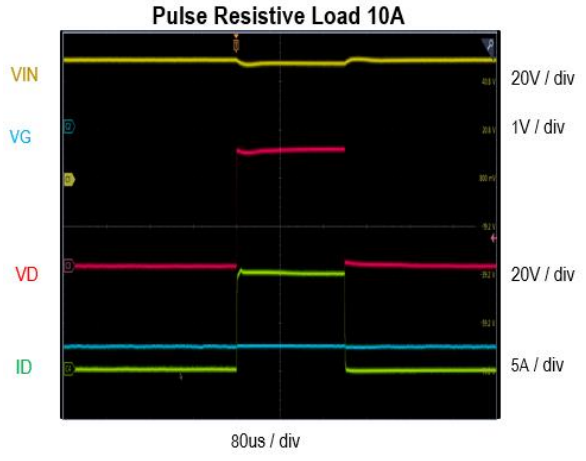
1) Turn off RF signal
2) Turn off the drain switch by pulling the ENTX pin to low logic level.
3) Adjust VG to –4.5V. Using GUI in Figure 4.
4) Measure VG to confirm it's -4.5V.
5) Power off the 50V voltage source
6) Wait for 2 seconds to discharge the drain voltage.
7) Turn off the 12V bias supply

## Test Results

Test condition, Input voltage=50V, Bias voltage=12V, Resistor load

Test condition, Input voltage=50V, Bias voltage=12V, RFPA QPD1004

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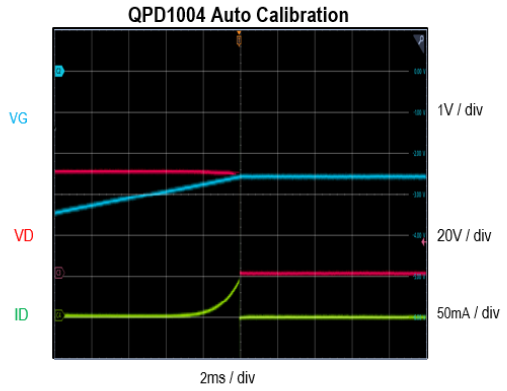
|  | |
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## Schematic

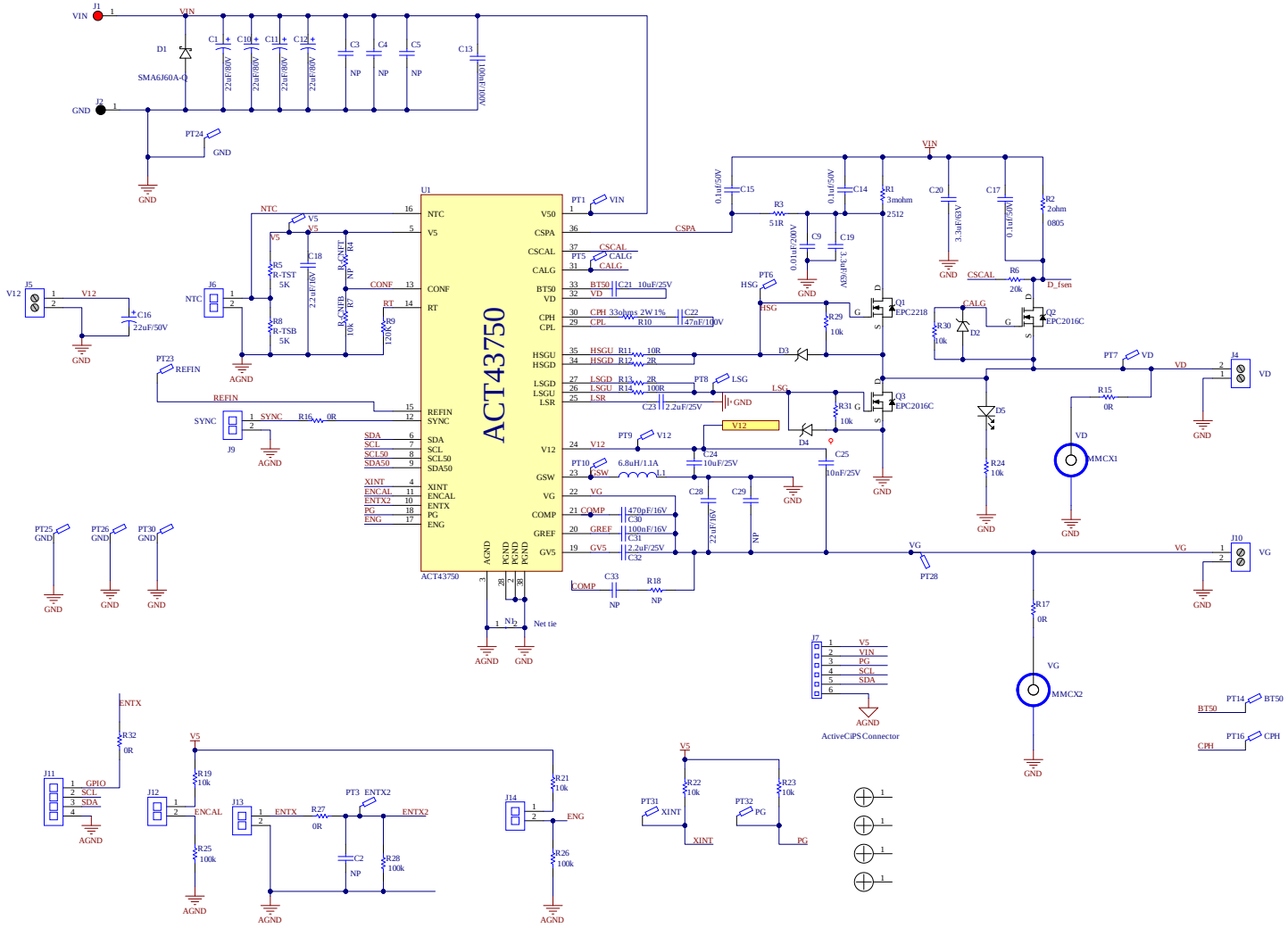


**Figure 6. Schematic ACT43750EVK3**

# Layout

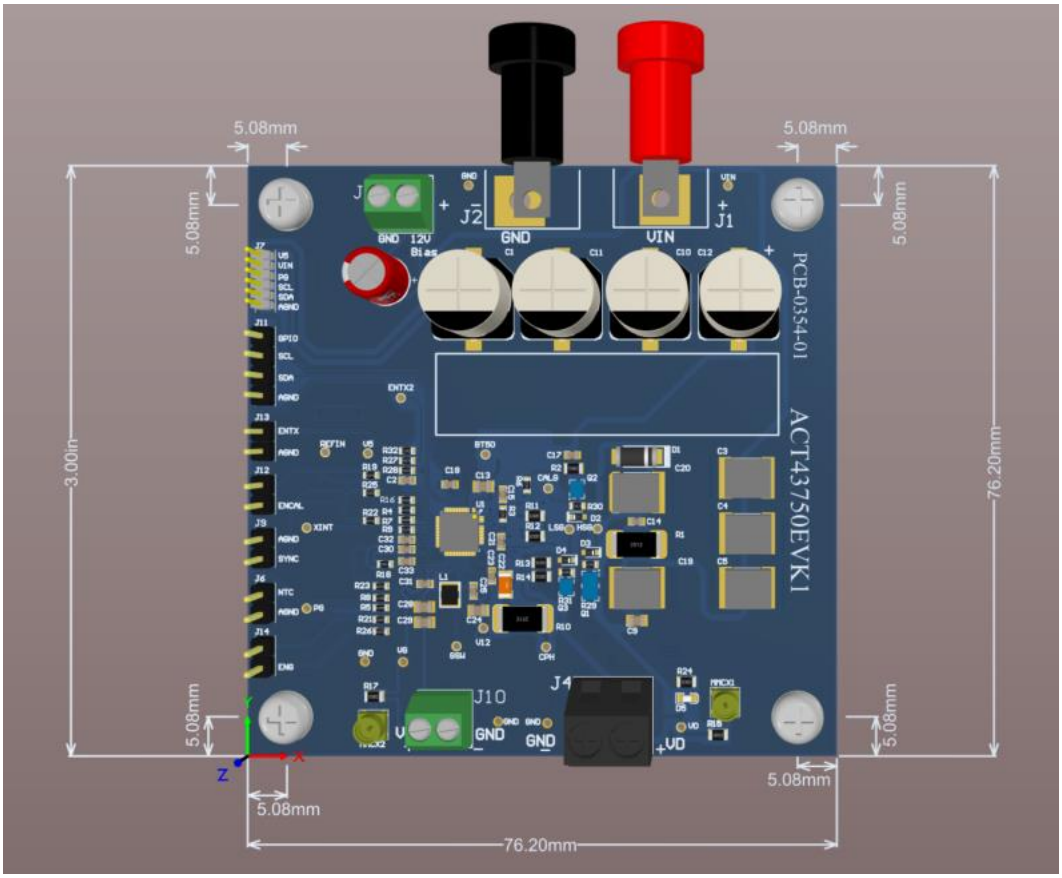


**Figure 7. Assembly Top Layer**

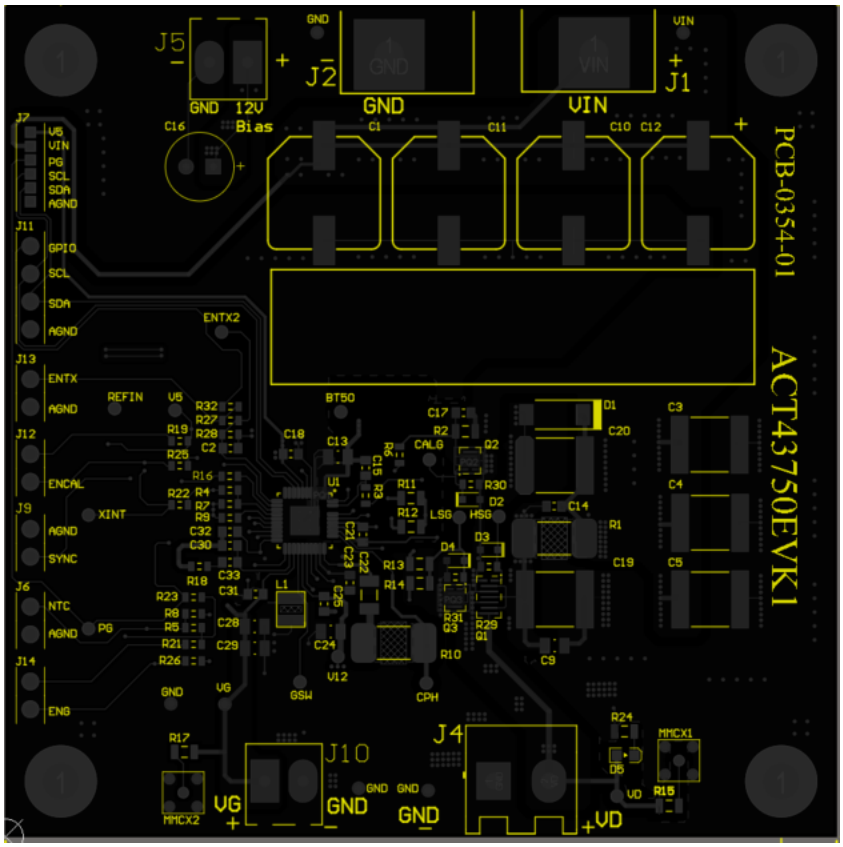


**Figure 8. Top Layer Silk Screen**

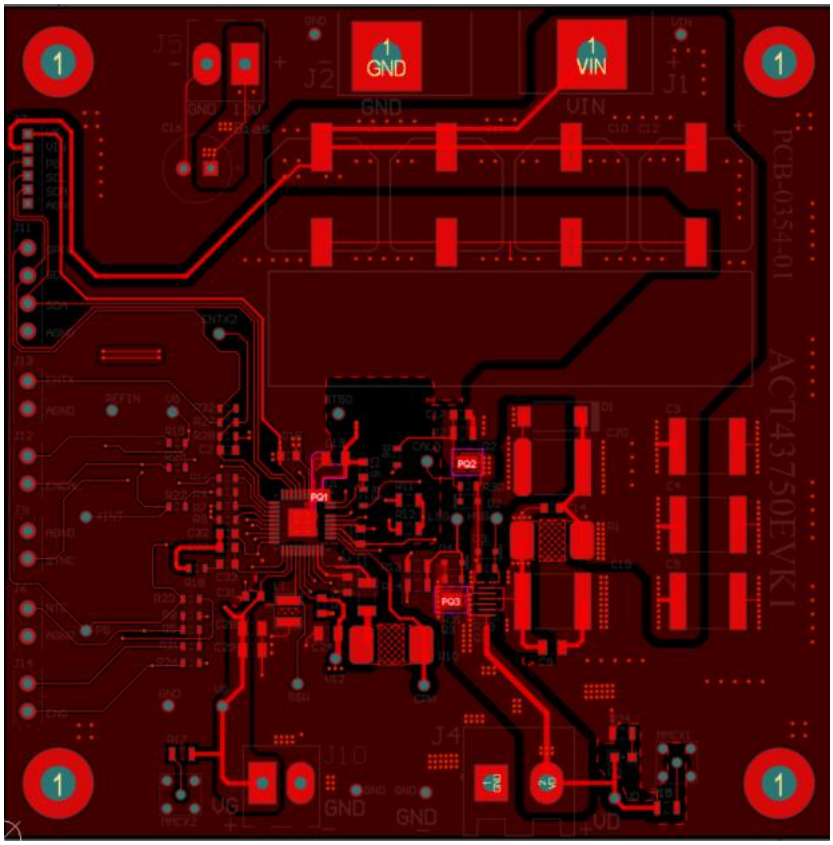


**Figure 9. Layout Top Layer**

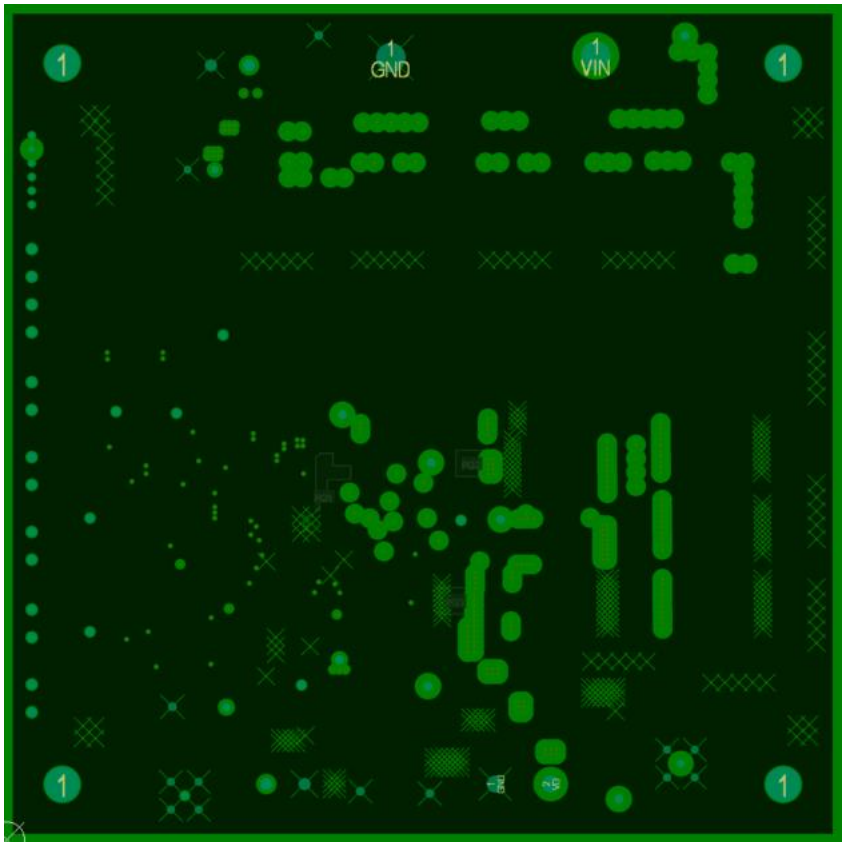


**Figure 10. Layer 2 – GND Plane**

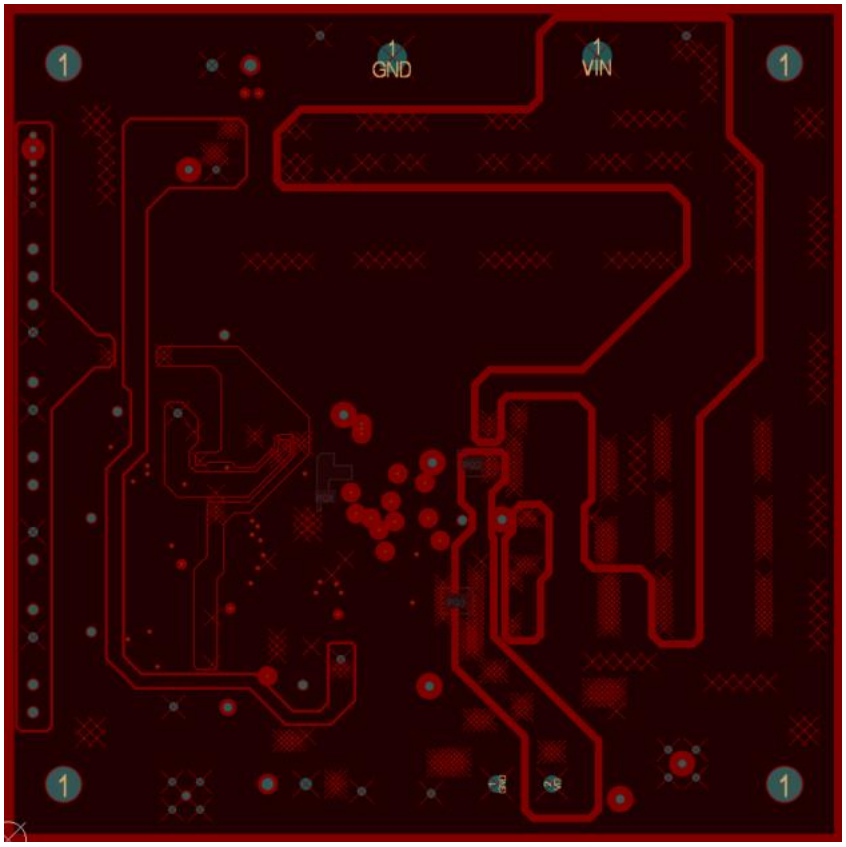


**Figure 11. Layer 3 - GND Plane**

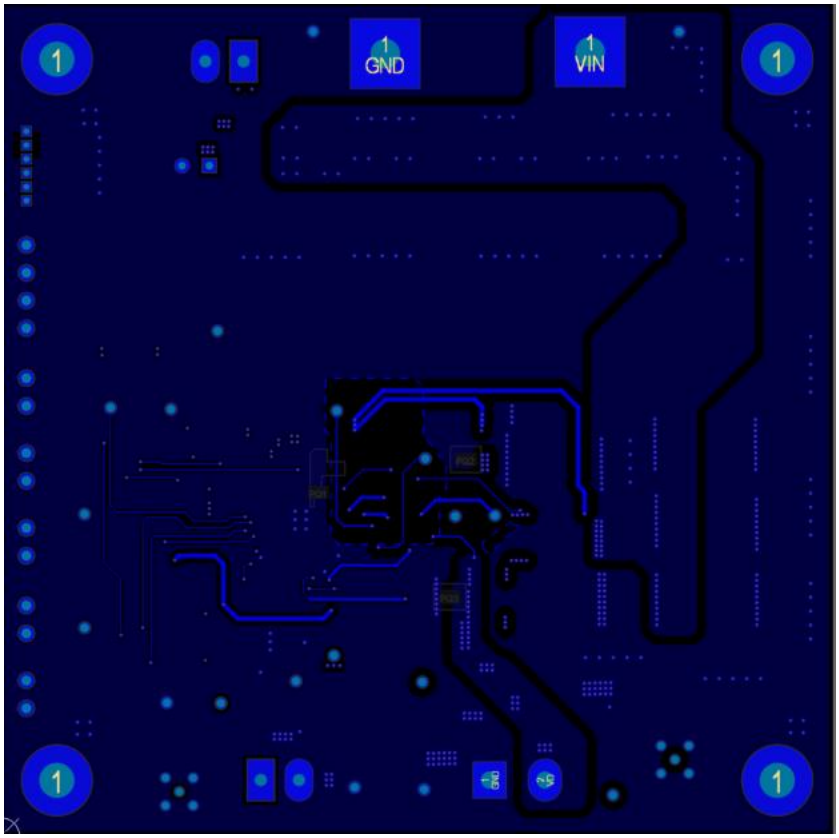


**Figure 12. Layout Bottom Layer**

## Bill of Materials

| Description | Designator | Footprint | Qty | Manufacturer | Part Number | Value | Comments |
|---|---|---|---|---|---|---|---|
| Capacitor, Aluminum | C1, C10, C11, C12 | E-Cap_PCV_10x12.7 | 4 | Nichicon or WE | PCV1K220MCL1GS or 875076161003 | 22uF/80V | Prefer WE |
| Capacitor, Ceramic, | C2 | C0603_H | 0 | Standard | Standard | NP | |
| Capacitor, Aluminum | C16 | WCAP-ATG5_6.3x11x2.5 | 1 | WE | 860130673002 | 22uF/50V | |
| Capacitor, Film Cap | C3, C4, C5 | C2220_Film_CAP | 0 | Rubycon | 63MU335MD35750 | NP | |
| Capacitor, Film Cap | C19, C20 | C2220_Film_CAP | 2 | Rubycon | 63MU335MD35750 | 3.3uF/63V | |
| Capacitor, Ceramic, | C9 | C0805_H | 1 | Standard | Standard | 0.01uF/200V | |
| Capacitor, Ceramic, | C13 | C0805_H | 1 | Murata Electronic | GCM21BR72A104KA37L | 100nF/100V | |
| Capacitor, Ceramic, | C14, C15, C17 | C0603_H | 3 | Standard | Standard | 0.1uf/50V | |
| Capacitor, Ceramic, | C18 | C0603_H | 1 | Standard | Standard | 2.2uF/16V | |
| Capacitor, Ceramic, | C21 | C0805_H | 1 | Standard | Standard | 10uF/25V | |
| Capacitor, Ceramic, | C22 | C1206_H | 1 | Standard | Standard | 47nF/100V | |
| Capacitor, Ceramic, | C23 | C0603_H | 1 | Standard | Standard | 2.2uF/25V | |
| Capacitor, Ceramic, | C24 | C0805_H | 1 | Standard | Standard | 10uF/25V | |
| Capacitor, Ceramic, | C25 | C0603_H | 1 | Standard | Standard | 10nF/25V | |
| Capacitor, Ceramic, | C29 | C0805_H | 1 | Standard | Standard | NP | |
| Capacitor, Ceramic, | C28 | C0805_H | 1 | Standard | Standard | 22uF/16V | |
| Capacitor, Ceramic, | C30 | C0603_H | 1 | Standard | Standard | 470pF/16V | |
| Capacitor, Ceramic, | C31 | C0603_H | 1 | Standard | Standard | 100nF/16V | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Capacitor, Ceramic, | C32 | C0603_H | 1 | Standard | Standard | 2.2uF/25V | |
| Capacitor, Ceramic, | C33 | C0603_H | 1 | Standard | Standard | NP | |
| Diode, TVS | D1 | DIODE,DO-213AB | 1 | Bourns | SMA6J60A-Q | 66.7V Breakdown | |
| Diode, Zener | D2, D3, D4 | DIODE,SOD-523 | 3 | MCC | BZT52C5V1T-TP | Zener 5.1V | |
| Diode, Led, Green | D5 | WL-SMCW_0603 | 1 | Rohm | SMLD12EN1W | Led Green | 5mA current |
| MACHINE SCREW | H1, H2, H3, H4 | 4-40 | 4 | McMaster-Carr | 92196A106 | 4-40 | |
| CON, BANANA PLUG,RED | J1 | CON, BANANA, CINCH | 1 | CINCH | 108-0902-001 | Banana plug red | |
| CON, BANANA PLUG, BLACK | J2 | CON, BANANA, CINCH - BLACK | 1 | CINCH | 108-0903-001 | Banana plug black | |
| Connector, Screw Terminal, 5.08, 2P | J4 | con,tbk,508-2p,molex-0395443002 | 1 | WURTH | 691236510002 | 5.08, 2P | |
| Connector, Screw Terminal, 1.27, 6P | J7 | con, tbk, 1.27, 6p | 1 | Sullins | GRPB061VWVN-RC | 1.27, 6P | |
| Connector, Screw Terminal, 3.50, 2P | J5, J10 | con,tbk,350-2p,kf350 | 2 | Wurth | 691214110002S | 3.50, 2P | |
| Header, Unshrouded , 2.54, Male, 2P | J6, J9, J12, J13, J14 | con,hdr,254-2p | 5 | Wurth | 61300211121 | 2.54, Male, 2P | |
| Header, Unshrouded , 2.54, Male, 4P | J11 | con,hdr,254-4p | 1 | Wurth | 61300411121 | 2.54, Male, 4P | |
| Inductor, | L1 | L25xx_MAPI_R | 1 | Murata Electronics | DFE252010F-6R8M=P2 | 6.8uH/1.1A | |
| MMCX | MMCX1, MMCX2 | MMCX THT | 2 | Taoglas limited TE | PCB.MMCXFSTJ.HTor 1_1634009_0 | | Prefer Taoglas |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Test point (Red) | PT1, VIN | TSP, PROBE | 1 | Keystone | Testpoint 5000 | | |
| Test point (Red) | PT7 (VD) | TSP, PROBE | 1 | Keystone | Testpoint 5000 | | |
| Test point (Red) | PT10 (GSW) | TSP, PROBE | 1 | Keystone | Testpoint 5001 | | |
| Test point (Red) | PT28 (VG) | TSP, PROBE | 1 | Keystone | Testpoint 5000 | | |
| Test point (Black) | PT24, PT25, PT26, PT30 (GND) | TSP, PROBE | 4 | Keystone | Testpoint 5001 | | |
| MOSFET, Single, | Q1 | GaN, FETs, EPC2218 | 1 | EPC | EPC2218 | 100V/60A/2.4m Ohm | |
| MOSFET, Single, | Q2, Q3 | GaN, FETs, EPC2016C | 2 | EPC | EPC2016C | 100V/18A/12mOhm | |
| Resistor, | R1 | R2512_L | 1 | Bourns | CRF2512-FZ-R003ELF | 0.003 Ohms 2W 1% | |
| Resistor, | R2 | R0805_H | 1 | Standard | Standard | 2ohms 0.125W 1% | |
| Resistor, | R3 | R0603_H | 1 | Standard | Standard | 51.1 | |
| Resistor, | R4 | R0603_H | 1 | Standard | Standard | NP | |
| Resistor, | R5 | R0603_H | 1 | Standard | Standard | 5K | |
| Resistor, | R6 | R0603_H | 1 | Standard | Standard | 20k | |
| Resistor, | R7 | R0603_H | 1 | Standard | Standard | 10k | |
| Resistor, | R8 | R0603_H | 1 | Standard | Standard | 5k | |
| Resistor, | R9 | R0603_H | 1 | Standard | Standard | 120K | |
| Resistor, | R10 | R2512_L | 1 | Bourns | CRM2512-FX-33R00ELF | 33ohms 2W 1% | |
| Resistor, | R11 | R0805_H | 1 | Standard | Standard | 10R | |
| Resistor, | R14 | R0805_H | 1 | Standard | Standard | 100R | |
| Resistor, | R15, R17 | R0805_H | 2 | Standard | Standard | 0R | |
| Resistor, | R12, R13 | R0805_H | 2 | Standard | Standard | 2R | |
| Resistor, | R16 | R0603_H | 1 | Standard | Standard | 0R | |
| Resistor, | R18 | R0603_H | 1 | Standard | Standard | NP | |
| Resistor, | R19, R21, R22, R23 | R0603_H | 4 | Standard | Standard | 10k | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Resistor, | R24 | R0805_H | 1 | Standard | Standard | 10k | |
| Resistor, | R25, R26, R28, | R0603_H | 3 | Standard | Standard | 100k | |
| Resistor, | R27, R32 | R0603_H | 2 | Standard | Standard | 0R | |
| Resistor, | R29, R30, R31 | R0603_H | 3 | Standard | Standard | 10k | |
| PCB | PCB | PCB-0354-01 | 1 | Standard | Standard | PCB-0354-01 | |
| IC, ACT43750 | U1 | HP34_QFN37-5X5 | 1 | Qorvo | ACT43750-101 | ACT43750-101 | |

# Application Note 1: Safe Operation at High Drain Switching Frequency

ACT43750 is designed for operation at low drain switching frequency, typically less than 1kHz. For drain switching frequency is higher than 500Hz, the charge pump circuit component R10 may need to be upgraded. The reason is that the power loss of resistor R10 is proportional to the drain switching frequency, capacitance, and drain voltage square. The following formula can calculate the power loss of R10:

$$P = 0.5 * C * V^2 * F$$

Where:

P – power loss of charge pump resistor, unit W.

C – charge pump capacitance, the unit is F. It's C22 and 47nF in ACT43750 EVK.

R – charge pump resistance, the unit is ohm. It's R10 and 33ohm in ACT43750 EVK.

F – drain switching frequency, the unit is Hz

V – drain voltage, the unit is Volt. It's 50V in a typical application.

At drain switch frequency 1kHz, power loss is 0.059w. R10 is 2512 size resistor, and the power rating is 2w. It's OK for the original board design. When the drain switch frequency is much higher, R10 power loss is higher than the rating value. So, the R10 may need to be changed to a higher-power resistor.

The process to determine the component change is listed below:

Step 1, Calculate the power loss of R10 at the desirable drain switch frequency

Step 2, If the power loss is less than 1.5w, no action is needed; if it's higher than 1.5w, then go to the next step

Step 3, Find the resistors power rating that is higher than the requirement with a good margin

Step 4, Locate R10 in the board, and replace it with higher power resistors

# Application Note 2: How to Configure Bias Current and Current Limit

Every RF PA has a specific dc bias drain current and drain current limit requirement.

### 1. DC Bias Drain Current

Drain current (IDQ) is set by resistor R2 according to the formula below. This setpoint can be adjusted by +/- 31% with register 0x13. If the drain current target needs to be adjusted by more than 31%, then the calibration resistor R2 can be changed. The following formula can calculate the calibration resistance.

$$R2 = 1.5V/Idq$$

Where:

Idq – RF PA dc bias current, unit A.

R2 – Calibration resistance, unit Ω.

### 2. Drain Current Limit

RF PA has the drain current limit to protect the device, and the current limit can be changed by resistor R1.

$$R1 = 35mV/ID$$

Where:

ID – RF PA drain current, unit A.

R1 – Current limit resistance, unit mΩ.

Please refer to the schematics and layout for resistor connection and location.

# Application Note 3: How to Configure Drain Switching Time

The drain switching time is defined by the drain voltage rising and falling from 10% peak to 90% peak or 90% to 10% peak. The drain voltage VD switching transition time can be changed by adjusting gate resistance. The default rising switching time is 10ns and falling switching time is 10ns. R11 is 10Ω. R12 and R13 are 2Ω. A typical drain voltage and current switching transition waveforms are listed below.

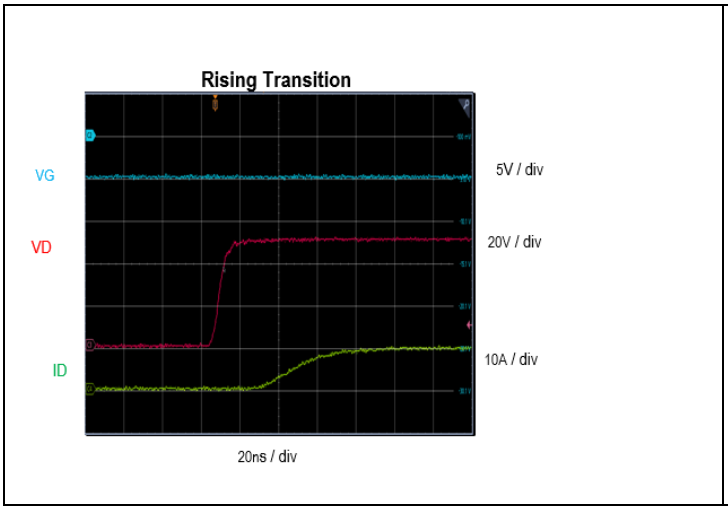


Figure 1. Rising Transition

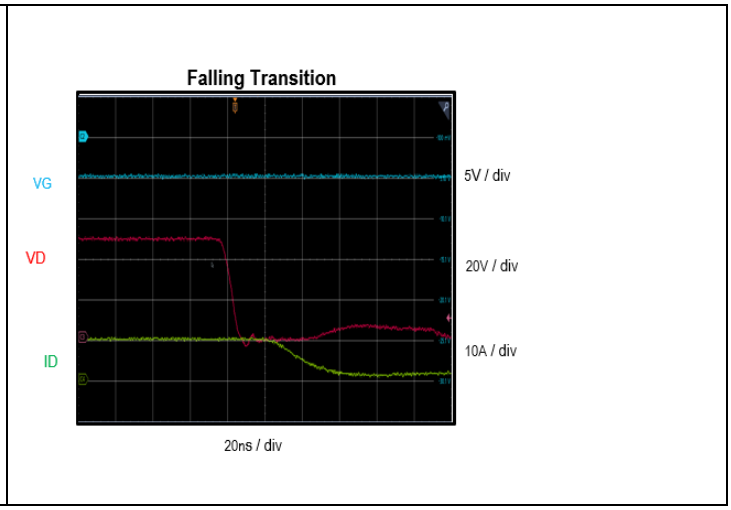


Figure 2. Falling Transition

To reduce rising switching time, R11 should be a smaller resistance value. To increase rising switching time, R11 should be larger resistance value. To reduce falling switching time, R12 and R13 should have smaller resistance value. To increase falling switching time, R12 and R13 should be larger resistance value.

Please refer to schematics and layout for resistor connection and location.

# Application Note 4: How to Select Dongle and GUI

Qorvo has two dongles available.

1. Old dongle is "active semi," which works with the ACT43750 Customer GUI Rev0.2.
   - Dongle connector GND is aligned with the AGND pin of J11 as shown in Figure 3.
   - GUI PWM function is available.


Figure 3. Old dongle connection at J11

2. Dongle is "Qorvo Rev2.0", which works with ACT43750 Customer GUI Rev0.5
   a. Version 1

   - Dongle connector on PCB needs flip 180 deg.
   - Dongle connector (black wire) is aligned with the GPIO pin of J11.
   - Silk screen GND on the top of the right corner as shown in Figure 4
   - GUI PWM function is not available.


Figure 4. Dongle 2.0 version 1


Figure 5. Dongle 2.0 version 2

   b. Version 2

- Dongle connector on PCB doesn't need flip 180 deg.
- Dongle connector (black wire) is aligned with the AGND pin of J11.
- Silk screen GND at bottom of the right corner as shown in Figure 5.
- GUI PWM function is not available.

# Application Note 5: Drain Capacitance for RFPA Drain Switching Operation

Most RFPA evaluation kits are designed with a large drain capacitor to improve stability in CW. For RFPA drain switching operation, it should be careful to calculate the inrush current of the drain switch and ensure it is less than the drain current limit (OCP). The following formula can calculate the inrush peak current:

$$Ipk = Cd * \frac{dVd}{dtr}$$

Where:

Ipk – RF PA drain peak current, unit A.

Cd – Drain capacitance, unit F.

Vd – Drain voltage, unit V.

tr – Rising time of the drain voltage, unit s.

For an example, C=4.7uF, V=50v, t=10ns

Ipk=23500A

OCP is 12A. So, OCP protection will be triggered. ACT43750 will shut down the drain switching and get bias error.

To do the drain pulsing operation, we need to remove the big drain capacitor. We change the drain capacitor to 1000pF.

Ipk=5A

With the inrush peak current 5A, the drain switching can work well.

The rise time depends on the gate resistance R11. The default gate resistance R11=10Ω. The rise time is 10ns. The R11=100Ω, the rise time is 100ns.

# Application Note 6: ACT43750 Operation without I2C

ACT43750 can properly operate without I2C and GUI.  The enable gate, calibration, and enable/disable drain functions can be controlled by both standard GPIO inputs. The detailed startup sequence can be found in the datasheet "Typical Startup Procedure". The simplified startup sequence can be summarized as follows:

**Power up:**

1. RF PA input signal is off.
2. ENTX, ENCAL, and ENG digital input signals must be actively terminated low.
3. Apply 12V bias voltage.
4. Apply drain power supply.
5. 5V to ENG pin to turn on the gate. In EVK, put the jumper to J14. Vgate=-4.5V.
6. 5V to ENCAL pin to do the calibration. (Note, Make sure the RF PA is connected to the ACT43750EVK.) In EVK, put the jumper to J12. The drain switch is turned on in a short time and turned off. The gate voltage ramps up to the value to achieve the desired bias current. The gate voltage will keep the desired value. Remove 5V to ENCAL.
7. Apply 5V PWM signal to ENTX pin (J13) to turn on and off the drain voltage. (Refer to App note 5.)
8. RF PA input signal is on.

**Power off:**

1. RF PA input signal is off.
2. Pull ENTX pin to logic low.
3. Turn off the drain power supply
4. Turn off the 12V bias voltage.

## Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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