USER'S GUIDE

ACT43750EVK2 User's Guide

Description

This document describes the characteristics and operation of the Qorvo ACT43750EVK2 evaluation kit (EVK). It provides setup and operation instructions, schematic, layout, BOM, GUI, and test data. This EVK ships as a standalone board that can be evaluated independently or with a GaN RF FET. The EVK is used for Qorvo's QPD1004 GaN RF FET, but can be easily modified for other GaN FETs.

The ACT43750 is an integrated power solution that controls GaN RF FETs: Negative gate voltage, properly sequenced turn on and turn off, automatic gate voltage/drain current calibration, and drain voltage switching. It is an ideal solution for radio frequency (RF) power amplifiers (PAs) that demand fast transient, high current pulsed loads.

Features

Qorvo recommends that the user evaluate the EVK functionality with an RF PA and with the EVK connected to a PC running the graphical user interface (GUI) software. The GUI allows the user to enable/disable the outputs and to customize the exact voltage and current requirements for any specific RF PA being tested. The user can use the ACT43750 GUI to set the RF PA Idq bias current requirement, and the EVK autonomously finds and stores the optimal gate voltage for the Idq bias current. After finding the optimal gate bias voltage, the user can apply an RF signal to test the RF PA functionality.

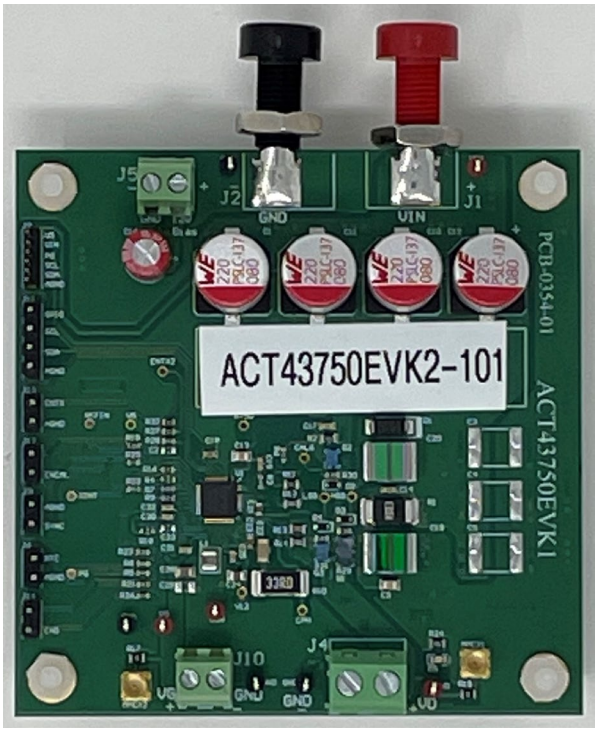


Figure 1. ACT43750EVK2 Board

EVK Contents

The EVK ships with the following:

- ACT43750EVK2 PCB
- USB-TO-I2C Dongle and cables
- The EVK does not ship with an RF PA

Figure 1 shows the ACT43750EVK2 board.

ACT43750EVK2 Board Overview

The ACT43750EVK2 generates the negative gate voltage required to drive a GaN FET RF PA. It generates this voltage from the 12V input bias voltage. It also provides the proper turn-on and turn-off sequencing between the gate and drain voltages. When Vg is commanded to turn on, the gate voltage will be -4.5V (default). Then, turning on auto-calibration finds Vg for the RF PA's Idq target. The user can search the Idq target in the RF PA datasheet. After Vg reaches the target value, the ACT43750 keeps this gate voltage. At this time, the user can apply an RF input to the RF PA. Note that RF is applied directly to the separate RF PA EVK PCB. The user can then apply a digital input to the EVK that enables the ACT43750 fast-switching drain circuit to enable RF PA drain switching. Note that the ACT43750 does not generate the Vd drain voltage but only passes it through from the input power source to the RF PA. The Vd output voltage can be turned on and off by applying a PWM signal to the EVK's ENTX connector.

APPENDIX

Application Note 1: Safe Operation at High Drain Switching Frequency

Application Note 2: How to Configure Bias Current and Current Limit

Application Note 3: How to Configure Drain Switching Time

Application Note 4: How to Select Dongle and GUI

Application Note 5: Drain Capacitance for RFPA Drain Switching Operation

Hardware Setup

Required Equipment

- ACT43750EVK2
- DC power supply - 10~65V @ 10A for full power operation
- DC power supply – 12V@ 1A
- Oscilloscope - 500MHz, 4 channels
- Function generator
- Current probe
- Digital Multi-meters (DMM)
- Windows compatible PC with spare USB port
- Qorvo USB-to-I^2C dongle
- Compatible GaN RF PA

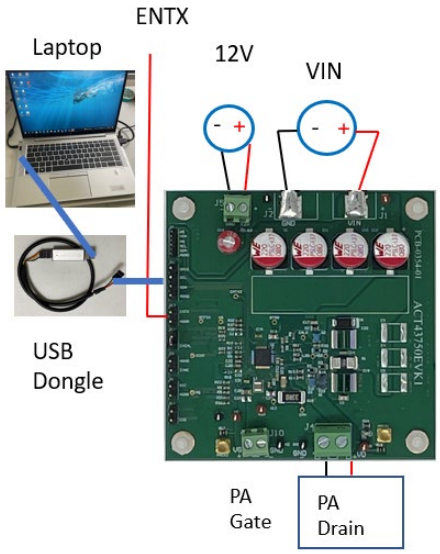


Figure 2. ACT43750EVK2 SET-UP

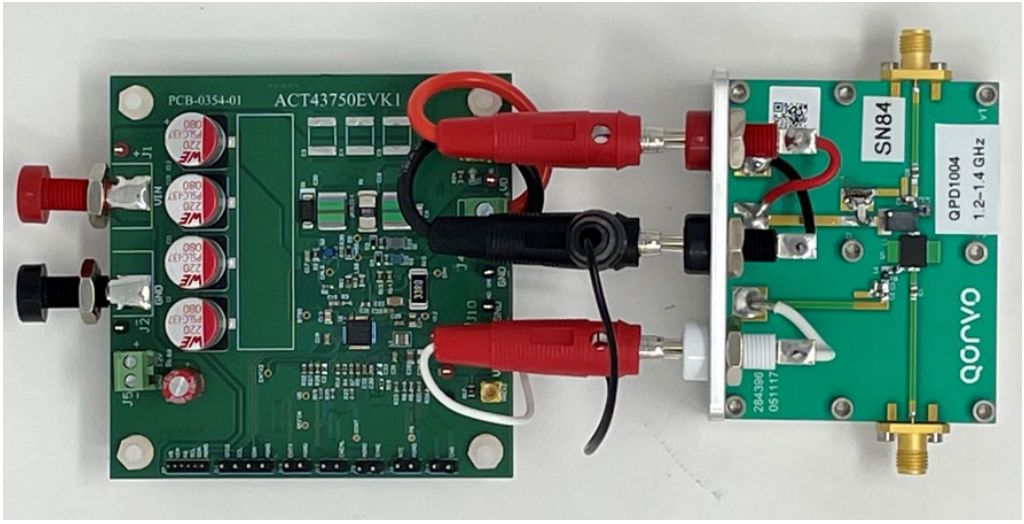


Figure 3. ACT43750EVK2 + QPD1004EVK SET-UP

Quick Start

Hardware Connections

Refer to Figure 2 & 3 for hardware connections.

1. Make all connections with power off.
2. Open the J12 (ENCAL) shorting jumper.
3. Open the J6 (NTC)
4. Open the J14 (ENG)
5. Connect the Qorvo USB-TO-I2C dongle cable to J11. The black wire connects to the AGND pin.
6. Optional: Connect a PWM generator to the J13 (ENTX) pin to AGND. The voltage level must be from 0V to 5V. Make sure the PWM generator is turned off. If an external PWM generator is not used, leave it open.
7. Connect a DC power supply between J1 (VIN) and J2 (GND). This is the voltage that is applied to the RF PA drain. Please use the required drain voltage for RF PA.
8. Connect a 12VDC power supply between J5 (V12) Bias and J5 (GND).
9. If testing a dummy resistor load
    a. Connect the resistor between VD and GND on J4.
10. If testing an RF PA
    a. Connect the RF PA Drain between VD and GND on J4.
    b. Connect the RF PA Gate between VG and GND on J10.
11. ENTX pin doesn't allow chattering. The drain switch can be turned on and off for DC testing by connecting a 5V lab supply or digital input to the J13 ENTX pin. It can also be controlled using the GUI. The drain switch can be turned on and off for pulsed testing by connecting a function generator to J13.
12. NTC Connection. Note that the EVK is configured with an on-board NTC that turns off the EVK if the temperature gets hotter than 85 deg C. This can be disabled by replacing NTC (R8) with a 5k resistor. If testing the EVK with an RF PA, the NTC can be placed on the RF PA and wired to the J6 NTC connector. Remember to remove R8 resistor for this external NTC option.

ACT43750 GUI Operation

GUI Setup

Refer to the end of this document for detailed instructions to install the ACT43750 Customer GUI.

ACT43750 GUI Operation

1. Select Basic for normal operation, see Figure 4.
2. Select Registers for view or change the register content
3. Click on the "Read" icon and confirm the GUI returns "Success"
4. Select Tool for I2C address

Configure the Settings

OCP current sense resistor setting

- Default current sense resistor is 3mΩ for typical 12A overcurrent protection.

Calibration current sense resistor setting

- Default calibration current sense resistor is 2Ω for 750mA bias current.

By entering the proper resistance (R2), the resulting bias current will display.

Note 1: Bias current can adjust +/- 31% digitally, Idq offset (%) button can do this function.

Note 2: If the bias current adjustment is larger than +/-31%, the calibration resistor must be changed.

Please refer to APP Note 2 for details.

Gate voltage control

- Default gate voltage is –4.5V
- Default min gate voltage is –4.5V and max gate voltage is –1.5V
- Gate voltage can be changed by drop down menu in setting

Note: Gate voltage can be changed when ENTX is low or PWM pulse operation. If ENTX is high, the gate voltage is not allowed to change.

- Auto calibration can be done after enabling Vgate

Drain voltage control

- Turn on /off drain switch by click Enable Vdrain
- "Enable Vdrain" is only for continuous operation of the drain switch
-

Steps to Enable the ACT43750

- Push Enable Vgate button
- Confirm the gate voltage is -4.5V

Steps to Enable the ACT43750 Autocalibration

- Push Enable Autocalibration button
- Confirm the gate voltage is around -2.6V

Steps to Enable/Disable the ACT43750 Drain Switch

- Push Enable Vdrain button
- Confirm the drain voltage is present
- Push this button again
- Confirm the drain voltage is zero

Note: " Enable Vdrain" function is only for continuous operation. For pulse operation, Apply PWM pulse to ENTX pin. Don't push this button.

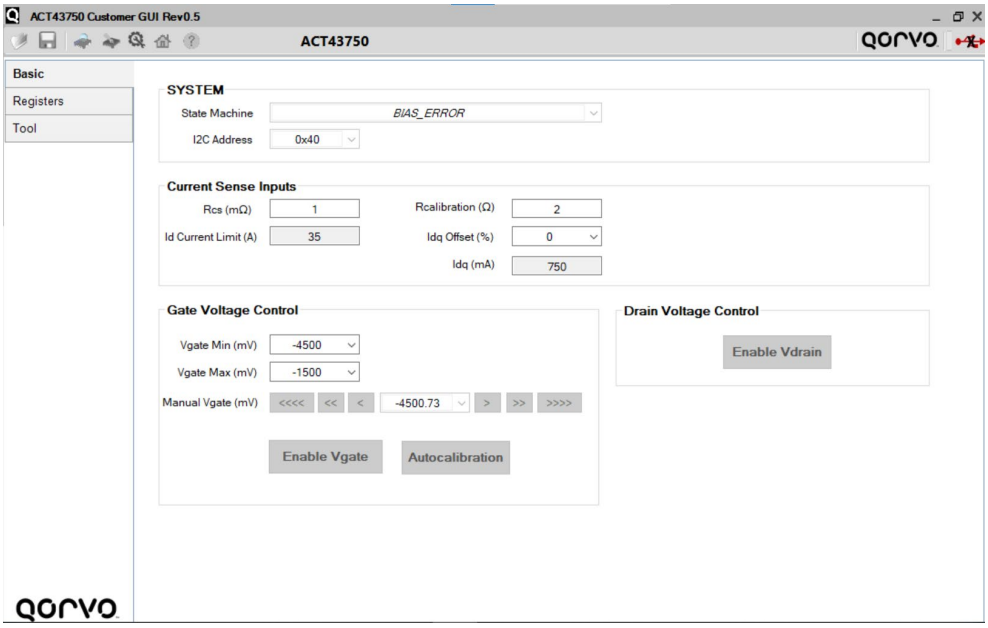


Figure 4. ACT43750EVK GUI interface

Recommended Operating Conditions

The ACT43750EVK1 operates with a 10V to 55V drain voltage and supports up to a 20A load.

Table 1. Recommended Operating Conditions for ACT43750

Parameter	Description	Min	Typ	Max	Unit
Vdrain	Drain voltage	10	50	55	V
Idrain	Drain current	0	-	10	A
Frequency	Drain pulsed frequency		100		Hz
V12V	12V DC bias	10.8	12	13.2	V
PWM On-Time		10	100	-	µs
Duty ratio			0.1		

ACT43750 Test Probing

Use DMM meter to measure input and output voltages at test points.

Use voltage probes to measure input voltage, gate and drain voltage waveforms at test points.

Use a current probe to measure the drain current waveforms.

ACT43750 Test Procedure

Warning:

- Devices may be damaged if the power up/power down procedure are not strictly followed.
- Don't touch the high voltage potentials: input voltage & output voltage terminals, test points, capacitors, and inductor.

Power up

1. Make sure the RF input signal is turned off.
2. Power on the 12V bias supply.
    a. The waveform at the VD test point should not be switching, and the 12V current is about 16mA.
3. Power on the 50V supply
    a. The waveform at the VD test point should still not be switching, and the current should be about 0mA.
4. Using the GUI, enable ACT43750 by pushing Enable Vgate. This sets the Vg voltage to -4.5V.
5. Enable the ACT43750 EVK drain switches by applying a pulsed voltage waveform to J13 and GND (ENTX). The pulse width on time should be greater than 10us. To limit the power dissipation of load devices, the typical duty ratio should be less than 10%. With sufficient heatsink for resistor load, the duty ratio can extend to 100%.
6. Measure the gate and drain voltage and drain current. The drain voltage will pulse at the same rate as the ENTX input signal. The drain current is determined by drain voltage and load.
7. Consider the load resistor power handling capability when setting the pulse duty cycle. We don't ship a resistor with EVK.
8. auto-calibration should be done after steps 1-4 if testing with RF Power. The gate voltage will increase to around negative 2.5V at bias current 50mA for QPD1004. If the bias current is much higher than the target due to the RFPA

temperature rise, the gate voltage can be increased slightly by GUI pull down menu to reduce the bias current until it's close to the target.

Note1: Calibration resistor change is necessary for certain dc bias current. Please refer to App Note 2.

Note 2: RFPA drain capacitor change is necessary. Please refer to App Note 5 for drain capacitance and drain switching operation.

9. Apply RF input signal for RFPA test.

Power down

1. If testing an RF PA with an RF input signal, disable the RF input.
2. Disable the drain switch by turning off the ENTX PWM pulses or using GUI
3. Power off 50V DC power supply.

   Note that the 50V DC supply must be turned off before the 12V bias supply
4. Power off 12V DC power supply

QPD1004EVB and ACT43750EVK2 System Test

RFPA QPD1004 is used as a load of ACT43750EVK2.

Note 1: Calibration resistor change is necessary for certain RFPA dc bias current. Please refer to App Note 2.

Note 2: RFPA drain capacitor change is necessary. Please refer to App Note 5 for drain capacitance and drain switching operation.

Note 3: For the high-frequency operation of RFPA, It's necessary to estimate the power loss of charge pump resistor R10. Please refer to App Note 1 for details.

Hardware connection

1. Connecting ACT43750 J10, Vg to Vgate of QPD1004 EVB in the Figure 3 & 5.
2. Connecting ACT43750 J4, VD to Vdrain of QPD1004 EVB in the Figure 3 & 5.
3. Connecting ACT43750 J10, J4 (GND) to GND of QPD1004 EVB in the Figure 3 & 5.
   - Make Vdrain cable as short and wide as possible.

Figure 5. QPD1004 EVB

QPD1004 Bias up

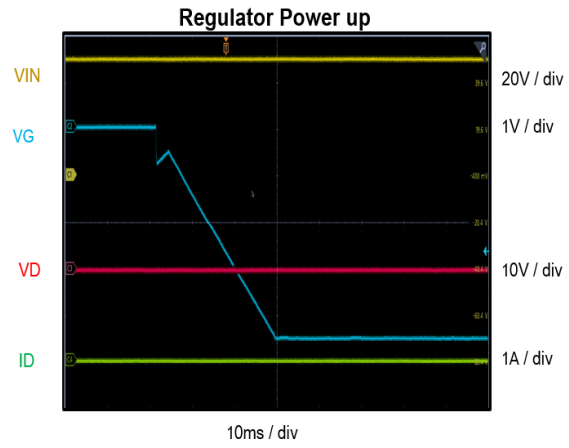
1. Make sure RF signal is off
2. Power up the ACT43750 12V bias supply
3. Power on 50V voltage source
4. Turn on VG to -4.5V by pushing Enable Vgate button
5. Do automatic calibration by pushing the Autocalibration button. The gate voltage should gradually rise to -2.5V.
   - Measure VG waveform to confirm VG change to -2.5V.
   - Adjust VG by GUI until the actual bias current is close to the target
6. Turn on/off the drain switch by applying a PWM pulse to the ENTX pin
   - Measure VD & ID waveform to confirm drain voltage & current pulse amplitude and frequency
7. Turn on RF signal

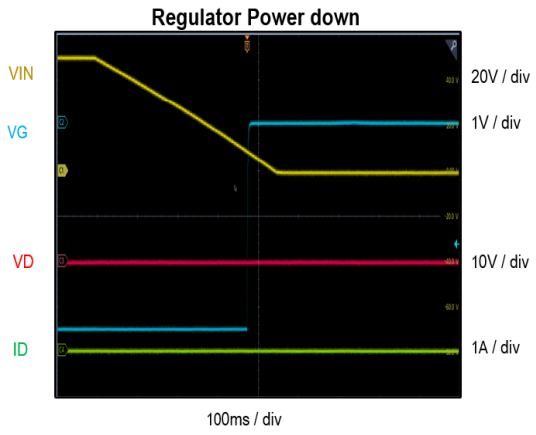
QPD1004 Bias Down

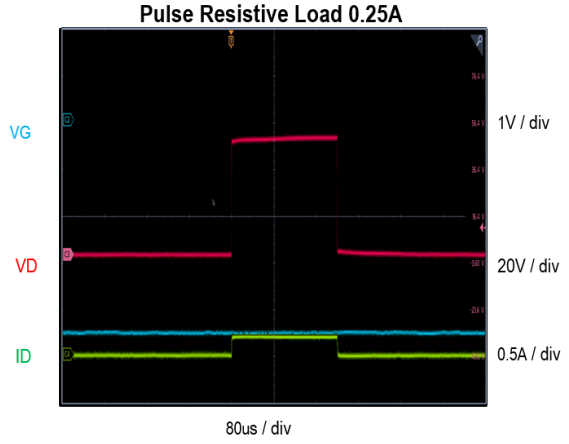
1. Turn off RF signal
2. Turn off the drain switch by pulling the ENTX pin to low logic level.
3. Adjust VG to –4.5V. Using GUI in Figure 4.
4. Measure VG to confirm it's -4.5V.
5. Power off the 50V voltage source
6. Wait for 2 seconds to discharge the drain voltage.
7. Turn off the 12V bias supply

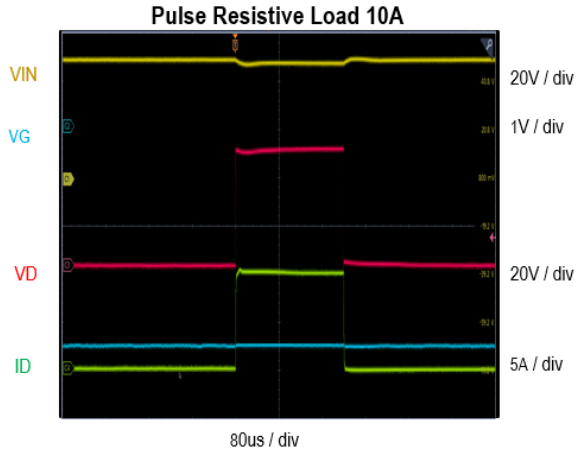
Test Results

Test condition, Input voltage=50V, Bias voltage=12V, Resistor load

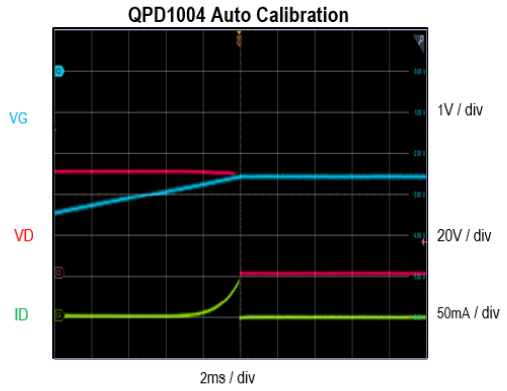








Test condition, Input voltage=50V, Bias voltage=12V, RFPA QPD1004



Schematic

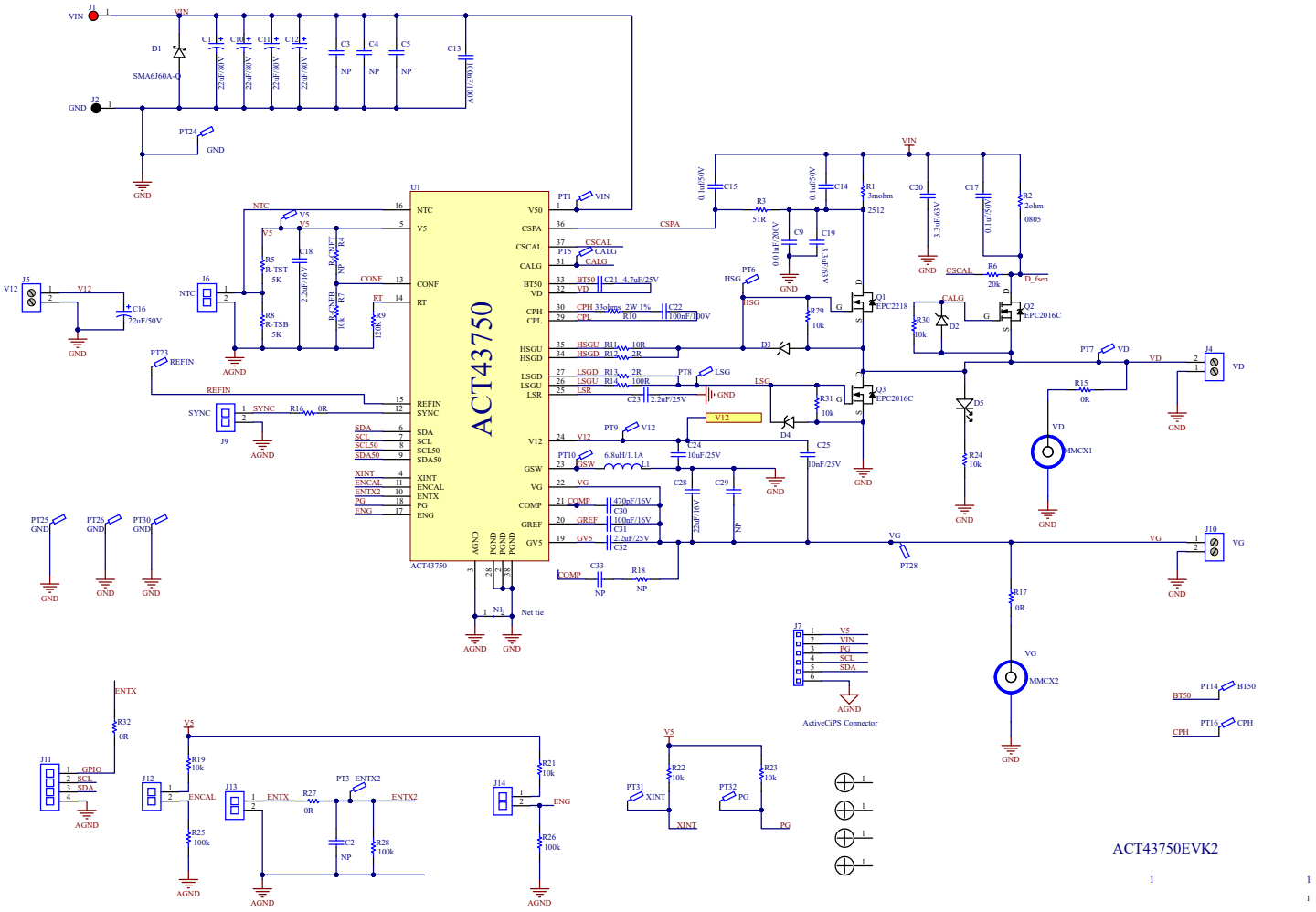


Figure 6. Schematic ACT43750EVK2

Layout

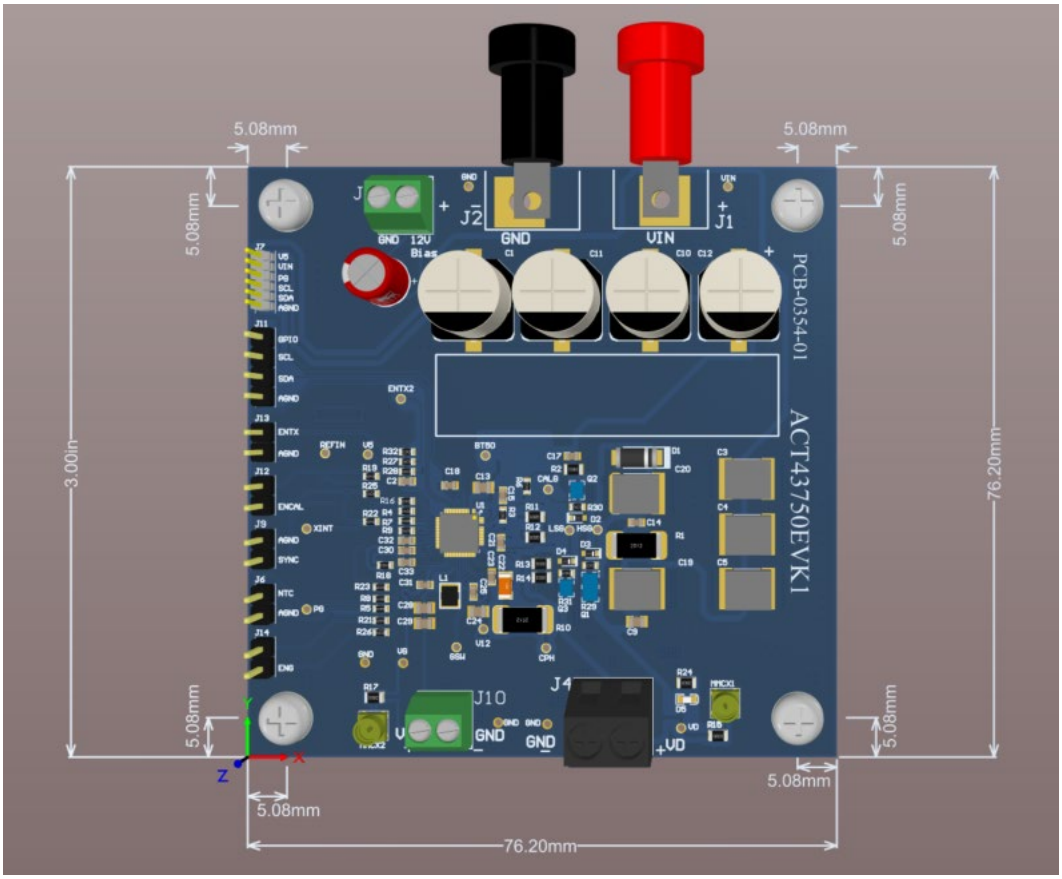


Figure 7. Assembly Top Layer

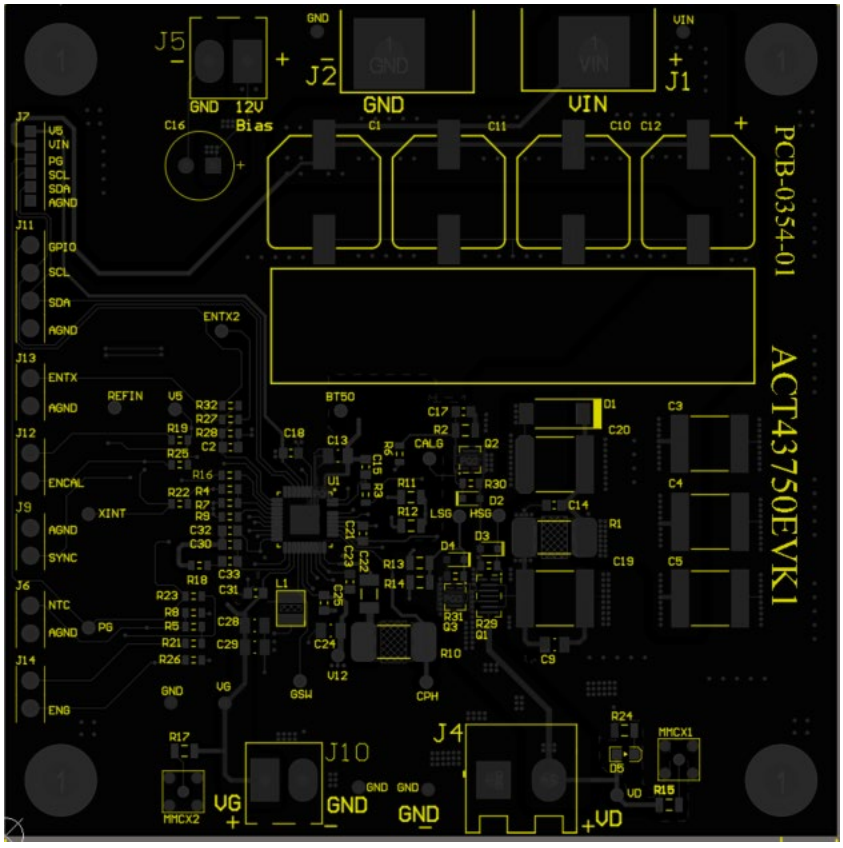


Figure 8. Top Layer Silk Screen

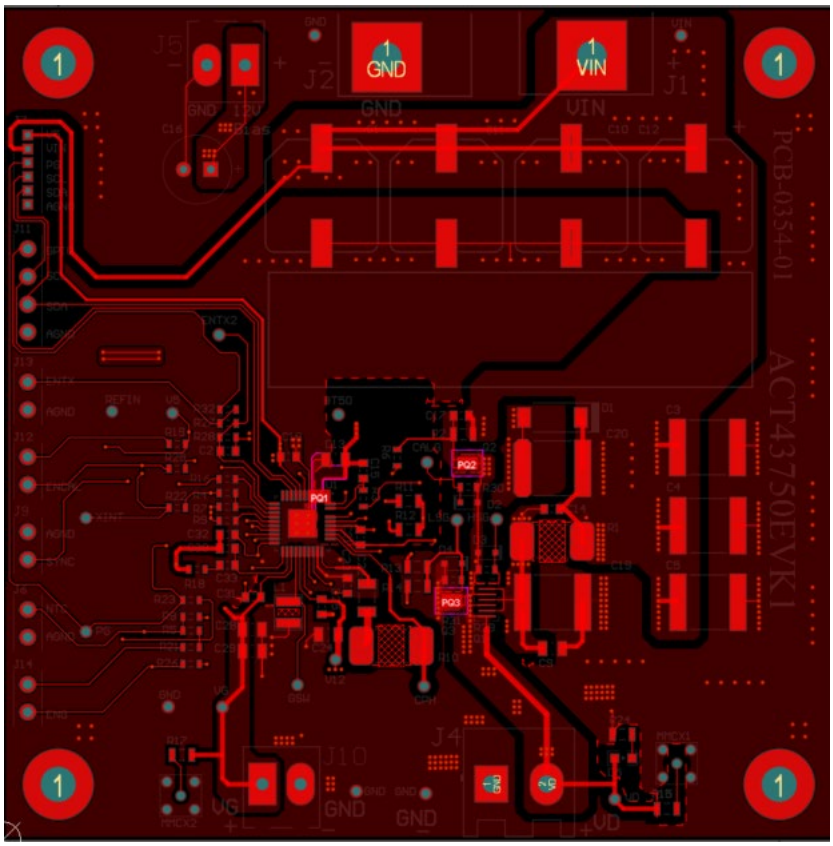


Figure 9. Layout Top Layer

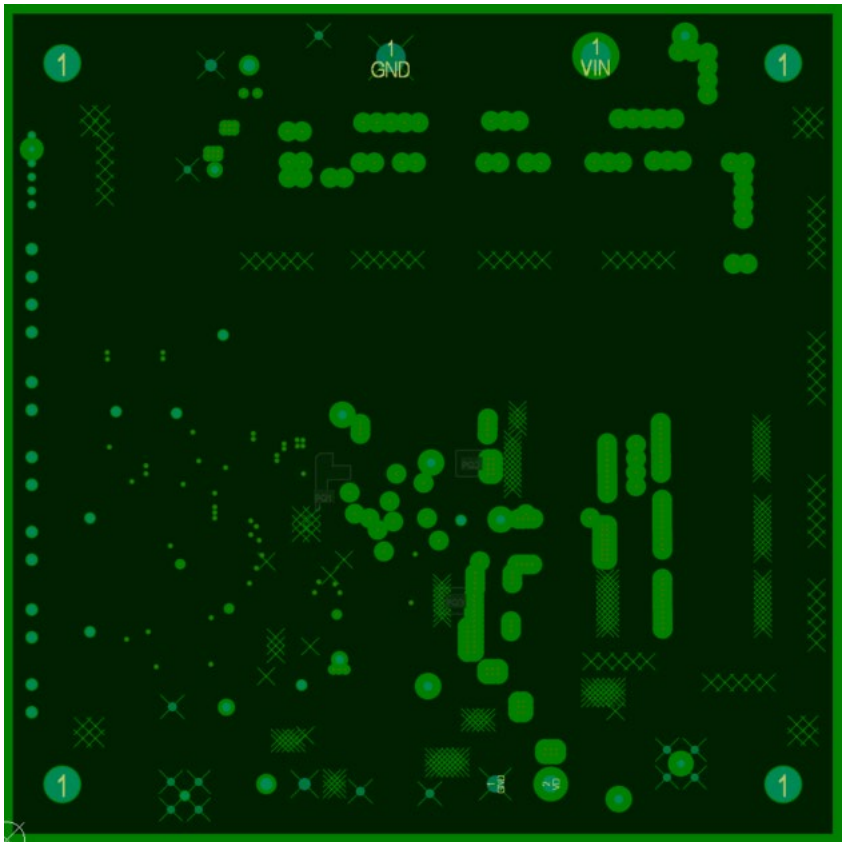


Figure 10. Layer 2 – GND Plane

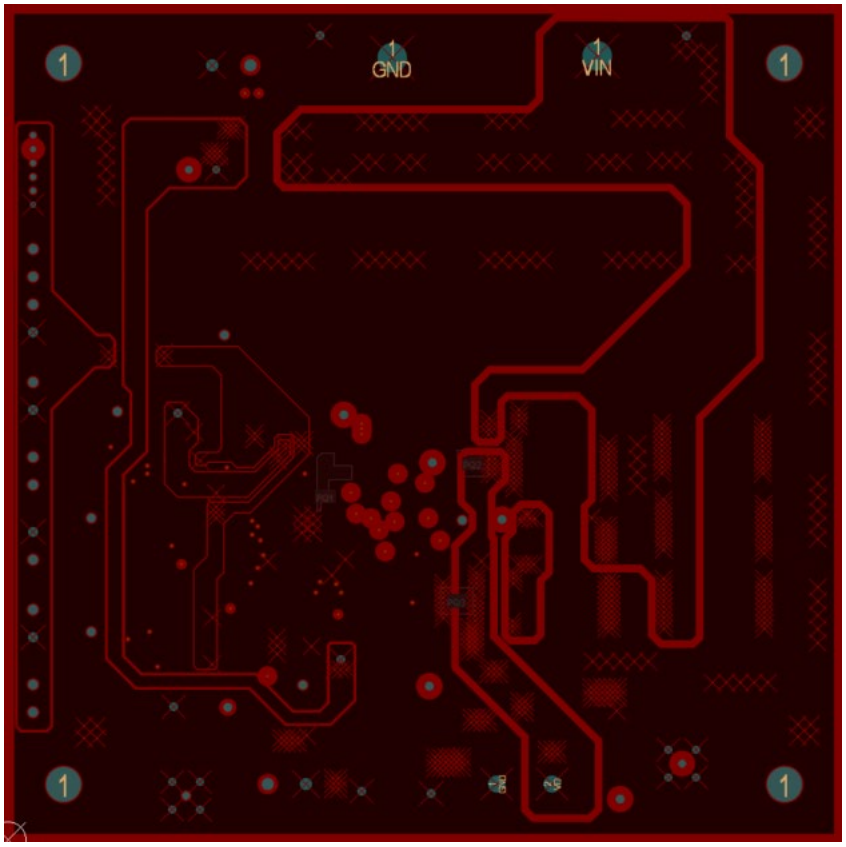


Figure 11. Layer 3 - GND Plane

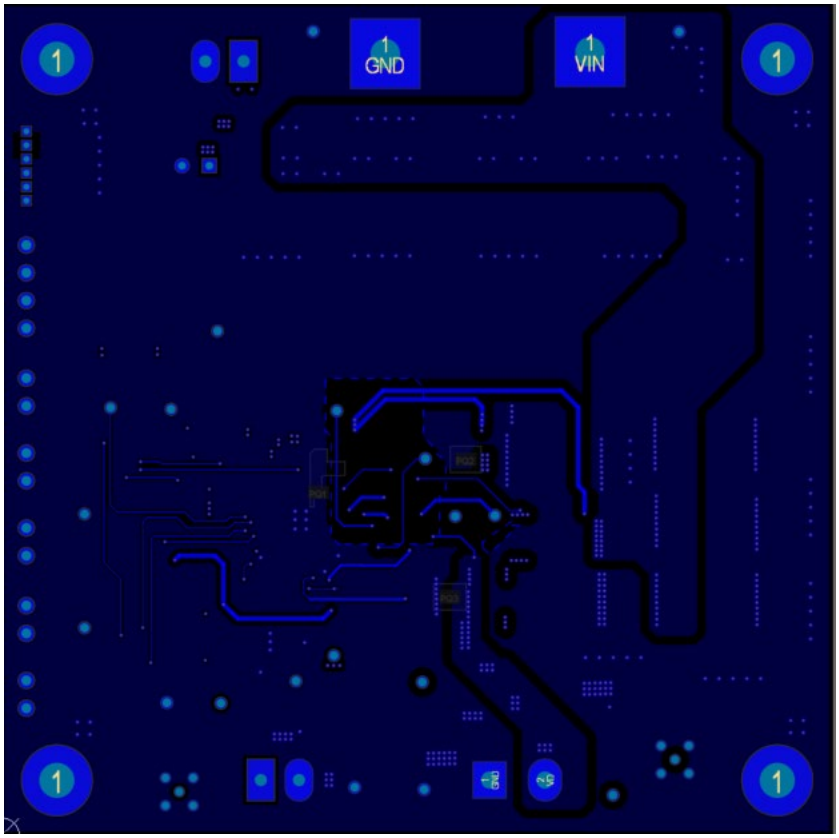


Figure 12. Layout Bottom Layer

Bill of Materials

ACT43750EVK2 BOM

Description	Designator	Footprint	Qty	Manufacturer	Part Number	Value	Comments
Capacitor, Aluminum	C1, C10, C11, C12	E-Cap_PCV_10x12.7	4	Nichicon or WE	PCV1K220MCL1GS or 875076161003	22uF/80V	Prefer WE
Capacitor, Ceramic,	C2	C0603_H	0	Standard	Standard	NP	
Capacitor, Aluminum	C16	WCAP-ATG5_6.3x11x2.5	1	WE	860130673002	22uF/50V	
Capacitor, Film Cap	C3, C4, C5	C2220_Film_CAP	0	Rubycon	63MU335MD35750	NP	
Capacitor, Film Cap	C19, C20	C2220_Film_CAP	2	Rubycon	63MU335MD35750	3.3uF/63V	
Capacitor, Ceramic,	C9	C0805_H	1	Standard	Standard	0.01uF/200V	
Capacitor, Ceramic,	C13	C0805_H	1	Murata Electronic	GCM21BR72A104KA37L	100nF/100V	
Capacitor, Ceramic,	C14, C15, C17	C0603_H	3	Standard	Standard	0.1uf/50V	
Capacitor, Ceramic,	C18	C0603_H	1	Standard	Standard	2.2uF/16V	
Capacitor, Ceramic,	C21	C0603_H	1	Standard	Standard	4.7uF/25V	
Capacitor, Ceramic,	C22	C1206_H	1	Standard	Standard	100nF/100V	
Capacitor, Ceramic,	C23	C0603_H	1	Standard	Standard	2.2uF/25V	
Capacitor, Ceramic,	C24	C0805_H	1	Standard	Standard	10uF/25V	
Capacitor, Ceramic,	C25	C0603_H	1	Standard	Standard	10nF/25V	
Capacitor, Ceramic,	C29	C0805_H	1	Standard	Standard	NP	
Capacitor, Ceramic,	C28	C0805_H	1	Standard	Standard	22uF/16V	
Capacitor,	C30	C0603_H	1	Standard	Standard	470pF/16V	

Ceramic,							
Capacitor, Ceramic,	C31	C0603_H	1	Standard	Standard	100nF/16V	
Capacitor, Ceramic,	C32	C0603_H	1	Standard	Standard	2.2uF/25V	
Capacitor, Ceramic,	C33	C0603_H	1	Standard	Standard	NP	
Diode, TVS	D1	DIODE,DO-213AB	1	Bourns	SMA6J60A-Q	66.7V Breakdown	
Diode, Zener	D2, D3, D4	DIODE,SOD-523	3	MCC	BZT52C5V1T-TP	Zener 5.1V	
Diode, Led, Green	D5	WL-SMCW_0603	1	Rohm	SMLD12EN1W	Led Green	5mA current
MACHINE SCREW	H1, H2, H3, H4	4-40	4	McMaster-Carr	92196A106	4-40	
CON, BANANA PLUG,RED	J1	CON, BANANA, CINCH	1	CINCH	108-0902-001	Banana plug red	
CON, BANANA PLUG, BLACK	J2	CON, BANANA, CINCH - BLACK	1	CINCH	108-0903-001	Banana plug black	
Connector, Screw Terminal, 5.08, 2P	J4	con,tbk,508-2p,molex-0395443002	1	WURTH	691236510002	5.08, 2P	
Connector, Screw Terminal, 1.27, 6P	J7	con, tbk, 1.27, 6p	1	Sullins	GRPB061VWVN-RC	1.27, 6P	
Connector, Screw Terminal, 3.50, 2P	J5, J10	con,tbk,350-2p,kf350	2	Wurth	691214110002S	3.50, 2P	
Header, Unshrouded , 2.54, Male, 2P	J6, J9, J12, J13, J14	con,hdr,254-2p	5	Wurth	61300211121	2.54, Male, 2P	
Header, Unshrouded , 2.54, Male, 4P	J11	con,hdr,254-4p	1	Wurth	61300411121	2.54, Male, 4P	
Inductor,	L1	L25xx_MAPI_R	1	Murata Electronic	DFE252010F-6R8M=P2	6.8uH/1.1A	

				s			
MMCX	MMCX1, MMCX2	MMCX THT	2	Taoglas limited TE	PCB.MMCXFSTJ.HT or 1_1634009_0		Prefer Taoglas
Test point (Red)	PT1, VIN	TSP, PROBE	1	Keystone	Testpoint 5000		
Test point (Red)	PT7 (VD)	TSP, PROBE	1	Keystone	Testpoint 5000		
Test point (Red)	PT10 (GSW)	TSP, PROBE	1	Keystone	Testpoint 5001		
Test point (Red)	PT28 (VG)	TSP, PROBE	1	Keystone	Testpoint 5000		
Test point (Black)	PT24, PT25, PT26, PT30 (GND)	TSP, PROBE	4	Keystone	Testpoint 5001		
MOSFET, Single,	Q1	GaN, FETs, EPC2218	1	EPC	EPC2218	100V/60A/2.4m Ohm	
MOSFET, Single,	Q2, Q3	GaN, FETs, EPC2016C	2	EPC	EPC2016C	100V/18A/12mO hm	
Resistor,	R1	R2512_L	1	Bourns	CRF2512-FZ-R003ELF	0.003 Ohms 2W 1%	
Resistor,	R2	R0805_H	1	Standard	Standard	2ohms 0.125W 1%	
Resistor,	R3	R0603_H	1	Standard	Standard	51.1	
Resistor,	R4	R0603_H	1	Standard	Standard	NP	
Resistor,	R5	R0603_H	1	Standard	Standard	5K	
Resistor,	R6	R0603_H	1	Standard	Standard	20k	
Resistor,	R7	R0603_H	1	Standard	Standard	10k	
Resistor,	R8	R0603_H	1	Standard	Standard	5k	
Resistor,	R9	R0603_H	1	Standard	Standard	120K	
Resistor,	R10	R2512_L	1	Bourns	CRM2512-FX-33R00ELF	33ohms 2W 1%	
Resistor,	R11	R0805_H	1	Standard	Standard	10R	
Resistor,	R14	R0805_H	1	Standard	Standard	100R	
Resistor,	R15, R17	R0805_H	2	Standard	Standard	0R	
Resistor,	R12, R13	R0805_H	2	Standard	Standard	2R	
Resistor,	R16	R0603_H	1	Standard	Standard	0R	

Resistor,	R18	R0603_H	1	Standard	Standard	NP	
Resistor,	R19, R21, R22, R23	R0603_H	4	Standard	Standard	10k	
Resistor,	R24	R0805_H	1	Standard	Standard	10k	
Resistor,	R25, R26, R28,	R0603_H	3	Standard	Standard	100k	
Resistor,	R27, R32	R0603_H	2	Standard	Standard	0R	
Resistor,	R29, R30, R31	R0603_H	3	Standard	Standard	10k	
PCB	PCB	PCB-0354-01	1	Standard	Standard	PCB-0354-01	
IC, ACT43750	U1	HP34_QFN37-5X5	1	Qorvo	ACT43750-101	ACT43750-101	

GUI Installation

1. Get GUI files from the Qorvo
2. Plug the Qorvo dongle USB-TO-I²C cable into a free USB port.
3. The USB driver will be automatically installed.
4. Double click on the ACT43750 Customer GUI Rev0.5.exe to start the ACT43750EVK.

Application Note 1: Safe Operation at High Drain Switching Frequency

ACT43750 is designed for operation at low drain switching frequency, typically less than 1kHz. For drain switching frequency is higher than 500Hz, the charge pump circuit component R10 may need to be upgraded. The reason is that the power loss of resistor R10 is proportional to the drain switching frequency, capacitance, and drain voltage square. The following formula can calculate the power loss of R10:

$$P = 0.5 * C * V^2 * F$$

Where:

P – power loss of charge pump resistor, unit W.

C – charge pump capacitance, the unit is F. It's C22 and 100nF in ACT43750 EVK.

R – charge pump resistance, the unit is ohm. It's R10 and 33ohm in ACT43750 EVK.

F – drain switching frequency, the unit is Hz

V – drain voltage, the unit is Volt. It's 50V in a typical application.

At drain switch frequency 1kHz, power loss is 0.125w. R10 is 2512 size resistor, and the power rating is 2w. It's OK for the original board design. When the drain switch frequency is much higher, R10 power loss is higher than the rating value. So, the R10 may need to be changed to a higher-power resistor.

The process to determine the component change is listed below:

Step 1, Calculate the power loss of R10 at the desirable drain switch frequency

Step 2, If the power loss is less than 1.5w, no action is needed; if it's higher than 1.5w, then go to the next step

Step 3, Find the resistors power rating that is higher than the requirement with a good margin

Step 3, Locate R10 in the board, and replace it with higher power resistors

For example, the frequency is 20KHz, P=2.5w. R10 must be larger size and higher power. It's recommended to stack 2pc 66ohm 2512 size resistor (4w) replace the original resistor.

Application Note 2: How to Configure Bias Current and Current Limit

Every RF PA has a specific dc bias drain current and drain current limit requirement.

1. DC Bias Drain Current

ACT43750 can provide setpoint +/- 31%, 1% step the drain current programming by I2C command. The register13 has 5 bits to change the setpoint. The adjustment detail can refer to Table 37 in the ACT43750 datasheet. The setting will be lost and returned to the default after the power recycle.

If the bias current adjustment is more than +/-31% setpoint, the calibration resistor R2 can be changed to get the right dc bias current. The following formula can calculate the calibration resistance.

$$R2 = 1.5V/Idq$$

Where:

Idq – RF PA dc bias current, unit A.

R2 – Calibration resistance, unit Ω.

2. Drain Current Limit

RF PA has the drain current limit to protect the device, and the current limit can be changed by resistor R1.

$$R1 = 35mV/ID$$

Where:

ID – RF PA drain current, unit A.

R1 – Current limit resistance, unit mΩ.

Please refer to the schematics and layout for resistor connection and location.

Application Note 3: How to Configure Drain Switching Time

The drain switching time is defined by the drain voltage rising and falling from 10% peak to 90% peak or 90% to 10% peak. The drain voltage VD switching transition time can be changed by adjusting gate resistance. The default rising switching time is 10ns and falling switching time is 10ns. R11 is 10Ω. R12 and R13 are 2Ω. A typical drain voltage and current switching transition waveforms are listed below.

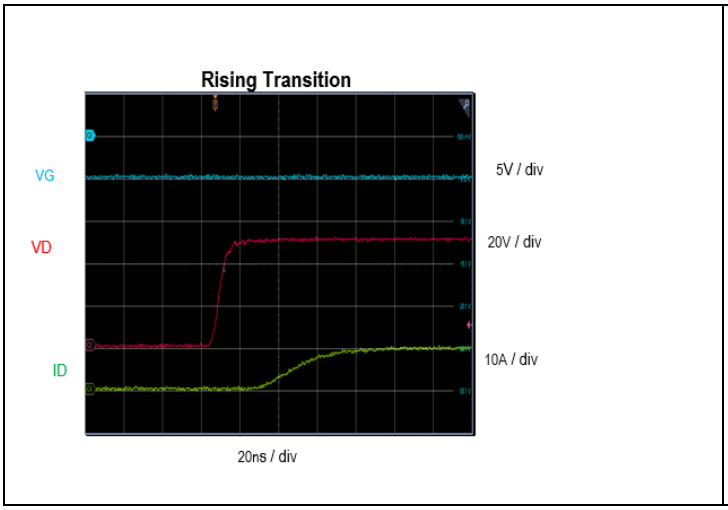


Figure 1. Rising Transition

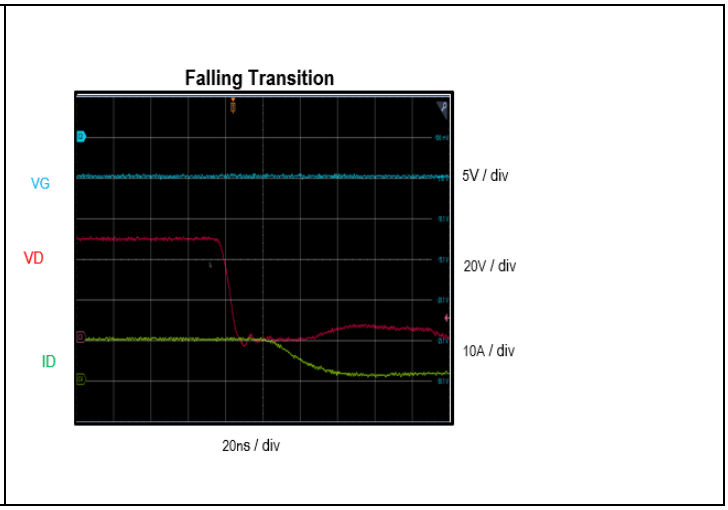


Figure 2. Falling Transition

To reduce rising switching time, R11 should be a smaller resistance value. To increase rising switching time, R11 should be larger resistance value. To reduce falling switching time, R12 and R13 should have smaller resistance value. To increase falling switching time, R12 and R13 should be larger resistance value.

Please refer to schematics and layout for resistor connection and location.

Application Note 4: How to Select Dongle and GUI

Qorvo has two dongles available.

1. Old dongle is "active semi," which works with the ACT43750 Customer GUI Rev0.2.
   - Dongle connector GND is aligned with the AGND pin of J11 as shown in Figure 3.
   - GUI PWM function is available.

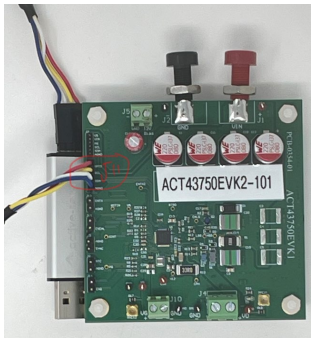


Figure 3. Old dongle connection at J11

2. Dongle is "Qorvo Rev2.0", which works with ACT43750 Customer GUI Rev0.5
   a. Version 1

   - Dongle connector on PCB needs flip 180 deg.
   - Dongle connector (black wire) is aligned with the GPIO pin of J11.
   - Silk screen GND on the top of the right corner as shown in Figure 4
   - GUI PWM function is not available.

Figure 4. Dongle 2.0 version 1

Figure 5. Dongle 2.0 version 2

   b. Version 2

- Dongle connector on PCB doesn't need flip 180 deg.
- Dongle connector (black wire) is aligned with the AGND pin of J11.
- Silk screen GND at bottom of the right corner as shown in Figure 5.
- GUI PWM function is not available.

Application Note 5: Drain Capacitance for RFPA Drain Switching Operation

Most RFPA evaluation kits are designed with a large drain capacitor to improve stability in CW. For RFPA drain switching operation, it should be careful to calculate the inrush current of the drain switch and ensure it is less than the drain current limit (OCP). The following formula can calculate the inrush peak current:

$$Ipk = Cd * \frac{dVd}{dtr}$$

Where:

Ipk – RF PA drain peak current, unit A.

Cd – Drain capacitance, unit F.

Vd – Drain voltage, unit V.

tr – Rising time of the drain voltage, unit s.

For an example, C=4.7uF, V=50v, t=10ns

Ipk=23500A

OCP is 12A. So, OCP protection will be triggered. ACT43750 will shut down the drain switching and get bias error.

To do the drain pulsing operation, we need to remove the big drain capacitor. We change the drain capacitor to 1000pF.

Ipk=5A

With the inrush peak current 5A, the drain switching can work well.

The rise time depends on the gate resistance R11. The default gate resistance R11=10Ω. The rise time is 10ns. The R11=100Ω, the rise time is 100ns.

Application Note 6: ACT43750 Operation without I2C

ACT43750 can properly operate without I2C and GUI. The enable gate, calibration, and enable/disable drain functions can be controlled by both standard GPIO inputs. The detailed startup sequence can be found in the datasheet "Typical Startup Procedure". The simplified startup sequence can be summarized as follows:

Power up:

1. RF PA input signal is off.
2. ENTX, ENCAL, and ENG digital input signals must be actively terminated low.
3. Apply 12V bias voltage.
4. Apply drain power supply.
5. 5V to ENG pin to turn on the gate. In EVK, put the jumper to J14. Vgate=-4.5V.
6. 5V to ENCAL pin to do the calibration. (Note, Make sure the RF PA is connected to the ACT43750EVK.) In EVK, put the jumper to J12. The drain switch is turned on in a short time and turned off. The gate voltage ramps up to the value to achieve the desired bias current. The gate voltage will keep the desired value. Remove 5V to ENCAL.
7. Apply 5V PWM signal to ENTX pin (J13) to turn on and off the drain voltage. (Refer to App note 5.)
8. RF PA input signal is on.

Power off:

1. RF PA input signal is off.
2. Pull ENTX pin to logic low.
3. Turn off the drain power supply
4. Turn off the 12V bias voltage.

Contact Information

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