

MOSFETs Silicon N-channel MOS (U-MOS X-H)

## TK9R6E15Q5

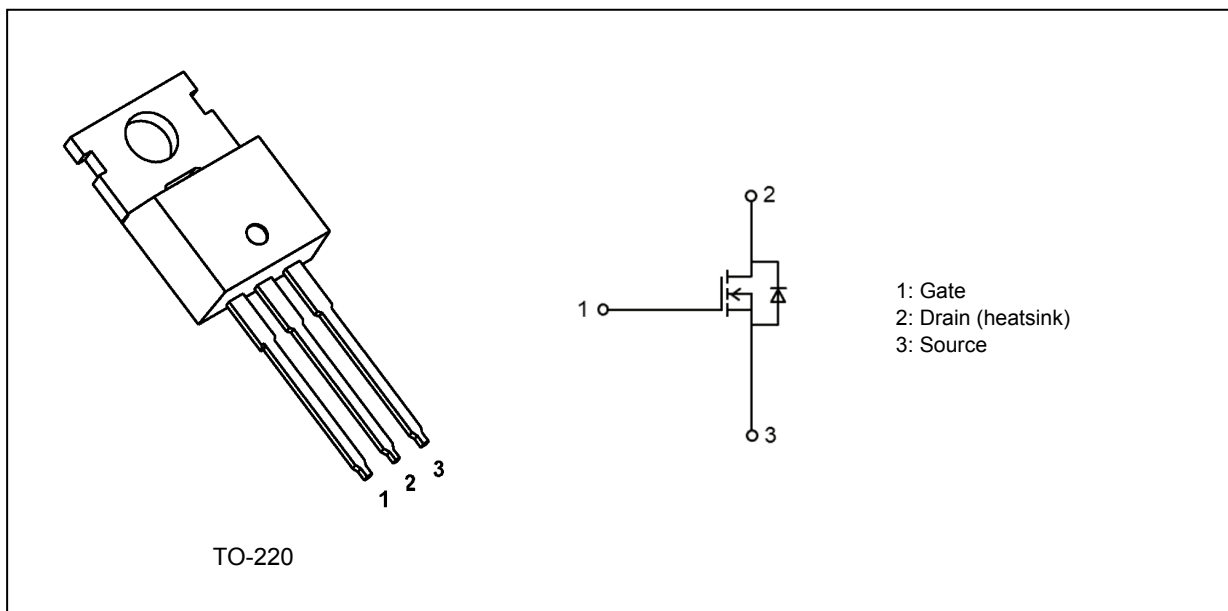
### 1. Applications

- High-Efficiency DC-DC Converters
- Switching Voltage Regulators
- Motor Drivers

### 2. Features

- (1) Fast reverse recovery time:  $t_{rr} = 40$  ns (typ.)
- (2) Small reverse recovery charge :  $Q_{rr} = 32$  nC (typ.)
- (3) Small gate charge:  $Q_{SW} = 17$  nC (typ.)
- (4) Low drain-source on-resistance:  $R_{DS(ON)} = 7.9$  m $\Omega$  (typ.) ( $V_{GS} = 10$  V)
- (5) Low leakage current:  $I_{DSS} = 10$   $\mu$ A (max) ( $V_{DS} = 150$  V)
- (6) Enhancement mode:  $V_{th} = 3.1$  to  $4.5$  V ( $V_{DS} = 10$  V,  $I_D = 1.1$  mA)

### 3. Packaging and Internal Circuit



Start of commercial production  
2024-07

## 4. Absolute Maximum Ratings (Note) ( $T_a = 25\text{ °C}$ unless otherwise specified)

| Characteristics  | Symbol    | Rating     | Unit               |
|--|-----------|------------|--------------------|
| Drain-source voltage   | $V_{DSS}$ | 150        | V                  |
| Gate-source voltage  | $V_{GSS}$ | $\pm 20$   |                    |
| Drain current (DC) ( $T_c = 25\text{ °C}$ ) (Note 1)             | $I_D$     | 52         | A                  |
| Drain current (DC) (Silicon limit) (Note 1), (Note 2)            | $I_D$     | 104        |                    |
| Drain current (pulsed) ( $t = 100\text{ }\mu\text{s}$ ) (Note 1) | $I_{DP}$  | 250        |                    |
| Power dissipation ( $T_c = 25\text{ °C}$ )                       | $P_D$     | 200        | W                  |
| Single-pulse avalanche energy (Note 3)                           | $E_{AS}$  | 55         | mJ                 |
| Single-pulse avalanche current (Note 3)                          | $I_{AS}$  | 52         | A                  |
| Channel temperature  | $T_{ch}$  | 175        | $^{\circ}\text{C}$ |
| Storage temperature  | $T_{stg}$ | -55 to 175 | $^{\circ}\text{C}$ |
| Mounting torque  | TOR       | 0.6        | N · m              |

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

## 5. Thermal Characteristics

| Characteristics  | Symbol         | Max  | Unit                        |
|--|----------------|------|-----------------------------|
| Channel-to-case thermal resistance ( $T_c = 25\text{ °C}$ )    | $R_{th(ch-c)}$ | 0.73 | $^{\circ}\text{C}/\text{W}$ |
| Channel-to-ambient thermal resistance ( $T_a = 25\text{ °C}$ ) | $R_{th(ch-a)}$ | 83.3 |                             |

Note 1: Ensure that the channel temperature does not exceed 175  $^{\circ}\text{C}$ .

Note 2: Limited by silicon chip capability.

Note 3:  $V_{DD} = 100\text{ V}$ ,  $T_{ch} = 25\text{ °C}$  (initial),  $L = 20\text{ }\mu\text{H}$ ,  $I_{AS} = 52\text{ A}$

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

### 6. Electrical Characteristics

#### 6.1. Static Characteristics ( $T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

| Characteristics                         | Symbol        | Test Condition                                  | Min | Typ. | Max       | Unit             |
|---|---------------|---|-----|------|-----------|------------------|
| Gate leakage current                    | $I_{GSS}$     | $V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$ | —   | —    | $\pm 0.1$ | $\mu\text{A}$    |
| Drain cut-off current                   | $I_{DSS}$     | $V_{DS} = 150\text{ V}, V_{GS} = 0\text{ V}$    | —   | —    | 10        |                  |
| Drain-source breakdown voltage          | $V_{(BR)DSS}$ | $I_D = 10\text{ mA}, V_{GS} = 0\text{ V}$       | 150 | —    | —         | V                |
| Drain-source breakdown voltage (Note 4) | $V_{(BR)DSX}$ | $I_D = 10\text{ mA}, V_{GS} = -20\text{ V}$     | 130 | —    | —         |                  |
| Gate threshold voltage                  | $V_{th}$      | $V_{DS} = 10\text{ V}, I_D = 1.1\text{ mA}$     | 3.1 | —    | 4.5       |                  |
| Drain-source on-resistance              | $R_{DS(ON)}$  | $V_{GS} = 8\text{ V}, I_D = 20\text{ A}$        | —   | 8.5  | 11.5      | $\text{m}\Omega$ |
|   |               | $V_{GS} = 10\text{ V}, I_D = 26\text{ A}$       | —   | 7.9  | 9.6       |                  |

Note 4: If a reverse bias is applied between gate and source, this device enters  $V_{(BR)DSX}$  mode. Note that the drain-source breakdown voltage is lowered in this mode.

#### 6.2. Dynamic Characteristics ( $T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

| Characteristics                | Symbol    | Test Condition  | Min | Typ. | Max | Unit        |
|--------------------------------|-----------|---|-----|------|-----|-------------|
| Input capacitance              | $C_{iss}$ | $V_{DS} = 75\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$ | —   | 3690 | —   | $\text{pF}$ |
| Reverse transfer capacitance   | $C_{rss}$ |   | —   | 23   | —   |             |
| Output capacitance             | $C_{oss}$ |   | —   | 770  | —   |             |
| Gate resistance                | $r_g$     | —   | —   | 1.6  | 2.4 | $\Omega$    |
| Switching time (rise time)     | $t_r$     | See Fig. 6.2.1  | —   | 48   | —   | ns          |
| Switching time (turn-on time)  | $t_{on}$  |   | —   | 76   | —   |             |
| Switching time (fall time)     | $t_f$     |   | —   | 40   | —   |             |
| Switching time (turn-off time) | $t_{off}$ |   | —   | 74   | —   |             |

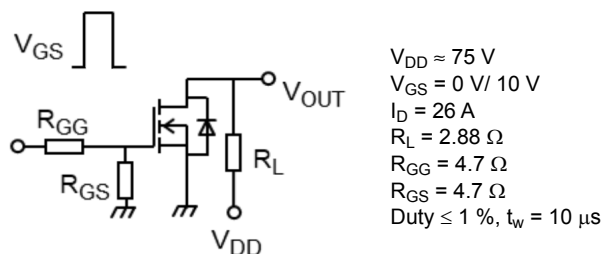


Fig. 6.2.1 Switching Time Test Circuit

#### 6.3. Gate Charge Characteristics ( $T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

| Characteristics                                 | Symbol    | Test Condition  | Min | Typ. | Max | Unit |
|---|-----------|---|-----|------|-----|------|
| Total gate charge (gate-source plus gate-drain) | $Q_g$     | $V_{DD} \approx 75\text{ V}, V_{GS} = 10\text{ V}, I_D = 26\text{ A}$ | —   | 50   | —   | nC   |
|   |           | $V_{DD} \approx 75\text{ V}, V_{GS} = 8\text{ V}, I_D = 20\text{ A}$  | —   | 40   | —   |      |
| Gate-source charge 1                            | $Q_{gs1}$ | $V_{DD} \approx 75\text{ V}, V_{GS} = 10\text{ V}, I_D = 26\text{ A}$ | —   | 24   | —   |      |
| Gate-drain charge                               | $Q_{gd}$  |   | —   | 8.7  | —   |      |
| Gate switch charge                              | $Q_{sw}$  |   | —   | 17   | —   |      |
| Output charge                                   | $Q_{oss}$ | $V_{DS} = 75\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$         | —   | 97   | —   |      |

## 6.4. Source-Drain Characteristics ( $T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

| Characteristics                         | Symbol  | Test Condition   | Min | Typ. | Max  | Unit |
|---|---|--|-----|------|------|------|
| Reverse drain current (pulsed) (Note 5) | $I_{DRP}$<br>( $t = 100\text{ }\mu\text{s}$ ) | —  | —   | —    | 250  | A    |
| Diode forward voltage                   | $V_{DSF}$                                     | $I_{DR} = 26\text{ A}, V_{GS} = 0\text{ V}$  | —   | —    | -1.2 | V    |
| Reverse recovery time (Note 6)          | $t_{rr}$                                      | $I_{DR} = 13\text{ A}, V_{GS} = 0\text{ V},$<br>$-di_{DR}/dt = 100\text{ A}/\mu\text{s}$ | —   | 40   | 60   | ns   |
| Reverse recovery charge (Note 6)        | $Q_{rr}$                                      |  | —   | 32   | 72   | nC   |

Note 5: Ensure that the channel temperature does not exceed  $175\text{ }^\circ\text{C}$ .

Note 6: Defined by design.

## 7. Marking

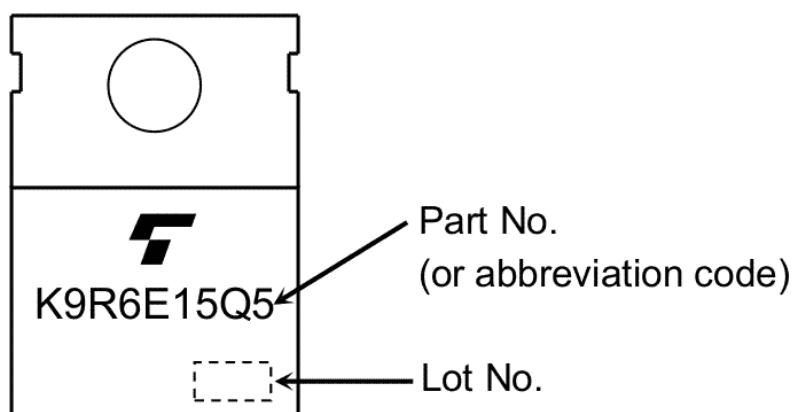


Fig. 7.1 Marking

## 8. Characteristics Curves (Note)

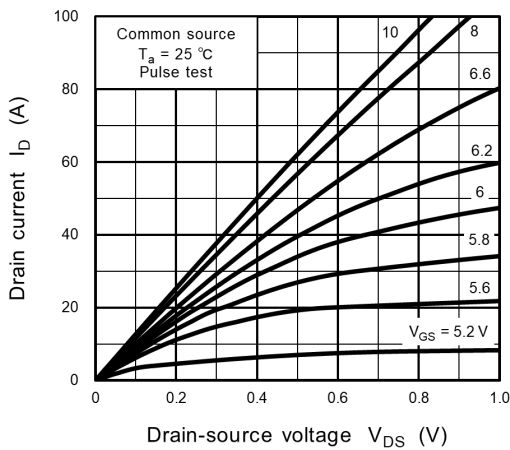


Fig. 8.1  $I_D - V_{DS}$

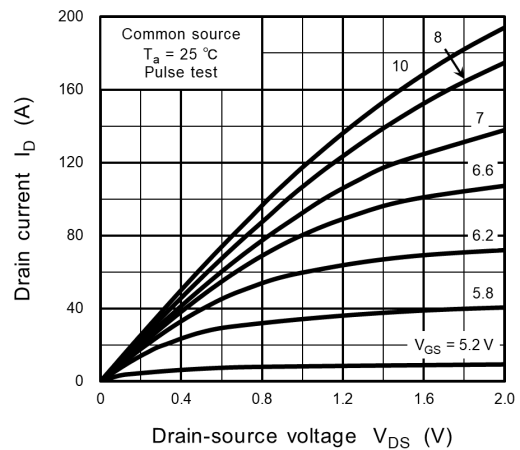


Fig. 8.2  $I_D - V_{DS}$

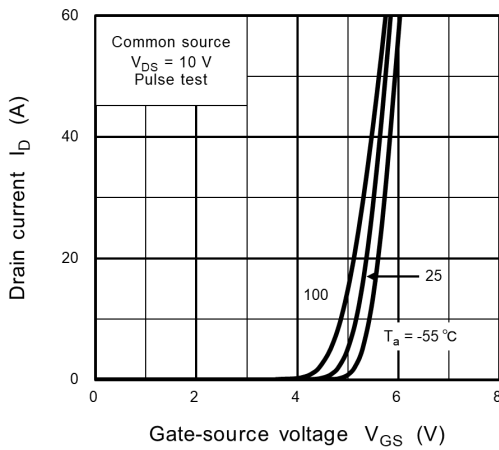


Fig. 8.3  $I_D - V_{GS}$

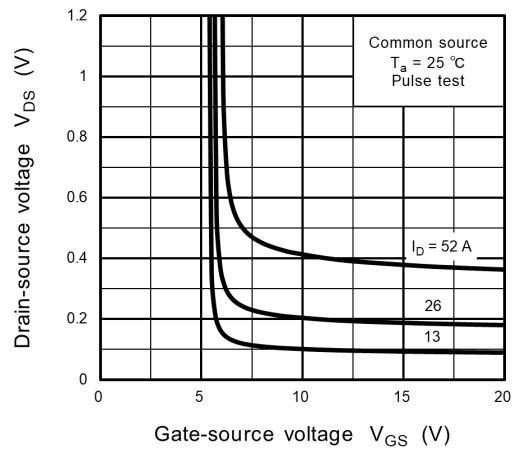


Fig. 8.4  $V_{DS} - V_{GS}$

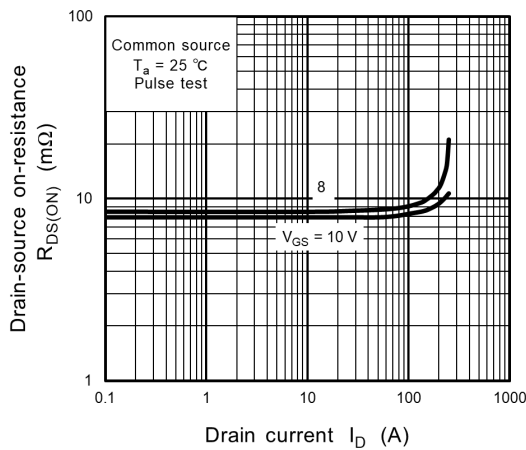


Fig. 8.5  $R_{DS(ON)} - I_D$

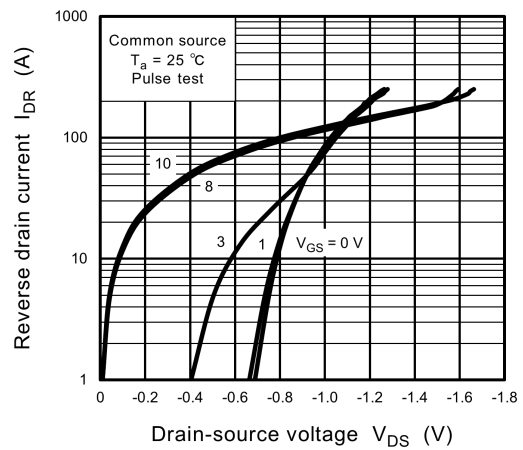
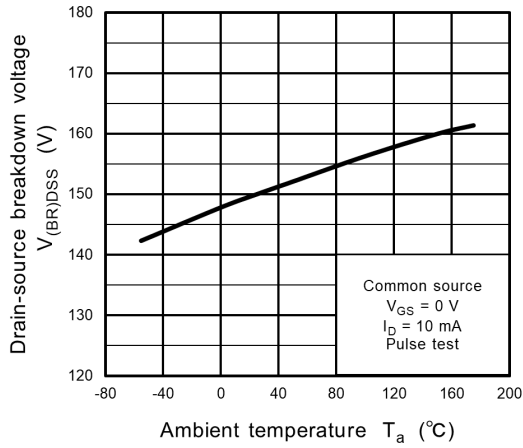
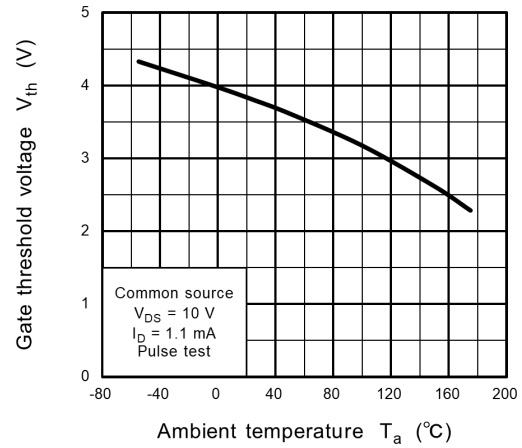


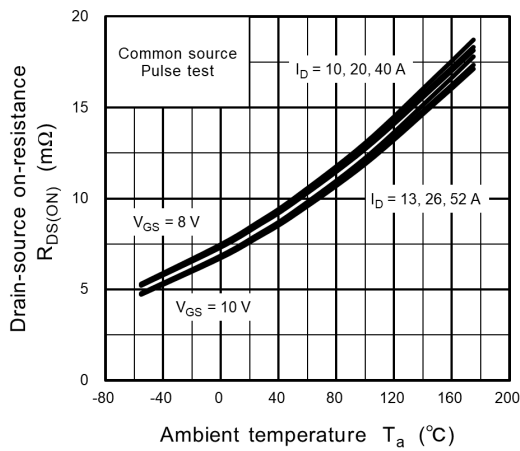
Fig. 8.6  $I_{DR} - V_{DS}$



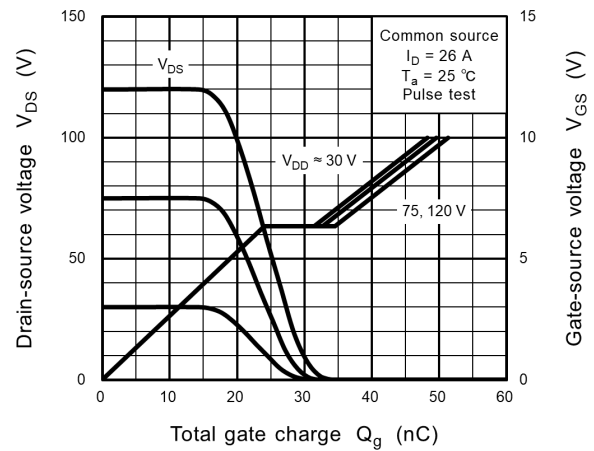
**Fig. 8.7  $V_{(BR)DSS} - T_a$**



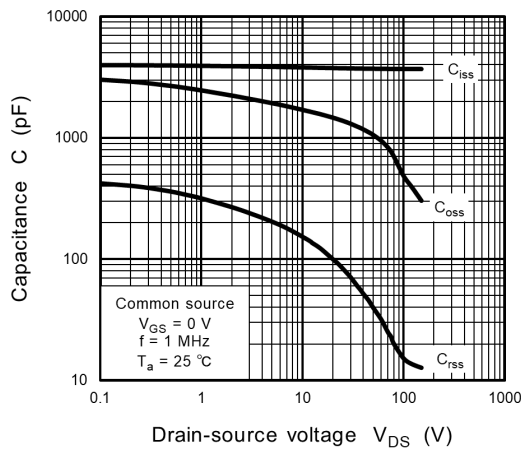
**Fig. 8.8  $V_{th} - T_a$**



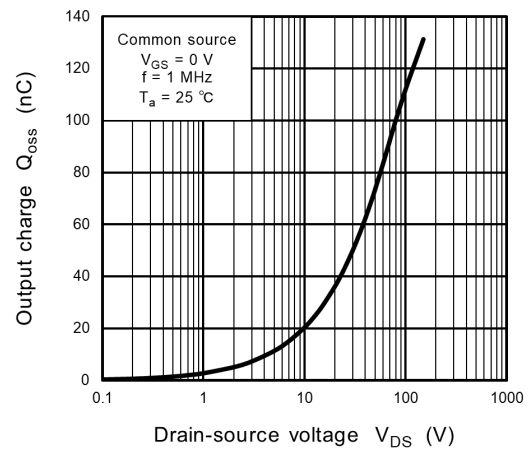
**Fig. 8.9  $R_{DS(ON)} - T_a$**



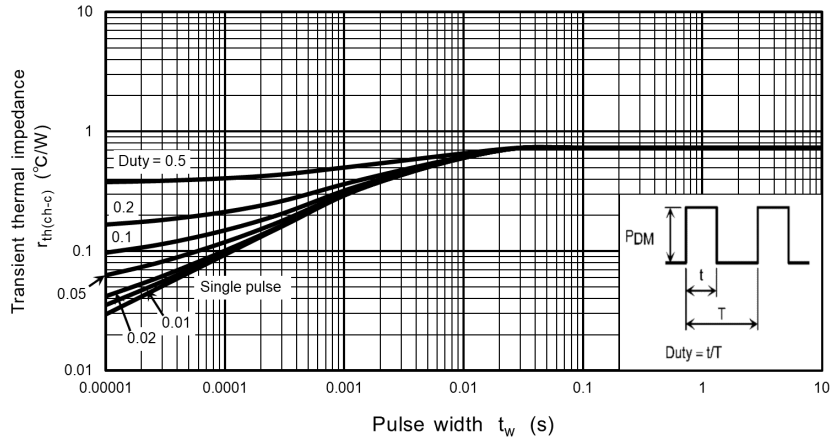
**Fig. 8.10 Dynamic Input/Output Characteristics**



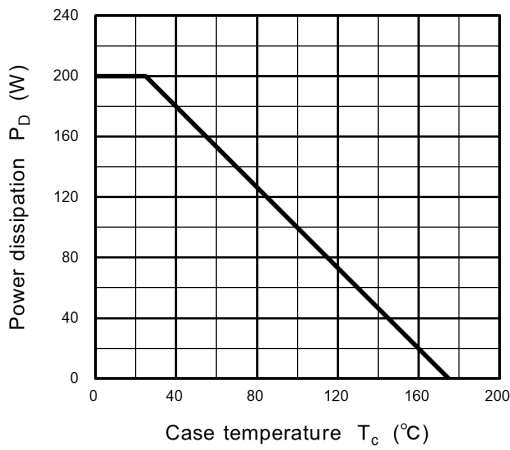
**Fig. 8.11 Capacitance -  $V_{DS}$**



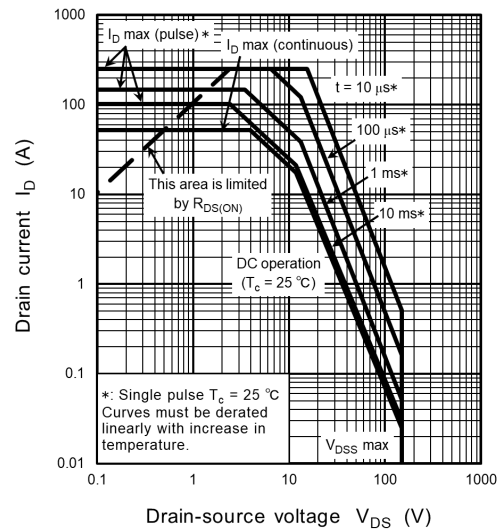
**Fig. 8.12  $Q_{oss} - V_{DS}$**



**Fig. 8.13  $r_{th} - t_w$**   
(Guaranteed Maximum)



**Fig. 8.14  $P_D - T_c$**   
(Guaranteed Maximum)

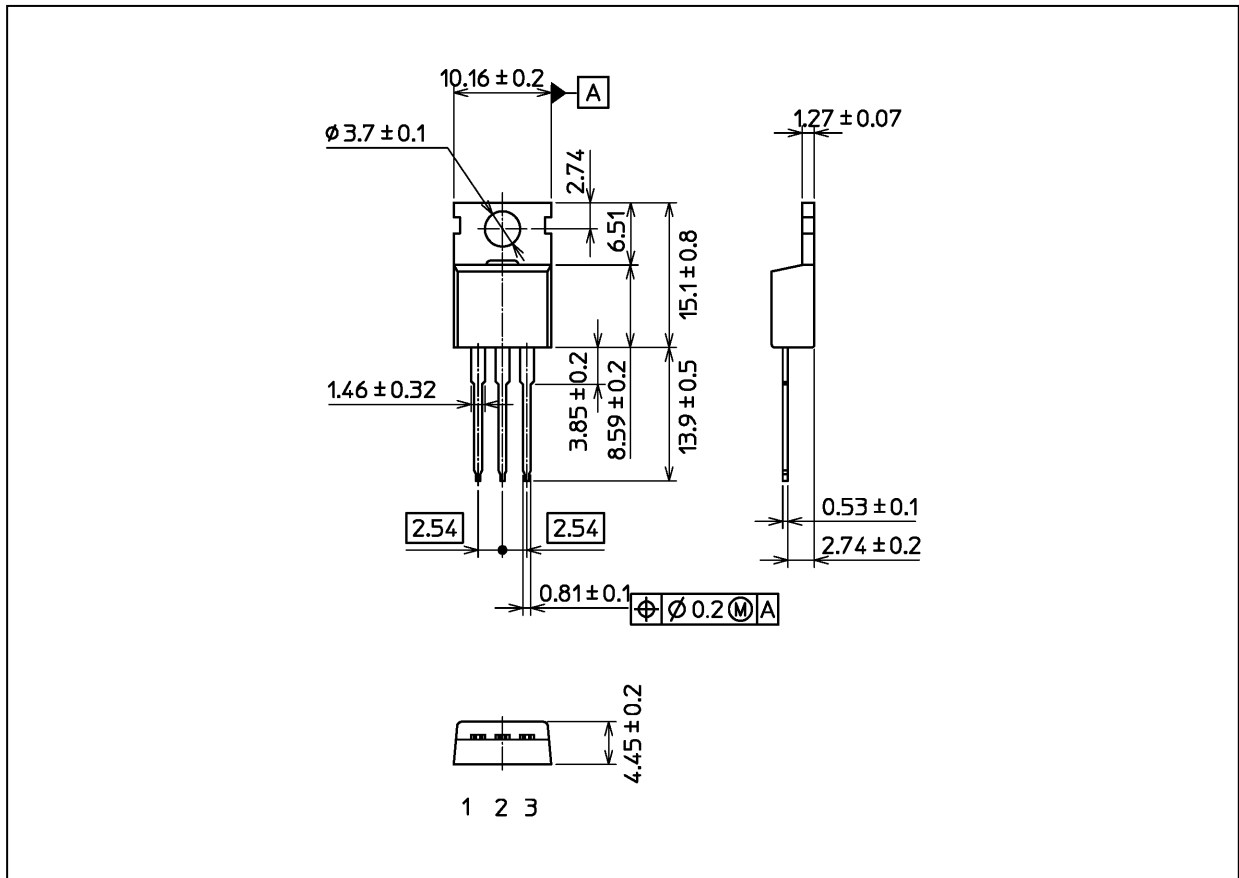


**Fig. 8.15 Safe Operating Area**  
(Guaranteed Maximum)

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

## Package Dimensions

Unit: mm



Weight: 1.96 g (typ.)

| Package Name(s)  |
|------------------|
| TOSHIBA: 2-10X1A |
| Nickname: TO-220 |



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