LM5002 High Voltage Switch Mode Regulator

Check for Samples: LM5002

FEATURES

- **Integrated 75 Volt N-Channel MOSFET**
- **Ultra-Wide Input Voltage Range from 3.1V to 75V**
- **Integrated High Voltage Bias Regulator**
- **Adjustable Output Voltage**
- **1.5% Output Voltage Accuracy**
- **Current Mode Control with Selectable Compensation**
- **Wide Bandwidth Error Amplifier**
- **Integrated Current Sensing and Limiting**
- **Integrated Slope Compensation**
- **85% Maximum Duty Cycle Limit**
- **Single Resistor Oscillator Programming**
- **Oscillator Synchronization Capability**
- **Enable / Undervoltage Lockout (UVLO) Pin**
- **Thermal Shutdown**

DESCRIPTION

The LM5002 high voltage switch mode regulator features all of the functions necessary to implement efficient high voltage Boost, Flyback, SEPIC and Forward converters, using few external components. This easy to use regulator integrates a 75 Volt N-Channel MOSFET with a 0.5 Amp peak current limit. Current mode control provides inherently simple loop compensation and line-voltage feed-forward for superior rejection of input transients. The switching frequency is set with a single resistor and is programmable up to 1.5MHz. The oscillator can also be synchronized to an external clock. Additional protection features include: current limit, thermal shutdown, under-voltage lockout and remote shutdown capability. The device is available in both SOIC-8 and WSON-8 packages.

Packages

- SOIC-8
- WSON-8 (4mm x 4mm)

Typical Application Circuit

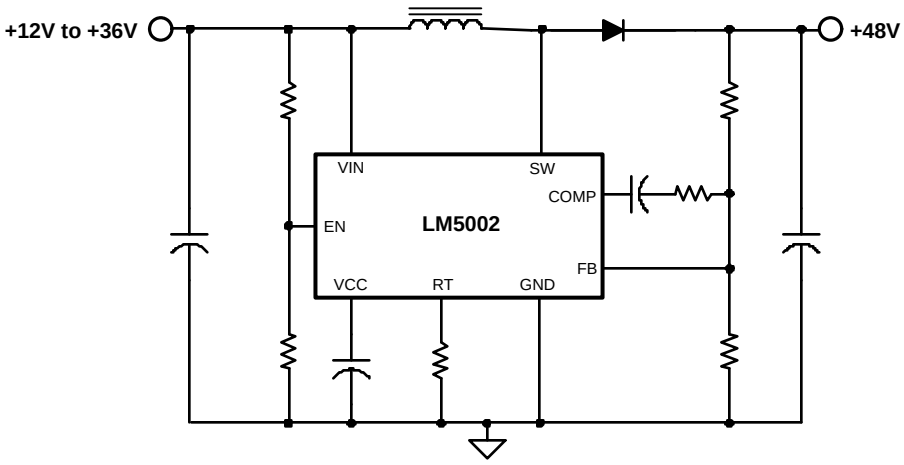


Figure 1. Boost Regulator Application Schematic

Connection Diagram

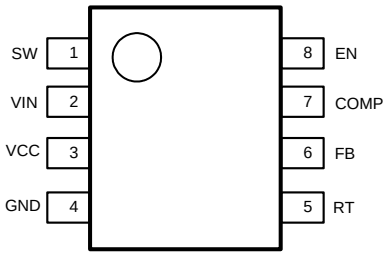


Figure 2. SOIC-8 Package
Top View

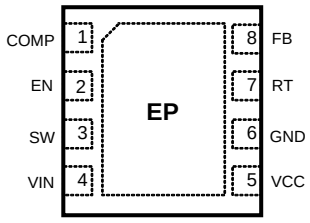


Figure 3. WSON-8 Package
Top View

PIN DESCRIPTIONS

Pin		Name	Description	Application Information
SOIC	WSON			
1	3	SW	Switch pin	The drain terminal of the internal power MOSFET.
2	4	VIN	Input supply pin	Nominal operating range: 3.1V to 75V.
3	5	VCC	Bias regulator output, or input for external bias supply	VCC tracks VIN up to 6.9V. Above VIN = 6.9V, VCC is regulated to 6.9 Volts. A 0.47 µF or greater ceramic decoupling capacitor is required. An external voltage (7V – 12V) can be applied to this pin which disables the internal VCC regulator to reduce internal power dissipation and improve converter efficiency.
4	6	GND	Ground	Internal reference for the regulator control functions and the power MOSFET current sense resistor connection.
5	7	RT	Oscillator frequency programming and optional synchronization pulse input	The internal oscillator is set with a resistor, between this pin and the GND pin. The recommended frequency range is 50KHz to 1.5 MHz. The RT pin can accept synchronization pulses from an external clock. A 100 pF capacitor is recommended for coupling the synchronizing clock to the RT pin.
6	8	FB	Feedback input from the regulated output voltage	This pin is connected to the inverting input of the internal error amplifier. The 1.26V reference is internally connected to the non-inverting input of the error amplifier.
7	1	COMP	Open drain output of the internal error amplifier	The loop compensation network should be connected between the COMP pin and the FB pin. COMP pull-up is provided by an internal 5 kΩ resistor which may be used to bias an opto-coupler transistor (while FB is grounded) for isolated ground applications.
8	2	EN	Enable / Under Voltage Lock-Out / Shutdown input	An external voltage divider can be used to set the line undervoltage lockout threshold. If the EN pin is left unconnected, a 6 µA pull-up current source pulls the EN pin high to enable the regulator.
NA	EP	EP	Exposed Pad, WSON only	Exposed metal pad on the underside of the package with a resistive connection to pin 6. It is recommended to connect this pad to the PC board ground plane in order to improve heat dissipation.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

VIN to GND		76V
SW to GND (Steady State)		-0.3V to 76V
VCC, EN to GND		14V
COMP, FB, RT to GND		-0.3V to 7V
Maximum Junction Temperature		150°C
Storage Temperature		−65°C to +150°C
ESD Rating[3]	Human Body Model	2kV

(1) Absolute maximum ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is intended to be functional, but device parameter specifications may not be ensured. For ensured specifications and test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin. Test Method is per JESD-22-A114.

Operating Conditions

VIN	3.1V to 75V
Operating Junction Temperature	−40°C to +125°C

Electrical Characteristics

Limits in standard type are for T_J = 25°C only; limits in **boldface type** apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are ensured through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. V_{VIN} = 10V, R_{RT} = 48.7kΩ unless otherwise stated[1].

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STARTUP REGULATOR						
$V_{VCC-REG}$	VCC Regulator Output		**6.55**	6.85	**7.15**	V
	VCC Current Limit	V_{VCC} = 6V	**15**	20		mA
	VCC UVLO Threshold	V_{VCC} increasing	**2.6**	2.8	**3**	V
	VCC Undervoltage Hysteresis			0.1		V
	Bias Current (I_{IN})	V_{FB} = 1.5V		3.1	**4.5**	mA
I_Q	Shutdown Current (I_{IN})	V_{EN} = 0V		95	**130**	µA
EN THRESHOLDS						
	EN Shutdown Threshold	V_{EN} increasing	**0.25**	0.45	**0.65**	V
	EN Shutdown Hysteresis			0.1		V
	EN Standby Threshold	V_{EN} increasing	**1.2**	1.26	**1.32**	V
	EN Standby Hysteresis			0.1		V
	EN Current Source			6		µA
MOSFET CHARACTERISTICS						
	MOSFET $R_{DS(ON)}$ plus Current Sense Resistance	I_D = 0.25A		850	**1600**	mΩ
	MOSFET Leakage Current	V_{SW} = 75V		0.05	**5**	µA
	MOSFET Gate Charge	V_{VCC} = 6.9V		2.4		nC
CURRENT LIMIT						
I_{LIM}	Cycle by Cycle Current Limit		**0.4**	0.5	**0.6**	A
	Cycle by Cycle Current Limit Delay			100	**200**	ns

(1) Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate TI's Average Outgoing Quality Level (AOQL).

Electrical Characteristics (continued)

Limits in standard type are for T_J = 25°C only; limits in **boldface type** apply over the junction temperature (T_J) range of -40°C to +125°C. Minimum and Maximum limits are ensured through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. V_{VIN} = 10V, R_{RT} = 48.7kΩ unless otherwise stated(1).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OSCILLATOR						
F_{SW1}	Frequency1	R_{RT} = 48.7 kΩ	**225**	260	**295**	KHz
F_{SW2}	Frequency2	R_{RT} = 15.8 kΩ	**660**	780	**900**	KHz
$V_{RT-SYNC}$	SYNC Threshold		**2.2**	2.6	**3.2**	V
	SYNC Pulse Width Minimum	$V_{RT} > V_{RT-SYNC}$ + 0.5V		15		ns
PWM COMPARATOR						
	Maximum Duty Cycle		**80**	85	**90**	%
	Min On-time	$V_{COMP} > V_{COMP-OS}$		25		ns
	Min On-time	$V_{COMP} < V_{COMP-OS}$		0		ns
$V_{COMP-OS}$	COMP to PWM Comparator Offset		**0.9**	1.30	**1.55**	V
ERROR AMPLIFIER						
V_{FB-REF}	Feedback Reference Voltage	Internal reference $V_{FB} = V_{COMP}$	**1.241**	1.260	**1.279**	V
	FB Bias Current			10		nA
	DC Gain			72		dB
	COMP Sink Current	V_{COMP} = 250mV	**2.5**			mA
	COMP Short Circuit Current	V_{FB} = 0, V_{COMP} = 0	**0.9**	1.2	**1.5**	mA
	COMP Open Circuit Voltage	V_{FB} = 0	**4.8**	5.5	**6.2**	V
	COMP to SW Delay			42		ns
	Unity Gain Bandwidth			3		MHz
THERMAL SHUTDOWN						
T_{SD}	Thermal Shutdown Threshold			165		°C
	Thermal Shutdown Hysteresis			20		°C
THERMAL RESISTANCE						
θ_{JC}	Junction to Case, SOIC-8			32		°C/W
θ_{JA}	Junction to Ambient, SOIC-8			140		°C/W
θ_{JC}	Junction to Case, WSON-8			4.5		°C/W
θ_{JA}	Junction to Ambient, WSON-8			40		°C/W

Typical Performance Characteristics

Efficiency, Boost Converter

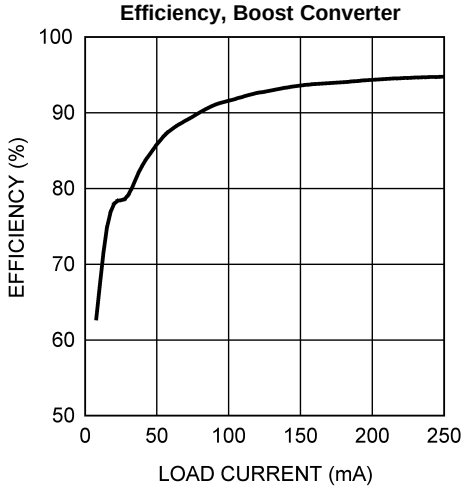


Figure 4.

V_{FB} vs Temperature

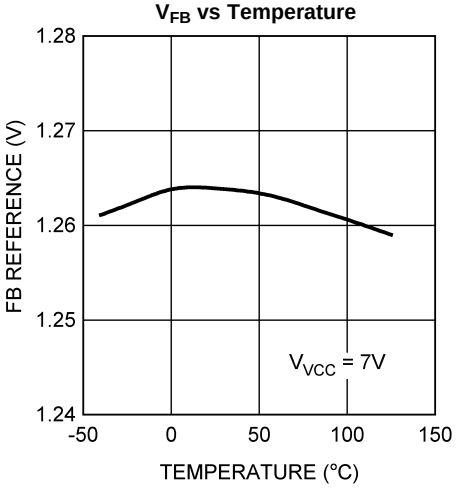


Figure 5.

I_Q (non-switching) vs V_{IN}

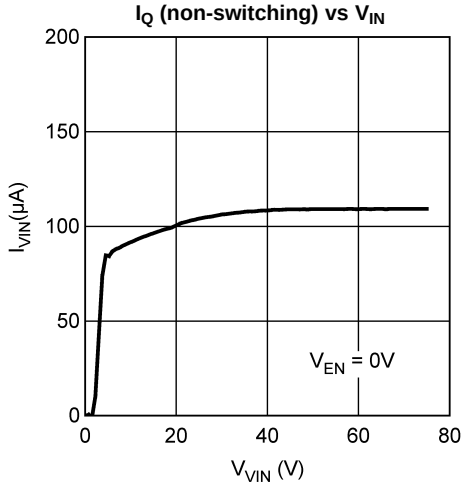


Figure 6.

V_{CC} vs V_{IN}

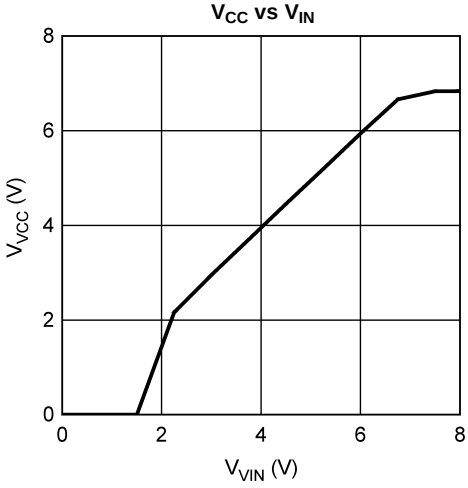


Figure 7.

$R_{DS(ON)}$ vs V_{CC}

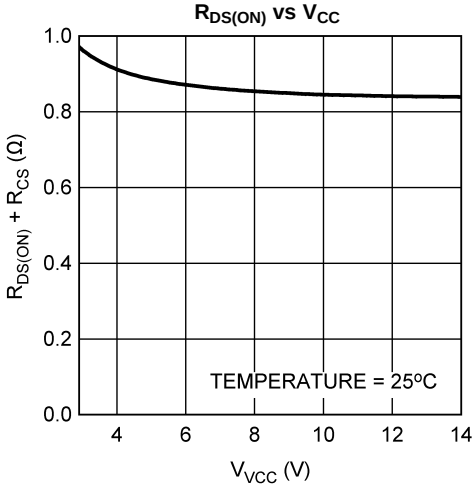


Figure 8.

$R_{DS(ON)}$ vs Temperature

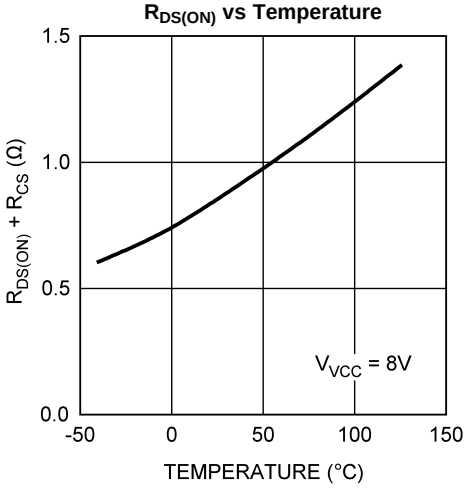


Figure 9.

Typical Performance Characteristics (continued)

I_{LIM} vs V_{CC}

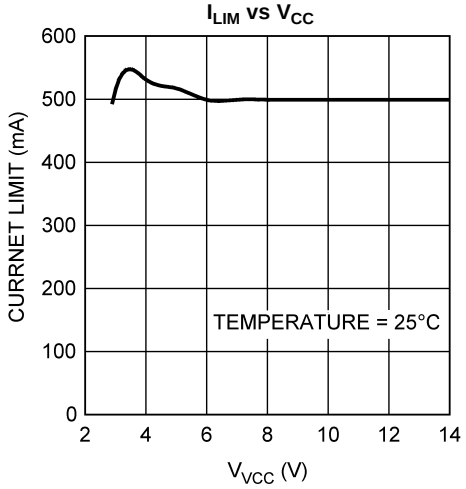


Figure 10.

I_{LIM} vs V_{CC} vs Temperature

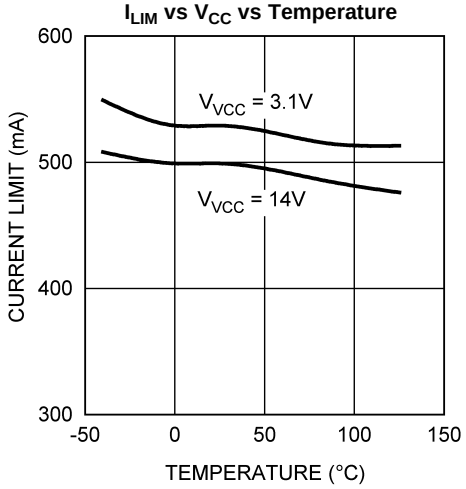


Figure 11.

F_{SW} vs R_{RT}

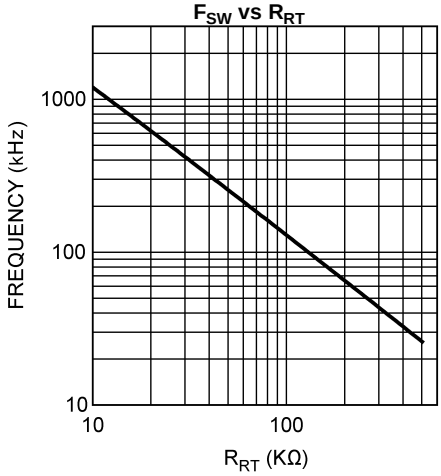


Figure 12.

F_{SW} vs Temperature

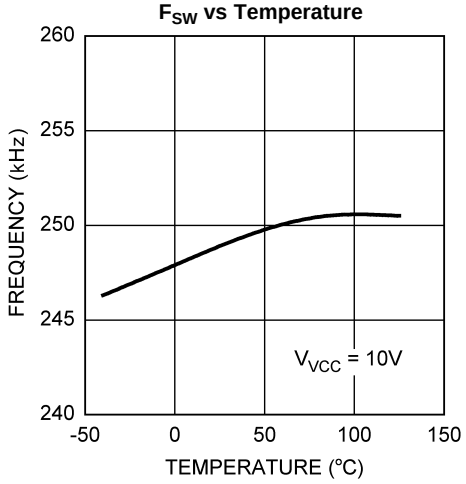


Figure 13.

F_{SW} vs V_{CC}

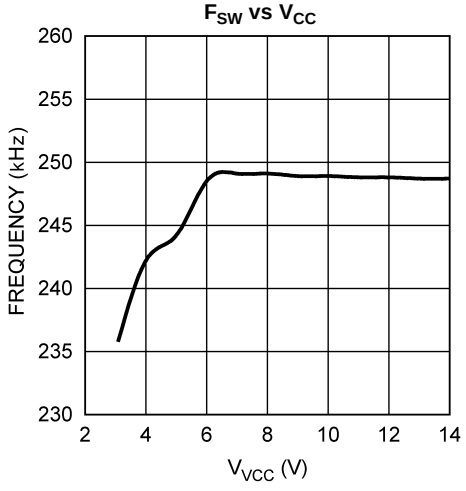


Figure 14.

I_{EN} vs V_{VIN} vs Temperature

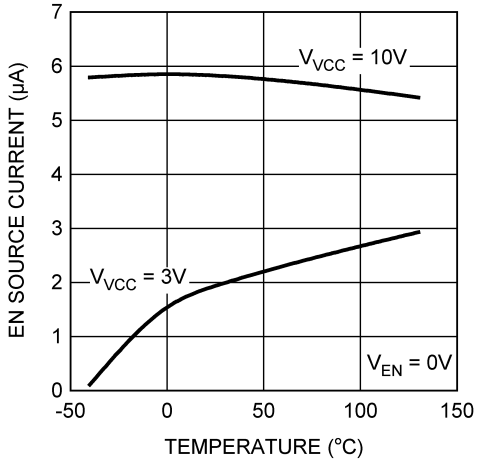
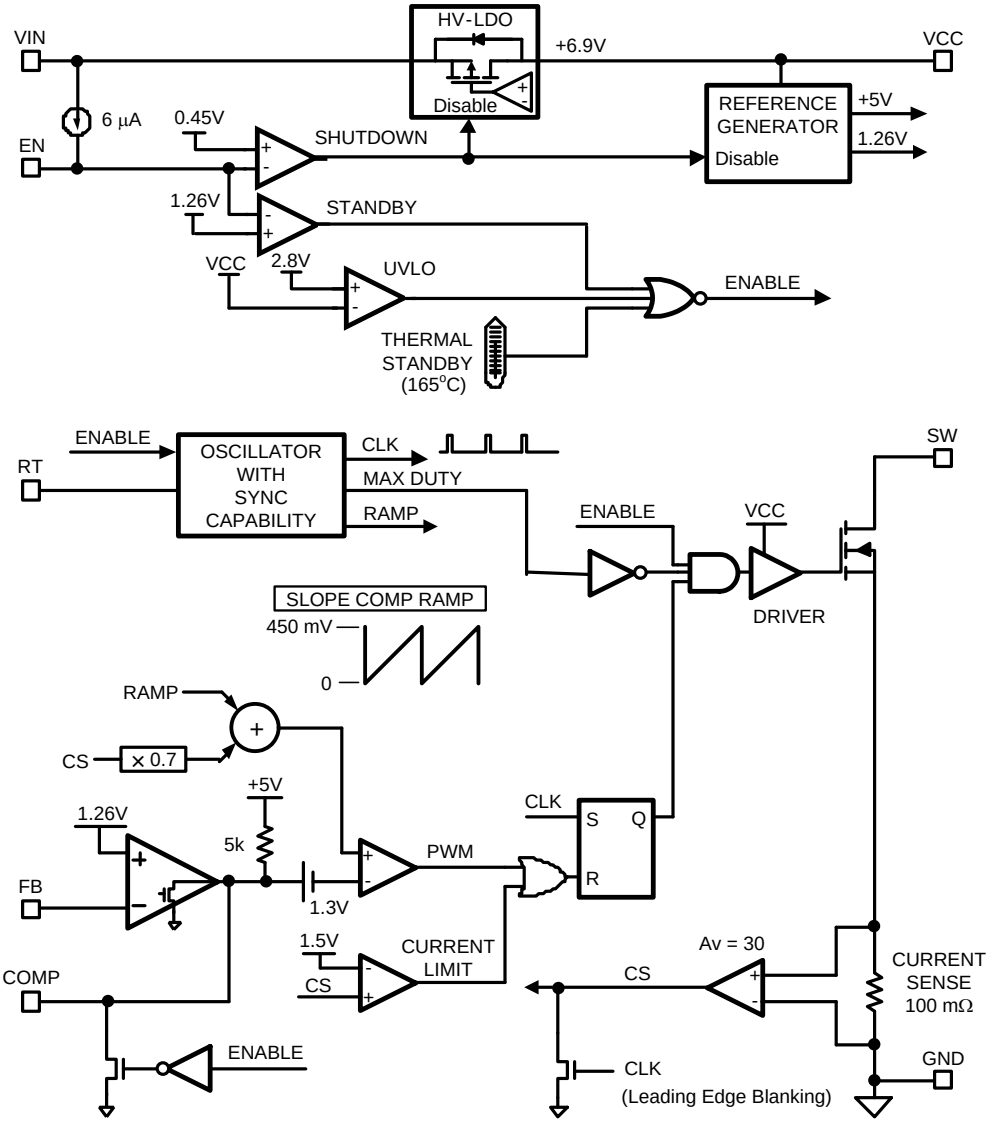


Figure 15.

Block Diagram



FUNCTIONAL DESCRIPTION

The LM5002 high voltage switching regulator features all the functions necessary to implement an efficient boost, flyback, SEPIC or forward current mode power converter. The operation can be best understood by referring to the block diagram. At the start of each cycle, the oscillator sets the driver logic and turns on the power MOSFET to conduct current through the inductor or transformer. The peak current in the MOSFET is controlled by the voltage at the COMP pin. The COMP voltage will increase with larger loads and decrease with smaller loads. This voltage is compared with the sum of a voltage proportional to the power MOSFET current and an internally generated Slope Compensation ramp. Slope Compensation is used in current mode PWM architectures to eliminate sub-harmonic current oscillation that occurs with static duty cycles greater than 50%. When the summed signal exceeds the COMP voltage, the PWM comparator resets the driver logic, turning off the power MOSFET. The driver logic is then set by the oscillator at the end of the switching cycle to initiate the next power period.

The LM5002 has dedicated protection circuitry to protect the IC from abnormal operating conditions. Cycle-by-cycle current limiting prevents the power MOSFET current from exceeding 0.5A. This feature can also be used to soft-start the regulator. Thermal Shutdown circuitry holds the driver logic in reset when the die temperature reaches 165°C, and returns to normal operation when the die temperature drops by approximately 20°C. The EN pin can be used as an input voltage under voltage lockout (UVLO) during start-up to prevent operation with less than the minimum desired input voltage.

High Voltage VCC Regulator

The LM5002 VCC Low Drop Out (LDO) regulator allows the LM5002 to operate at the lowest possible input voltage. The VCC pin voltage is very nearly equal to the input voltage from 2.8V up to approximately 6.9V. As the input voltage continues to increase, the VCC pin voltage is regulated at the 6.9V set-point. The total input operating range of the VCC LDO regulator is 3.1V to 75V.

The output of the VCC regulator is current limited to 20mA. During power-up, the VCC regulator supplies current into the required decoupling capacitor (0.47 µF or greater ceramic capacitor) at the VCC pin. When the voltage at the VCC pin exceeds the VCC UVLO threshold of 2.8V and the EN pin is greater than 1.26V the PWM controller is enabled and switching begins. The controller remains enabled until VCC falls below 2.7V or the EN pin falls below 1.16V.

An auxiliary supply voltage can be applied to the VCC pin to reduce the IC power dissipation. If the auxiliary voltage is greater than 6.9V, the internal regulator will essentially shut-off, and internal power dissipation will be decreased by the VIN voltage times the operating current. The overall converter efficiency will also improve if the VIN voltage is much higher than the auxiliary voltage. The externally applied VCC voltage should not exceed 14V. The VCC regulator series pass MOSFET includes a body diode (see the Block Diagram) between VCC and VIN that should not be forward biased in normal operation. Therefore, the auxiliary VCC voltage should never exceed the VIN voltage.

In high voltage applications extra care should be taken to ensure the VIN pin does not exceed the absolute maximum voltage rating of 76V. Voltage ringing on the VIN line during line transients that exceeds the Absolute Maximum Ratings will damage the IC. Both careful PC board layout and the use of quality bypass capacitors located close to the VIN and GND pins are essential.

Oscillator

A single external resistor connected between RT and GND pins sets the LM5002 oscillator frequency. To set a desired oscillator frequency (F_{SW}), the necessary value for the RT resistor can be calculated from the following equation:

$$RT = 13.1 \times 10^9 \times \left(\frac{1}{F_{SW}} - 83\ ns \right) \quad (1)$$

The tolerance of the external resistor and the frequency tolerance indicated in the Electrical Characteristics must be taken into account when determining the worst case frequency range.

External Synchronization

The LM5002 can be synchronized to the rising edge of an external clock. The external clock must have a higher frequency than the free running oscillator frequency set by the RT resistor. The clock signal should be coupled through a 100pF capacitor into the RT pin. A peak voltage level greater than 2.6V at the RT pin is required for detection of the sync pulse. The DC voltage across the RT resistor is internally regulated at 1.5 volts. The negative portion of the AC voltage of the synchronizing clock is clamped to this 1.5V by an amplifier inside the LM5002 with ~100Ω output impedance. Therefore, the AC pulse superimposed on the RT resistor must have positive pulse amplitude of 1.1V or greater to successfully synchronize the oscillator. The sync pulse width measured at the RT pin should have a duration greater than 15ns and less than 5% of the switching period. The sync pulse rising edge initiates the internal CLK signal rising edge, which turns off the power MOSFET. The RT resistor is always required, whether the oscillator is free running or externally synchronized. The RT resistor should be located very close to the device and connected directly to the RT and GND pins of the LM5002.

Enable / Standby

The LM5002 contains a dual level Enable circuit. When the EN pin voltage is below 450 mV, the IC is in a low current shutdown mode with the VCC LDO disabled. When the EN pin voltage is raised above the shutdown threshold but below the 1.26V standby threshold, the VCC LDO regulator is enabled, while the remainder of the IC is disabled. When the EN pin voltage is raised above the 1.26V standby threshold, all functions are enabled and normal operation begins. An internal 6 µA current source pulls up the EN pin to activate the IC when the EN pin is left disconnected.

An external set-point resistor divider from VIN to GND can be used to determine the minimum operating input range of the regulator. The divider must be designed such that the EN pin exceeds the 1.26V standby threshold when VIN is in the desired operating range. The internal 6 µA current source should be included when determining the resistor values. The shutdown and standby thresholds have 100 mV hysteresis to prevent noise from toggling between modes. When the VIN voltage is below 3.5VDC during start-up and the operating temperature is below -20°C, the EN pin should have a pull-up resistor that will provide 2 µA or greater current. The EN pin is internally protected by a 6V Zener diode through a 1 kΩ resistor. The enabling voltage may exceed the Zener voltage, however the Zener current should be limited to less than 4mA.

Error Amplifier and PWM Comparator

An internal high gain error amplifier generates an error signal proportional to the difference between the regulated output voltage and an internal precision reference. The output of the error amplifier is connected to the COMP pin allowing the user to add loop compensation, typically a Type II network, as illustrated in Figure 16. This network creates a low frequency pole that rolls off the high DC gain of the amplifier, which is necessary to accurately regulate the output voltage. F_{DC_POLE} is the closed loop unity gain (0 dB) frequency of this pole. A zero provides phase boost near the closed loop unity gain frequency, and a high frequency pole attenuates switching noise. The PWM comparator compares the current sense signal from the current sense amplifier to the error amplifier output voltage at the COMP pin.

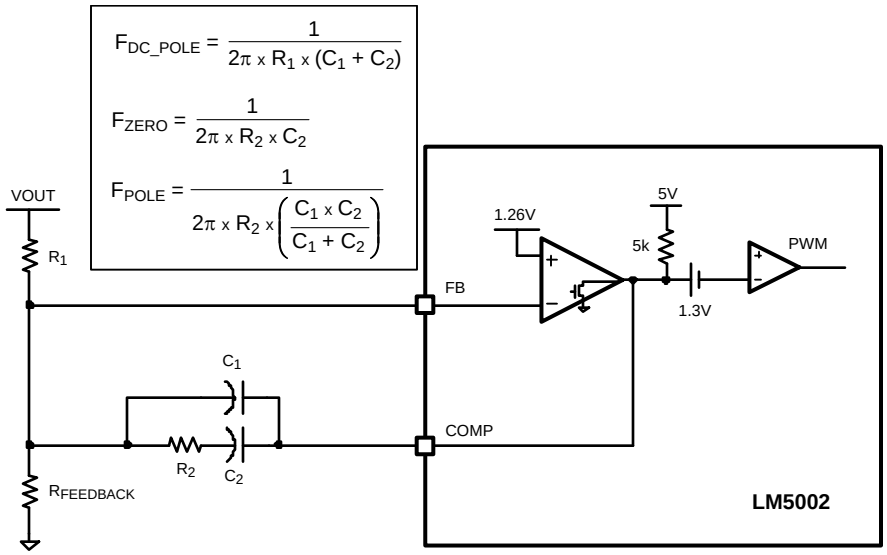


Figure 16. Type II Compensator

When isolation between primary and secondary circuits is required, the Error Amplifier is usually disabled by connecting the FB pin to GND. This allows the COMP pin to be driven directly by the collector of an opto-coupler. In isolated designs the external error amplifier is located on the secondary circuit and drives the opto-coupler LED. The compensation network is connected to the secondary side error amplifier. An example of an isolated regulator with an opto-coupler is shown in Figure 22.

Current Amplifier and Slope Compensation

The LM5002 employs peak current mode control which also provides a cycle-by-cycle over current protection feature. An internal 100 mΩ current sense resistor measures the current in the power MOSFET source. The sense resistor voltage is amplified 30 times to provide a 3V/A signal into the current limit comparator. Current limiting is initiated if the internal current limit comparator input exceeds the 1.5V threshold, corresponding to 0.5A. When the current limit comparator is triggered, the SW output pin immediately switches to a high impedance state.

The current sense signal is reduced to a scale factor of 2.1V/A for the PWM comparator signal. The signal is then summed with a 450mV peak slope compensation ramp. The combined signal provides the PWM comparator with a control signal that reaches 1.5V when the MOSFET current is 0.5A. For duty cycles greater than 50%, current mode control circuits are subject to sub-harmonic oscillation (alternating between short and long PWM pulses every other cycle). Adding a fixed slope voltage ramp signal (slope compensation) to the current sense signal prevents this oscillation. The 450mV ramp (zero volts when the power MOSFET turns on, and 450mV at the end of the PWM clock cycle) adds a fixed slope to the current sense ramp to prevent oscillation.

To prevent erratic operation at low duty cycle, a leading edge blanking circuit attenuates the current sense signal when the power MOSFET is turned on. When the MOSFET is initially turned on, current spikes from the power MOSFET drain-source and gate-source capacitances flow through the current sense resistor. These transient currents normally cease within 50 ns with proper selection of rectifier diodes and proper PC board layout.

Thermal Protection

Internal Thermal Shutdown circuitry is provided to protect the IC in the event the maximum junction temperature is exceeded. When the 165°C junction temperature threshold is reached, the regulator is forced into a low power standby state, disabling all functions except the VCC regulator. Thermal hysteresis allows the IC to cool down before it is re-enabled. Note that since the VCC regulator remains functional during this period, the soft-start circuit shown in Figure 20 should be augmented if soft-start from Thermal Shutdown state is required.

Power MOSFET

The LM5002 switching regulator includes an N-Channel MOSFET with 850 mΩ on-resistance. The on-resistance of the LM5002 MOSFET varies with temperature as shown in the Typical Performance Characteristics graph. The typical total gate charge for the MOSFET is 2.4 nC which is supplied from the VCC pin when the MOSFET is turned on.

APPLICATION INFORMATION

The following information is intended to provide guidelines for the power supply designer using the LM5002.

VIN

The voltage applied to the VIN pin can vary within the range of 3.1V to 75V. The current into the VIN pin depends primarily on the gate charge of the power MOSFET, the switching frequency, and any external load on the VCC pin. It is recommended the filter shown in Figure 17 be used to suppress transients which may occur at the input supply. This is particularly important when VIN is operated close to the maximum operating rating of the LM5002.

When power is applied and the VIN voltage exceeds 2.8V with the EN pin voltage greater than 0.45V, the VCC regulator is enabled, supplying current into the external capacitor connected to the VCC pin. When the VIN voltage is between 2.8V and 6.9V, the VCC voltage is approximately equal to the VIN voltage. When the voltage on the VCC pin exceeds 6.9V, the VCC pin voltage is regulated at 6.9V. In typical flyback applications, an auxiliary transformer winding is connected through a diode to the VCC pin. This winding must raise the VCC voltage above 6.9V to shut off the internal start-up regulator. The current requirements from this winding are relatively small, typically less than 20 mA. If the VIN voltage is much higher than the auxiliary voltage, the auxiliary winding will significantly improve conversion efficiency. It also reduces the power dissipation within the LM5002. The externally applied VCC voltage should never exceed 14V. Also the applied VCC should never exceed the VIN voltage to avoid reverse current through the internal VCC to VIN diode shown in the LM5002 Block Diagram.

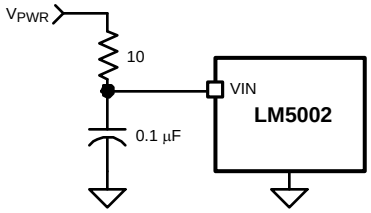


Figure 17. Input Transient Protection

SW PIN

Attention must be given to the PC board layout for the SW pin which connects to the power MOSFET drain. Energy can be stored in parasitic inductance and capacitance which cause switching spikes that negatively effect efficiency, and conducted and radiated emissions. These connections should be as short as possible to reduce inductance and as wide as possible to reduce resistance. The loop area, defined by the SW and GND pin connections, the transformer or inductor terminals, and their respective return paths, should be minimized.

EN / UVLO VOLTAGE DIVIDER SELECTION

Two dedicated comparators connected to the EN pin are used to detect under-voltage and shutdown conditions. When the EN pin voltage is below 0.45V, the controller is in a low current shutdown mode where the VIN current is reduced to 95 µA. For an EN pin voltage greater than 0.45V but less than 1.26V the controller is in standby mode, with all internal circuits operational, but the PWM gate driver signal is blocked. Once the EN pin voltage is greater than 1.26V, the controller is fully enabled. Two external resistors can be used to program the minimum operational voltage for the power converter as shown in Figure 18. When the EN pin voltage falls below the 1.26V threshold, an internal 100 mV threshold hysteresis prevents noise from toggling the state, so the voltage must be reduced to 1.16V to transition to standby. Resistance values for R1 and R2 can be determined from the following equations:

$$R1 = \frac{V_{PWR} - 1.26V}{I_{DIVIDER}} \quad (2)$$

$$R2 = \frac{1.26V}{I_{DIVIDER} + 6\ \mu A}$$

where

- V_{PWR} is the desired turn-on voltage
- $I_{DIVIDER}$ is an arbitrary current through R1 and R2 (3)

For example, if the LM5002 is to be enabled when V_{PWR} reaches 16V, $I_{DIVIDER}$ could be chosen as 501 µA which would set R1 to 29.4 kΩ and R2 to 2.49 kΩ. The voltage at the EN pin should not exceed 10V unless the current into the 6V protection Zener diode is limited below 4 mA. The EN pin voltage should not exceed 14V at any time. Be sure to check both the power and voltage rating (some 0603 resistors are rated as low as 50V) for the selected R1 resistor.

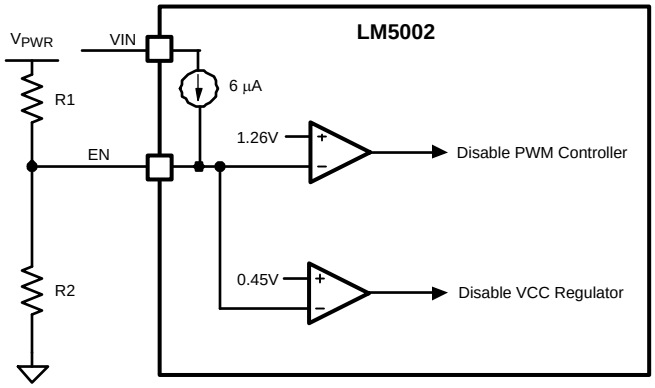


Figure 18. Basic EN (UVLO) Configuration

Remote configuration of the controller's operational modes can be accomplished with open drain device(s) connected to the EN pin as shown in Figure 19. A MOSFET or an NPN transistor connected to the EN pin can force the regulator into the low power 'off' state. Adding a PN diode in the drain (or collector) provides the offset to achieve the standby state. The advantage of standby is that the VCC LDO is not disabled and external circuitry powered by VCC remains functional.

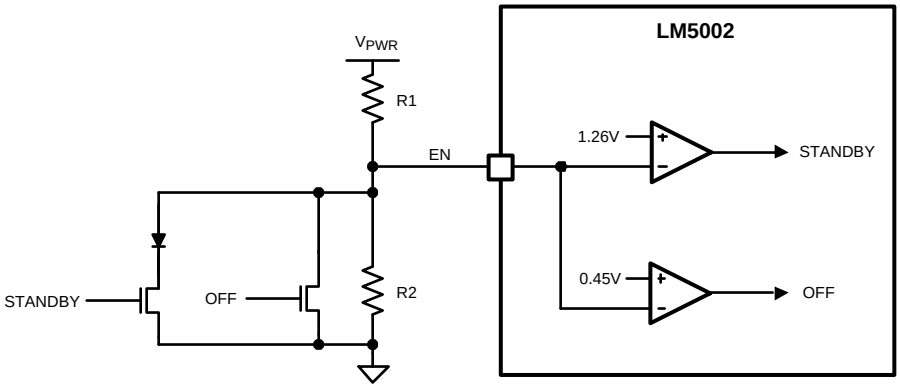


Figure 19. Remote Standby and Disable Control

SOFTSTART

Soft-start (SS) can be implemented with an external capacitor connected to COMP through a diode as shown in Figure 20. The COMP discharge MOSFET conducts during Shutdown and Standby modes to keep the COMP voltage below the PWM offset (1.3V), which inhibits PWM pulses. The error amplifier will attempt to raise the COMP voltage after the EN pin exceeds the 1.26V standby threshold. Because the error amplifier output can only sink current, the internal COMP pull-up resistor (~5 kΩ) will supply the charging current to the SS capacitor. The SS capacitor will cause the COMP voltage to gradually increase, until the output voltage achieves regulation and FB assumes control of the COMP and the PWM duty cycle. The SS capacitor continues charging through a large resistance, R_{SS}, preventing the SS circuit from interfering with the normal error amplifier function. During shutdown, the VCC diode discharges the SS capacitor.

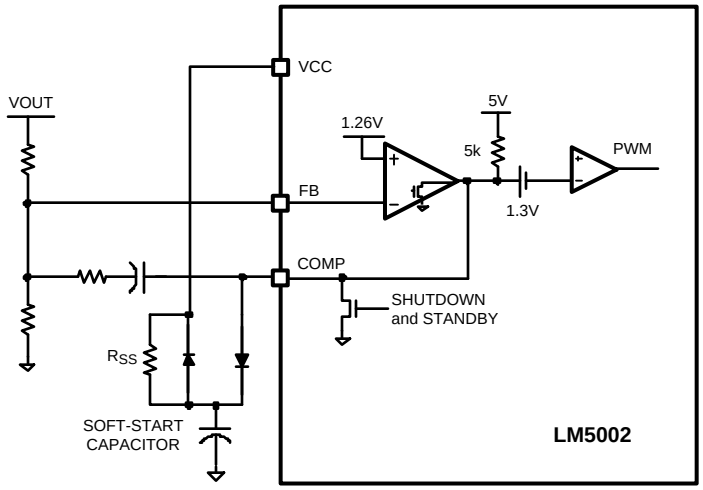


Figure 20. Soft-Start

Printed Circuit Board Layout

The LM5002 Current Sense and PWM comparators are very fast and may respond to short duration noise pulses. The components at the SW, COMP, EN and the RT pins should be as physically close as possible to the IC, thereby minimizing noise pickup on the PC board tracks.

The SW output pin of the LM5002 should have a short, wide conductor to the power path inductors, transformers and capacitors in order to minimize parasitic inductance that reduces efficiency and increases conducted and radiated noise. Ceramic decoupling capacitors are recommended between the VIN pin to the GND pin and between the VCC pin to the GND pin. Use short, direct connections to avoid clock jitter due to ground voltage differentials. Small package surface mount X7R or X5R capacitors are preferred for high frequency performance and limited variation over temperature and applied voltage.

If an application using the LM5002 produces high junction temperatures during normal operation, multiple vias from the GND pin to a PC board ground plane will help conduct heat away from the IC. Judicious positioning of the PC board within the end product, along with use of any available air flow will help reduce the junction temperatures. If using forced air cooling, avoid placing the LM5002 in the airflow shadow of large components, such as input capacitors, inductors or transformers.

Application Circuit Examples

The following schematics present examples of a Non-Isolated Flyback, Isolated Flyback, Boost, 24V SEPIC and a 12V Automotive range SEPIC converters utilizing the LM5002 switching regulator.

NON-ISOLATED FLYBACK

The Non-Isolated Flyback converter (Figure 21) utilizes the internal voltage reference for the regulation setpoint. The output is +5V at 500mA while the input voltage can vary from 16V to 42V. The switching frequency is set to 250kHz. An auxiliary winding on transformer (T1) provides 7.5V to power the LM5002 when the output is in regulation. This disables the internal high voltage VCC LDO regulator and improves efficiency. The input under-voltage threshold is 13.9V. The converter can be shut down by driving the EN input below 1.26V with an open-collector or open-drain transistor. An external synchronizing frequency can be applied to the SYNC input. An optional soft-start circuit is connected to the COMP pin input. When power is applied, the soft-start capacitor (C7) is discharged and limits the voltage applied to the PWM comparator by the internal error amplifier. The internal ~5 kΩ COMP pull-up resistor charges the soft-start capacitor until regulation is achieved. The VCC pull-up resistor (R7) continues to charge C7 so that the soft-start circuit will not affect the compensation network in normal operation. If the output capacitance is small, the soft-start circuit can be adjusted to limit the power-on output voltage overshoot. If the output capacitance is sufficiently large, no soft-start circuit is needed because the LM5002 will gradually charge the output capacitor by current limiting at approximately 500mA (I_{LIM}) until regulation is achieved.

ISOLATED FLYBACK

The Isolated Flyback converter (Figure 22) utilizes a 2.5V voltage reference (LM431) located on the isolated secondary side for the regulation setpoint. The LM5002 internal error amplifier is disabled by grounding the FB pin. The LM431 controls the current through the opto-coupler LED, which sets the COMP pin voltage. The R4 and C3 network boosts the phase response of the opto-coupler to increase the loop bandwidth. The output is +5V at 500mA and the input voltage ranges from 16V to 42V. The switching frequency is set to 250kHz.

BOOST

The Boost converter (Figure 23) utilizes the internal voltage reference for the regulation setpoint. The output is +48V at 125 mA, while the input voltage can vary from 16V to 36V. The switching frequency is set to 250kHz. The internal VCC regulator provides 6.9V bias power, since there isn't a simple method for creating an auxiliary voltage with the boost topology. Note that the boost topology does not provide output short-circuit protection because the power MOSFET cannot interrupt the path between the input and the output.

24V SEPIC

The 24V SEPIC converter (Figure 24) utilizes the internal voltage reference for the regulation setpoint. The output is +24V at 125 mA while the input voltage can vary from 16V to 48V. The switching frequency is set to 250kHz. The internal VCC regulator provides 6.9V bias power for the LM5002. An auxiliary voltage can be created by adding a winding on L2 and a diode into the VCC pin.

12V AUTOMOTIVE SEPIC

The 12V Automotive SEPIC converter (Figure 25) utilizes the internal bandgap voltage reference for the regulation setpoint. The output is +12V at 25 mA while the input voltage can vary from 3.1V to 60V. The output current rating can be increased if the minimum VIN voltage requirement is increased. The switching frequency is set to 750kHz. The internal VCC regulator provides 6.9V bias power for the LM5002. The output voltage can be used as an auxiliary voltage if the nominal VIN voltage is greater than 12V by adding a diode from the output into the VCC pin. In this configuration, the minimum input voltage must be greater than 12V to prevent the internal VCC to VIN diode from conducting. If the applied VCC voltage exceeds the minimum VIN voltage, then an external blocking diode is required between the VIN pin and the power source to block current flow from VCC to the input supply.

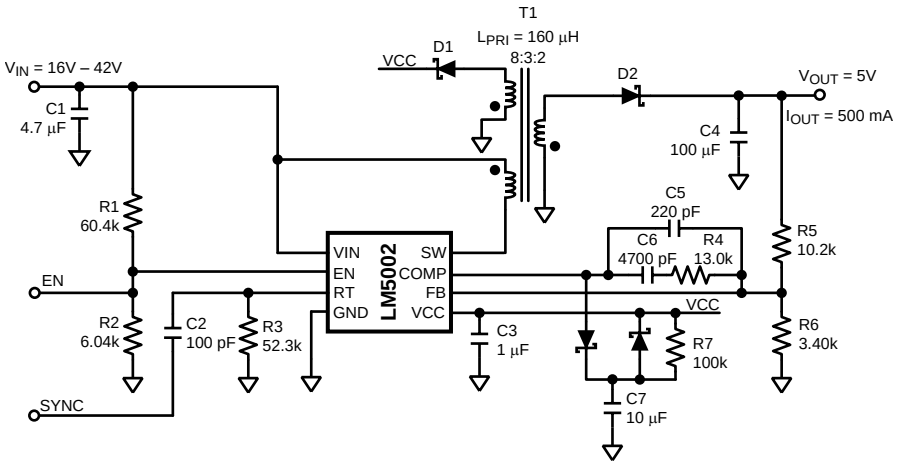


Figure 21. Non-Isolated Flyback

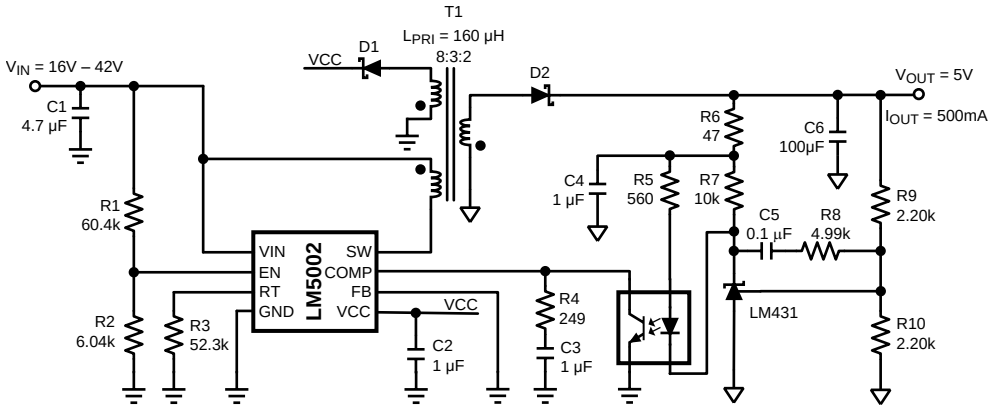


Figure 22. Isolated Flyback

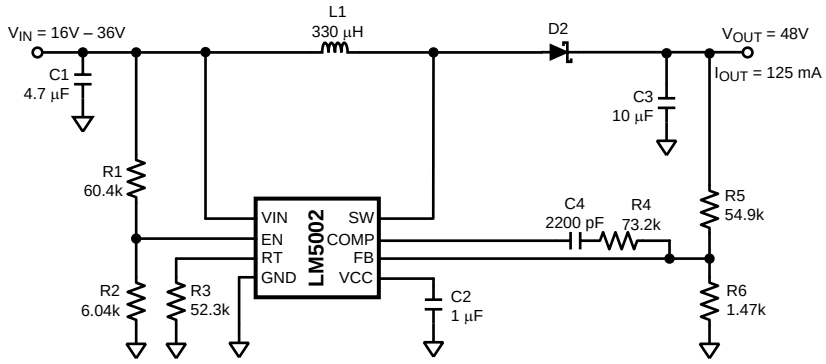


Figure 23. Boost

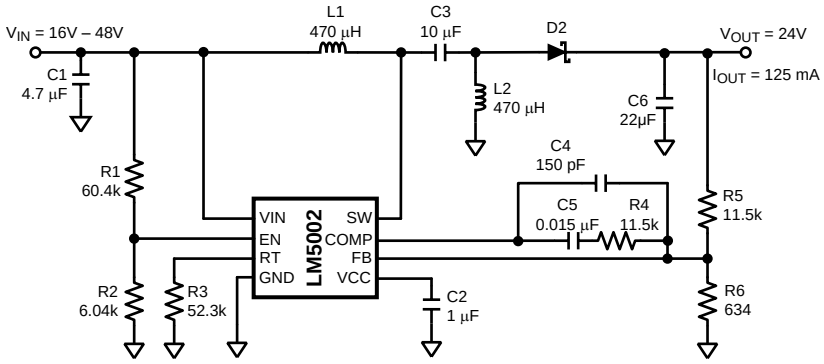


Figure 24. 24V SEPIC

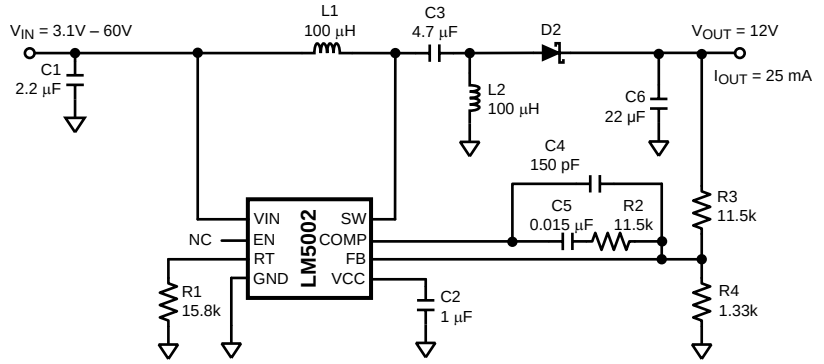


Figure 25. 12V SEPIC

REVISION HISTORY

Changes from Revision C (March 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	16

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5002MA/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L5002 MA	Samples
LM5002MAX	NRND	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 125	L5002 MA	
LM5002MAX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L5002 MA	Samples
LM5002SD/NOPB	ACTIVE	WSON	NGT	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM5002	Samples
LM5002SDX/NOPB	ACTIVE	WSON	NGT	8	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM5002	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

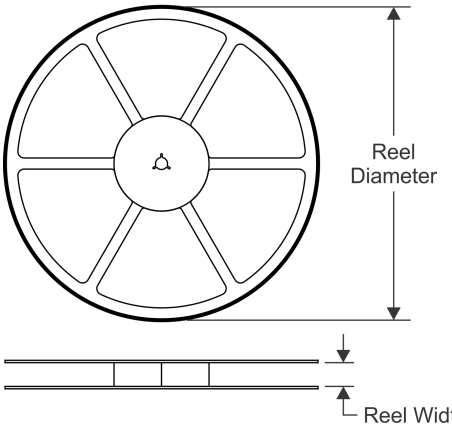
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

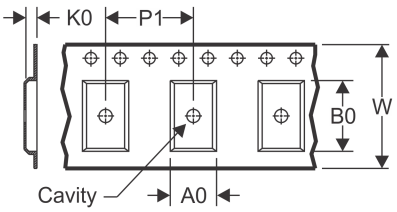
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

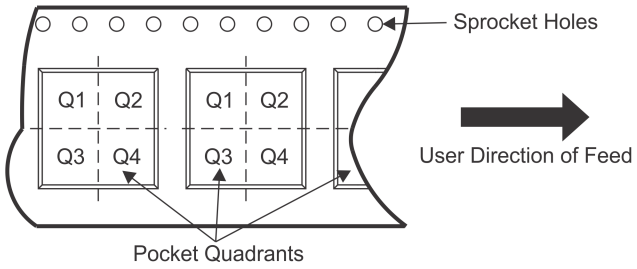


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

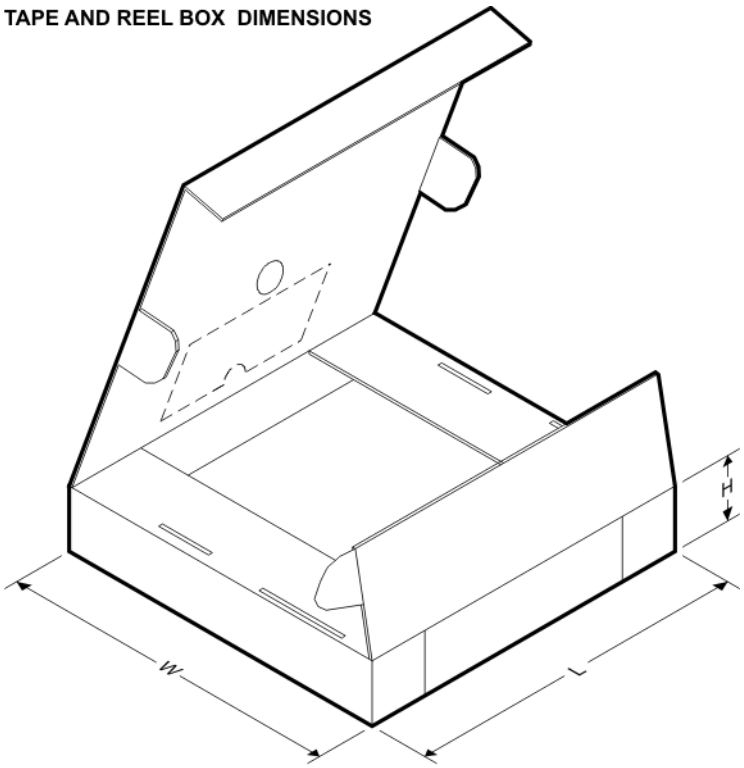
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5002MAX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5002MAX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM5002SD/NOPB	WSON	NGT	8	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM5002SDX/NOPB	WSON	NGT	8	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

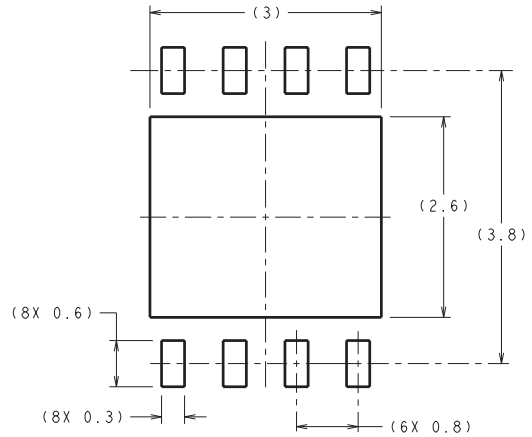
TAPE AND REEL BOX DIMENSIONS



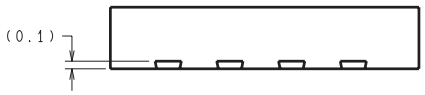
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5002MAX	SOIC	D	8	2500	367.0	367.0	35.0
LM5002MAX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM5002SD/NOPB	WSON	NGT	8	1000	210.0	185.0	35.0
LM5002SDX/NOPB	WSON	NGT	8	4500	367.0	367.0	35.0

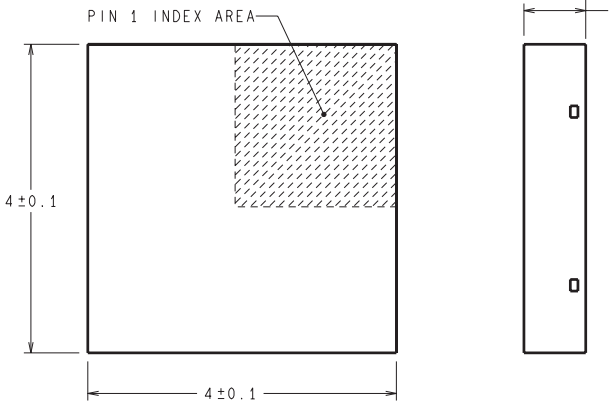
NGT0008A

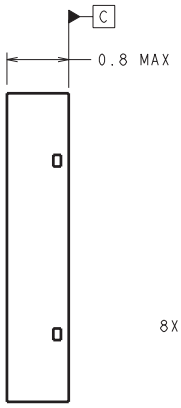


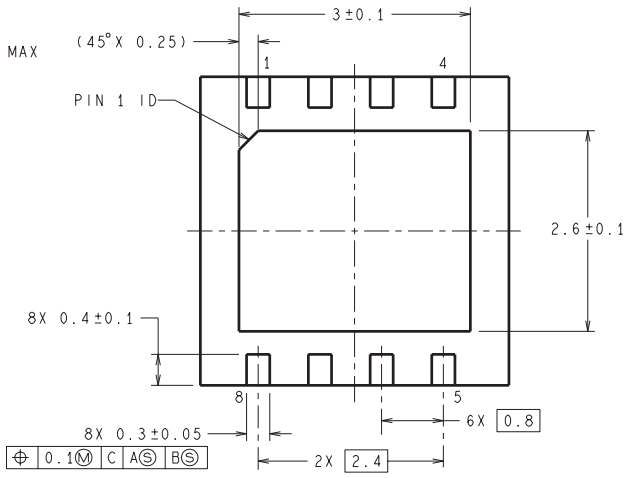
DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY



RECOMMENDED LAND PATTERN

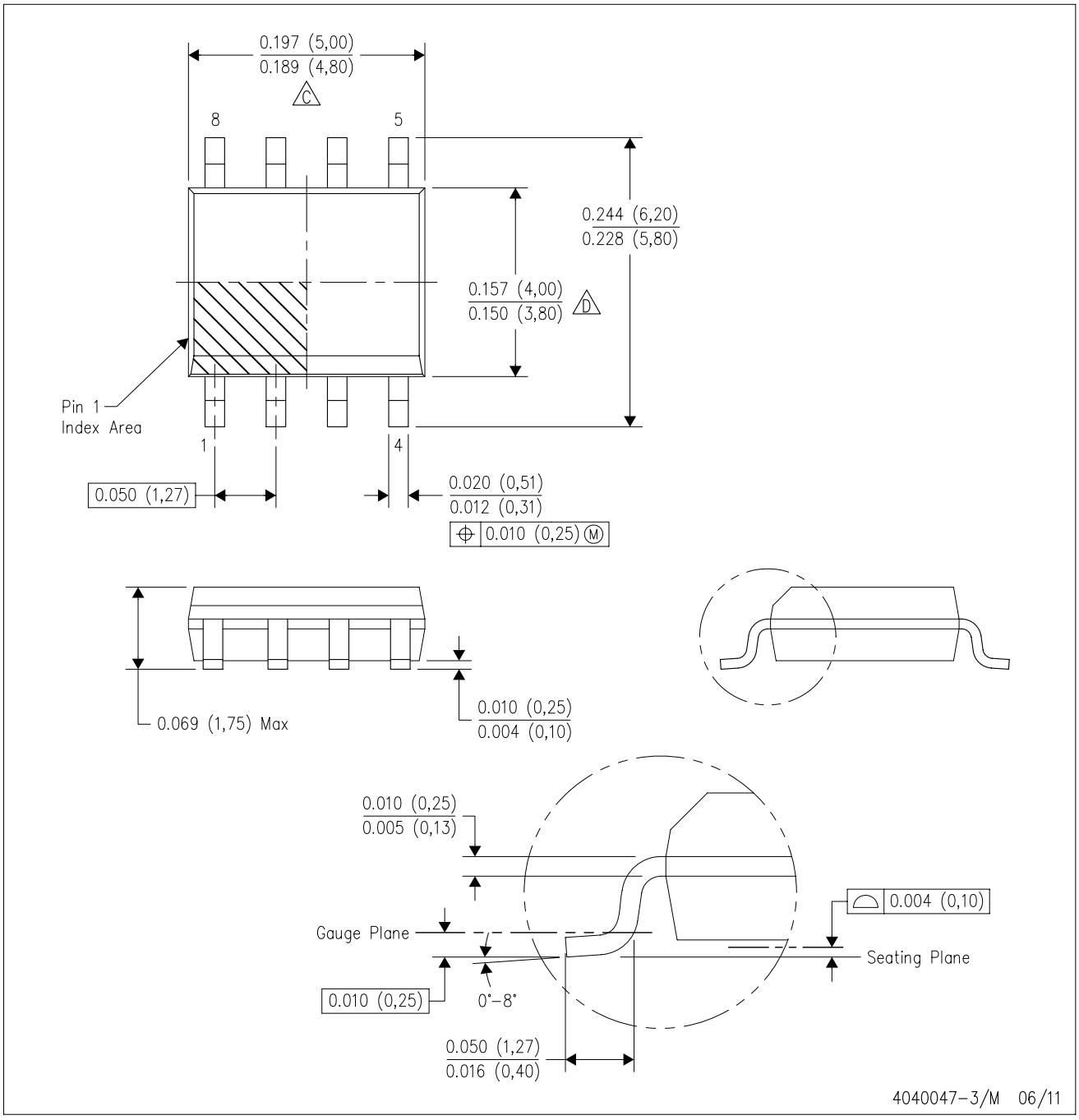






SDC08A (Rev A)

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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