





Support & 2.2 Community

Reference Design



ISO7720, ISO7721

SLLSEP3C - NOVEMBER 2016 - REVISED JULY 2018

ISO772x High-Speed, Robust EMC Reinforced Dual-Channel Digital Isolators

Technical

Documents

Features 1

- Signaling Rate: Up to 100 Mbps
- Wide Supply Range: 2.25 V to 5.5 V
- 2.25-V to 5.5-V Level Translation
- Default Output High and Low Options
- Wide Temperature Range: -55°C to +125°C
- Low Power Consumption, Typical 1.7 mA per Channel at 1 Mbps
- Low Propagation Delay: 11 ns Typical (5-V Supplies)
- High CMTI: ±100 kV/µs Typical
- Robust Electromagnetic Compatibility (EMC)
 - System-Level ESD, EFT, and Surge Immunity
 - Low Emissions
- Isolation Barrier Life: >40 Years
- Wide-SOIC (DW-16, DWV-8) and Narrow-SOIC (D-8) Package Options
- Safety-Related Certifications:
 - VDE Reinforced Insulation according to DIN V VDE V 0884-11:2017-01
 - 5000 V_{RMS} (DW and DWV) and 3000 V_{RMS} (D) Isolation Rating per UL 1577
 - CSA Certification per IEC 60950-1, IEC 62368-1, IEC 61010-1, and IEC 60601-1 End Equipment Standards
 - CQC Certification per GB4943.1-2011
 - TUV Certification according to EN 60950-1 and EN 61010-1
 - DWV Package Certifications are Planned; All Other Certifications Complete

2 Applications

- Industrial Automation
- Hybrid Electric Vehicles
- Motor Control
- **Power Supplies**
- Solar Inverters
- Medical Equipment

3 Description

The ISO772x devices are high-performance, dualchannel digital isolators with 5000 V_{RMS} (DW and DWV packages) and 3000 V_{RMS} (D package) isolation ratings per UL 1577. These devices are also certified by VDE, TUV, CSA, and CQC.

The ISO772x devices provide high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic input and output buffer separated by a silicon dioxide (SiO₂) insulation barrier. The ISO7720 device has both channels in the same direction while the ISO7721 device has both channels in the opposite direction. In the event of input power or signal loss, the default output is high for devices without suffix F and low for devices with suffix F. See the Device Functional Modes section for further details.

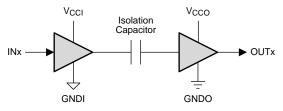
Used in conjunction with isolated power supplies, these devices help prevent noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. design and lavout Through innovative chip techniques, the electromagnetic compatibility of the ISO772x devices has been significantly enhanced to ease system-level ESD, EFT, surge, and emissions compliance. The ISO772x family of devices is available in 16-pin SOIC wide-body (DW), 8-pin SOIC wide-body (DWV), and 8-pin SOIC narrow-body (D) packages.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
	D (8)	4.90 mm × 3.91 mm
ISO7720, ISO7721 ISO7721F, ISO7721F	DWV (8)	5.85 mm × 7.50 mm
10011211,10011211	DW (16)	10.30 mm × 7.50 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



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V_{CCI} and GNDI are supply and ground connections respectively for the input channels.

V_{CCO} and GNDO are supply and ground connections respectively for the output channels.



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4 Revision History

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NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (March 2017) to Revision C

•	Added the 8-pin SOIC package (DWV) to the data sheet	1	
•	Updated the VDE and CSA certification description throughout the document	1	
•	Changed all certifications to complete for the DW and D packages in the Features section	1	
•	Changed the climatic category for the D package from 5/125/21 to 55/125/21	7	
•	Changed the maximum working voltages for DW-16 and D-8 from 400 to 700 V _{RMS} and 250 to 400 V _{RMS} (respectively) in the <i>Safety-Related Certifications</i> table	8	
•	Switched the line colors for V _{CC} at 2.5 V and V _{CC} at 3.3 V in the <i>Low-Level Output Voltage vs Low-Level Output Current</i> graph	15	
•	Deleted EN from the Common-Mode Transient Immunity Test Circuit figure	17	
•	Added the Device Support section	24	

Changes from Revision A (December 2016) to Revision B

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•	Added D-8 values for TUV in the Safety-Related Certifications table	8
•	Changed the minimum CMTI value from 40 kV/µs to 85 kV/µs in all Electrical Characteristics tables	10
•	Added the Receiving Notification of Documentation Updates section	24
•	Changed the Electrostatic Discharge Caution statement	24

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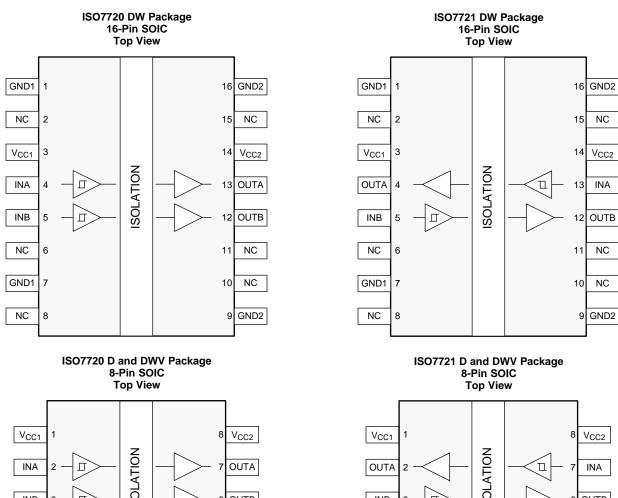
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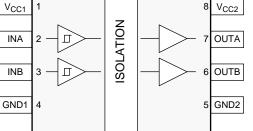
Changes from Original (November 2016) to Revision A

Page

•	Changed Feature From: IEC 60950-1, IEC 60601-1 and IEC 61010-1 End Equipment Standards To: IEC 60950-1 and IEC 60601-1 End Equipment Standards	1
•	Added Climatic category to the Insulation Specifications	7
•	Changed the CSA column of Regulatory Information	8
•	Changed DW package) To: (DW-16) in the TUV column of Regulatory Information	8
•	Changed t _{ie} TYP value From: 1.5 To 1 in Switching Characteristics—5-V Supply	13
•	Changed t _{ie} TYP value From: 1.5 To 1 in Switching Characteristics—3.3-V Supply	13
•	Changed t _{ie} TYP value From: 1.5 To 1 in Switching Characteristics—2.5-V Supply	13

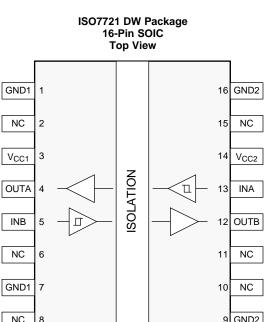
5 Pin Configuration and Functions

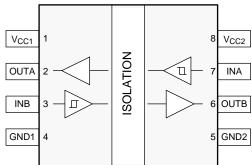




Pin Functions

	PIN			PIN							
NAME	DW PACKAGE		D, DWV PACKAGE		I/O	DESCRIPTION					
NAME	ISO7720	ISO7721	ISO7720	IS07721							
GND1	1, 7	1, 7	4	4	_	Ground connection for V _{CC1}					
GND2	9	9	5	_		Cround connection for V					
GND2	16	16	Э	5	_	Ground connection for V_{CC2}					
INA	4	13	2	7	Ι	Input, channel A					
INB	5	5	3	3	Ι	Input, channel B					
NC	2, 6, 8, 10, 11, 15	2, 6, 8, 10, 11, 15	_	_	_	Not connected					
OUTA	13	4	7	2	0	Output, channel A					
OUTB	12	12	6	6	0	Output, channel B					
V _{CC1}	3	3	1	1	-	Power supply, V _{CC1}					
V _{CC2}	14	14	8	8	—	Power supply, V _{CC2}					





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6 Specifications

6.1 Absolute Maximum Ratings

See (1).

		MIN	MAX	UNIT
V _{CC1} , V _{CC2}	Supply voltage ⁽²⁾	-0.5	6	V
V	Voltage at INx, OUTx	-0.5	V_{CC} + 0.5 ⁽³⁾	V
I _O	Output current	-15	15	mA
TJ	Junction temperature		150	°C
T _{stg}	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak

voltage values.

(3) Maximum voltage must not exceed 6 V.

6.2 ESD Ratings

			VALUE	UNIT
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±6000	V
V _{ESD}	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all $\ensuremath{\text{pins}}^{(2)}$	±1500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V _{CC1} , V _{CC2}	Supply voltage		2.25		5.5	V
V _{CC(UVLO+)}	UVLO threshold when supply	voltage is rising		2	2.25	V
V _{CC(UVLO-)}	UVLO threshold when supply	voltage is falling	1.7	1.8		V
V _{HYS(UVLO)}	Supply voltage UVLO hystere	esis	100	200		mV
		$V_{CCO}^{(1)} = 5 V$	-4			
I _{OH}	High-level output current	V _{CCO} = 3.3 V	-2			mA
		V _{CCO} = 2.5 V	-1			
		$V_{CCO} = 5 V$			4	4
I _{OL}	Low-level output current	V _{CCO} = 3.3 V			2	mA
		V _{CCO} = 2.5 V			1	
V _{IH}	High-level input voltage		0.7 × V _{CCI} ⁽¹⁾		V _{CCI}	V
V _{IL}	Low-level input voltage		0		0.3 × V _{CCI}	V
DR	Signaling rate		0		100	Mbps
T _A	Ambient temperature		-55	25	125	°C

(1) V_{CCI} = Input-side V_{CC} ; V_{CCO} = Output-side V_{CC} .

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6.4 Thermal Information

		ISO772x				
	THERMAL METRIC ⁽¹⁾	DW (SOIC)	DWV (SOIC)	D (SOIC)	UNIT	
		16 PINS	16 PINS	8 PINS		
R_{\thetaJA}	Junction-to-ambient thermal resistance	86.5	84.3	137.7	°C/W	
R _{0JC(top)}	Junction-to-case(top) thermal resistance	49.6	36.3	54.9	°C/W	
$R_{\theta JB}$	Junction-to-board thermal resistance	49.7	47.0	71.7	°C/W	
ΨJT	Junction-to-top characterization parameter	32.3	7.4	7.1	°C/W	
ΨJB	Junction-to-board characterization parameter	49.2	45.1	70.7	°C/W	
R _{θJC(botto} m)	Junction-to-case(bottom) thermal resistance	N/A	N/A	N/A	°C/W	

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Power Ratings

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISO7720						
P _D	Maximum power dissipation	$V_{CC1} = V_{CC2} = 5.5 \text{ V}, T_J = 150^{\circ}\text{C}, C_L = 15 \text{ pF},$ input a 50 MHz 50% duty cycle square wave			100	mW
P _{D1}	Maximum power dissipation by side-1	$V_{CC1} = V_{CC2} = 5.5 \text{ V}, T_J = 150^{\circ}\text{C}, C_L = 15 \text{ pF},$ input a 50 MHz 50% duty cycle square wave			20	mW
P _{D2}	Maximum power dissipation by side-2	$V_{CC1} = V_{CC2} = 5.5 \text{ V}, T_J = 150^{\circ}\text{C}, C_L = 15 \text{ pF},$ input a 50 MHz 50% duty cycle square wave			80	mW
IS07721						
P _D	Maximum power dissipation	$V_{CC1} = V_{CC2} = 5.5 \text{ V}, T_J = 150^{\circ}\text{C}, C_L = 15 \text{ pF},$ input a 50 MHz 50% duty cycle square wave			100	mW
P _{D1}	Maximum power dissipation by side-1	$V_{CC1} = V_{CC2} = 5.5 \text{ V}, T_J = 150^{\circ}\text{C}, C_L = 15 \text{ pF},$ input a 50 MHz 50% duty cycle square wave			50	mW
P _{D2}	Maximum power dissipation by side-2	$V_{CC1} = V_{CC2} = 5.5 \text{ V}, \text{ T}_{\text{J}} = 150^{\circ}\text{C}, \text{ C}_{\text{L}} = 15 \text{ pF},$ input a 50 MHz 50% duty cycle square wave			50	mW

6.6 Insulation Specifications

	PARAMETER	TEST CONDITIONS		VALUE		UNIT
	PARAMETER	TEST CONDITIONS	DW	DWV	D	UNIT
CLR	External clearance (1)	Shortest terminal-to-terminal distance through air	8	8.5	4	mm
CPG	External creepage (1)	Shortest terminal-to-terminal distance across the package surface	8	8.5	4	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	21	21	21	μm
СТІ	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112; UL 746A	>600	>600	>600	V
	Material group	According to IEC 60664-1	I	I	Ι	
		Rated mains voltage \leq 150 V _{RMS}	I–IV	I–IV	I–IV	
	Overvoltage category per IEC	Rated mains voltage \leq 300 V _{RMS}	I–IV	I–IV	I–III	
	60664-1	Rated mains voltage $\leq 600 \text{ V}_{\text{RMS}}$	I–IV	I–IV	n/a	
		Rated mains voltage ≤ 1000 V _{RMS}	I–III	I–III	n/a	
DIN V	VDE V 0884-11:2017-01 ⁽²⁾					
V _{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1414	1414	637	V _{PK}
V _{IOWM}	Maximum working isolation	AC voltage; Time dependent dielectric breakdown (TDDB) test	1000	1000	450	V _{RMS}
	voltage	DC voltage	1414	1414	637	V _{DC}
V _{IOTM}	Maximum transient isolation voltage	$V_{\text{TEST}} = V_{\text{IOTM}}$, t = 60 s (qualification); t = 1 s (100% production)	8000	7071	4242	V _{PK}
V _{IOSM}	Maximum surge isolation voltage ⁽³⁾	Test method per IEC 60065, 1.2/50 μ s waveform, V _{TEST} = 1.6 × V _{IOSM} (qualification)	8000	8000	5000	V _{PK}
		Method a, After Input/Output safety test subgroup 2/3, V _{ini} = V _{IOTM} , t _{ini} = 60 s; V _{pd(m)} = 1.2 × V _{IORM} , t _m = 10 s	≤5	≤5	≤5	
q _{pd}	Apparent charge ⁽⁴⁾	Method a, After environmental tests subgroup 1, $V_{ini} = V_{IOTM}, t_{ini} = 60 \text{ s}; V_{pd(m)} = 1.6 \times V_{IORM}, t_m = 10 \text{ s}$	≤5	≤5	≤5	рС
		Method b1; At routine test (100% production) and preconditioning (type test), $V_{ini} = V_{IOTM}$, $t_{ini} = 1 s$; $V_{pd(m)} = 1.875 \times V_{IORM}$, $t_m = 1 s$	≤5	≤5	≤5	
C _{IO}	Barrier capacitance, input to output ⁽⁵⁾	$V_{IO} = 0.4 \times \sin (2\pi ft), f = 1 \text{ MHz}$	~0.5	~0.5	~0.5	pF
		V _{IO} = 500 V, T _A = 25°C	>10 ¹²	>10 ¹²	>10 ¹²	
R _{IO}	Isolation resistance ⁽⁵⁾	$V_{IO} = 500 \text{ V}, 100^{\circ}\text{C} \le T_{A} \le 125^{\circ}\text{C}$	>10 ¹¹	>10 ¹¹	>10 ¹¹	Ω
		$V_{IO} = 500 \text{ V at } T_{S} = 150^{\circ}\text{C}$	>10 ⁹	>10 ⁹	>10 ⁹]
	Pollution degree		2	2	2	
	Climatic category		55/125/21	55/125/21	55/125/21	
UL 157	77					
V _{ISO}	Withstanding isolation voltage	$V_{\text{TEST}} = V_{\text{ISO}}$, t = 60 s(qualification); $V_{\text{TEST}} = 1.2 \times V_{\text{ISO}}$, t = 1 s (100% production)	5000	5000	3000	V _{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by (2) means of suitable protective circuits.

Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier. (3)

Apparent charge is electrical discharge caused by a partial discharge (pd).

(4) (5) All pins on each side of the barrier tied together creating a two-terminal device. SLLSEP3C -NOVEMBER 2016-REVISED JULY 2018

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6.7 Safety-Related Certifications

DWV package certifications are planned; all other certifications are complete.

VDE	CSA	UL	CQC	TUV
Certified according to DIN V VDE V 0884-11:2017-01	Certified according to IEC 60950-1, IEC 62368-1, IEC 61010-1, and IEC 60601-1	Certified according to UL 1577 Component Recognition Program	Certified according to GB4943.1-2011	Certified according to EN 61010-1:2010 (3rd Ed) and EN 60950- 1:2006/A11:2009/A1:201 0/A12:2011/A2:2013
Maximum transient isolation voltage, 8000 V_{PK} (DW-16, Reinforced) and 4242 V_{PK} (D-8); Maximum repetitive peak isolation voltage, 1414 V_{PK} (DW-16, Reinforced) and 637 V_{PK} (D-8); Maximum surge isolation voltage, 8000 V_{PK} (DW-16, Reinforced) and 5000 V_{PK} (D-8)	Reinforced insulation per CSA 60950-1- 07+A1+A2 and IEC 60950-1 2nd Ed., 800 V _{RMS} (DW-16) and 400 V _{RMS} (D-8) max working voltage (pollution degree 2, material group I); 2 MOPP (Means of Patient Protection) per CSA 60601-1:14 and IEC 60601-1 Ed. 3.1, 250 V _{RMS} (DW-16) max working voltage	DW-16: Single protection, 5000 V _{RMS} ; D-8: Single protection, 3000 V _{RMS}	DW-16: Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate, 700 V _{RMS} maximum working voltage; D-8: Basic Insulation, Altitude ≤ 5000 m, Tropical Climate, 400 V _{RMS} maximum working voltage	$\begin{array}{c} 5000 \ V_{RMS} \ (DW-16) \ and \\ 3000 \ V_{RMS} \ (D-8) \\ Reinforced \ insulation \\ per EN \ 61010-1:2010 \\ (3rd \ Ed) \ up \ to \ working \\ voltage \ of \ 600 \ V_{RMS} \\ (DW-16) \ and \ 300 \ V_{RMS} \\ (DW-16) \ and \ 300 \ V_{RMS} \\ (D-8) \\ \hline \\ 5000 \ V_{RMS} \ (DW-16) \ and \\ 3000 \ V_{RMS} \ (D-8) \\ Reinforced \ insulation \\ per \ EN \ 60950- \\ 1:2006/A11:2009/A1:201 \\ 0/A12:2011/A2:2013 \ up \\ to \ working \ voltage \ of \\ 800 \ V_{RMS} \ (DW-16) \ and \\ 400 \ V_{RMS} \ (D-8) \end{array}$
Certificate number: 40040142	Master contract number: 220991	File number: E181974	Certificate number: CQC15001121716 (DW-16), CQC15001121656 (D-8)	Client ID number: 77311

6.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DW-	16 PACKAGE					
	0 ())))))))))))))))))	$R_{\theta JA}$ = 86.5 °C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C, see Figure 1			263	
I_S	Safety input, output, or supply current ⁽¹⁾	$R_{\theta JA}$ = 86.5 °C/W, V_{I} = 3.6 V, T_{J} = 150°C, T_{A} = 25°C, see Figure 1			401	mA
		$R_{\theta JA}$ = 86.5 °C/W, V_I = 2.75 V, T_J = 150°C, T_A = 25°C, see Figure 1			525	
P _S	Safety input, output, or total power ⁽¹⁾	$R_{\theta JA}$ = 86.5 °C/W, T_J = 150°C, T_A = 25°C, see Figure 2			1445	mW
Τs	Maximum safety temperature ⁽¹⁾				150	°C
DWV	/-8 PACKAGE	•				
	Safety input, output, or supply s current ⁽¹⁾	$R_{\theta JA} = 84.3 \text{ °C/W}, V_1 = 5.5 \text{ V}, T_J = 150 \text{ °C}, T_A = 25 \text{ °C}, \text{ see Figure 3}$			270	
I _S		$R_{\theta JA} = 84.3 \text{ °C/W}, V_1 = 3.6 \text{ V}, T_J = 150 \text{ °C}, T_A = 25 \text{ °C}, \text{ see Figure 3}$			412	mA
	ounone	$R_{\theta JA} = 84.3 \text{ °C/W}, V_1 = 2.75 \text{ V}, T_J = 150 \text{ °C}, T_A = 25 \text{ °C}, \text{ see Figure 3}$			539	
P_S	Safety input, output, or total power ⁽¹⁾	$R_{\theta JA} = 84.3 \text{ °C/W}, T_J = 150 \text{ °C}, T_A = 25 \text{ °C}, \text{ see Figure 4}$			1483	mW
Τs	Maximum safety temperature ⁽¹⁾				150	°C
D-8	PACKAGE					
		$R_{\theta JA} = 137.7 \text{ °C/W}, V_I = 5.5 \text{ V}, T_J = 150 \text{ °C}, T_A = 25 \text{ °C}, \text{ see Figure 5}$			165	
I _S	Safety input, output, or supply current ⁽¹⁾	$R_{\theta JA} = 137.7 \text{ °C/W}, V_I = 3.6 \text{ V}, T_J = 150 \text{ °C}, T_A = 25 \text{ °C}, \text{ see Figure 5}$			252	mA
	ounone	$R_{\theta JA} = 137.7 \text{ °C/W}, V_I = 2.75 \text{ V}, T_J = 150 \text{ °C}, T_A = 25 \text{ °C}, \text{ see Figure 5}$	330			
P_S	Safety input, output, or total power ⁽¹⁾	$R_{\theta JA} = 137.7 \text{ °C/W}, T_J = 150 \text{ °C}, T_A = 25 \text{ °C}, \text{ see Figure 6}$			908	mW
Τs	Maximum safety temperature ⁽¹⁾				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.

The junction-to-air thermal resistance, R_{0JA}, in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

 $T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.

 $T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.

 $P_S = I_S \times V_I$, where V_I is the maximum input voltage.

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6.9 Electrical Characteristics—5-V Supply

 $V_{CC1} = V_{CC2} = 5 \text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

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	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OH}	High-level output voltage	I _{OH} = -4 mA; see Figure 15	V _{CCO} ⁽¹⁾ – 0.4	4.8		V
V _{OL}	Low-level output voltage	I _{OL} = 4 mA; see Figure 15		0.2	0.4	V
V _{IT+(IN)}	Rising input threshold voltage			$0.6 \ x \ V_{CCI}$	$0.7 \mathrm{~x~V_{CCI}}$	V
V _{IT-(IN)}	Falling input threshold voltage		$0.3 \times V_{CCI}$	$0.4 ext{ x V}_{\text{CCI}}$		V
V _{I(HYS)}	Input threshold voltage hysteresis		$0.1 \times V_{CCI}$	$0.2 \times V_{CCI}$		V
I _{IH}	High-level input current	$V_{IH} = V_{CCI}^{(1)}$ at INx			10	μA
IIL	Low-level input current	V _{IL} = 0 V at INx	-10			μA
CMTI	Common-mode transient immunity	$V_I = V_{CCI}$ or 0 V, VCM = 1200 V; see Figure 17	85	100		kV/μs
CI	Input Capacitance ⁽²⁾	$V_{I} = V_{CC}/2 + 0.4 \times sin(2\pi ft), f = 1 MHz, V_{CC} = 5 V$		2		pF

 $\label{eq:V_CC} V_{CCI} = \mbox{Input-side } V_{CC}; \ V_{CCO} = \mbox{Output-side } V_{CC}.$ Measured from input pin to ground. (1)

(2)

6.10 Supply Current Characteristics—5-V Supply

 $V_{CC1} = V_{CC2} = 5 \text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITION	SUPPLY CURRENT	MIN	ТҮР	МАХ	UNIT	
ISO7720							
	$V_I = V_{CCI}$ (ISO7720), $V_I = 0 V$ (ISO7720 with F suffix)		I _{CC1}		0.8	1.1	
Supply surrant DC signal			I _{CC2}		1.1	1.7	
Supply current - DC signal		$V_{I} = 0 V (ISO7720), V_{I} = V_{CCI} (ISO7720 \text{ with F suffix})$			2.9	4.2	
	$v_1 = 0$ v (ISO7720), $v_1 = v_{CCI}$ (ISO772				1.2	1.9	
		1 Mhaa	I _{CC1}		1.8	2.7	mA
Supply current - AC signal		1 Mbps	I _{CC2}		1.3	1.9	mA
	All channels switching with square wave clock input; $C_L = 15 \text{ pF}$	10 Mhaa	I _{CC1}		1.9	2.7	
		10 Mbps	I _{CC2}		2.2	3	
		100 Mbaa	I _{CC1}		2.5	3.2	
		100 Mbps	I _{CC2}		11.6	14	
ISO7721			· · ·			·	
Quark automatic DO size al			I _{CC1} , I _{CC2}		1	1.6	
Supply current - DC signal	$V_I = 0 V (ISO7721),$ $V_I = V_{CCI} (ISO7721 \text{ with F suffix})$		I _{CC1} , I _{CC2}	2.2 3.2		3.2	mA
		1 Mbps	I _{CC1} , I _{CC2}		1.7	2.4	
Supply current - AC signal	All channels switching with square wave clock input; $C_1 = 15 \text{ pF}$	10 Mbps	I _{CC1} , I _{CC2}		2.2	3	
		100 Mbps	I _{CC1} , I _{CC2}		7.3	9	



6.11 Electrical Characteristics—3.3-V Supply

 $V_{CC1} = V_{CC2} = 3.3 \text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

002	1 8	,			
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level output voltage	$I_{OH} = -2 \text{ mA}; \text{ see Figure 15}$	$V_{CCO}^{(1)} - 0.3$	3.2		V
Low-level output voltage	I _{OL} = 2 mA; see Figure 15		0.1	0.3	V
Rising input voltage threshold			$0.6 \times V_{CCI}$	$0.7 \mathrm{~x~V_{CCI}}$	V
Falling input voltage threshold		0.3 x V _{CCI}	$0.4 ext{ x V}_{\text{CCI}}$		V
Input threshold voltage hysteresis		$0.1 \times V_{CCI}$	$0.2 \times V_{CCI}$		V
High-level input current	$V_{IH} = V_{CCI}^{(1)}$ at INx			10	μA
Low-level input current	V _{IL} = 0 V at INx	-10			μA
Common-mode transient immunity	$V_I = V_{CCI}$ or 0 V, VCM = 1200 V; see Figure 17	85	100		kV/μs
	PARAMETER High-level output voltage Low-level output voltage Rising input voltage threshold Falling input voltage threshold Input threshold voltage hysteresis High-level input current Low-level input current	PARAMETERTEST CONDITIONSHigh-level output voltage $I_{OH} = -2 \text{ mA}$; see Figure 15Low-level output voltage $I_{OL} = 2 \text{ mA}$; see Figure 15Rising input voltage thresholdFalling input voltage thresholdFalling input voltage thresholdInput threshold voltage hysteresisHigh-level input current $V_{IH} = V_{CCI}^{(1)}$ at INxLow-level input current $V_{IL} = 0 \text{ V at INx}$	PARAMETERTEST CONDITIONSMINHigh-level output voltage $I_{OH} = -2 \text{ mA}$; see Figure 15 $V_{CCO}^{(1)} - 0.3$ Low-level output voltage $I_{OL} = 2 \text{ mA}$; see Figure 15 $V_{CCO}^{(1)} - 0.3$ Rising input voltage threshold $0.3 \times V_{CCI}$ Falling input voltage threshold $0.3 \times V_{CCI}$ Input threshold voltage hysteresis $0.1 \times V_{CCI}^{(1)}$ High-level input current $V_{IH} = V_{CCI}^{(1)}$ at INxLow-level input current $V_{IL} = 0 \vee$ at INx -10	PARAMETERTEST CONDITIONSMINTYPHigh-level output voltage $I_{OH} = -2 \text{ mA}$; see Figure 15 $V_{CCO}^{(1)} - 0.3$ 3.2Low-level output voltage $I_{OL} = 2 \text{ mA}$; see Figure 150.1Rising input voltage threshold $0.6 \times V_{CCI}$ 0.4 × V_{CCI} Falling input voltage threshold $0.1 \times V_{CCI}$ $0.2 \times V_{CCI}$ Input threshold voltage hysteresis $0.1 \times V_{CCI}$ $0.2 \times V_{CCI}$ High-level input current $V_{IH} = V_{CCI}^{(1)}$ at INx -10	PARAMETERTEST CONDITIONSMINTYPMAXHigh-level output voltage $I_{OH} = -2 \text{ mA}$; see Figure 15 $V_{CCO}^{(1)} - 0.3$ 3.2 0.3 Low-level output voltage $I_{OL} = 2 \text{ mA}$; see Figure 15 0.1 0.3 0.3 Rising input voltage threshold $0.6 \times V_{CCI}$ $0.7 \times V_{CCI}$ Falling input voltage threshold $0.3 \times V_{CCI}$ $0.4 \times V_{CCI}$ Input threshold voltage hysteresis $0.1 \times V_{CCI}$ $0.2 \times V_{CCI}$ High-level input current $V_{IH} = V_{CCI}^{(1)}$ at INx -10

(1) V_{CCI} = Input-side V_{CC} ; V_{CCO} = Output-side V_{CC} .

6.12 Supply Current Characteristics—3.3-V Supply

 $V_{CC1} = V_{CC2} = 3.3 \text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	ТҮР	МАХ	UNIT
ISO7720						·	
	$V_{I} = V_{CCI}$ (ISO7720), $V_{I} = 0$ V (ISO7720 with F suffix)		I _{CC1}		0.8	1.1	
Supply current - DC signal			I _{CC2}		1.1	1.7	
Supply current - DC signal	V 0.V (ISO7720) V V (ISO7720 ···	the E auffini)	I _{CC1}		2.9	4.2	
	$v_1 = 0$ v (ISO7720), $v_1 = v_{CC1}$ (ISO7720 w	SO7720), $V_I = V_{CCI}$ (ISO7720 with F suffix)			1.2	1.9	
		1 Mhna	I _{CC1}		1.8	2.7	
		1 Mbps	I _{CC2}		1.2	1.9	mA
Supply surrant AC signal	All channels switching with square wave clock input; $C_L = 15 \text{ pF}$	10 Mbps	I _{CC1}		1.9	2.7	
Supply current - AC signal			I _{CC2}		1.9	2.6	
		100 Mbps	I _{CC1}		2.2	3.1	
			I _{CC2}		8.6	11	
IS07721							
	V _I = V _{CCI} (ISO7721), V _I = 0 V (ISO7721 w	th F suffix)	I _{CC1} , I _{CC2}		1	1.6	
Supply current - DC signal	V _I = 0 V (ISO7721), V _I = V _{CCI} (ISO7721 w	th F suffix)	I _{CC1} , I _{CC2}		2.2	3.2	
		1 Mbps	I _{CC1} , I _{CC2}		1.6	2.4	mA
Supply current - AC signal	All channels switching with square wave clock input; $C_1 = 15 \text{ pF}$	10 Mbps	I _{CC1} , I _{CC2}		2	2.8	
		100 Mbps	I _{CC1} , I _{CC2}		5.6	7	

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6.13 Electrical Characteristics—2.5-V Supply

 $V_{CC1} = V_{CC2} = 2.5 \text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	ТҮР	MAX	UNIT
V _{OH}	High-level output voltage	I _{OH} = -1 mA; see Figure 15	$V_{CCO}^{(1)} - 0.2$	2.45		V
V _{OL}	Low-level output voltage	I _{OL} = 1 mA; see Figure 15		0.05	0.2	V
V _{IT+(IN)}	Rising input voltage threshold			0.6 x V _{CCI}	$0.7 \mathrm{~x~V}_{\mathrm{CCI}}$	V
V _{IT-(IN)}	Falling input voltage threshold		0.3 x V _{CCI}	$0.4 ext{ x V}_{\text{CCI}}$		V
V _{I(HYS)}	Input threshold voltage hysteresis		$0.1 \times V_{CCI}$	$0.2 \times V_{CCI}$		V
I _{IH}	High-level input current	$V_{IH} = V_{CCI}^{(1)}$ at INx			10	μA
IIL	Low-level input current	V _{IL} = 0 V at INx	-10			μA
CMTI	Common-mode transient immunity	$V_I = V_{CCI}$ or 0 V, VCM = 1200 V; see Figure 17	85	100		kV/μs

(1) V_{CCI} = Input-side V_{CC} ; V_{CCO} = Output-side V_{CC} .

6.14 Supply Current Characteristics—2.5-V Supply

 $V_{CC1} = V_{CC2} = 2.5 \text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITION	IS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7720							
	$V_{I} = V_{CCI}$ (ISO7720), $V_{I} = 0 V$ (ISO7720 with F suffix)		I _{CC1}		0.8	1.1	
Supply surrent DC signal			I _{CC2}		1.1	1.7	
Supply current - DC signal	V ₁ = 0 V (ISO7720), V ₁ = V _{CC1} (ISO772		I _{CC1}		2.9	4.2	
	$v_1 = 0$ v (1307720), $v_1 = v_{CCI}$ (130772	to with F Sullix)	I _{CC2}		1.2	1.9	
	All channels switching with square wave clock input; $C_L = 15 \text{ pF}$	1 Mbpa	I _{CC1}		1.8	2.7	mA
		1 Mbps	I _{CC2}		1.3	1.9	ША
Supply surrent AC signal		10 Mhao	I _{CC1}		1.9	2.7	
Supply current - AC signal		10 Mbps	I _{CC2}		1.7	2.4	
		100 Mbps	I _{CC1}		2.2	3	
		TOO Mbps	I _{CC2}		6.8	9	
IS07721		-					
Supply surrent DC signal	V _I = V _{CCI} (ISO7721), V _I = 0 V (ISO772	21 with F suffix)	I _{CC1} , I _{CC2}		1	1.6	
Supply current - DC signal	V _I = 0 V (ISO7721), V _I = V _{CCI} (ISO772	21 with F suffix)	I _{CC1} , I _{CC2}		2.2	3.2	
		1 Mbps	I _{CC1} , I _{CC2}		1.6	2.4	mA
Supply current - AC signal	All channels switching with square wave clock input; $C_1 = 15 \text{ pF}$	10 Mbps	I _{CC1} , I _{CC2}		1.9	2.7	
		100 Mbps	I _{CC1} , I _{CC2}		4.6	6	

6.15 Switching Characteristics—5-V Supply

 $V_{CC1} = V_{CC2} = 5 \text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH} , t _{PHL}	Propagation delay time		6	11	16	ns
PWD	Pulse width distortion ⁽¹⁾ t _{PHL} – t _{PLH}	See Figure 15		0.5	4.9	ns
t _{sk(o)}	Channel-to-channel output skew time ⁽²⁾	Same direction channels			4	ns
t _{sk(pp)}	Part-to-part skew time ⁽³⁾				4.5	ns
t _r	Output signal rise time			1.8	3.9	ns
t _f	Output signal fall time	See Figure 15		1.9	3.9	ns
t _{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See Figure 16		0.1	0.3	μS
t _{ie}	Time interval error	2 ¹⁶ – 1 PRBS data at 100 Mbps		1		ns

(1) Also known as pulse skew.

 t_{sk(0)} is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

(3) t_{sk(pp)} is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.16 Switching Characteristics—3.3-V Supply

 $V_{CC1} = V_{CC2} = 3.3 \text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH} , t _{PHL}	Propagation delay time	See Figure 15	6	11	16	ns
PWD	Pulse width distortion ⁽¹⁾ t _{PHL} – t _{PLH}	See Figure 15		0.5	5	ns
t _{sk(o)}	Channel-to-channel output skew time ⁽²⁾	Same direction channels			4.1	ns
t _{sk(pp)}	Part-to-part skew time ⁽³⁾				4.5	ns
t _r	Output signal rise time			0.7	3	ns
t _f	Output signal fall time	See Figure 15		0.7	3	ns
t _{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See Figure 16		0.1	0.3	μS
t _{ie}	Time interval error	2 ¹⁶ – 1 PRBS data at 100 Mbps		1		ns

(1) Also known as pulse skew.

(2) t_{sk(0)} is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

(3) t_{sk(pp)} is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.17 Switching Characteristics—2.5-V Supply

 $V_{CC1} = V_{CC2} = 2.5 \text{ V} \pm 10\%$ (over recommended operating conditions unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{PLH} , t _{PHL}	Propagation delay time	Occ Finne 45	7.5	12	18.5	ns
PWD	Pulse width distortion ⁽¹⁾ t _{PHL} - t _{PLH}	See Figure 15		0.5	5.1	ns
t _{sk(o)}	Channel-to-channel output skew time ⁽²⁾	Same direction channels			4.1	ns
t _{sk(pp)}	Part-to-part skew time ⁽³⁾				4.6	ns
t _r	Output signal rise time			1	3.5	ns
t _f	Output signal fall time	See Figure 15		1	3.5	ns
t _{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See Figure 16 $$		0.1	0.3	μS
t _{ie}	Time interval error	2 ¹⁶ – 1 PRBS data at 100 Mbps		1		ns

(1) Also known as pulse skew.

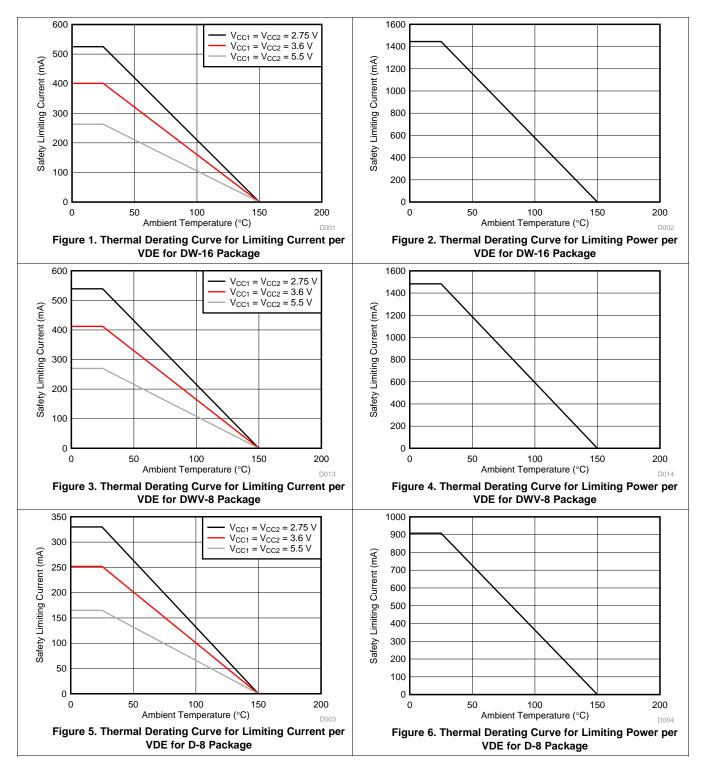
(2) t_{sk(0)} is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

(3) t_{sk(pp)} is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

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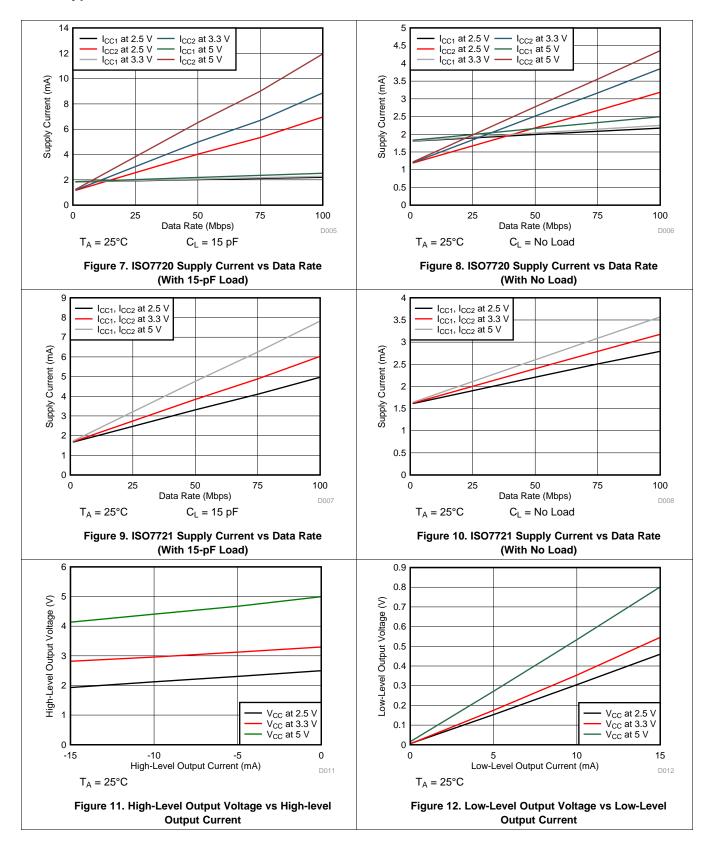
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6.18 Insulation Characteristics Curves





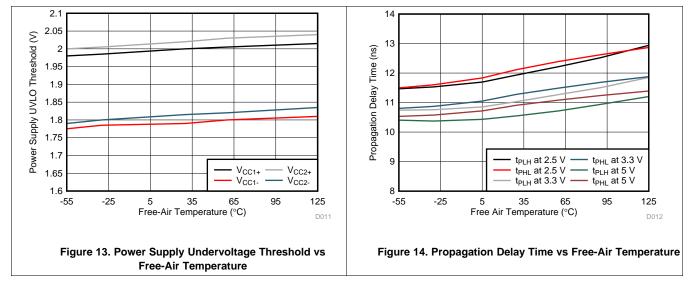
6.19 Typical Characteristics



ISO7720, ISO7721 SLLSEP3C – NOVEMBER 2016 – REVISED JULY 2018

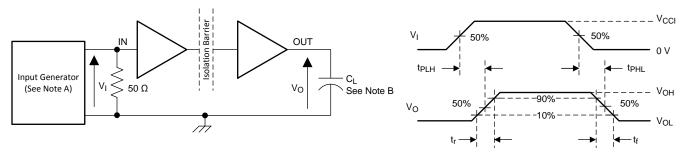
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Typical Characteristics (continued)



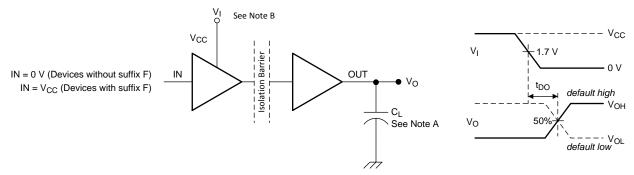


7 Parameter Measurement Information



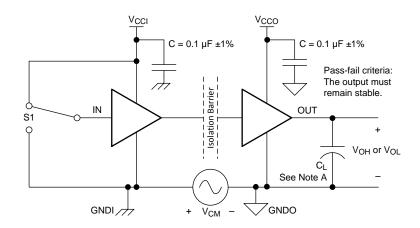
- A. The input pulse is supplied by a generator having the following characteristics: PRR \leq 50 kHz, 50% duty cycle, t_r \leq 3 ns, t_f \leq 3 ns, Z_O = 50 Ω . At the input, 50 Ω resistor is required to terminate Input Generator signal. It is not needed in actual application.
- B. $C_L = 15 \text{ pF}$ and includes instrumentation and fixture capacitance within ±20%.

Figure 15. Switching Characteristics Test Circuit and Voltage Waveforms



- A. $C_L = 15 \text{ pF}$ and includes instrumentation and fixture capacitance within $\pm 20\%$.
- B. Power Supply Ramp Rate = 10 mV/ns

Figure 16. Default Output Delay Time Test Circuit and Voltage Waveforms



A. $C_L = 15 \text{ pF}$ and includes instrumentation and fixture capacitance within ±20%.

Figure 17. Common-Mode Transient Immunity Test Circuit

TEXAS INSTRUMENTS

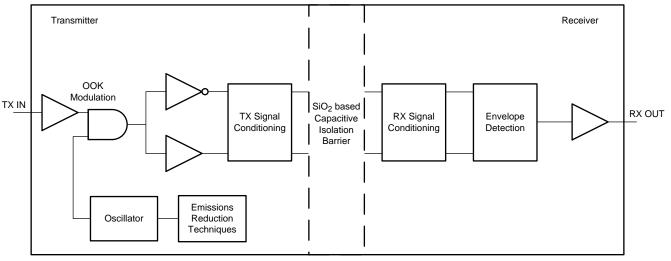
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8 Detailed Description

8.1 Overview

The ISO772x family of devices has an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. These devices also incorporate advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions due the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, Figure 18, shows a functional block diagram of a typical channel.

8.2 Functional Block Diagram



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Figure 18. Conceptual Block Diagram of a Digital Capacitive Isolator

Figure 19 shows a conceptual detail of how the OOK scheme works.

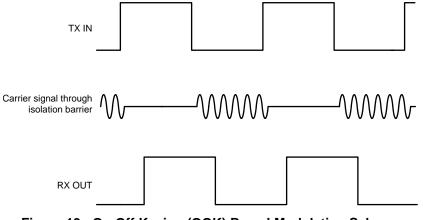


Figure 19. On-Off Keying (OOK) Based Modulation Scheme



8.3 Feature Description

The ISO772x family of devices is available in two channel configurations and default output state options to enable a variety of application uses. Table 1 lists the device features of the ISO772x devices.

PART NUMBER	MAXIMUM DATA RATE	CHANNEL DIRECTION	DEFAULT OUTPUT STATE	PACKAGE	RATED ISOLATION ⁽¹⁾						
				DW-16	5000 V _{RMS} / 8000 V _{PK}						
ISO7720	100 Mbps	2 Forward, 0 Reverse	High	DWV-8	5000 V _{RMS} / 7071 V _{PK}						
				D-8	3000 V _{RMS} / 4242 V _{PK}						
ISO7720F				DW-16	5000 V _{RMS} / 8000 V _{PK}						
	100 Mbps	2 Forward, 0 Reverse	Low	DWV-8	5000 V _{RMS} / 7071 V _{PK}						
				D-8	3000 V _{RMS} / 4242 V _{PK}						
	100 Mbps	1 Forward, 1 Reverse		DW-16	5000 V _{RMS} / 8000 V _{PK}						
ISO7721			High	DWV-8	5000 V _{RMS} / 7071 V _{PK}						
				D-8	3000 V _{RMS} / 4242 V _{PK}						
	100 Mbps			DW-16	5000 V _{RMS} / 8000 V _{PK}						
ISO7721F		1 Forward, 1 Reverse	Low	DWV-8	5000 V _{RMS} / 7071 V _{PK}						
				D-8	3000 V _{RMS} / 4242 V _{PK}						

Table 1. Device Features

(1) See the Safety-Related Certifications section for detailed isolation ratings.

8.3.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO772x family of devices incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.

8.4 Device Functional Modes

Table 2 lists the functional modes for the ISO772x devices.

V _{CCI}	V _{cco}	INPUT (INx) ⁽²⁾	OUTPUT (OUTx)	COMMENTS						
		н	н	Normal Operation:						
		L	L	A channel output assumes the logic state of the input.						
PU	PU	Open	Default	Default mode: When INx is open, the corresponding channel output goes to th default high logic state. The default is <i>High</i> for ISO772x and <i>Low</i> for ISO772x with F suffix.						
PD	PU	x	Default	Default mode: When V_{CCI} is unpowered, a channel output assumes the logic state based on the selected default option. The default is <i>High</i> for ISO772x and <i>Low</i> for ISO772x with F suffix. When V_{CCI} transitions from unpowered to powered-up, a channel output assumes the logic state of the input. When V_{CCI} transitions from powered-up to unpowered, channel output assumes the selected default state.						
X	PD	х	Undetermined	When V_{CCO} is unpowered, a channel output is undetermined ⁽³⁾ . When V_{CCO} transitions from unpowered to powered-up, a channel output assumes the logic state of the input						

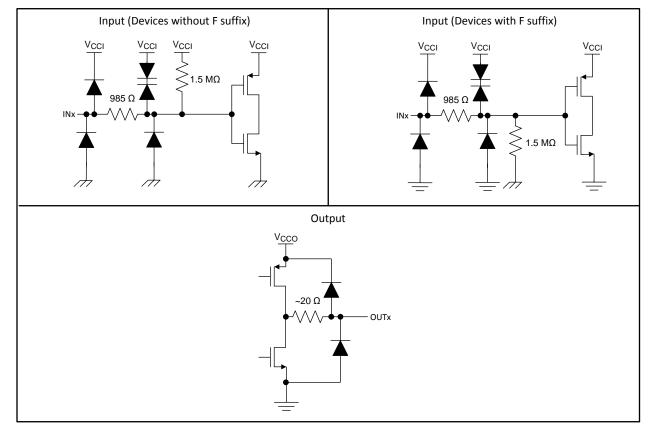
Table 2. Function Table⁽¹⁾

(1) V_{CCI} = Input-side V_{CC} ; V_{CCO} = Output-side V_{CC} ; PU = Powered up ($V_{CC} \ge 2.25$ V); PD = Powered down ($V_{CC} \le 1.7$ V); X = Irrelevant; H = High level; L = Low level

A strongly driven input signal can weakly power the floating V_{CC} via an internal protection diode and cause undetermined output. The outputs are in undetermined state when 1.7 V < V_{CCI}, V_{CCO} < 2.25 V. (2)

(3)

8.4.1 Device I/O Schematics







9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant the accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The ISO772x devices are high-performance, dual-channel digital isolators. The devices use single-ended CMOS-logic switching technology. The supply voltage range is from 2.25 V to 5.5 V for both supplies, V_{CC1} and V_{CC2} . When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, μ C or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

9.2 Typical Application

The ISO7721 device can be used with Texas Instruments' mixed signal microcontroller, digital-to-analog converter, transformer driver, and voltage regulator to create an isolated 4-mA to 20-mA current loop.

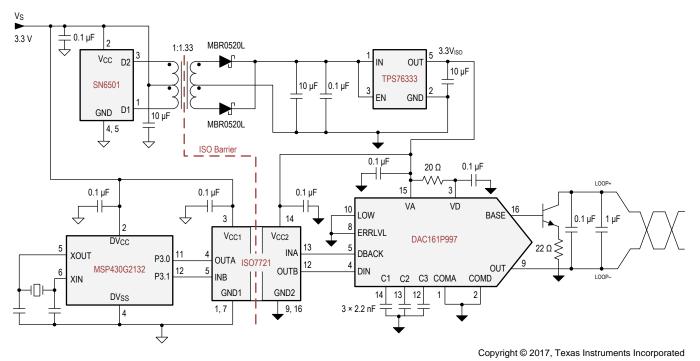


Figure 21. Isolated 4-mA to 20-mA Current Loop



Typical Application (continued)

9.2.1 Design Requirements

To design with these devices, use the parameters listed in Table 3.

PARAMETER	VALUE
Supply voltage, V_{CC1} and V_{CC2}	2.25 V to 5.5 V
Decoupling capacitor between V _{CC1} and GND1	0.1 µF
Decoupling capacitor from V_{CC2} and GND2	0.1 µF

9.2.2 Detailed Design Procedure

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO772x devices only require two external bypass capacitors to operate.

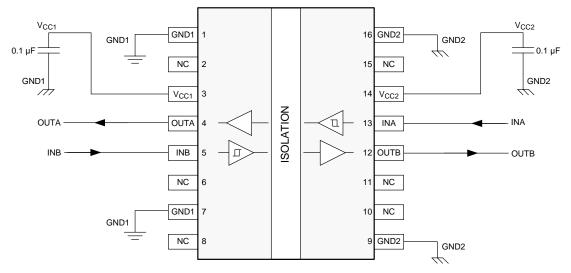
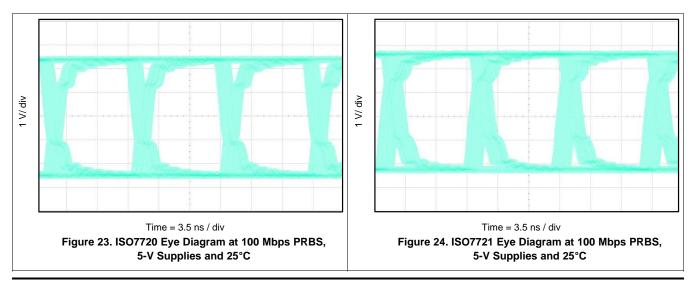


Figure 22. Typical ISO7721 Circuit Hook-up

9.2.3 Application Curve

The following typical eye diagrams of the ISO772x family of devices indicate low jitter and wide open eye at the maximum data rate of 100 Mbps.



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10 Power Supply Recommendations

To help ensure reliable operation at data rates and supply voltages, a $0.1-\mu$ F bypass capacitor is recommended at the input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501 or SN6505A. For such applications, detailed power supply design and transformer selection recommendations are available in *SN6501 Transformer Driver for Isolated Power Supplies* or *SN6505 Low-Noise 1-A Transformer Drivers for Isolated Power Supplies*.

11 Layout

11.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 25). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in².
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

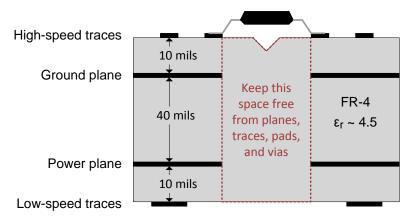
If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

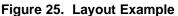
For detailed layout recommendations, refer to the Digital Isolator Design Guide.

11.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

11.2 Layout Example





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12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

For development support, refer to:

- Isolated CAN Flexible Data (FD) Rate Repeater Reference Design
- Isolated 16-Channel AC Analog Input Module Reference Design Using Dual Simultaneously Sampled ADCs
- Polyphase Shunt Metrology with Isolated AFE Reference Design
- Reference Design for Power-Isolated Ultra-Compact Analog Output Module

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, DAC161P997 Single-Wire 16-bit DAC for 4- to 20-mA Loops data sheet
- Texas Instruments, Digital Isolator Design Guide
- Texas Instruments, Isolation Glossary
- Texas Instruments, MSP430G2132 Mixed Signal Microcontroller data sheet
- Texas Instruments, SN6501 Transformer Driver for Isolated Power Supplies data sheet
- Texas Instruments, TPS76333Low-Power 150-mA Low-Dropout Linear Regulators data sheet

12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY					
ISO7720	Click here	Click here	Click here	Click here	Click here					
ISO7721	Click here	Click here	Click here	Click here	Click here					

Table 4. Related Links

12.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.5 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E[™] Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.6 Trademarks

E2E is a trademark of Texas Instruments. All other trademarks are the property of their respective owners.



12.7 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.8 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

D0008B



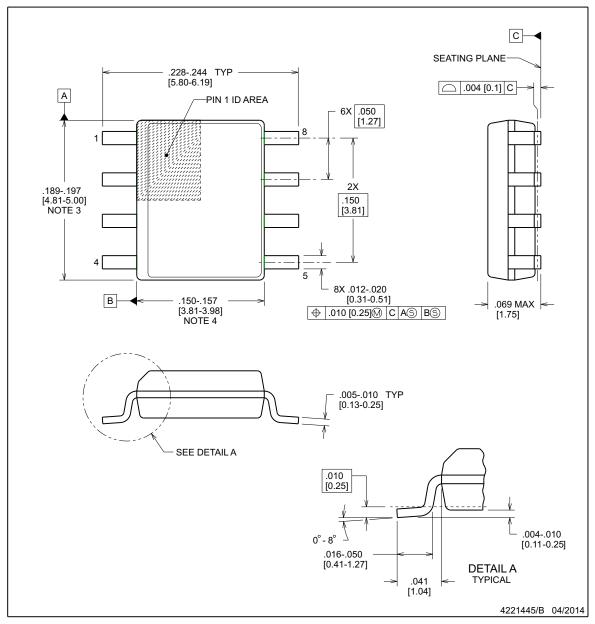
www.ti.com



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SOIC



NOTES:

- 1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed .006 [0.15], per side.
- 4. This dimension does not include interlead flash.
- 5. Reference JEDEC registration MS-012, variation AA.

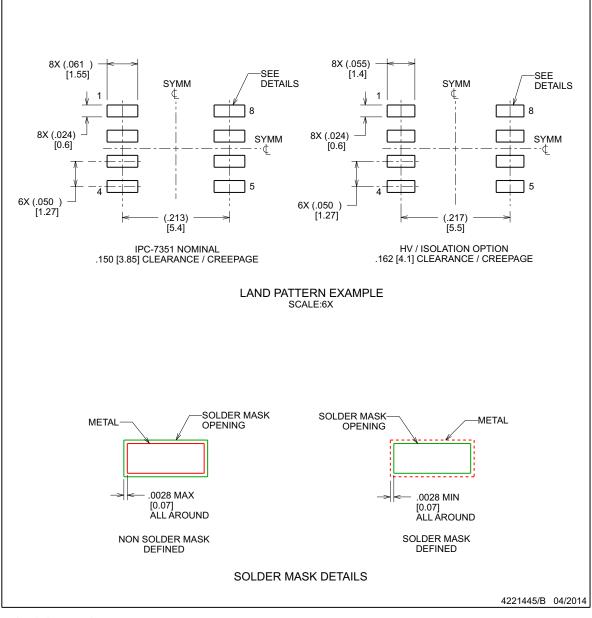


EXAMPLE BOARD LAYOUT

SOIC - 1.75 mm max height

D0008B

SOIC



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

D0008B

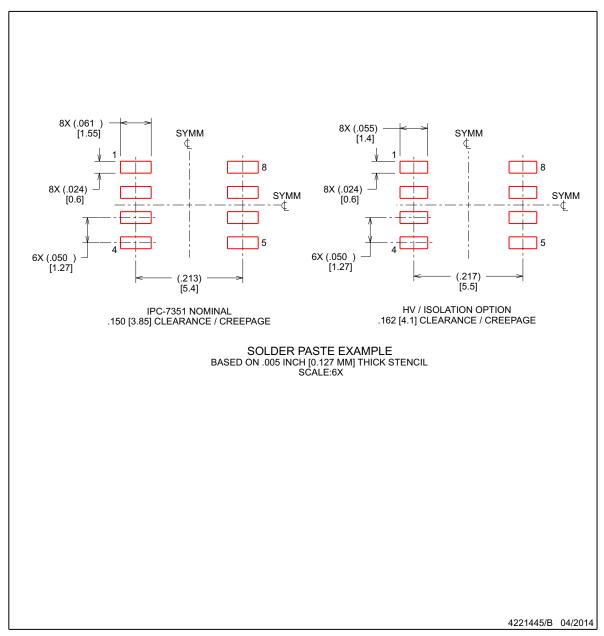
Texas Instruments

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EXAMPLE STENCIL DESIGN

SOIC - 1.75 mm max height

SOIC



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.

28



24-Aug-2018

PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package Drawing	Pins	•		Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)				Qty	(2)	(6)	(3)		(4/5)	
ISO7720D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7720	Samples
ISO7720DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7720	Samples
ISO7720DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7720	Samples
ISO7720DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7720	Samples
ISO7720DWV	ACTIVE	SOIC	DWV	8	64	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-55 to 125	7720	Samples
ISO7720DWVR	ACTIVE	SOIC	DWV	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-55 to 125	7720	Samples
ISO7720FD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7720F	Samples
ISO7720FDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7720F	Samples
ISO7720FDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7720F	Samples
ISO7720FDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7720F	Samples
ISO7720FDWV	ACTIVE	SOIC	DWV	8	64	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-55 to 125	7720F	Samples
ISO7720FDWVR	ACTIVE	SOIC	DWV	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-55 to 125	7720F	Samples
ISO7721D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7721	Samples
ISO7721DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7721	Samples
ISO7721DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7721	Samples
ISO7721DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7721	Samples
ISO7721DWV	ACTIVE	SOIC	DWV	8	64	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-55 to 125	7721	Samples



24-Aug-2018

Orderable Device	Status	Package Type	Package	Pins	Package	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking	Samples
	(1)		Drawing		Qty	(2)	(6)	(3)		(4/5)	
ISO7721DWVR	ACTIVE	SOIC	DWV	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-55 to 125	7721	Samples
ISO7721FD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7721F	Samples
ISO7721FDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	7721F	Samples
ISO7721FDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7721F	Samples
ISO7721FDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-55 to 125	ISO7721F	Samples
ISO7721FDWV	ACTIVE	SOIC	DWV	8	64	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-55 to 125	7721F	Samples
ISO7721FDWVR	ACTIVE	SOIC	DWV	8	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-55 to 125	7721F	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <= 1000ppm threshold. Antimony trioxide based flame retardants must also meet the <= 1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.



PACKAGE OPTION ADDENDUM

24-Aug-2018

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF ISO7720, ISO7721 :

• Automotive: ISO7720-Q1, ISO7721-Q1

NOTE: Qualified Version Definitions:

• Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7720DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7720DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7720DWVR	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
ISO7720FDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7720FDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7720FDWVR	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
ISO7721DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7721DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7721DWVR	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
ISO7721FDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7721FDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7721FDWVR	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1

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PACKAGE MATERIALS INFORMATION

7-Aug-2018



*All dimensions are nominal							
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7720DR	SOIC	D	8	2500	367.0	367.0	38.0
ISO7720DWR	SOIC	DW	16	2000	367.0	367.0	38.0
ISO7720DWVR	SOIC	DWV	8	1000	367.0	367.0	38.0
ISO7720FDR	SOIC	D	8	2500	367.0	367.0	38.0
ISO7720FDWR	SOIC	DW	16	2000	367.0	367.0	38.0
ISO7720FDWVR	SOIC	DWV	8	1000	367.0	367.0	38.0
ISO7721DR	SOIC	D	8	2500	367.0	367.0	38.0
ISO7721DWR	SOIC	DW	16	2000	367.0	367.0	38.0
ISO7721DWVR	SOIC	DWV	8	1000	367.0	367.0	38.0
ISO7721FDR	SOIC	D	8	2500	367.0	367.0	38.0
ISO7721FDWR	SOIC	DW	16	2000	367.0	367.0	38.0
ISO7721FDWVR	SOIC	DWV	8	1000	367.0	367.0	38.0

DWV0008A



SOIC - 2.8 mm max height

SOIC



- NOTES:
- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing
- Per ASME Y14.5M.
 This drawing is subject to change without notice.
 This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

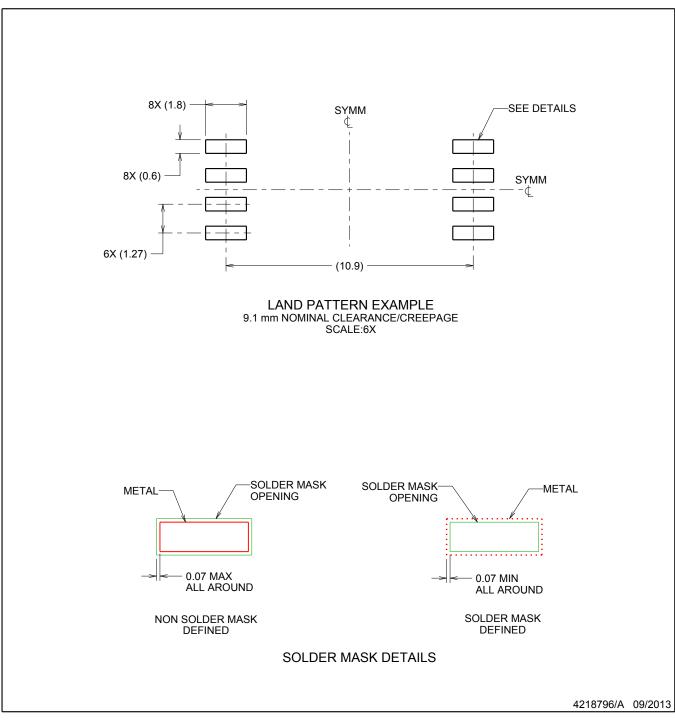


DWV0008A

EXAMPLE BOARD LAYOUT

SOIC - 2.8 mm max height

SOIC



NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



EXAMPLE STENCIL DESIGN

DWV0008A

SOIC - 2.8 mm max height

SOIC



NOTES: (continued)



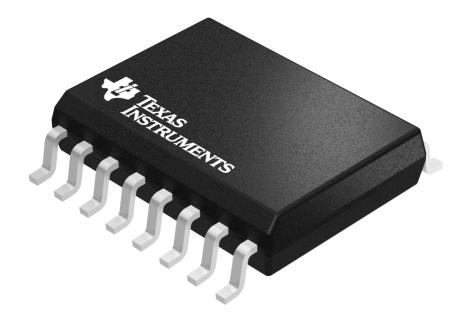
^{7.} Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

^{8.} Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

SOIC - 2.65 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



4040000-2/H

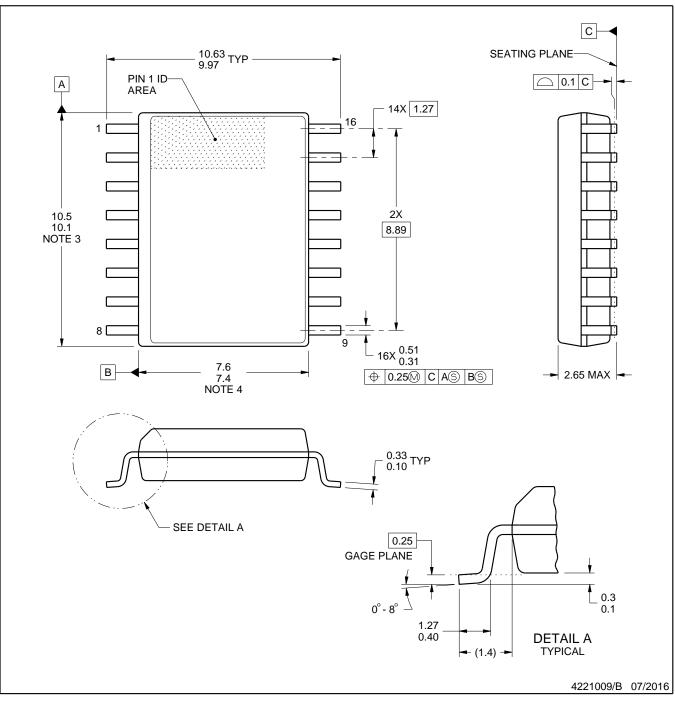
DW0016B



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



NOTES:

- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing
- Per ASME Y14.5M.
 This drawing is subject to change without notice.
 This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
- 5. Reference JEDEC registration MS-013.



DW0016B

EXAMPLE BOARD LAYOUT

SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



DW0016B

EXAMPLE STENCIL DESIGN

SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.



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