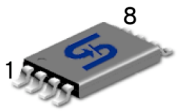
TSM6866D

20V Dual N-Channel MOSFET

TSSOP-8



Pin Definition:

1. Drain 1	8. Drain 2
2. Source 1	7. Source 2
3. Source 1	6. Source 2
4. Gate 1	5. Gate 2

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$(mΩ)	I_D (A)
20	30 @ V_{GS} = 4.5V	6.0
	40 @ V_{GS} = 2.5V	5.2

Features

- Advance Trench Process Technology
- High Density Cell Design for Ultra Low On-resistance

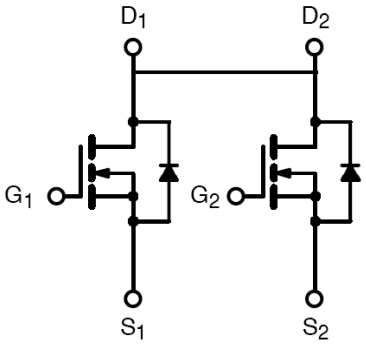
Application

- Specially Designed for Li-on Battery Packs
- Battery Switch Application

Ordering Information

Part No.	Package	Packing
TSM6866DCA RV	TSSOP-8	T&R

Block Diagram



Dual N-Channel MOSFET

Absolute Maximum Rating (Ta = 25 °C unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current		I_D	6	A
Pulsed Drain Current		I_{DM}	30	A
Continuous Source Current (Diode Conduction)[a,b]		I_S	1.7	A
Maximum Power Dissipation	Ta = 25 °C	P_D	1.6	W
	Ta = 75 °C		1.1	
Operating Junction Temperature		T_J	+150	°C
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Thermal Performance

Parameter	Symbol	Limit	Unit
Junction to Case Thermal Resistance	$R\Theta_{JC}$	40	°C/W
Junction to Ambient Thermal Resistance (PCB mounted)	$R\Theta_{JA}$	77	°C/W

Notes:

a. Pulse width limited by the Maximum junction temperature

b. Surface Mounted on FR4 Board, t ≤ 5 sec.

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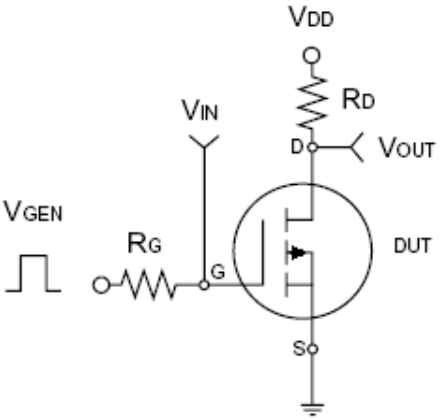
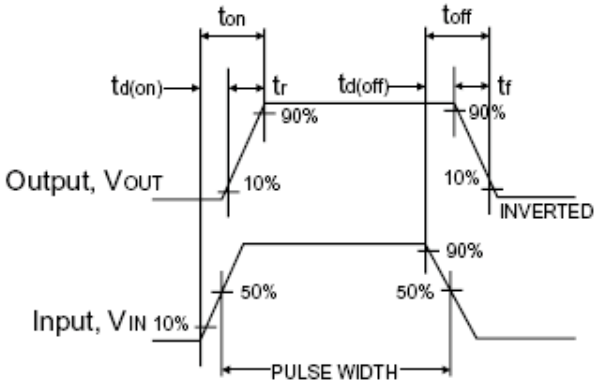
Electrical Specifications

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250uA	BV_{DSS}	20	--	--	V
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250uA	$V_{GS(TH)}$	0.6	--	--	V
Gate Body Leakage	V_{GS} = ±12V, V_{DS} = 0V	I_{GSS}	--	--	±100	nA
Zero Gate Voltage Drain Current	V_{DS} = 20V, V_{GS} = 0V	I_{DSS}	--	--	1.0	uA
On-State Drain Current	V_{DS} =5V, V_{GS} = 4.5V	$I_{D(ON)}$	30	--	--	A
Drain-Source On-State Resistance	V_{GS} = 4.5V, I_D = 6.0A	$R_{DS(ON)}$	--	21	30	mΩ
	V_{GS} = 2.5V, I_D = 5.2A		--	30	40	
Forward Transconductance	V_{DS} = 10V, I_D = 6A	g_{fs}	--	30	--	S
Diode Forward Voltage	I_S = 1.7A, V_{GS} = 0V	V_{SD}	--	0.7	1.2	V
Dynamic[b]						
Total Gate Charge	V_{DS} = 10V, I_D = 6A, V_{GS} = 4.5V	Q_g	--	4.86	--	nC
Gate-Source Charge		Q_{gs}	--	0.92	--	
Gate-Drain Charge		Q_{gd}	--	1.4	--	
Input Capacitance	V_{DS} = 8V, V_{GS} = 0V, f = 1.0MHz	C_{iss}	--	562	--	pF
Output Capacitance		C_{oss}	--	106	--	
Reverse Transfer Capacitance		C_{rss}	--	75	--	
Switching[c]						
Turn-On Delay Time	V_{DD} = 10V, R_L = 10Ω, I_D = 1A, V_{GEN} = 4.5V, R_G = 6Ω	$t_{d(on)}$	--	8.1	--	nS
Turn-On Rise Time		t_r	--	9.95	--	
Turn-Off Delay Time		$t_{d(off)}$	--	21.85	--	
Turn-Off Fall Time		t_f	--	5.35	--	

Notes:
a. pulse test: PW ≤300μS, duty cycle ≤2%
b. For DESIGN AID ONLY, not subject to production testing.
b. Switching time is essentially independent of operating temperature.



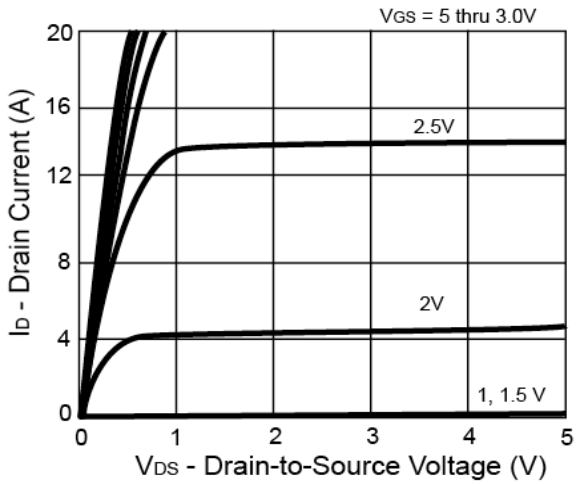
Switching Test Circuit



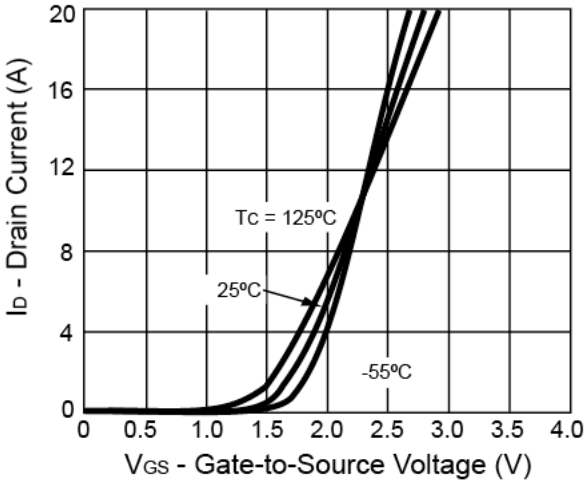
Switchin Waveforms

Electrical Characteristics Curve (Ta = 25 °C, unless otherwise noted)

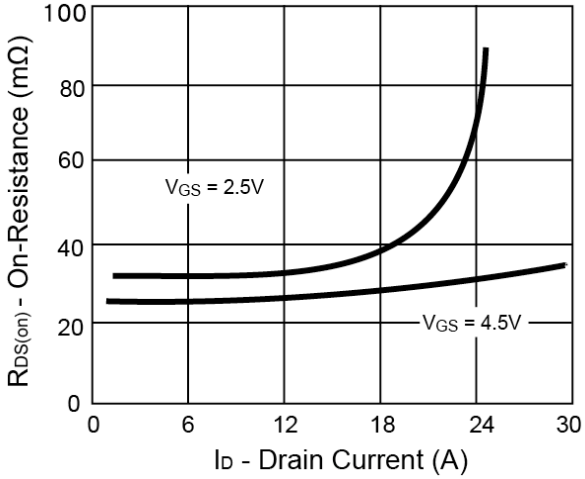
Output Characteristics



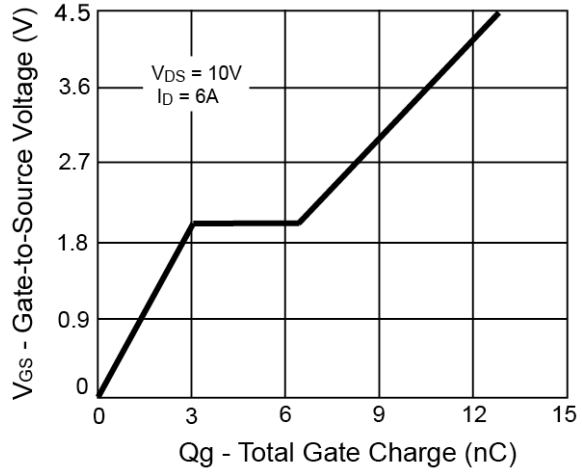
Transfer Characteristics



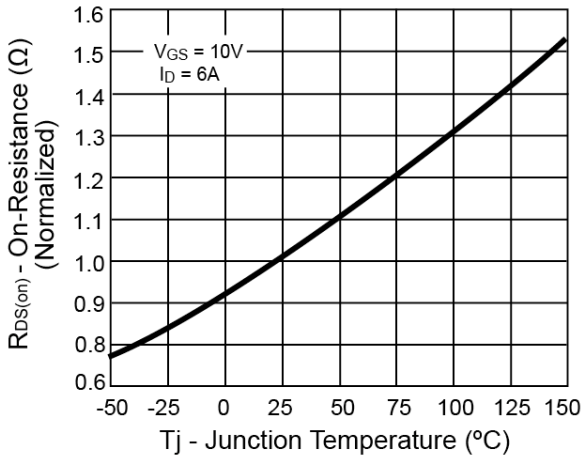
On-Resistance vs. Drain Current



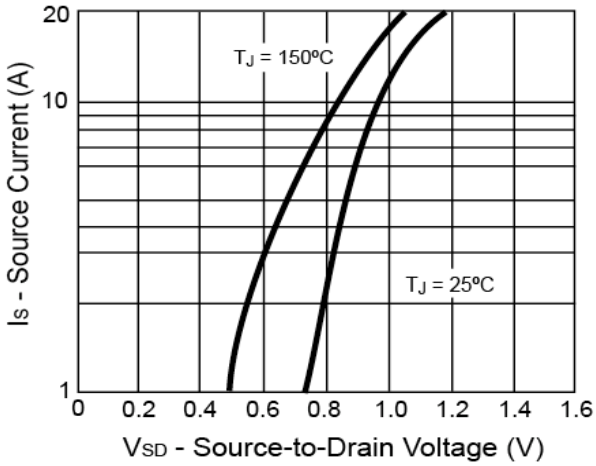
Gate Charge



On-Resistance vs. Junction Temperature

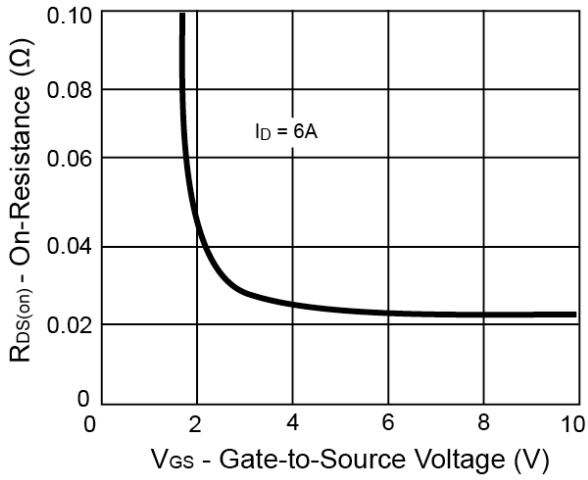


Source-Drain Diode Forward Voltage

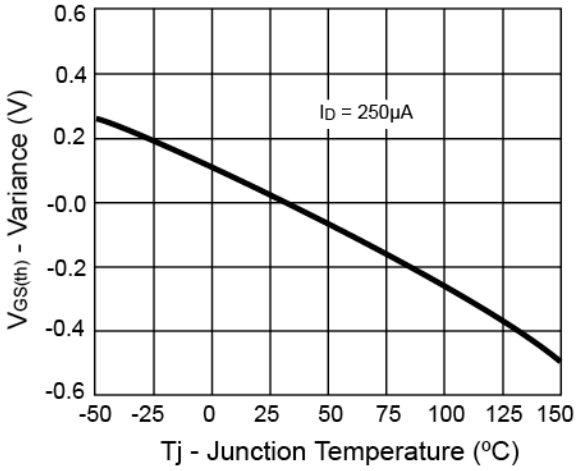


Electrical Characteristics Curve (Ta = 25 °C, unless otherwise noted)

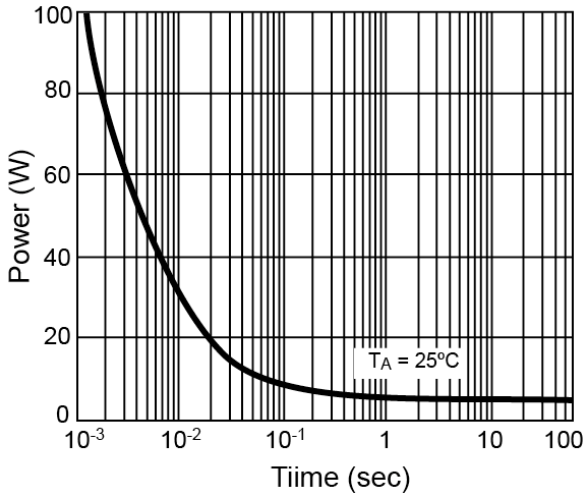
On-Resistance vs. Gate-Source Voltage



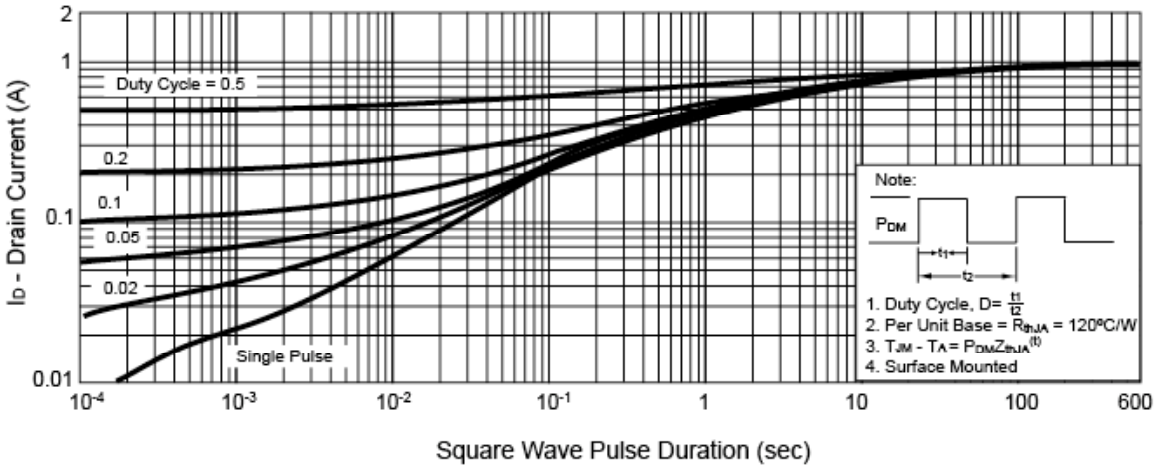
Threshold Voltage



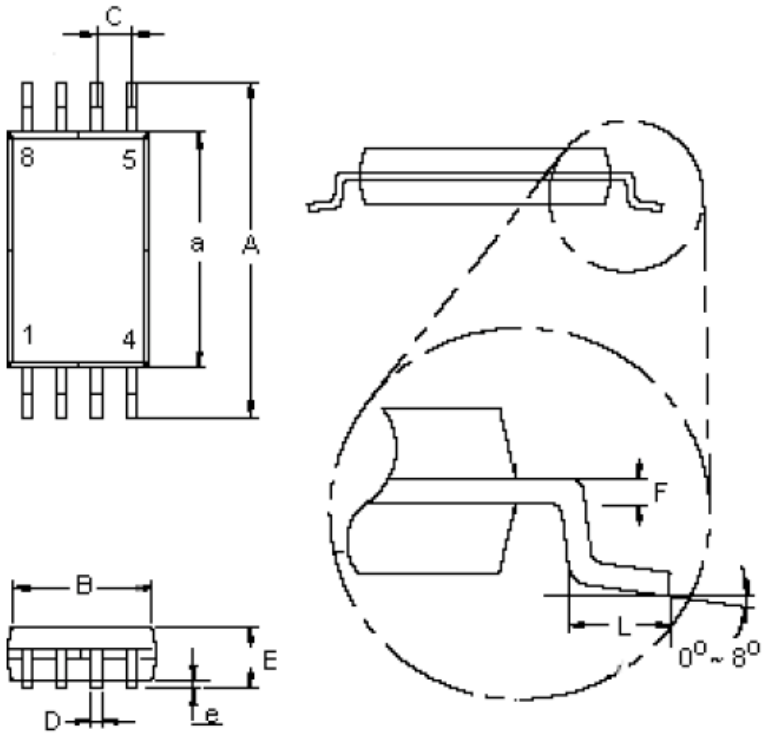
Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient



TSSOP-8 Mechanical Drawing



TSSOP-8 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.20	6.60	0.244	0.260
a	4.30	4.50	0.170	0.177
B	2.90	3.10	0.114	0.122
C	0.65 (typ)		0.025 (typ)	
D	0.25	0.30	0.010	0.019
E	1.05	1.20	0.041	0.049
e	0.05	0.15	0.002	0.009
F	0.127		0.005	
L	0.50	0.70	0.020	0.028

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