

N- and P-Channel 60V (D-S) Power MOSFET

FEATURES

- Low $R_{DS(on)}$ to minimize conductive losses
- Low gate charge for fast power switching
- 100% UIS and R_g tested
- Compliant to RoHS directive 2011/65/EU and in accordance to WEEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21

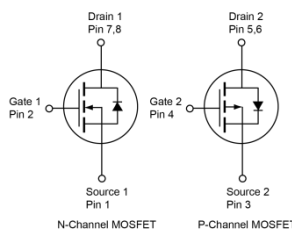
APPLICATIONS

- DC-DC Converters
- Power Routing
- Motor Drives

KEY PERFORMANCE PARAMETERS			
PARAMETER	TYPE	VALUE	UNIT
V_{DS}	N-ch	60	V
	P-ch	-60	
$R_{DS(on)}$ (max)	N-ch	$V_{GS} = 10V$	34
		$V_{GS} = 4.5V$	40
	P-ch	$V_{GS} = -10V$	68
		$V_{GS} = -4.5V$	110
Q_g	N-ch	10.3	nC
	P-ch	9.5	



PDFN56 Dual



Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)				
PARAMETER	SYMBOL	N-ch	P-ch	UNIT
Drain-Source Voltage	V_{DS}	60	-60	V
Gate-Source Voltage	V_{GS}	± 20	± 20	V
Continuous Drain Current (Note 1)	I_D	$T_C = 25^\circ\text{C}$	24	-18
		$T_A = 25^\circ\text{C}$	5.4	-4
Pulsed Drain Current	I_{DM}	96	-72	A
Single Pulse Avalanche Current (Note 2)	I_{AS}	12.7	-12.7	A
Single Pulse Avalanche Energy (Note 2)	E_{AS}	24	24	mJ
Total Power Dissipation	P_D	$T_C = 25^\circ\text{C}$	40	40
		$T_C = 125^\circ\text{C}$	8.1	8.1
Total Power Dissipation	P_D	$T_A = 25^\circ\text{C}$	2	2
		$T_A = 125^\circ\text{C}$	0.4	0.4
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to +150		$^\circ\text{C}$

THERMAL PERFORMANCE			
PARAMETER	SYMBOL	LIMIT	UNIT
Thermal Resistance – Junction to Case	$R_{\theta JC}$	3.1	$^\circ\text{C/W}$
Thermal Resistance – Junction to Ambient	$R_{\theta JA}$	61	

Thermal Performance Note: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. $R_{\theta JA}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

ELECTRICAL SPECIFICATIONS ($T_A = 25^\circ\text{C}$ unless otherwise noted)							
PARAMETER	CONDITIONS	SYMBOL	TYPE	MIN	TYP	MAX	UNIT
Static							
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu\text{A}$	BV_{DSS}	N-ch	60	--	--	V
	$V_{GS} = 0V, I_D = -250\mu\text{A}$		P-ch	-60	--	--	
Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	$V_{GS(TH)}$	N-ch	1.2	1.7	2.5	V
	$V_{GS} = V_{DS}, I_D = -250\mu\text{A}$		P-ch	-1.2	-1.5	-2.5	
Gate-Source Leakage Current	$V_{GS} = \pm 20V, V_{DS} = 0V$	I_{GSS}	N-ch	--	--	± 100	nA
	$V_{GS} = \pm 20V, V_{DS} = 0V$		P-ch	--	--	± 100	nA
Drain-Source Leakage Current	$V_{GS} = 0V, V_{DS} = 60V$	I_{DSS}	N-ch	--	--	1	μA
	$V_{GS} = 0V, V_{DS} = 60V$ $T_J = 125^\circ\text{C}$			--	--	100	
	$V_{GS} = 0V, V_{DS} = -60V$		P-ch	--	--	-1	
	$V_{GS} = 0V, V_{DS} = -60V$ $T_J = 125^\circ\text{C}$			--	--	-100	
Drain-Source On-State Resistance ^(Note 3)	$V_{GS} = 10V, I_D = 5.4A$	$R_{DS(on)}$	N-ch	--	28	34	m Ω
	$V_{GS} = 4.5V, I_D = 4.9A$			--	33	40	
	$V_{GS} = -10V, I_D = -4A$		P-ch	--	57	68	
	$V_{GS} = -4.5V, I_D = -3.2A$			--	73	110	
Forward Transconductance ^(Note 3)	$V_{DS} = 5V, I_D = 5.4A$	g_{fs}	N-ch	--	19	--	S
	$V_{DS} = -5V, I_D = -4A$		P-ch	--	11	--	
Dynamic ^(Note 4)							
Total Gate Charge	N-ch $V_{DS} = 30V, I_D = 5.4A$ P-ch $V_{DS} = -30V, I_D = -4A$	$Q_{g(VGS=10V)}$	N-ch	--	20.8	--	nC
		$Q_{g(VGS=-10V)}$	P-ch	--	18.1	--	
Total Gate Charge	N-ch	$Q_{g(VGS=4.5V)}$	N-ch	--	10.3	--	nC
		$Q_{g(VGS=-4.5V)}$	P-ch	--	9.5	--	
Gate-Source Charge	$V_{DS} = 30V, I_D = 4.9A$	Q_{gs}	N-ch	--	3.9	--	nC
			P-ch	--	2.6	--	
Gate-Drain Charge	$V_{DS} = -30V, I_D = -3.2A$	Q_{gd}	N-ch	--	4.2	--	nC
			P-ch	--	4.8	--	
Input Capacitance	N-ch $V_{GS} = 0V, V_{DS} = 30V$	C_{iss}	N-ch	--	1159	--	pF
			P-ch	--	930	--	
Output Capacitance	f = 1.0MHz P-ch	C_{oss}	N-ch	--	59	--	pF
			P-ch	--	65	--	
Reverse Transfer Capacitance	$V_{GS} = 0V, V_{DS} = -30V$ f = 1.0MHz	C_{rss}	N-ch	--	15	--	pF
			P-ch	--	26	--	
Gate Resistance	f = 1.0MHz	R_g	N-ch	0.6	2	4	Ω
			P-ch	4.5	15	30	

ELECTRICAL SPECIFICATIONS ($T_A = 25^\circ\text{C}$ unless otherwise noted)							
PARAMETER	CONDITIONS	SYMBOL	TYPE	MIN	TYP	MAX	UNIT
Switching (Note 4)							
Turn-On Delay Time	N-ch	$t_{d(on)}$	N-ch	--	7.4	--	ns
			P-ch	--	4	--	
Turn-On Rise Time	$V_{GS} = 10\text{V}, V_{DS} = 30\text{V}, I_D = 5.4\text{A}, R_G = 2\Omega$	t_r	N-ch	--	25	--	
			P-ch	--	28	--	
Turn-Off Delay Time	P-ch	$t_{d(off)}$	N-ch	--	18	--	
			P-ch	--	44	--	
Turn-Off Fall Time	$I_D = -4\text{A}, R_G = 2\Omega$	t_f	N-ch	--	18	--	
			P-ch	--	44	--	
Source-Drain Diode							
Forward Voltage (Note 3)	$V_{GS} = 0\text{V}, I_S = 5.4\text{A}$	V_{SD}	N-ch	--	--	1	V
	$V_{GS} = 0\text{V}, I_S = -4\text{A}$		P-ch	--	--	-1	
Reverse Recovery Time	N-ch $I_S = 5.4\text{A}, di/dt = 100\text{A}/\mu\text{s}$	t_{rr}	N-ch	--	16	--	ns
			P-ch	--	13	--	
Reverse Recovery Charge	P-ch $I_S = -4\text{A}, di/dt = 100\text{A}/\mu\text{s}$	Q_{rr}	N-ch	--	11	--	nC
			P-ch	--	7.8	--	

Notes:

- Silicon limited current only.
- N-ch : $L = 0.3\text{mH}, V_{GS} = 10\text{V}, V_{DD} = 25\text{V}, R_G = 25\Omega, I_{AS} = 12.7\text{A}$, Starting $T_J = 25^\circ\text{C}$
 P-ch : $L = 0.3\text{mH}, V_{GS} = -10\text{V}, V_{DD} = -25\text{V}, R_G = 25\Omega, I_{AS} = -12.7\text{A}$, Starting $T_J = 25^\circ\text{C}$
- Pulse test: Pulse Width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
- Switching time is essentially independent of operating temperature.

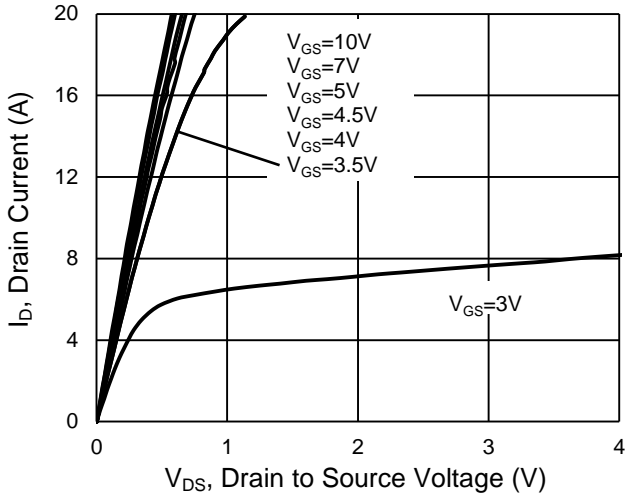
ORDERING INFORMATION

PART NO.	PACKAGE	PACKING
TSM6502CR RLG	PDFN56 Dual	2,500pcs / 13" Reel

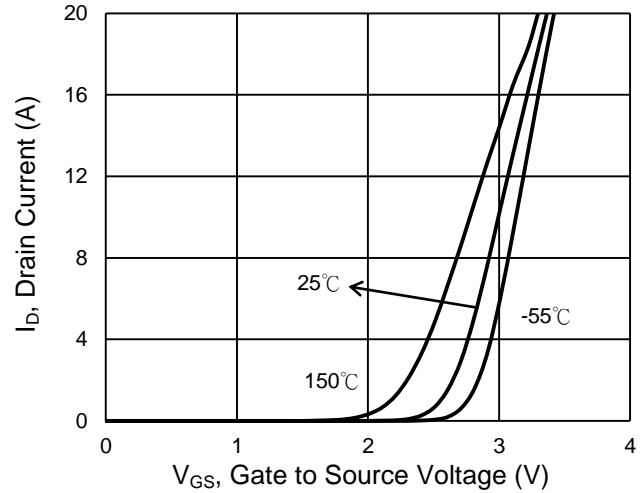
CHARACTERISTICS CURVES (N-Channel)

($T_A = 25^\circ\text{C}$ unless otherwise noted)

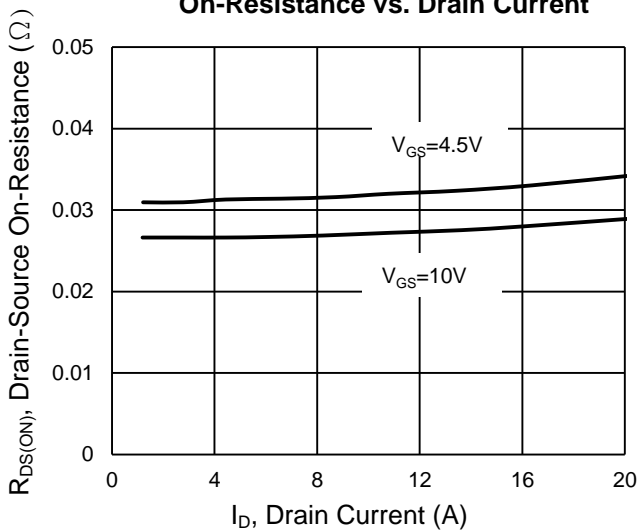
Output Characteristics



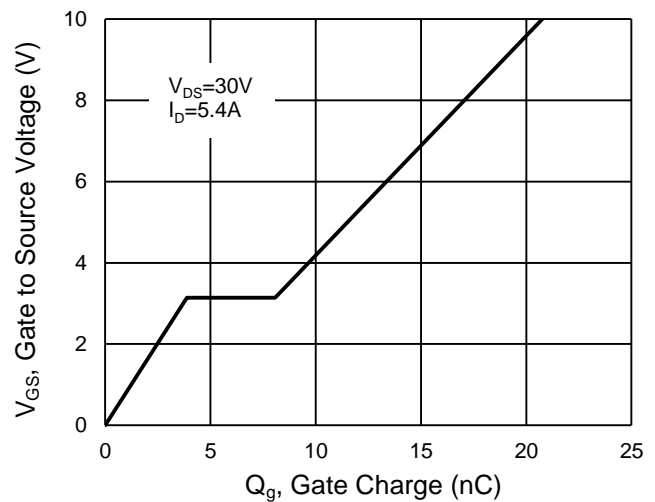
Transfer Characteristics



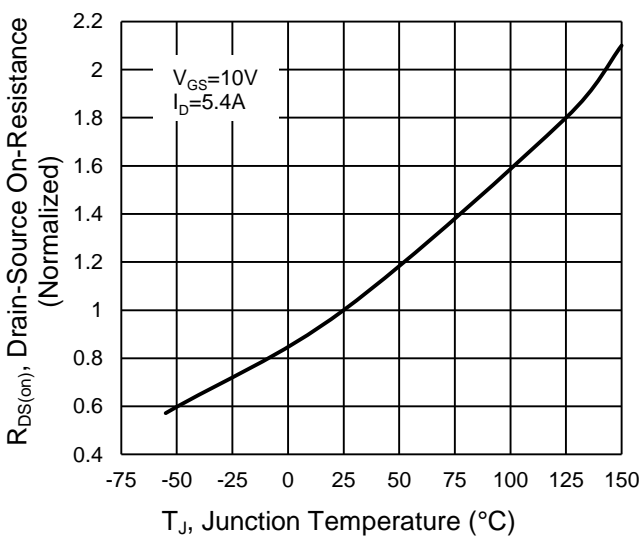
On-Resistance vs. Drain Current



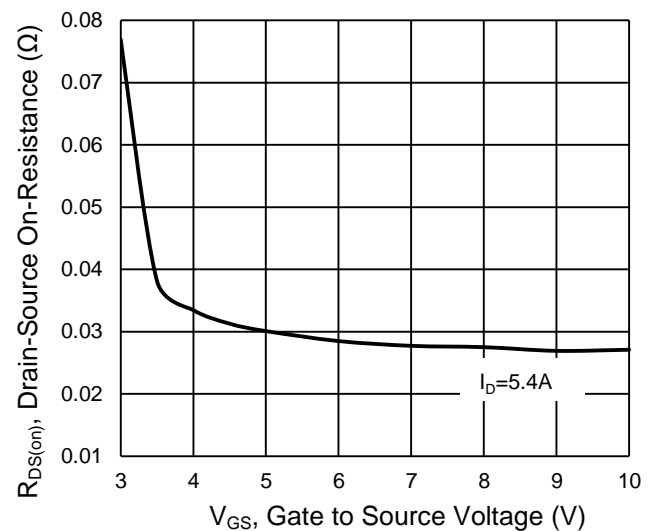
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature



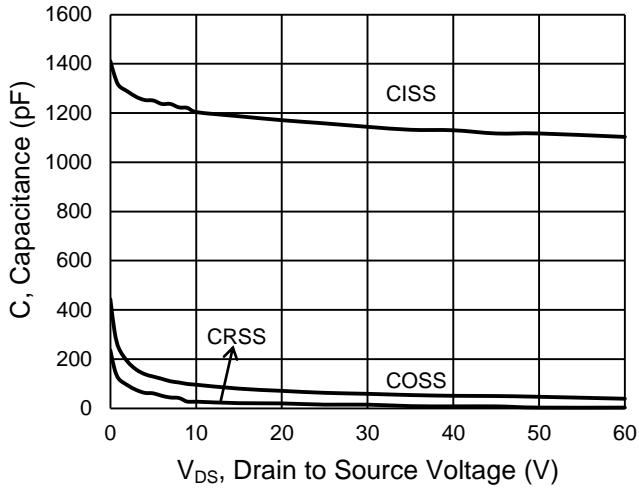
On-Resistance vs. Gate-Source Voltage



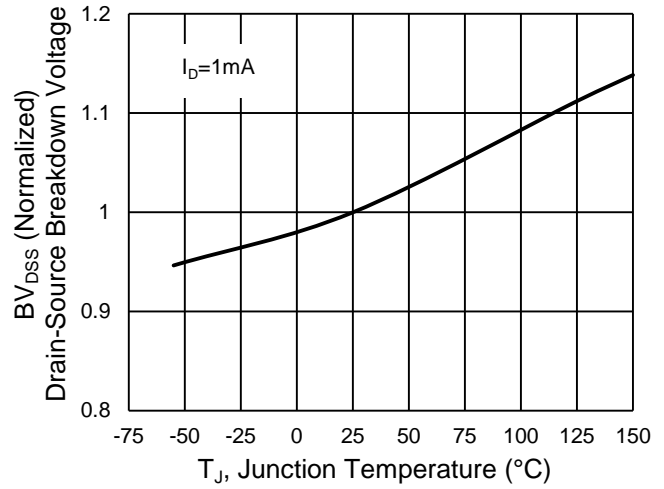
CHARACTERISTICS CURVES (N-Channel)

($T_A = 25^\circ\text{C}$ unless otherwise noted)

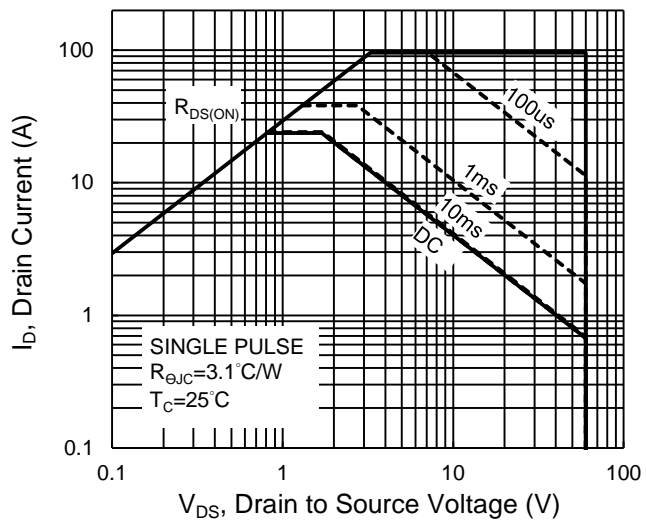
Capacitance vs. Drain-Source Voltage



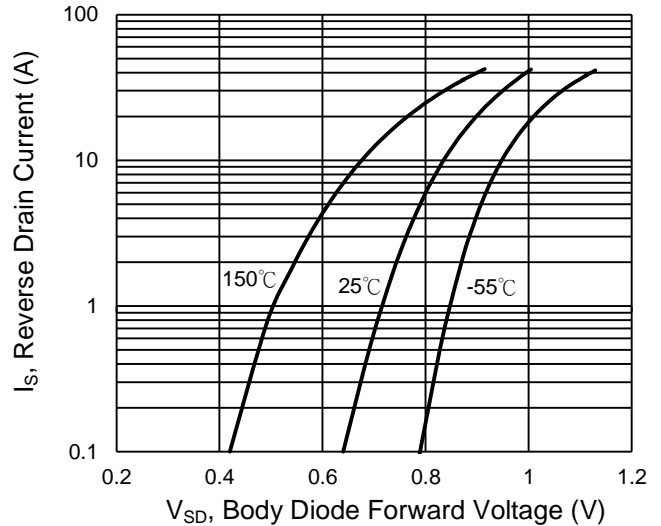
BV_{DSS} vs. Junction Temperature



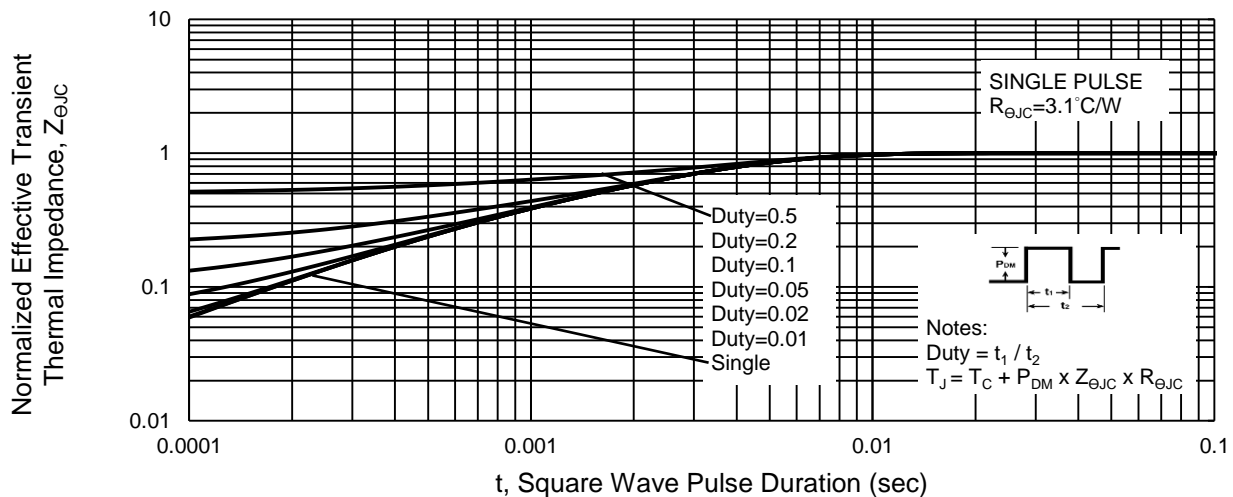
Maximum Safe Operating Area, Junction-to-Case



Source-Drain Diode Forward Current vs. Voltage

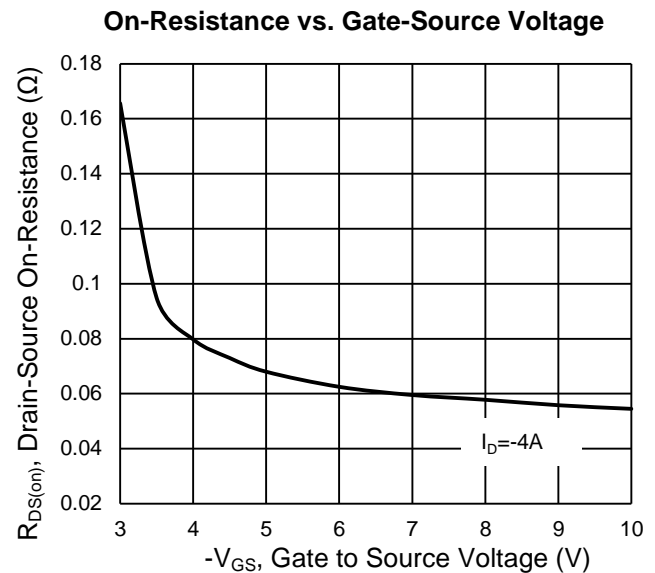
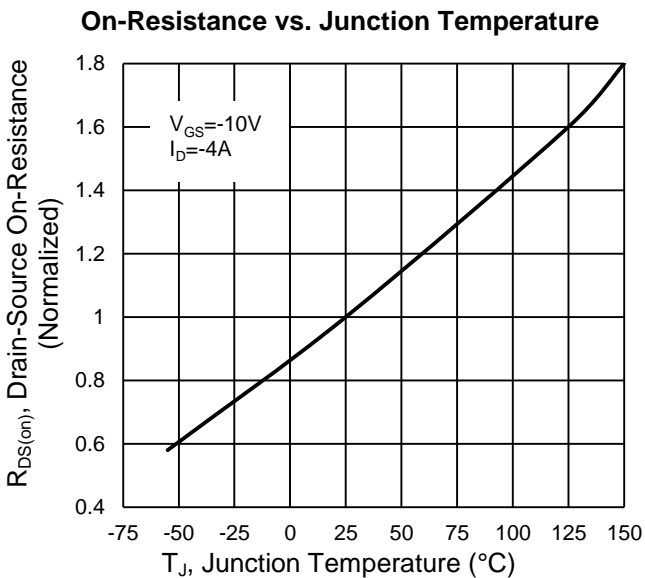
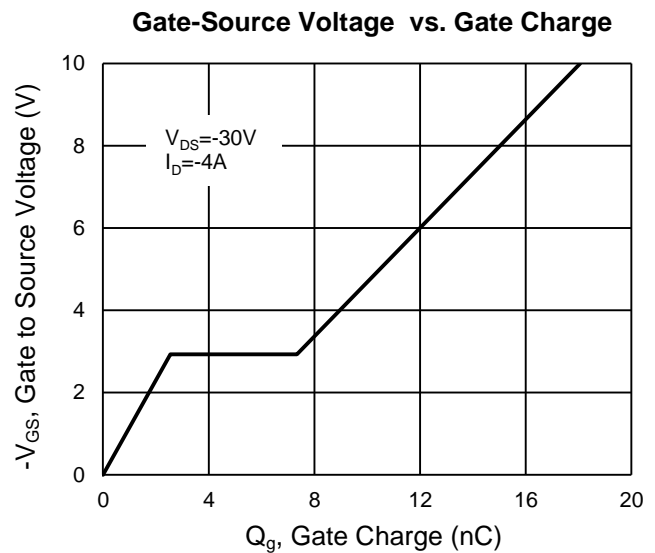
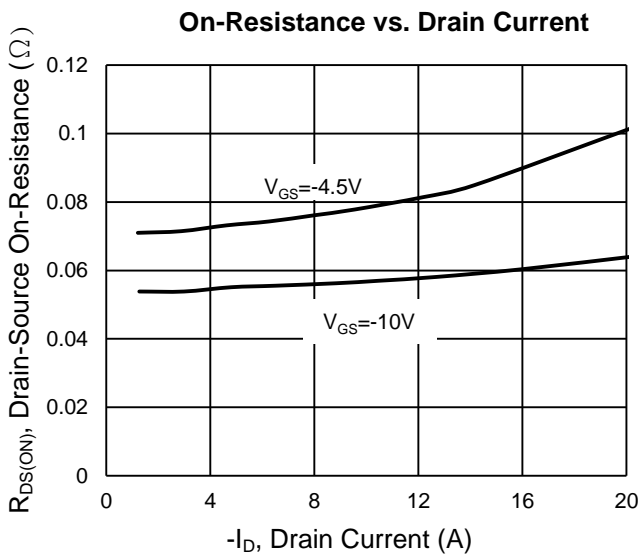
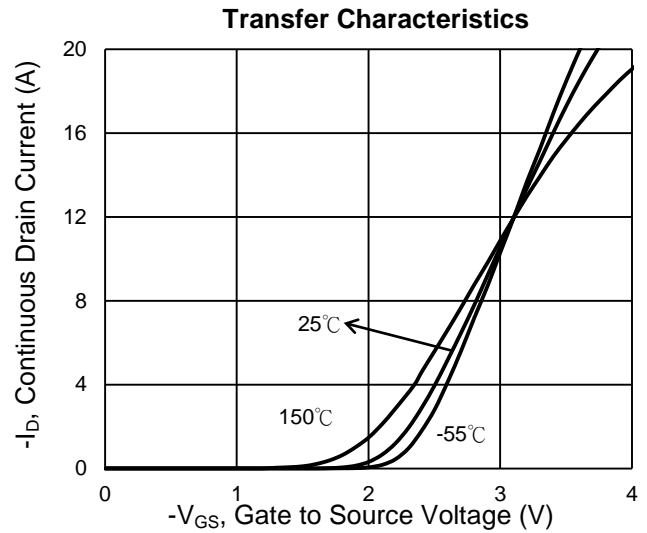
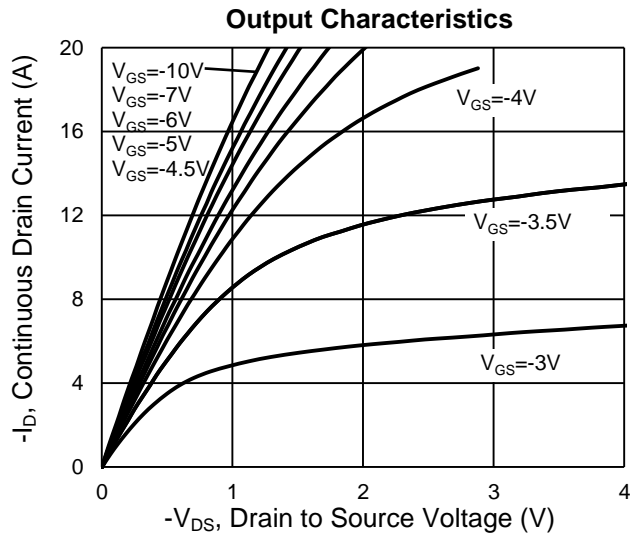


Normalized Thermal Transient Impedance, Junction-to-Case



CHARACTERISTICS CURVES (P-Channel)

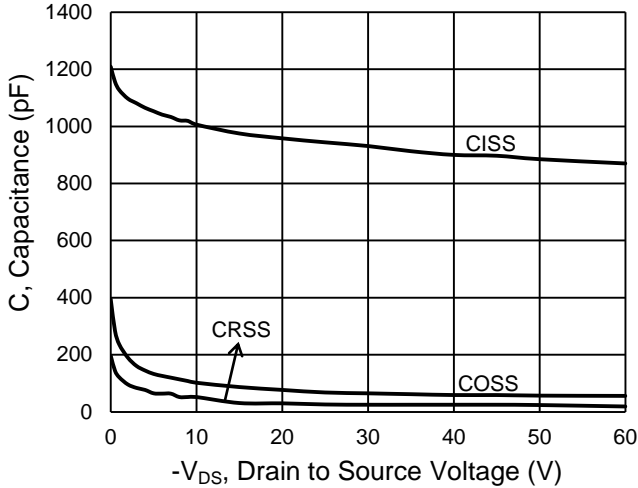
($T_A = 25^\circ\text{C}$ unless otherwise noted)



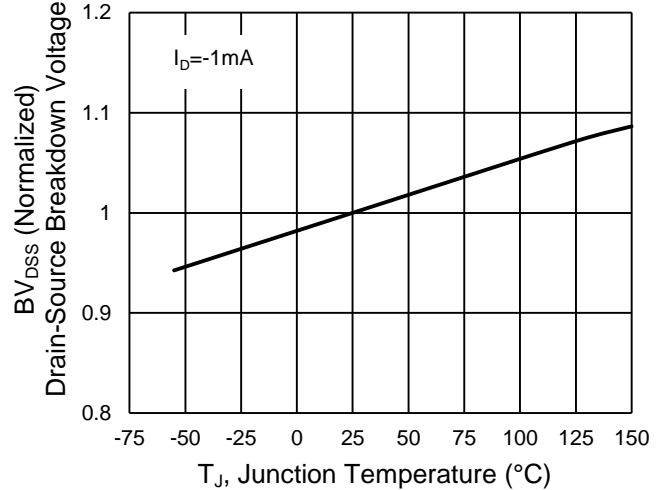
CHARACTERISTICS CURVES (P-Channel)

($T_A = 25^\circ\text{C}$ unless otherwise noted)

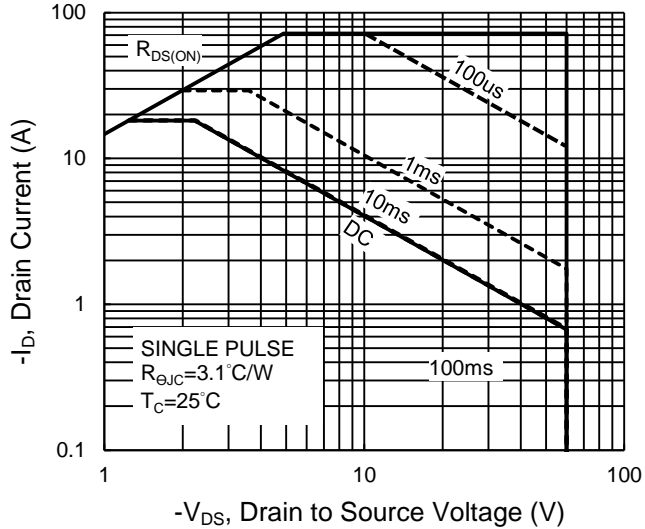
Capacitance vs. Drain-Source Voltage



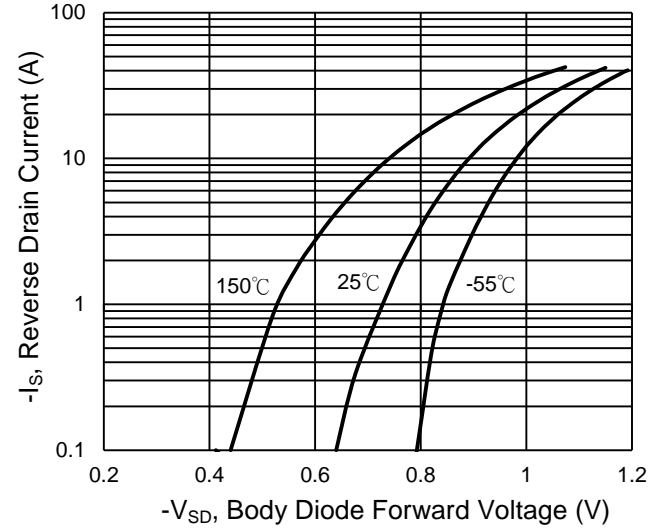
BV_{DSS} vs. Junction Temperature



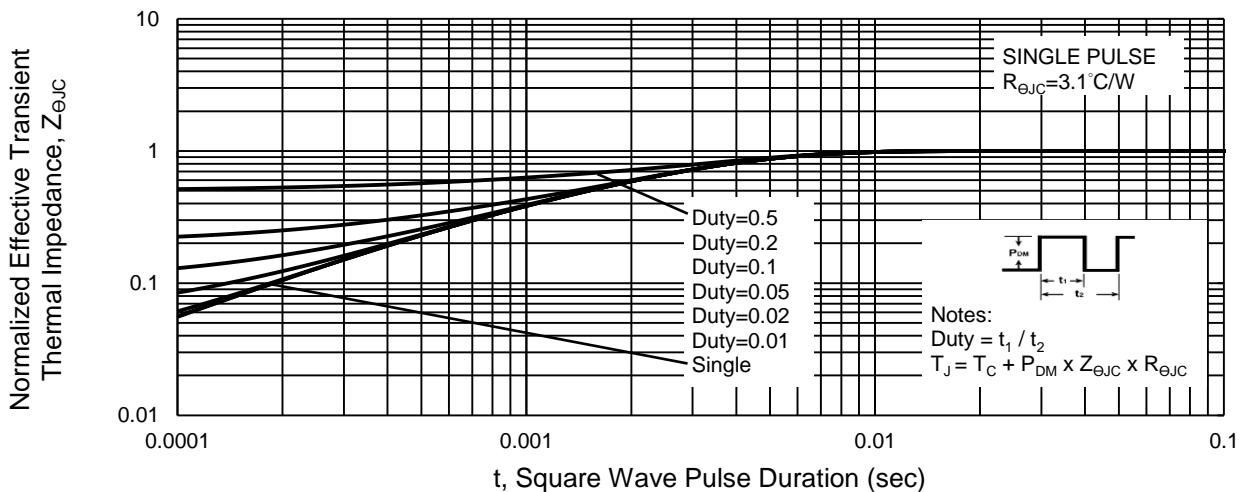
Maximum Safe Operating Area, Junction-to-Case



Source-Drain Diode Forward Current vs. Voltage



Normalized Thermal Transient Impedance, Junction-to-Case



Notice

Specifications of the products displayed herein are subject to change without notice. TSC or anyone on its behalf, assumes no responsibility or liability for any errors or inaccuracies.

Information contained herein is intended to provide a product description only. No license, express or implied, to any intellectual property rights is granted by this document. Except as provided in TSC's terms and conditions of sale for such products, TSC assumes no liability whatsoever, and disclaims any express or implied warranty, relating to sale and/or use of TSC products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright, or other intellectual property right.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications. Customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify TSC for any damages resulting from such improper use or sale.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Taiwan Semiconductor:](#)

[TSM6502CR RLG](#)