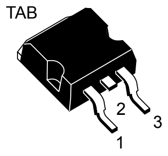
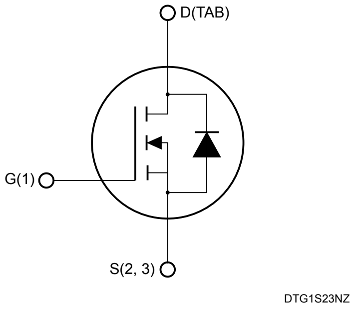
STH2N120K5-2AG

Datasheet

Automotive-grade N-channel 1200 V, 7.25 Ω typ., 1.5 A, MDmesh™ K5 Power MOSFET in an H^2PAK-2 package



H^2PAK-2



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STH2N120K5-2AG	1200 V	10 Ω	1.5 A	60 W

- AEC-Q101 qualified
- Industry's lowest $R_{DS(on)}$ x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Product status
STH2N120K5-2AG

Product summary(1)	
Order code	STH2N120K5-2AG
Marking	2N120K5
Package	H^2PAK-2
Packing	Tape and reel

1. *HTRB test was performed at 80% of $V_{(BR)DSS}$ according to AEC-Q101 rev. C. All other tests were performed according to AEC-Q101 rev. D.*

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±30	V
I_D	Drain current (continuous) at T_{case} = 25 °C	1.5	A
	Drain current (continuous) at T_{case} = 100 °C	1	
I_{DM}(1)	Drain current (pulsed)	2.5	A
P_{TOT}	Total dissipation at T_{case} = 25 °C	60	W
dv/dt(2)	Peak diode recovery voltage slope	4.5	V/ns
dv/dt(3)	MOSFET dv/dt ruggedness	50	
T_{stg}	Storage temperature range	-55 to 150	°C
T_j	Operating junction temperature range		

1. *Pulse width is limited by safe operating area.*
2. *$I_{SD} \leq 1.5$ A, di/dt = 100 A/µs, V_{DS} peak < $V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$*
3. *$V_{DS} \leq 960$ V*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	2.08	°C/W
$R_{thj-pcb}$(1)	Thermal resistance junction-pcb	30	

1. *When mounted on an 1-inch² FR-4, 2 Oz copper board.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}(1)	Avalanche current, repetitive or not repetitive	0.5	A
E_{AS}(2)	Single pulse avalanche energy	80	mJ

1. *Pulse width is limited by T_{jmax}.*
2. *Starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V*

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 4. **Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	1200			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 1200 V			0.5	µA
		V_{GS} = 0 V, V_{DS} = 1200 V, T_{case} = 125 °C[1]			100	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 0.5 A		7.25	10	Ω

1. *Defined by design, not subject to production test.*

Table 5. **Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	124	-	pF
C_{oss}	Output capacitance		-	13	-	
C_{rss}	Reverse transfer capacitance		-	0.5	-	
$C_{o(tr)}$[1]	Time-related equivalent capacitance	V_{GS} = 0 V, V_{DS} = 0 to 960 V	-	15	-	pF
$C_{o(er)}$[2]	Energy-related equivalent capacitance		-	5	-	
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	16	-	Ω
Q_g	Total gate charge	V_{DD} = 960 V, I_D = 1.5 A, V_{GS} = 0 to 10 V (see Figure 13. Test circuit for gate charge behavior)	-	5.3	-	nC
Q_{gs}	Gate-source charge		-	0.8	-	
Q_{gd}	Gate-drain charge		-	3.5	-	

1. *$C_{o(tr)}$ is a constant capacitance value giving the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.*
2. *$C_{o(er)}$ is a constant capacitance value giving the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.*

Table 6. **Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 600 V, I_D = 0.75 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	10.3	-	ns
t_r	Rise time		-	7.8	-	
$t_{d(off)}$	Turn-off delay time		-	34	-	
t_f	Fall time		-	39	-	

Table 7. **Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		1.5	A
I_{SDM}(1)	Source-drain current (pulsed)		-		2.5	A
V_{SD}(2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 1.5 A	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 1.5 A, di/dt = 100 A/μs, V_{DD} = 60 V (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	350		ns
Q_{rr}	Reverse recovery charge		-	1.35		μC
I_{RRM}	Reverse recovery current		-	7.7		A
t_{rr}	Reverse recovery time	I_{SD} = 1.5 A, di/dt = 100 A/μs, V_{DD} = 60 V, T_j = 150 °C (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	600		ns
Q_{rr}	Reverse recovery charge		-	2.09		μC
I_{RRM}	Reverse recovery current		-	7.7		A

1. *Pulse width is limited by safe operating area.*
2. *Pulse test: pulse duration = 300 μs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

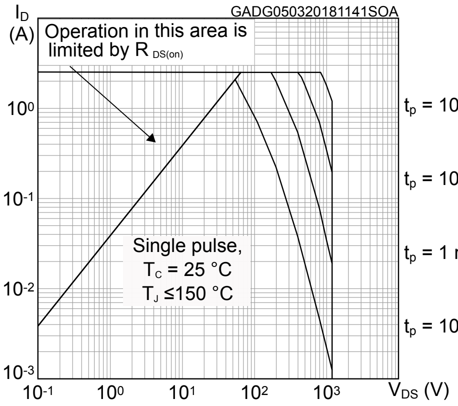


Figure 2. Thermal impedance

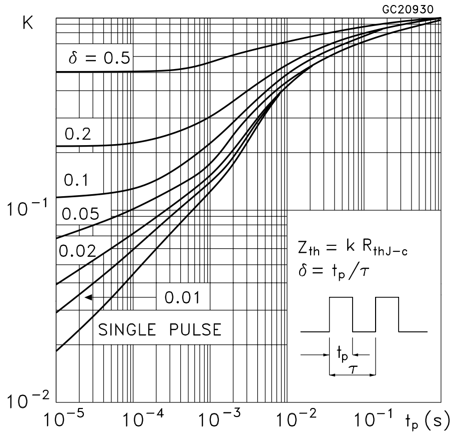


Figure 3. Output characteristics

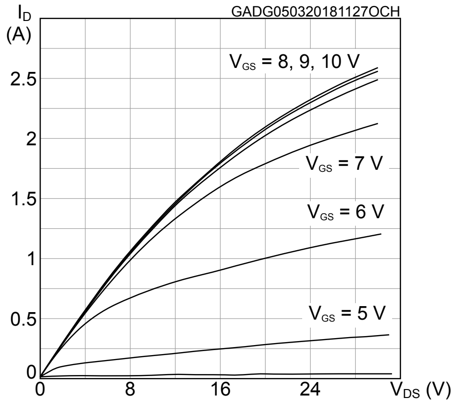


Figure 4. Transfer characteristics

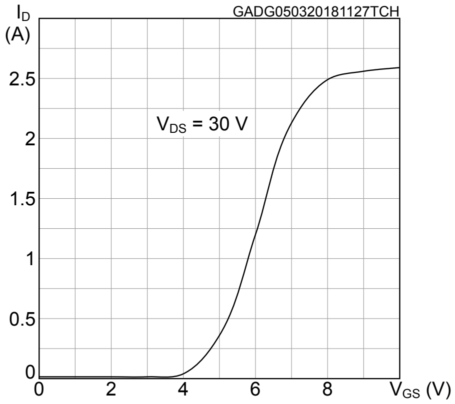


Figure 5. Gate charge vs gate-source voltage

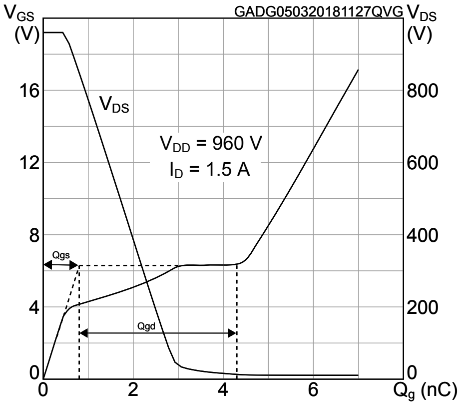


Figure 6. Static drain-source on-resistance

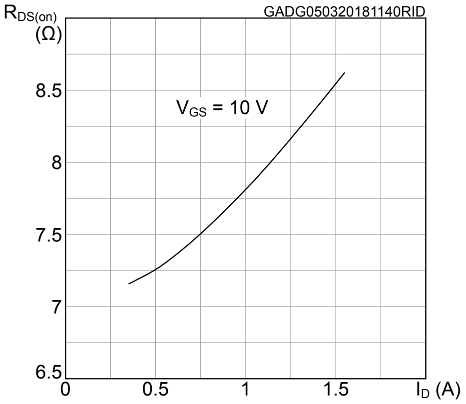


Figure 7. Capacitance variations

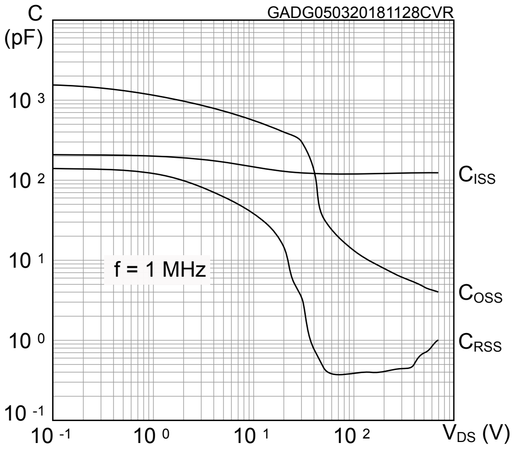


Figure 8. Normalized gate threshold voltage vs temperature

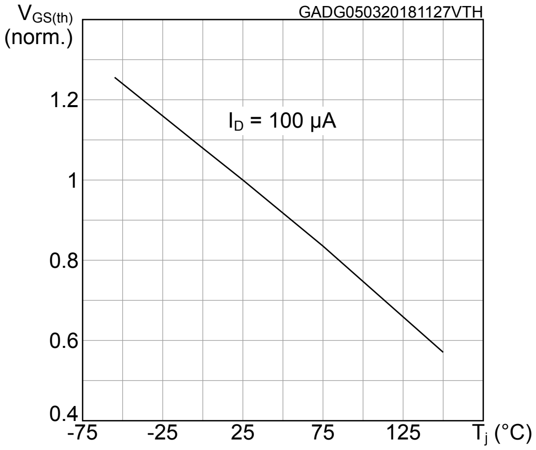


Figure 9. Normalized on-resistance vs temperature

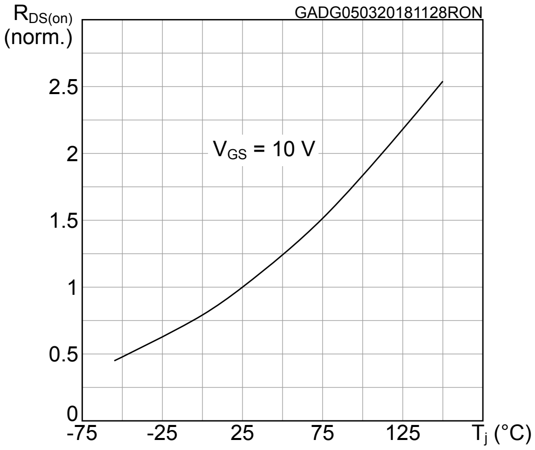


Figure 10. Normalized $V_{(BR)DSS}$ vs temperature

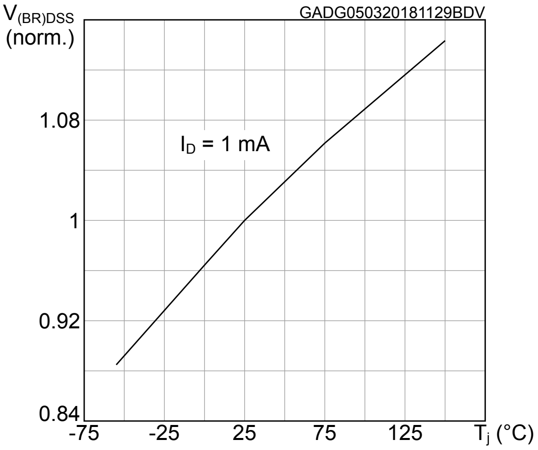
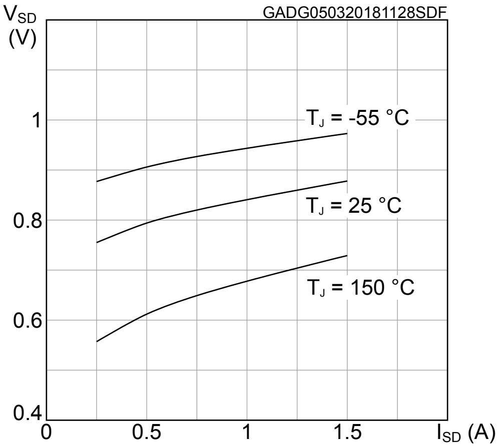


Figure 11. Source- drain diode forward characteristics



3 Test circuits

Figure 12. Test circuit for resistive load switching times

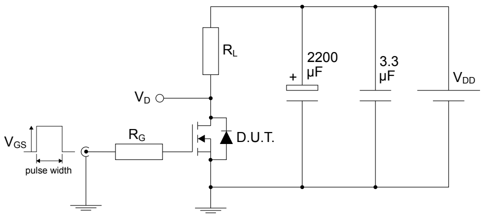


Figure 13. Test circuit for gate charge behavior

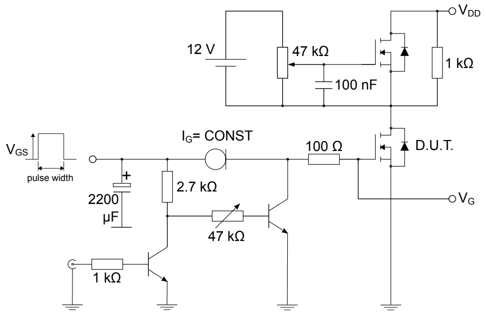


Figure 14. Test circuit for inductive load switching and diode recovery times

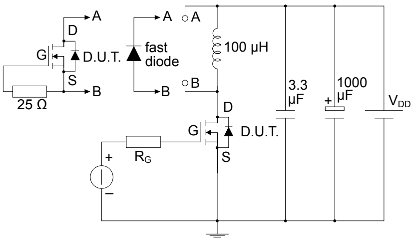


Figure 15. Unclamped inductive load test circuit

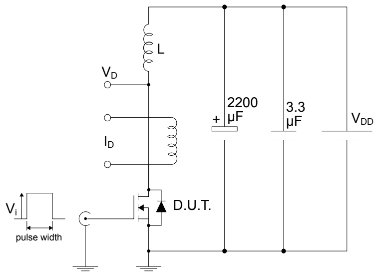


Figure 16. Unclamped inductive waveform

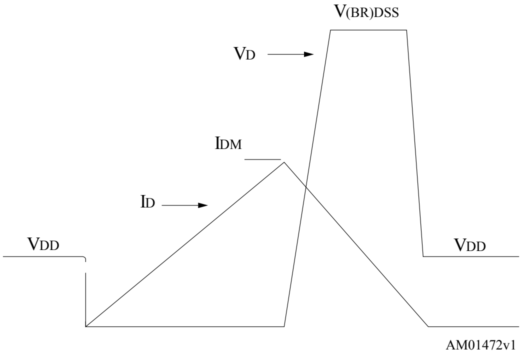
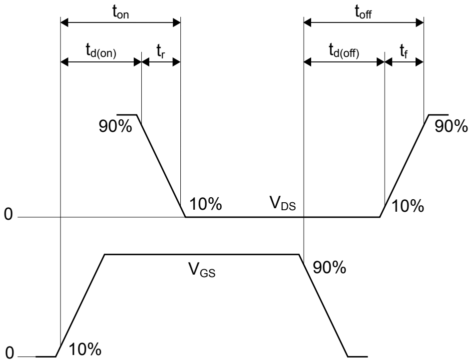


Figure 17. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 H²PAK-2 package information

Figure 18. H²PAK-2 package outline

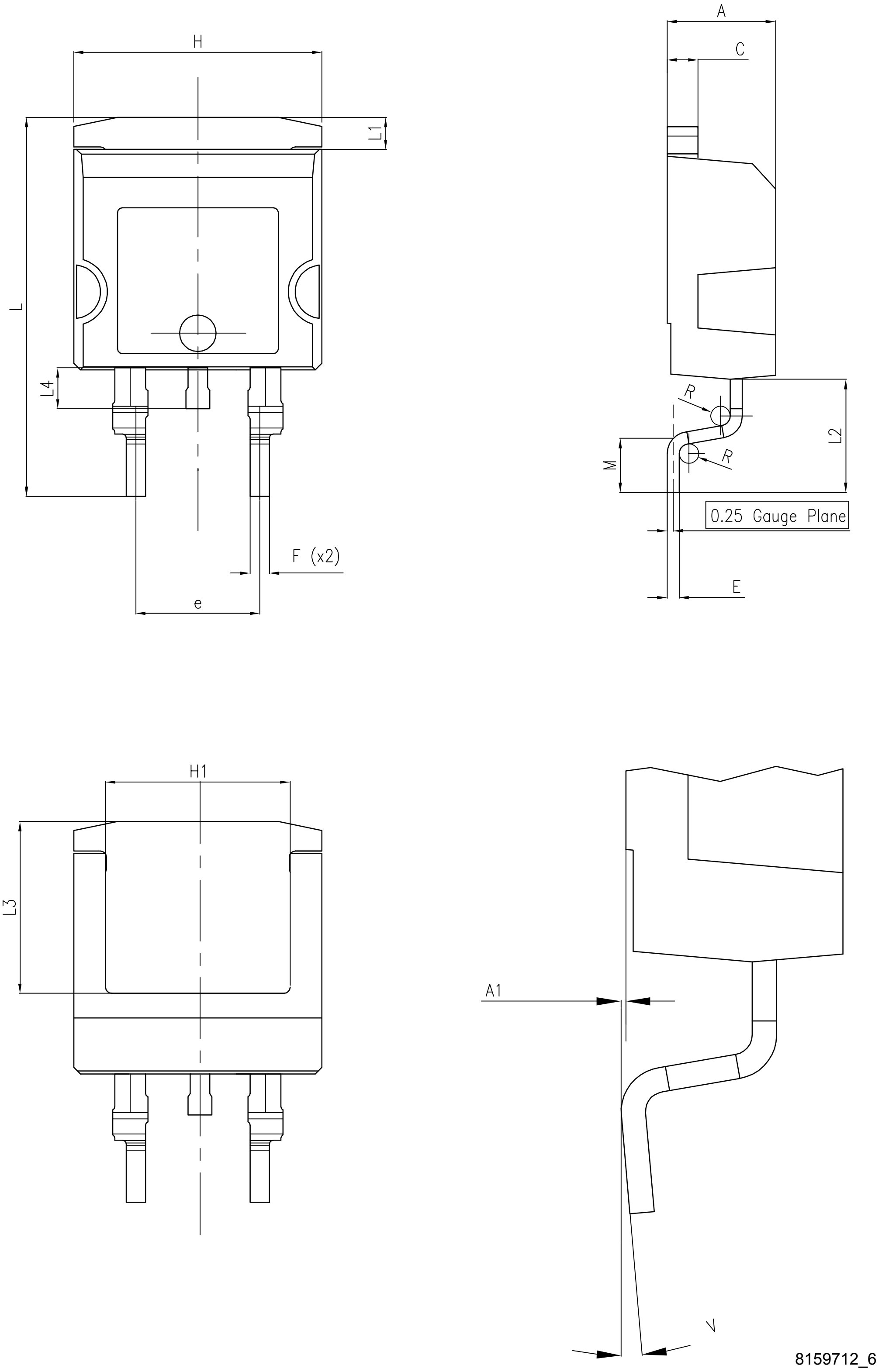
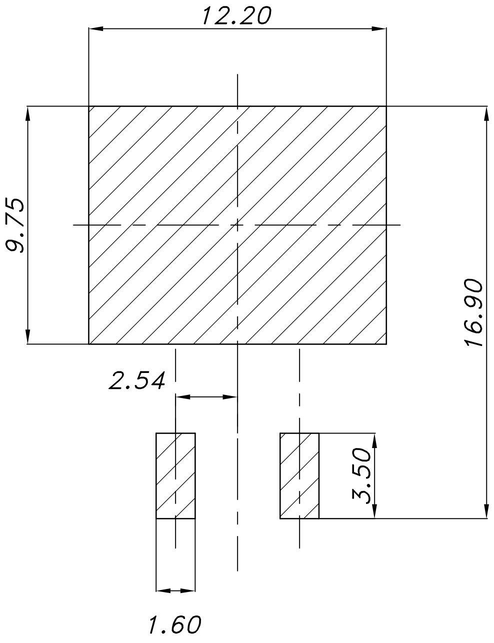


Table 8. **H²PAK-2 package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.30	-	4.70
A1	0.03		0.20
C	1.17		1.37
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
H	10.00		10.40
H1	7.40		7.80
L	15.30		15.80
L1	1.27		1.40
L2	4.93		5.23
L3	6.85		7.25
L4	1.5		1.7
M	2.6		2.9
R	0.20		0.60
V	0°		8°

Figure 19. **H²PAK-2 recommended footprint**



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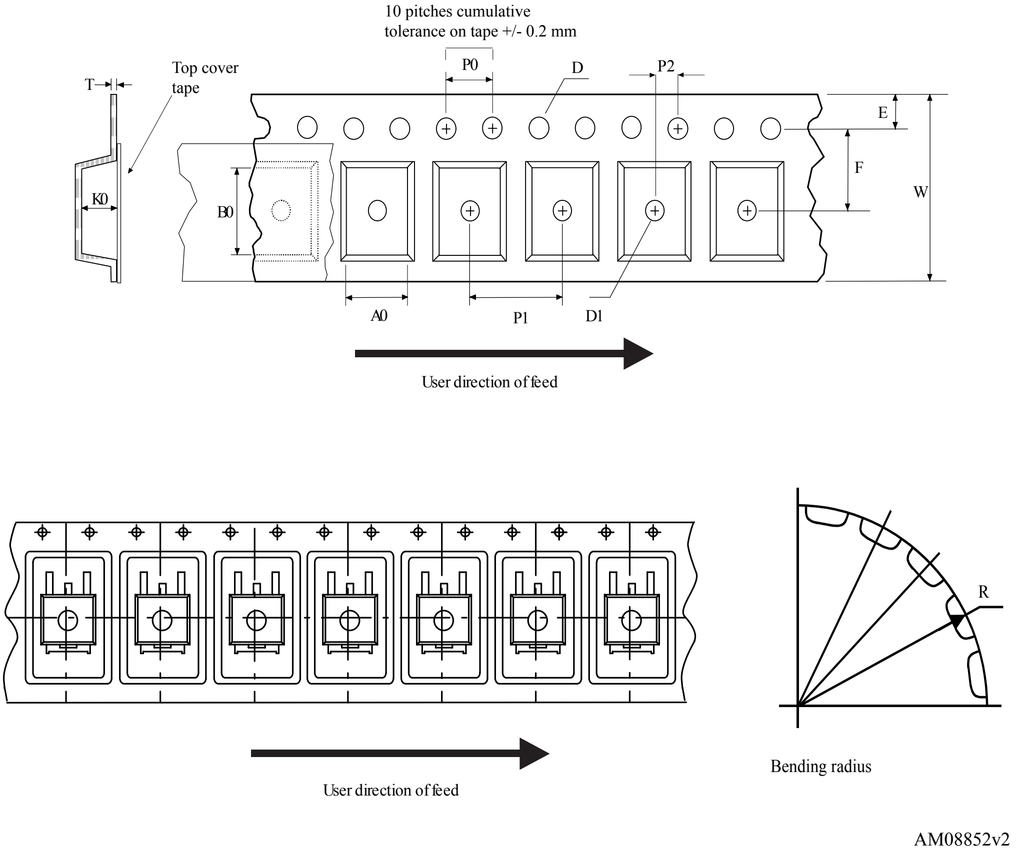
Note: Dimensions are in mm.

4.2 Packing information

Figure 20. Tape outline



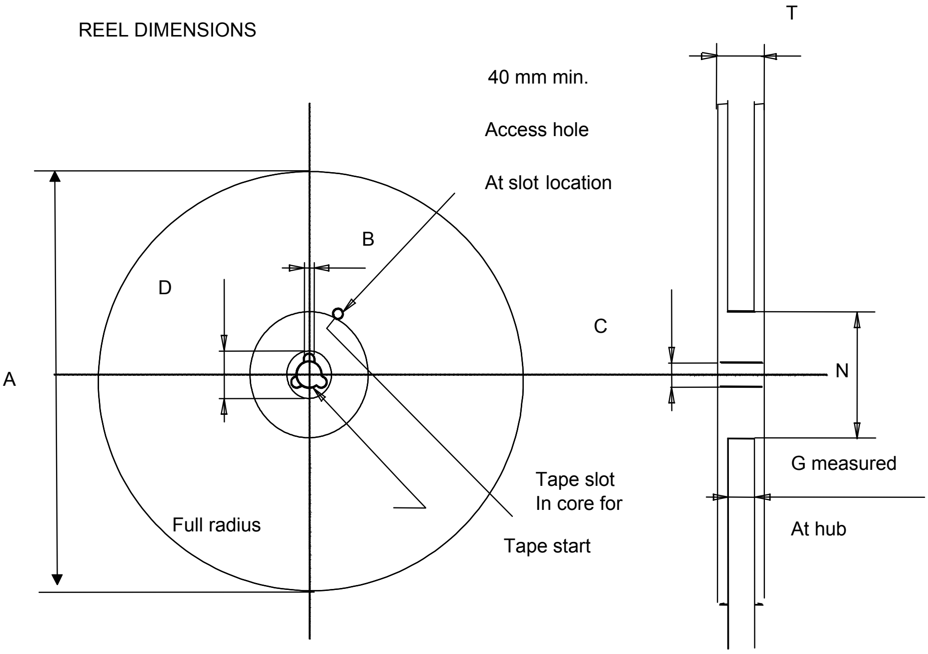


Figure 21. Reel outline

Table 9. Tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Revision history

Table 10. **Document revision history**

Date	Version	Changes
23-Mar-2018	1	Initial release. The document status is preliminary data.
30-Jul-2018	2	The document status was promoted from preliminary to production data. Updated title and features on cover page.
31-Jul-2018	3	Updated the current table. The date for revision 2 was erroneously reported as "19-Jun-2018" instead of "30-Jul-2018".
05-Sep-2018	4	Updated I_{DSS} parameter in Table 4. Static.

Contents