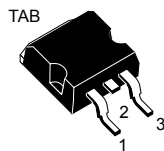
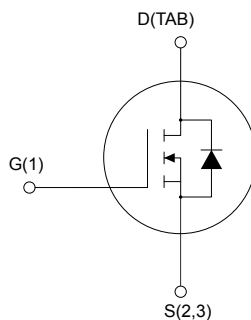


N-channel 100 V, 3.9 mΩ typ., 180 A STripFET F3 Power MOSFET in H²PAK-2 package



H²PAK-2



NCHG1DTABS23

Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STH180N10F3-2	100 V	4.5 mΩ	180 A

- Ultra low on-resistance
- 100% avalanche tested

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using STripFET F3 technology. It is designed to minimize on-resistance and gate charge to provide superior switching performance.



Product status link

[STH180N10F3-2](#)

Product summary

Order code	STH180N10F3-2
Marking	180N10F3
Package	H2PAK-2
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	180	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	120	A
$I_{DM}^{(2)}$	Drain current (pulsed)	720	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	315	W
	Derating factor	2.1	W/ $^\circ\text{C}$
dv/dt	Peak diode recovery voltage slope	20	V/ns
$E_{AS}^{(3)}$	Single pulse avalanche energy	350	mJ
T_J	Operating junction temperature	-55 to 175	$^\circ\text{C}$
T_{stg}	Storage temperature		$^\circ\text{C}$

1. Current limited by package
2. Pulse width limited by safe operating area
3. Starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = 80$, $V_{DD} = 50\text{ V}$

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.48	$^\circ\text{C/W}$
$R_{thJB}^{(1)}$	Thermal resistance, junction-to-board	35	$^\circ\text{C/W}$

1. When mounted on FR-4 board of 1 inch², 2 oz Cu

2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Table 3. On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage ($V_{GS} = 0\text{ V}$)	$I_D = 250\text{ }\mu\text{A}$	100			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0\text{ V}$)	$V_{DS} = 100\text{ V}$			10	μA
		$V_{DS} = 100\text{ V}; T_C = 125\text{ }^{\circ}\text{C}$			100	μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0\text{ V}$)	$V_{GS} = \pm 20\text{ V}$			± 200	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2		4	V
$R_{DS(on)}$	Static drain-source on- resistance	$V_{GS} = 10\text{ V}, I_D = 60\text{ A}$		3.9	4.5	m Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}, f = 1\text{ MHz},$ $V_{GS} = 0\text{ V}$	-	6665	-	pF
C_{oss}	Output capacitance			786		pF
C_{rss}	Reverse transfer capacitance			49		pF
Q_g	Total gate charge	$V_{DD} = 50\text{ V}, I_D = 120\text{ A}$		114.6		nC
Q_{gs}	Gate-source charge	$V_{GS} = 10\text{ V}$		38.8		nC
Q_{gd}	Gate-drain charge	See Figure 13. Test circuit for gate charge behavior		31.9		nC

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 50 V, I _D = 60 A,	-	25.6	-	ns
t _r	Rise time	R _G = 4.7 Ω, V _{GS} = 10 V		97.1		ns
t _{d(off)}	Turn-off delay time	See Figure 12. Test circuit for resistive load switching times		99.9		ns
t _f	Fall time			6.9		ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		180	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				720	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 120\text{ A}$, $V_{GS} = 0\text{ V}$			1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 120\text{ A}$,		83.4		ns
Q_{rr}	Reverse recovery charge	$di/dt = 100\text{ A}/\mu\text{s}$,		295.7		nC
I_{RRM}	Reverse recovery current	$V_{DD} = 80\text{ V}$, $T_J = 150\text{ }^{\circ}\text{C}$		7.1		A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

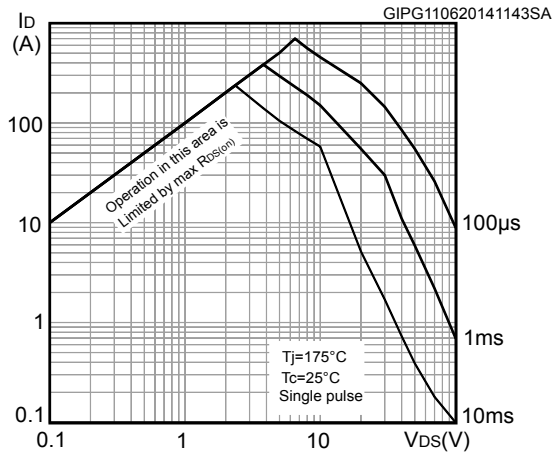


Figure 2. Thermal impedance

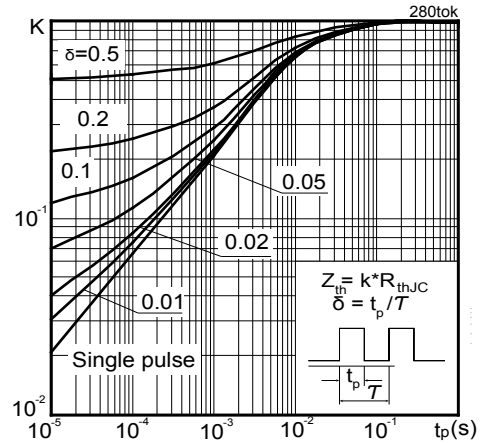


Figure 3. Output characteristics

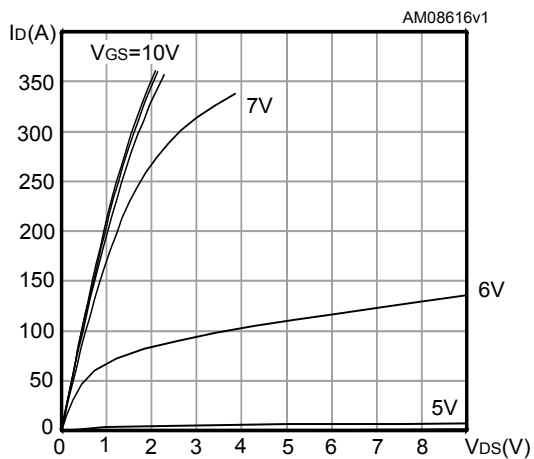


Figure 4. Transfer characteristics

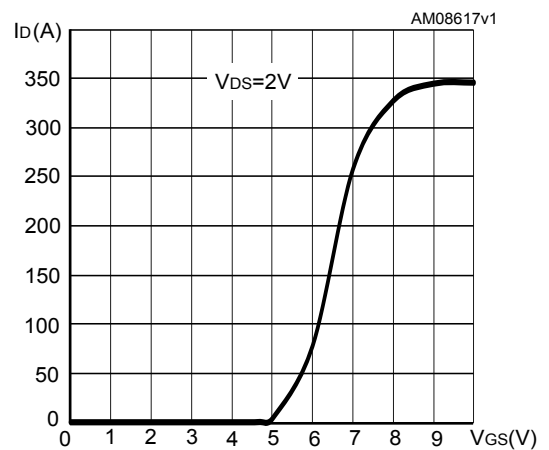


Figure 5. Normalized $V_{(BR)DSS}$ vs temperature

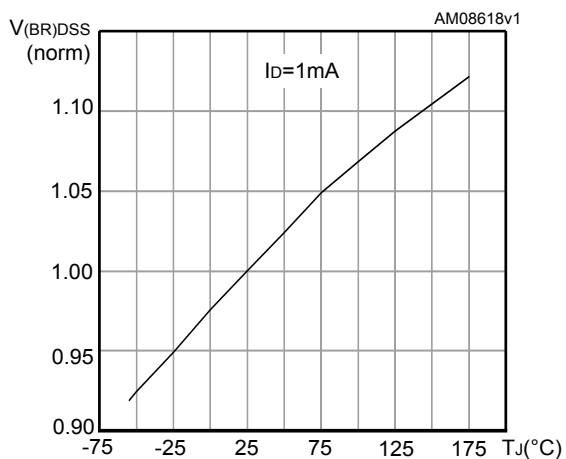


Figure 6. Static drain-source on-resistance

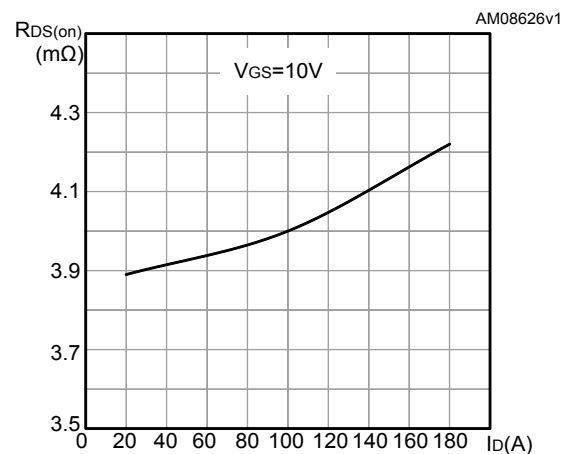


Figure 7. Gate charge vs gate-source voltage

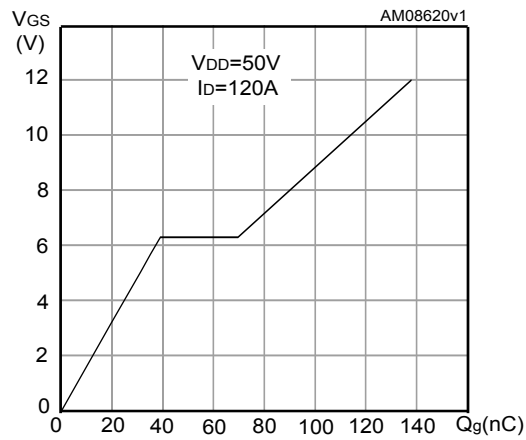


Figure 8. Capacitance variations

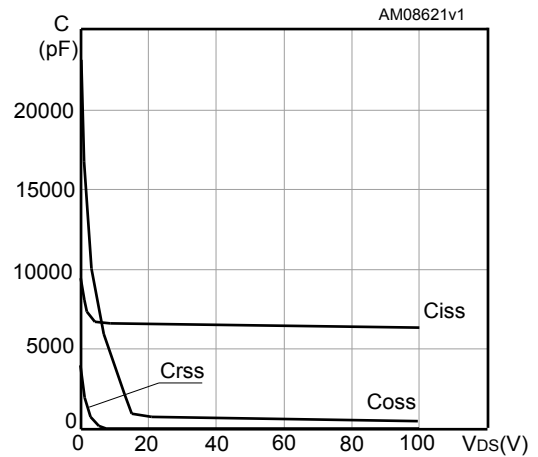


Figure 9. Normalized gate threshold voltage vs temperature

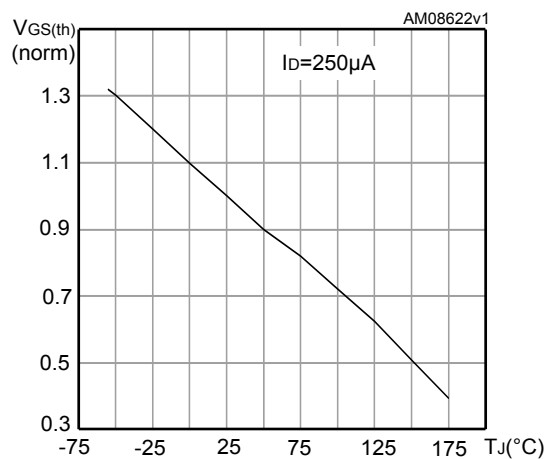


Figure 10. Normalized on-resistance vs temperature

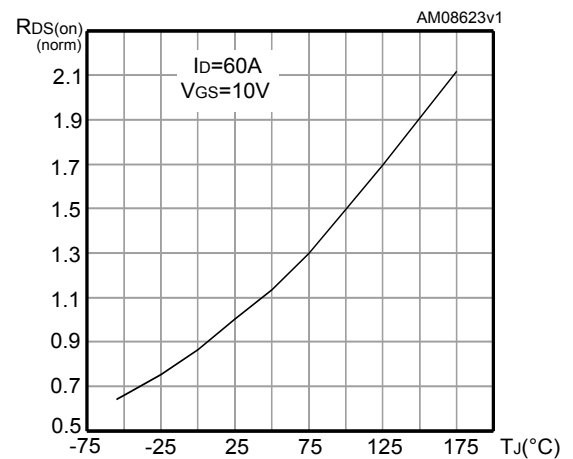
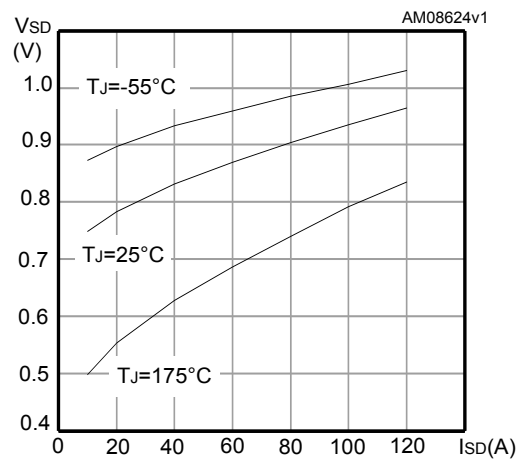
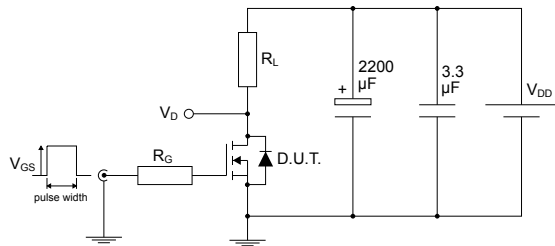


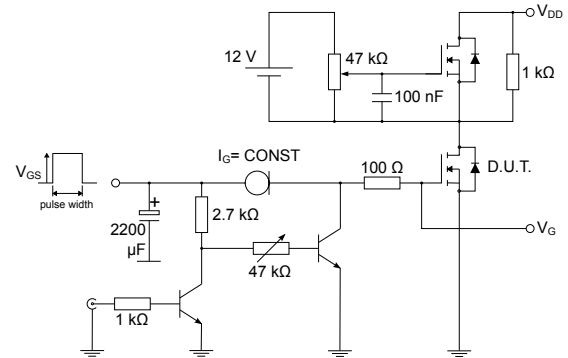
Figure 11. Source-drain diode forward characteristics



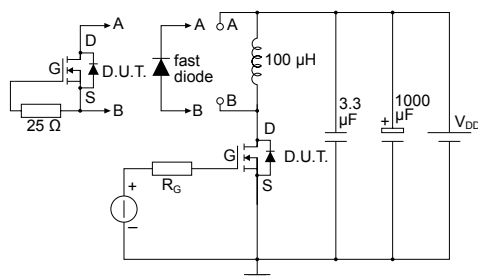
3 Test circuits

Figure 12. Test circuit for resistive load switching times


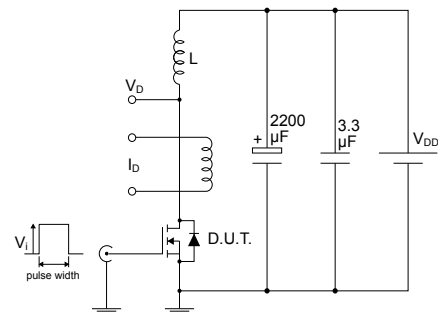
AM01468v1

Figure 13. Test circuit for gate charge behavior


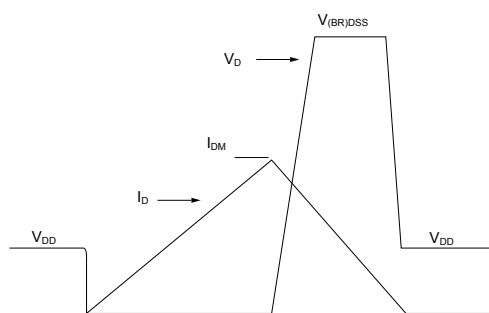
AM01469v1

Figure 14. Test circuit for inductive load switching and diode recovery times


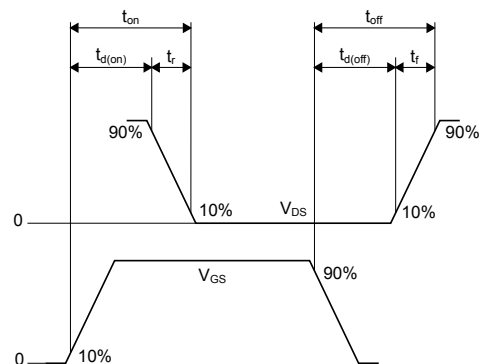
AM01470v1

Figure 15. Unclamped inductive load test circuit


AM01471v1

Figure 16. Unclamped inductive waveform


AM01472v1

Figure 17. Switching time waveform


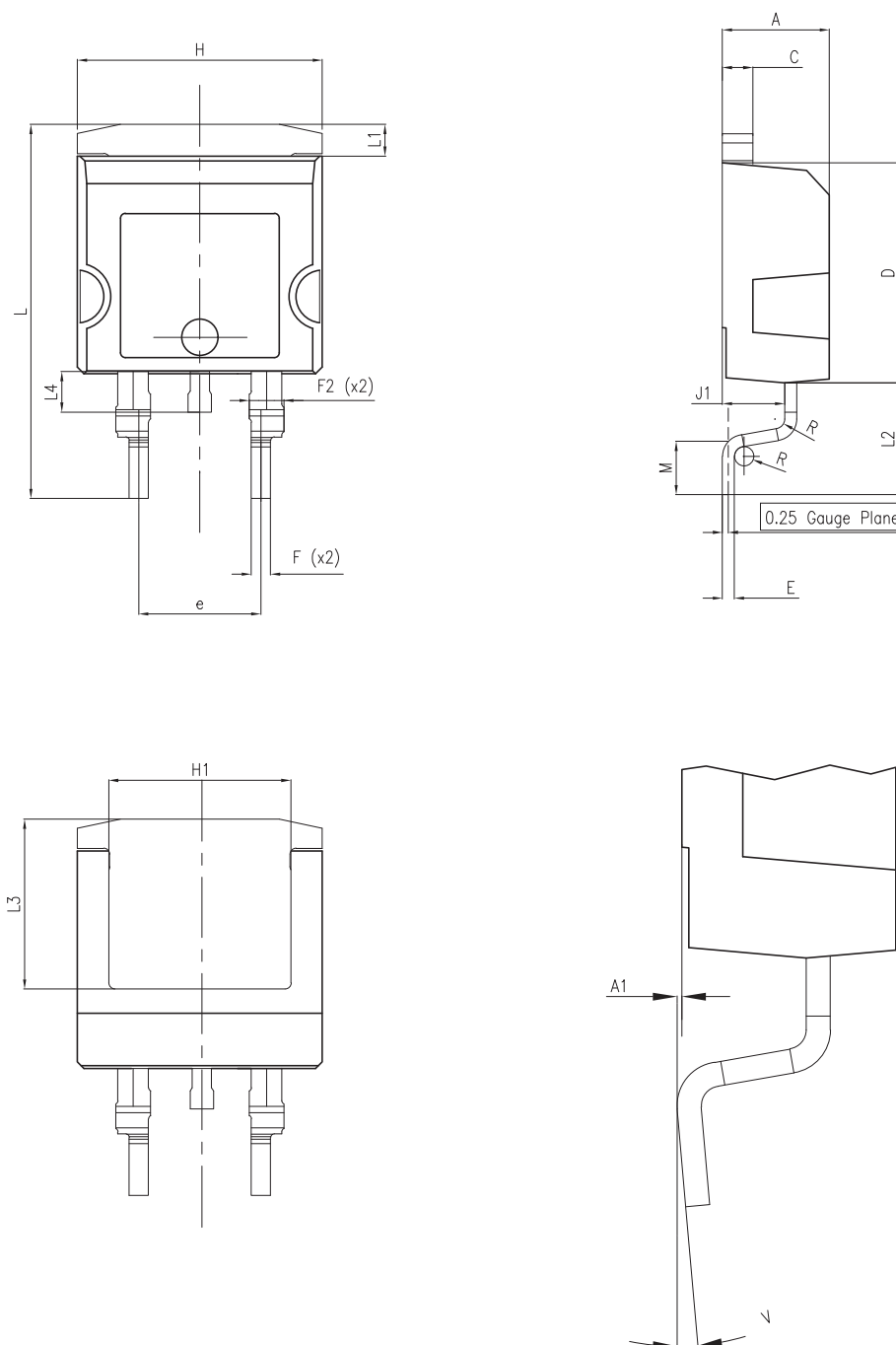
AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 H²PAK-2 package information

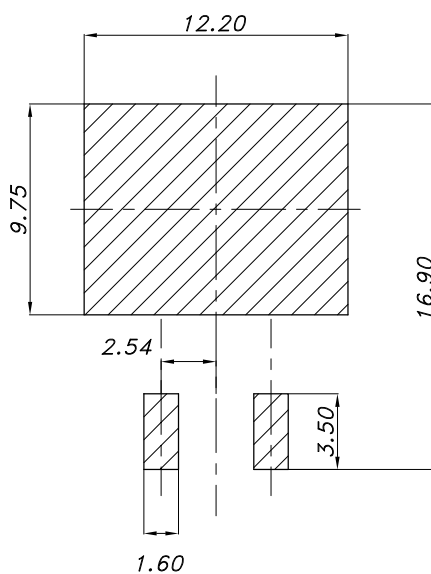
Figure 18. H²PAK-2 package outline



8159712_9

Table 7. H²PAK-2 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.30	-	4.70
A1	0.03		0.20
C	1.17		1.37
D	8.95		9.35
e	4.98		5.18
E	0.50		0.90
F	0.78		0.85
F2	1.14		1.70
H	10.00		10.40
H1	7.40		7.80
J1	2.49		2.69
L	15.30		15.80
L1	1.27		1.40
L2	4.93		5.23
L3	6.85		7.25
L4	1.50		1.70
M	2.60		2.90
R	0.20		0.60
V	0°		8°

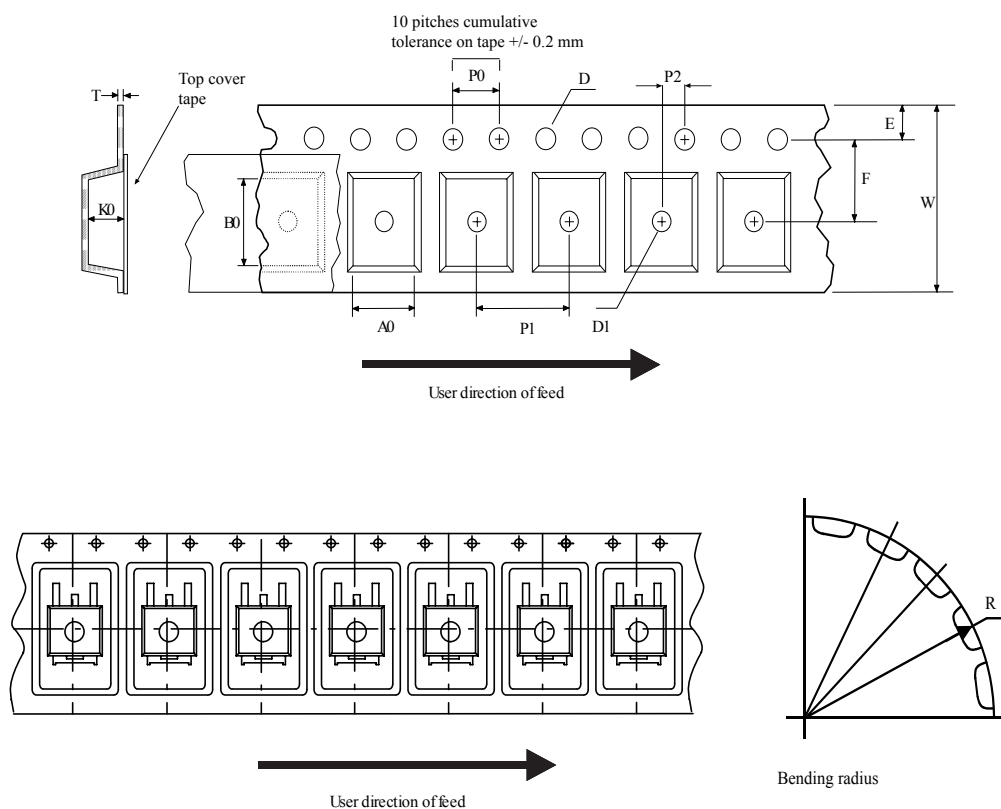
Figure 19. H²PAK-2 recommended footprint


8159712_9

Note: Dimensions are in mm.

4.2 Packing information

Figure 20. Tape outline



AM08852v2

Figure 21. Reel outline

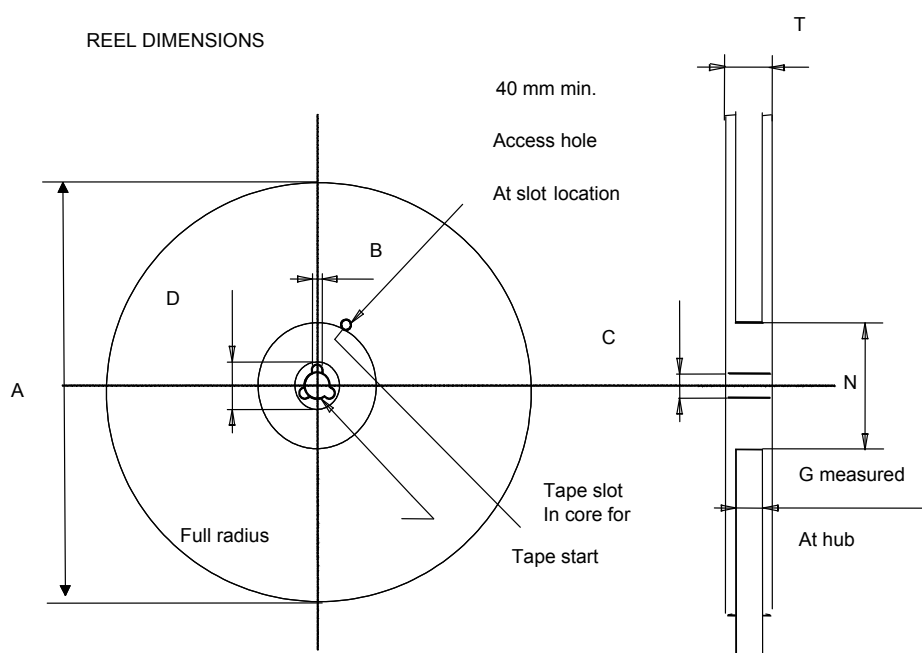


Table 8. Tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Revision history

Table 9. Document revision history

Date	Revision	Changes
18-Jul-2011	1	First version
26-Nov-2014	2	- Modified fig 2. - Updated package mechanical data. - Updated the title, features and description.
02-Mar-2022	3	Updated Figure 1. Safe operating area . Minor text changes.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, please refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2022 STMicroelectronics – All rights reserved

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[STMicroelectronics:](#)

[STH180N10F3-6](#)