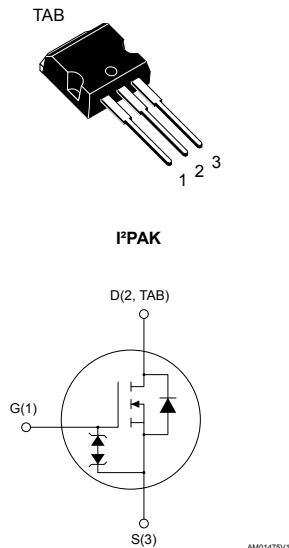



## Automotive-grade N-channel 600 V, 70 mΩ typ., 36 A MDmesh™ DM6 Power MOSFET in an I<sup>2</sup>PAK package



### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STI47N60DM6AG	600 V	80 mΩ	36 A

- AEC-Q101 qualified 
- Fast-recovery body diode
- Lower R<sub>DS(on)</sub> per area vs previous generation
- Low gate charge, input capacitance and resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

### Applications

- Switching applications

### Description

This high-voltage N-channel Power MOSFET is part of the MDmesh™ DM6 fast-recovery diode series. Compared with the previous MDmesh fast generation, DM6 combines very low recovery charge (Q<sub>rr</sub>), recovery time (t<sub>rr</sub>) and excellent improvement in R<sub>DS(on)</sub> per area with one of the most effective switching behaviors available in the market for the most demanding high-efficiency bridge topologies and ZVS phase-shift converters.

#### Product status link

[STI47N60DM6AG](#)

#### Product summary

<b>Order code</b>	STI47N60DM6AG
<b>Marking</b>	47N60DM6
<b>Package</b>	I <sup>2</sup> PAK
<b>Packing</b>	Tube

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	±25	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ °C}$	36	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ °C}$	23	A
$I_D^{(1)}$	Drain current (pulsed)	137	A
$P_{TOT}$	Total power dissipation at $T_C = 25\text{ °C}$	250	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	50	V/ns
$dv/dt^{(3)}$	MOSFET $dv/dt$ ruggedness	100	
$T_J$	Operating junction temperature range	-55 to 150	°C
$T_{stg}$	Storage temperature range		

1. Pulse width limited by safe operating area
2.  $I_{SD} \leq 36\text{ A}$ ,  $di/dt \leq 800\text{ A}/\mu\text{s}$ ,  $V_{DS(peak)} < V_{(BR)DSS}$ ,  $V_{DD} = 480\text{ V}$
3.  $V_{DS} \leq 480\text{ V}$

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.5	°C/W
$R_{thj-amb}$	Thermal resistance junction-amb	62.5	

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not repetitive (pulse width limited by $T_{jmax}$ )	7	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ °C}$ , $I_D = I_{AR}$ , $V_{DD} = 100\text{ V}$ )	700	mJ

## 2 Electrical characteristics

$T_C = 25\text{ }^\circ\text{C}$  unless otherwise specified

**Table 4. On/off state**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	600			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$ , $T_C = 125\text{ }^\circ\text{C}^{(1)}$			100	$\mu\text{A}$
$I_{GSS}$	Gate body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 25\text{ V}$			$\pm 1$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	3.25	4	4.75	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 18\text{ A}$		70	80	$\text{m}\Omega$

1. Defined by design, not subject to production test.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	2350	-	$\text{pF}$
$C_{oss}$	Output capacitance		-	160	-	$\text{pF}$
$C_{rss}$	Reverse transfer capacitance		-	2	-	$\text{pF}$
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }480\text{ V}$ , $V_{GS} = 0\text{ V}$	-	416	-	$\text{pF}$
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	1.6	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 480\text{ V}$ , $I_D = 36\text{ A}$ ,	-	55	-	$\text{nC}$
$Q_{gs}$	Gate-source charge	$V_{GS} = 0\text{ to }10\text{ V}$	-	12	-	$\text{nC}$
$Q_{gd}$	Gate-drain charge	(see Figure 14. Test circuit for gate charge behavior)	-	31	-	$\text{nC}$

1.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$ , $I_D = 18\text{ A}$ ,	-	23	-	ns
$t_r$	Rise time	$R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$	-	5.5	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	57	-	ns
$t_f$	Fall time		-	9	-	ns

**Table 7. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		36	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		137	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 36\text{ A}$ , $V_{GS} = 0\text{ V}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 36\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$	-	115		ns
$Q_{rr}$	Reverse recovery charge		-	0.54		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	9.5		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 36\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$	-	210		ns
$Q_{rr}$	Reverse recovery charge		-	2.1		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	20.4	

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

**Table 8. Gate-source Zener diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$ , $I_D = 0\text{ A}$	$\pm 30$	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

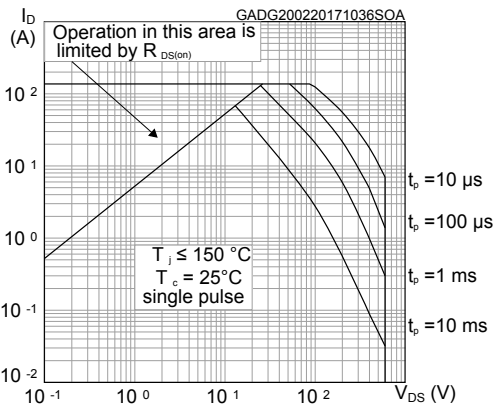


Figure 2. Thermal impedance

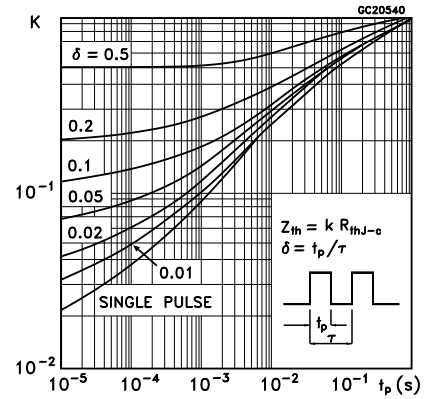


Figure 3. Output characteristics

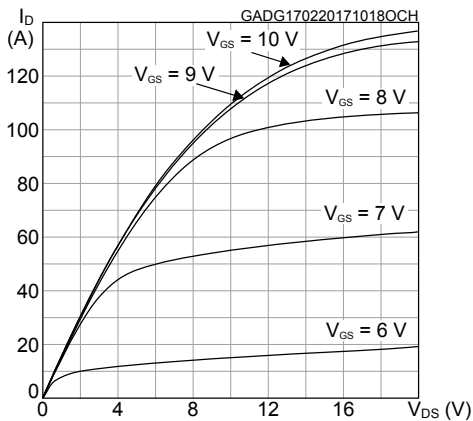


Figure 4. Transfer characteristics

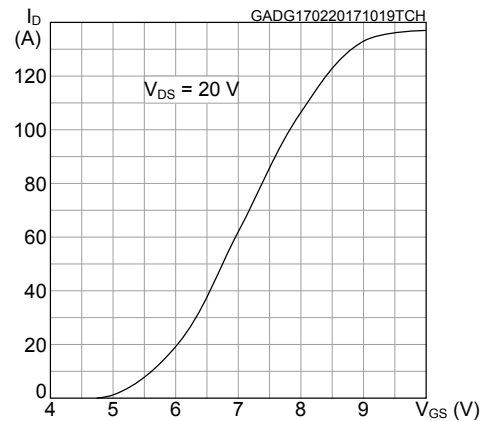


Figure 5. Gate charge vs gate-source voltage

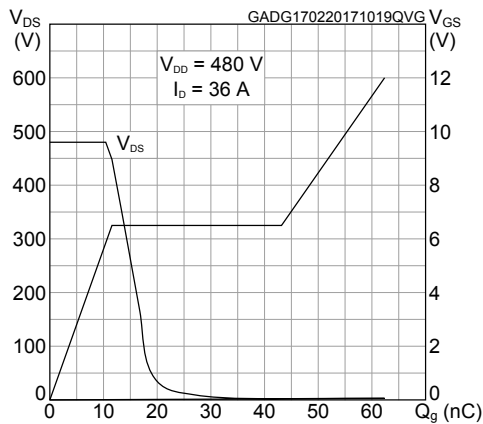


Figure 6. Static drain-source on-resistance

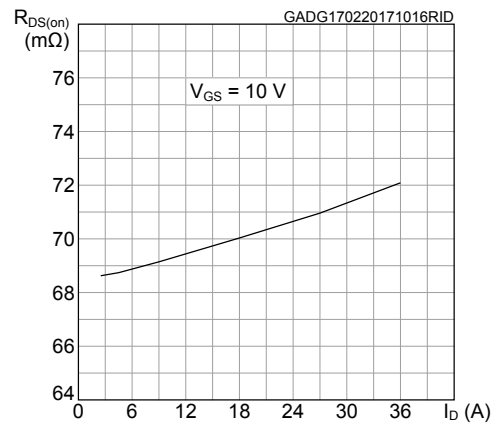


Figure 7. Capacitance variations

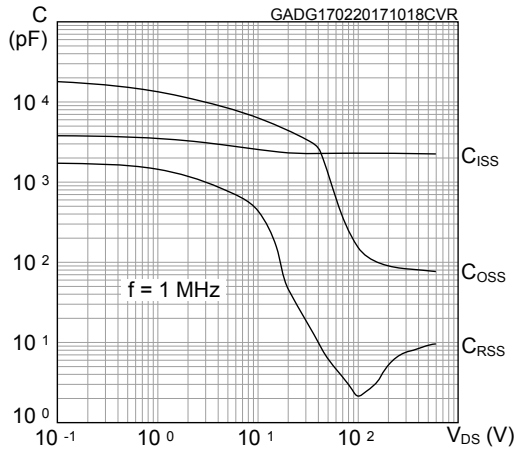


Figure 8. Normalized gate threshold voltage vs temperature

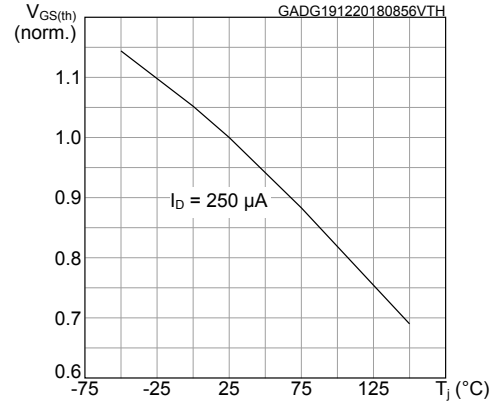


Figure 9. Normalized on-resistance vs temperature

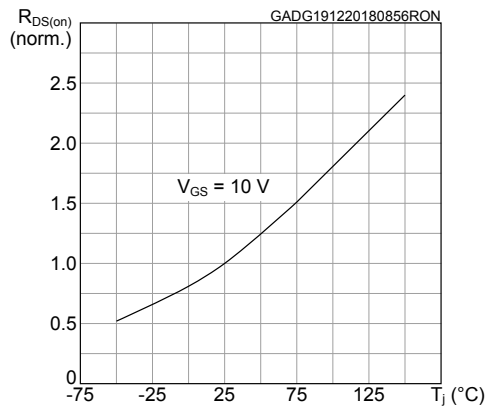


Figure 10. Normalized  $V_{(BR)DSS}$  vs temperature

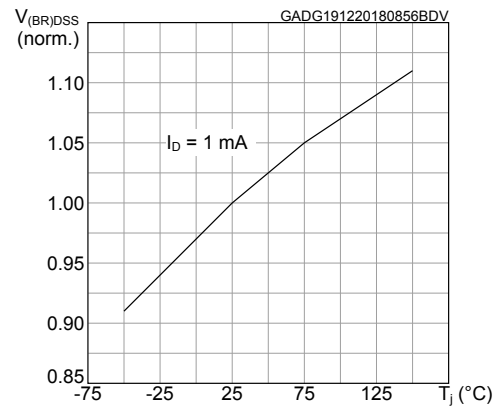


Figure 11. Source-drain diode forward characteristics

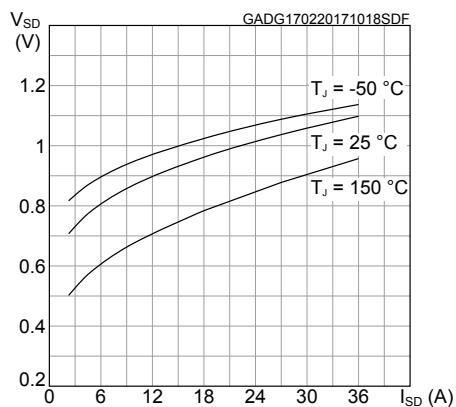
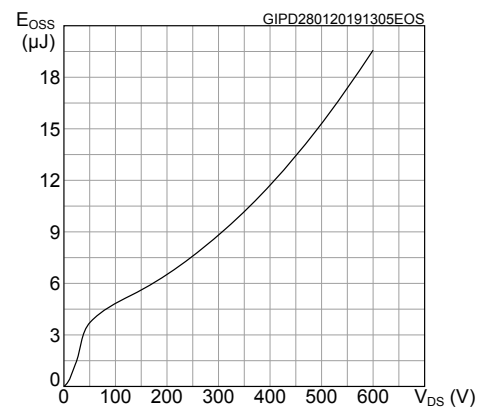


Figure 12. Output capacitance stored energy





## 4 Package information

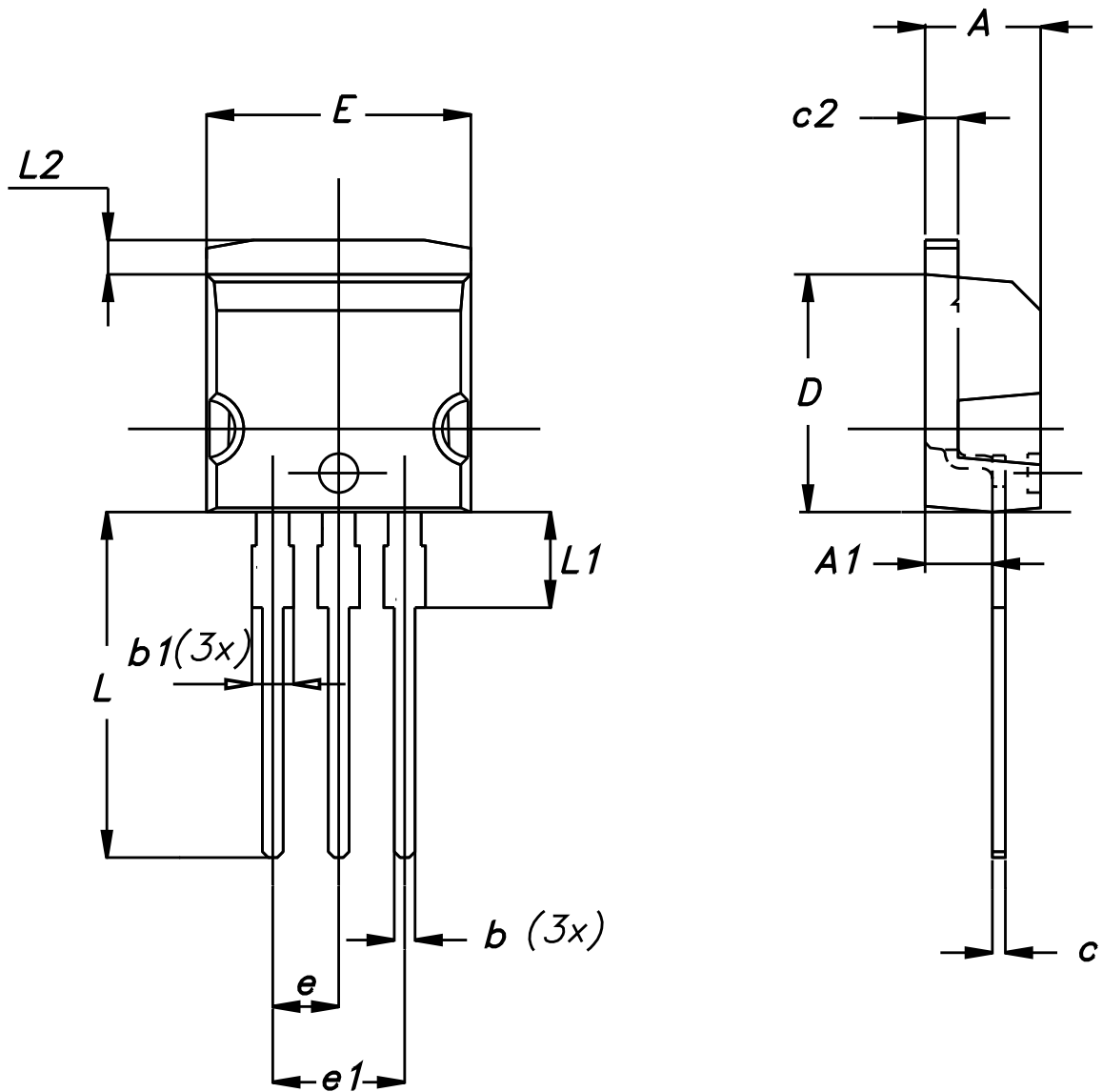
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In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK<sup>®</sup>** packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.



#### 4.1 I<sup>2</sup>PAK package information

Figure 19. I<sup>2</sup>PAK package outline



0004982\_Rev\_H

**Table 9.** I<sup>2</sup>PAK package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40	-	4.60
A1	2.40	-	2.72
b	0.61	-	0.88
b1	1.14	-	1.70
c	0.49	-	0.70
c2	1.23	-	1.32
D	8.95	-	9.35
e	2.40	-	2.70
e1	4.95	-	5.15
E	10	-	10.40
L	13	-	14
L1	3.50	-	3.93
L2	1.27	-	1.40

## Revision history

**Table 10. Document revision history**

Date	Revision	Changes
12-Apr-2017	1	Initial release.
15-Mar-2018	2	Removed maturity status indication from cover page. The document status is production data.
11-Mar-2019	3	Modified <a href="#">Table 1. Absolute maximum ratings</a> . Added <a href="#">Figure 12. Output capacitance stored energy</a> . Minor text changes.

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