

N-channel 100 V, 17 mΩ typ., 8 A STripFET™ F7 Power MOSFET in a PowerFLAT™ 3.3x3.3 package

Datasheet - production data

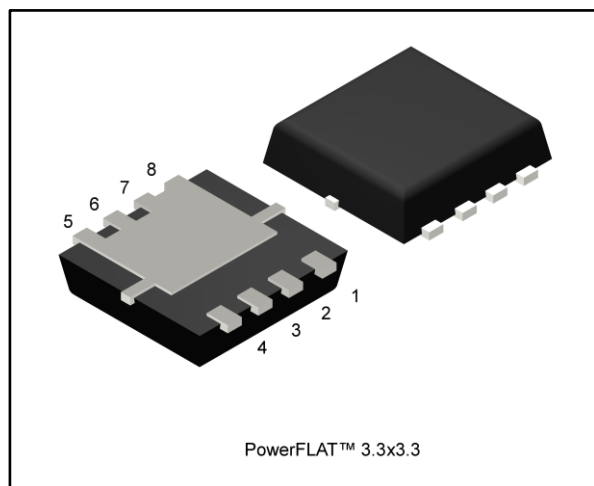
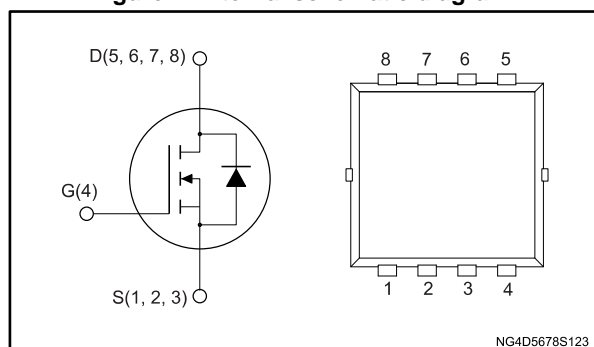


Figure 1: Internal schematic diagram



Features

| Order code | V _{DS} | R _{DS(on)} max. | I _D | P _{TOT} |
|------------|-----------------|--------------------------|----------------|------------------|
| STL8N10F7 | 100 V | 20 mΩ | 8 A | 2.9 W |

- Among the lowest R_{DS(on)} on the market
- Excellent FoM (figure of merit)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

| Order code | Marking | Package | Packing |
|------------|---------|--------------------|---------------|
| STL8N10F7 | 8N10F | PowerFLAT™ 3.3x3.3 | Tape and reel |

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1 Electrical ratings

Table 2: Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|-------------------|---|------------|------------------|
| V_{DS} | Drain-source voltage | 100 | V |
| V_{GS} | Gate-source voltage | ± 20 | V |
| $I_D^{(1)}$ | Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$ | 8 | A |
| $I_D^{(1)}$ | Drain current (continuous) at $T_{pcb} = 100\text{ }^\circ\text{C}$ | 6 | A |
| $I_D^{(2)}$ | Drain current (continuous) at $T_c = 25\text{ }^\circ\text{C}$ | 35 | A |
| $I_D^{(2)}$ | Drain current (continuous) at $T_c = 100\text{ }^\circ\text{C}$ | 22 | A |
| $I_{DM}^{(1)(3)}$ | Drain current (pulsed) | 32 | A |
| $I_{DM}^{(2)(3)}$ | Drain current (pulsed) | 140 | A |
| $P_{TOT}^{(2)}$ | Total dissipation at $T_c = 25\text{ }^\circ\text{C}$ | 50 | W |
| $P_{TOT}^{(1)}$ | Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$ | 2.9 | W |
| T_{stg} | Storage temperature range | -55 to 150 | $^\circ\text{C}$ |
| T_j | Operating junction temperature range | | $^\circ\text{C}$ |

Notes:

- (1) This value is rated according to $R_{thj-pcb}$.
 (2) This value is rated according to $R_{thj-case}$.
 (3) Pulse width limited by safe operating area.

Table 3: Thermal data

| Symbol | Parameter | Value | Unit |
|---------------------|----------------------------------|-------|---------------------------|
| $R_{thj-case}$ | Thermal resistance junction-case | 2.5 | $^\circ\text{C}/\text{W}$ |
| $R_{thj-pcb}^{(1)}$ | Thermal resistance junction-pcb | 42.8 | |

Notes:

- (1) When mounted on FR-4 board of 1inch², 2oz Cu, $t < 10\text{ s}$.

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 4: Static

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|-----------------------------------|---|------|------|-----------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$ | 100 | | | V |
| I_{DSS} | Zero gate voltage drain current | $V_{GS} = 0\text{ V}$, $V_{DS} = 100\text{ V}$ | | | 1 | μA |
| | | $V_{GS} = 0\text{ V}$, $V_{DS} = 100\text{ V}$, $T_c = 125\text{ °C}$ ⁽¹⁾ | | | 100 | μA |
| I_{GSS} | Gate-body leakage current | $V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$ | | | ± 100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$ | 2.5 | | 4.5 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS} = 10\text{ V}$, $I_D = 4\text{ A}$ | | 17 | 20 | m Ω |

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 5: Dynamic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------|------------------------------|--|------|------|------|------|
| C_{iss} | Input capacitance | $V_{DS} = 50\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$ | - | 1640 | - | pF |
| C_{oss} | Output capacitance | | - | 360 | - | pF |
| C_{rss} | Reverse transfer capacitance | | - | 25 | - | pF |
| Q_g | Total gate charge | $V_{DD} = 50\text{ V}$, $I_D = 8\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 14: "Test circuit for gate charge behavior") | - | 25 | - | nC |
| Q_{gs} | Gate-source charge | | - | 12 | - | nC |
| Q_{gd} | Gate-drain charge | | - | 5 | - | nC |

Table 6: Switching times

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--------------|---------------------|--|------|------|------|------|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD} = 50\text{ V}$, $I_D = 4\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 13: "Test circuit for resistive load switching times" and Figure 18: "Switching time waveform") | - | 15 | - | ns |
| t_r | Rise time | | - | 17 | - | ns |
| $t_{d(off)}$ | Turn-off-delay time | | - | 24 | - | ns |
| t_f | Fall time | | - | 8 | - | ns |

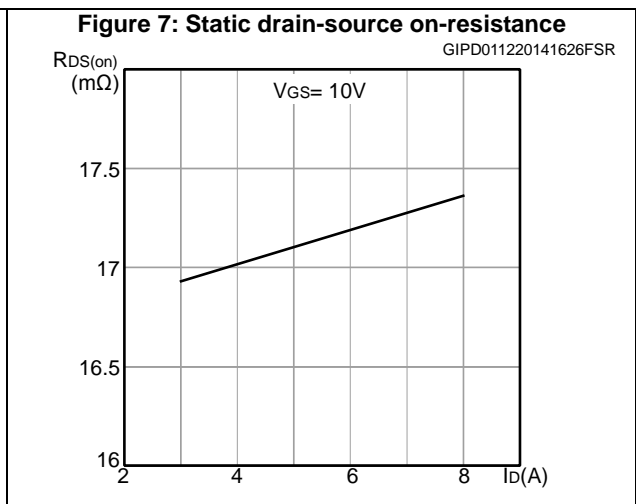
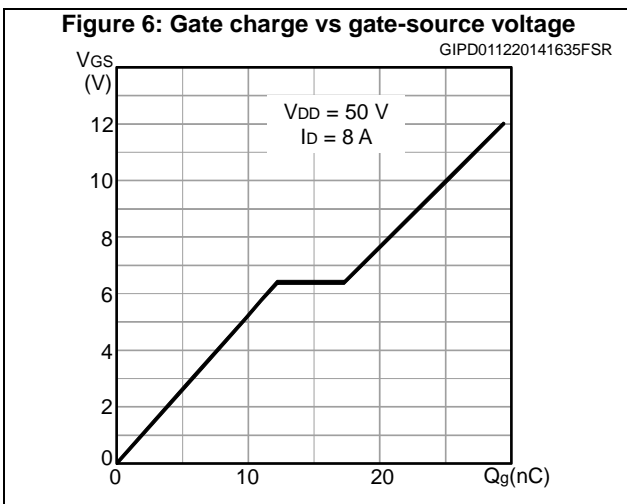
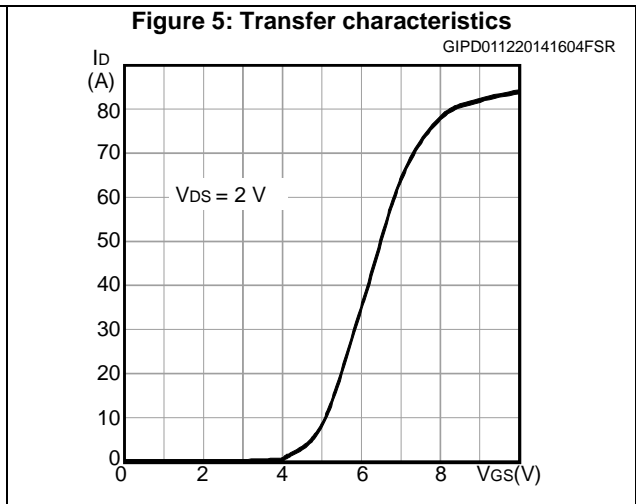
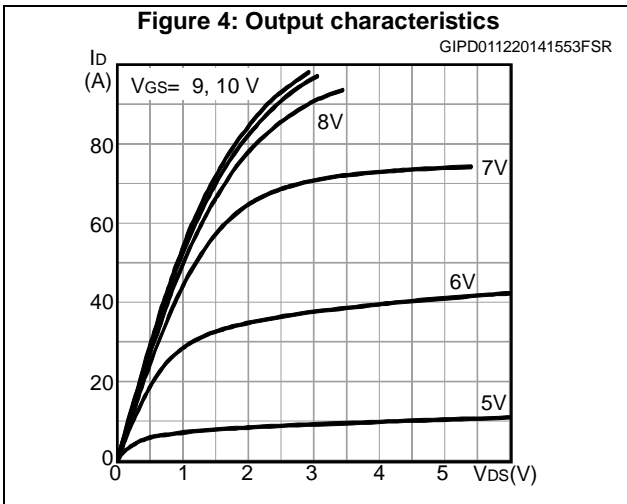
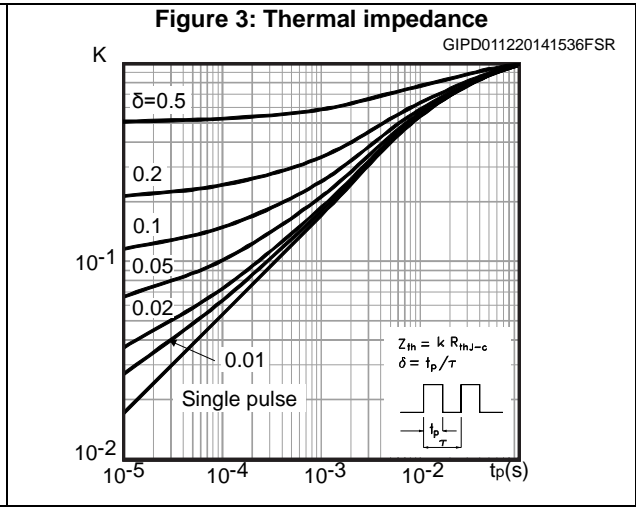
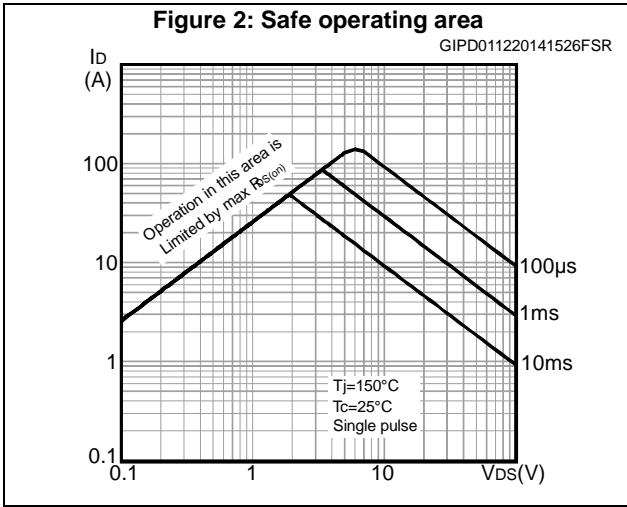
Table 7: Source-drain diode

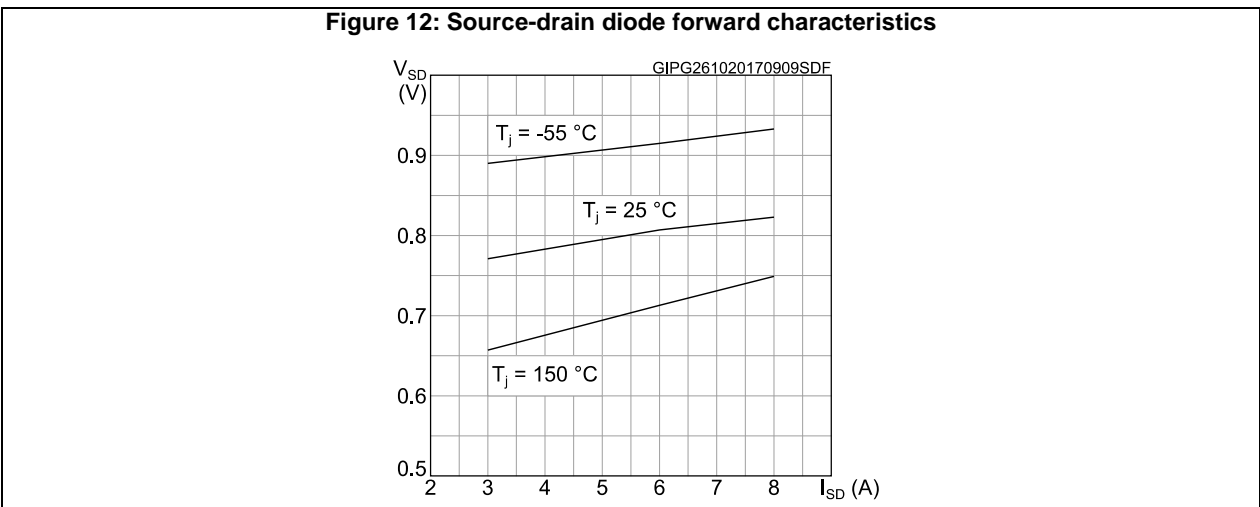
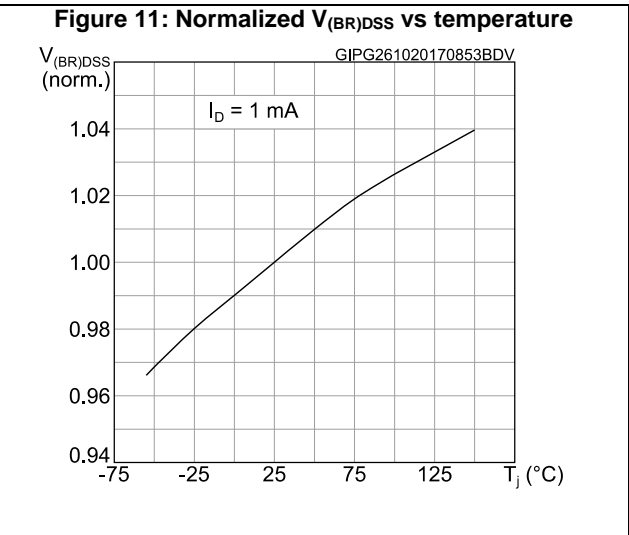
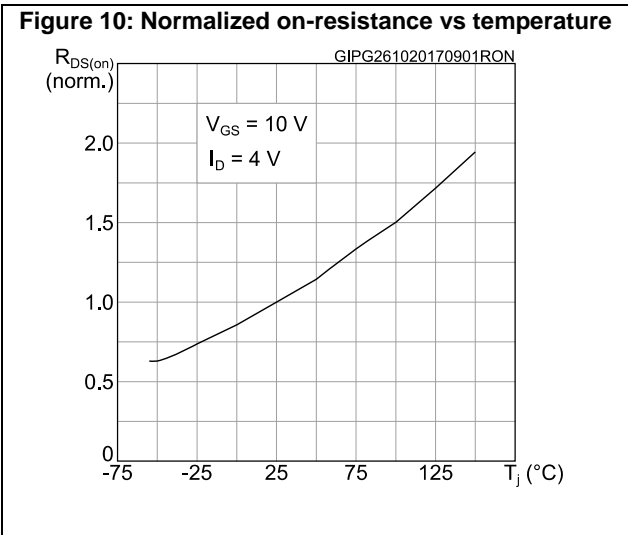
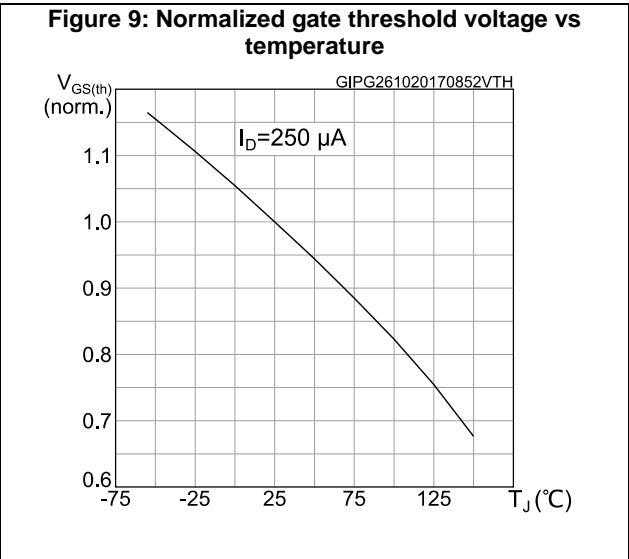
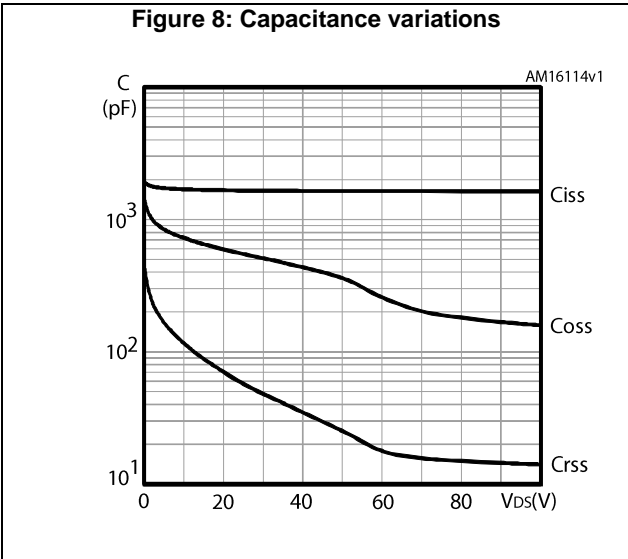
| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|----------------|--------------------------|--|------|------|------|------|
| $V_{SD}^{(1)}$ | Forward on voltage | $V_{GS} = 0\text{ V}$, $I_{SD} = 8\text{ A}$ | - | | 1.1 | V |
| t_{rr} | Reverse recovery time | $I_{SD} = 8\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 80\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 15: "Test circuit for inductive load switching and diode recovery times") | - | 53 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 67 | | nC |
| I_{RRM} | Reverse recovery current | | - | 2.5 | | A |

Notes:

⁽¹⁾Pulse test: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)





3 Test circuits

Figure 13: Test circuit for resistive load switching times



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Figure 14: Test circuit for gate charge behavior



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Figure 15: Test circuit for inductive load switching and diode recovery times



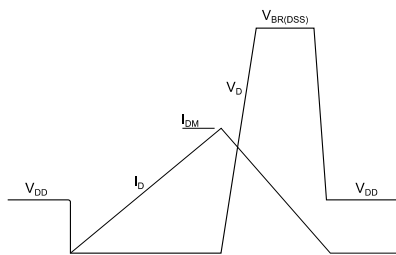
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Figure 16: Unclamped inductive load test circuit



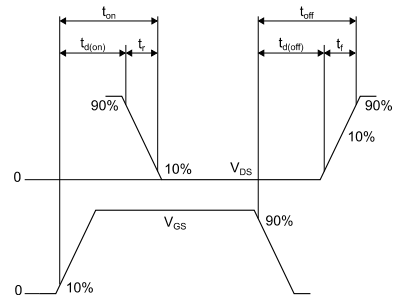
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Figure 17: Unclamped inductive waveform



AM01472v1

Figure 18: Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 PoweFLAT 3.3x3.3 package information

Figure 19: PowerFLAT™ 3.3x3.3 package outline

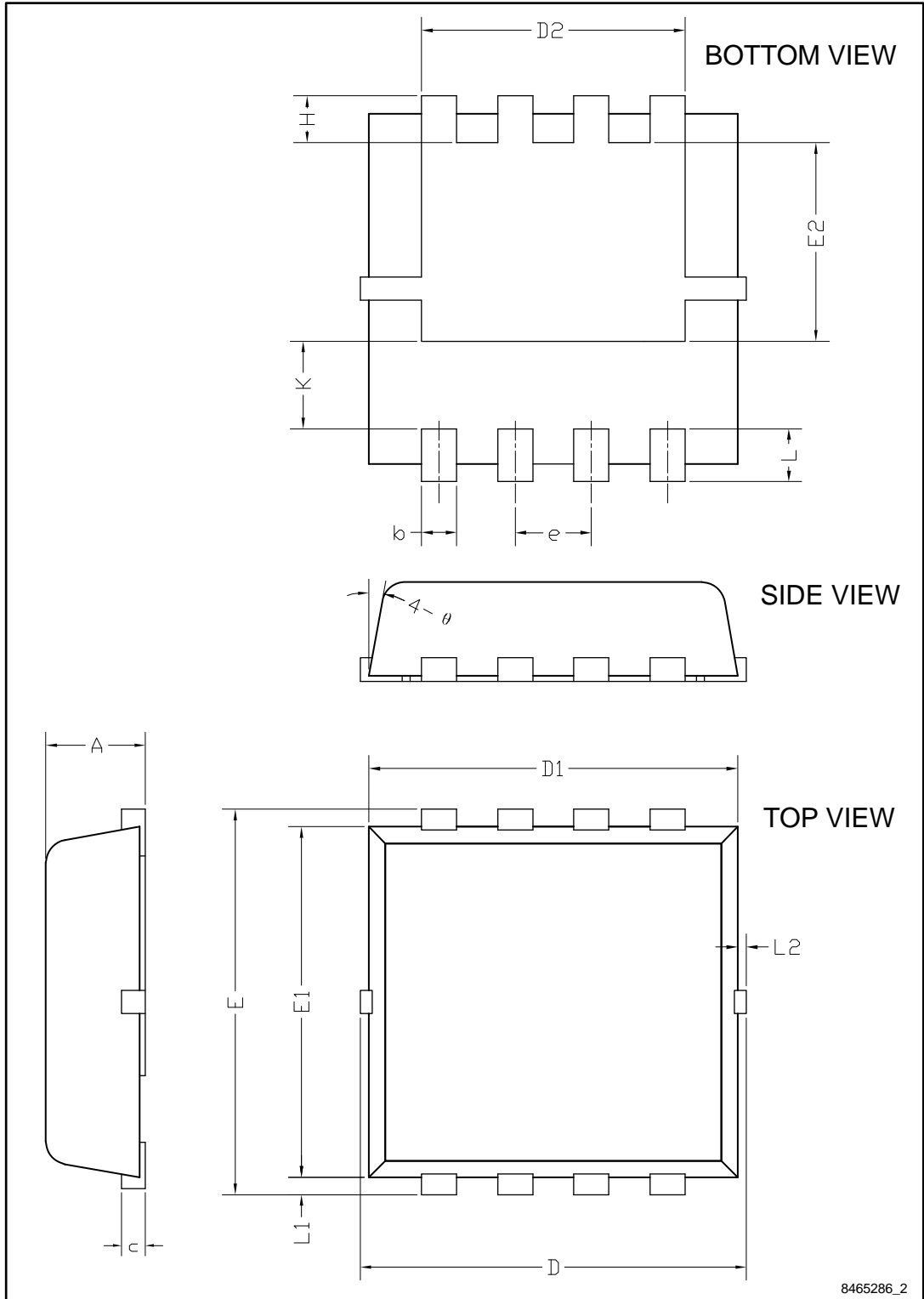
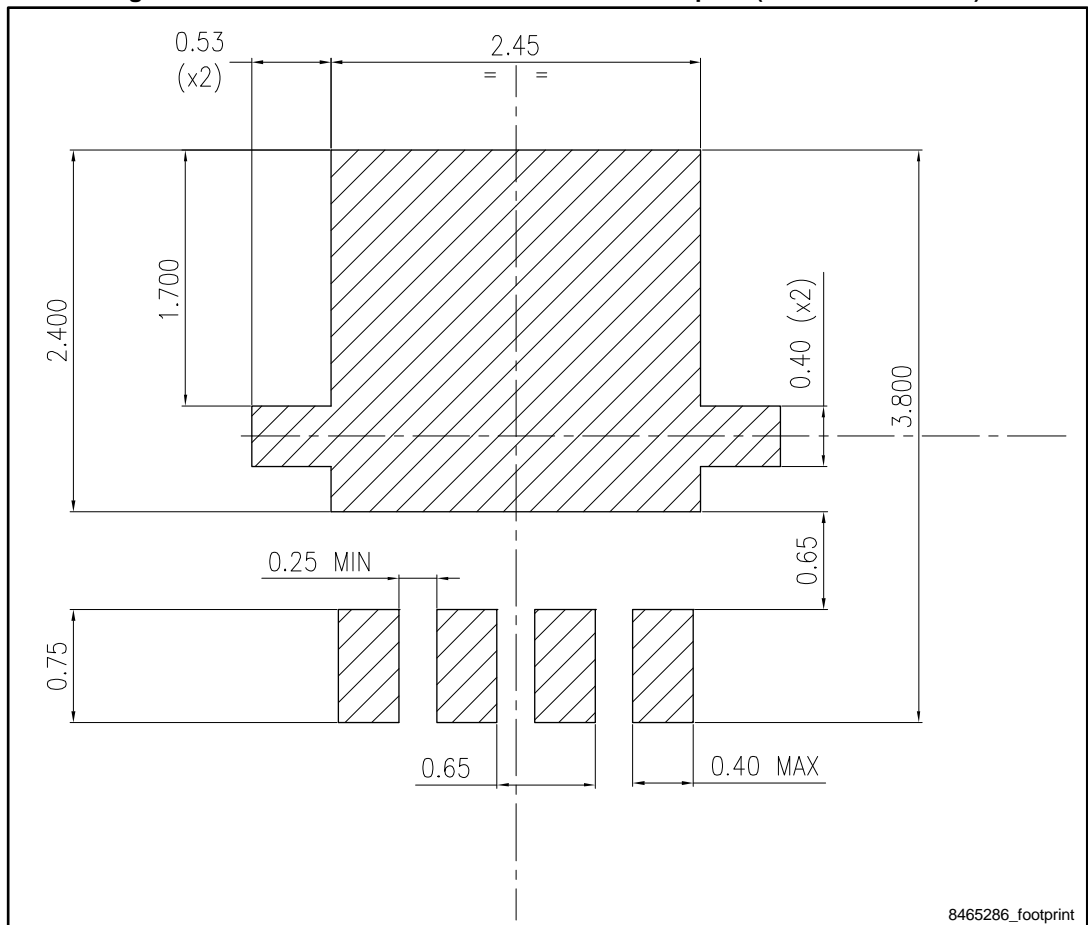


Table 8: PowerFLAT™ 3.3x3.3 package mechanical data

| Dim. | mm | | |
|----------|------|------|------|
| | Min. | Typ. | Max. |
| A | 0.70 | 0.80 | 0.90 |
| b | 0.25 | 0.30 | 0.39 |
| c | 0.14 | 0.15 | 0.20 |
| D | 3.10 | 3.30 | 3.50 |
| D1 | 3.05 | 3.15 | 3.25 |
| D2 | 2.15 | 2.25 | 2.35 |
| e | 0.55 | 0.65 | 0.75 |
| E | 3.10 | 3.30 | 3.50 |
| E1 | 2.90 | 3.00 | 3.10 |
| E2 | 1.60 | 1.70 | 1.80 |
| H | 0.25 | 0.40 | 0.55 |
| K | 0.65 | 0.75 | 0.85 |
| L | 0.30 | 0.45 | 0.60 |
| L1 | 0.05 | 0.15 | 0.25 |
| L2 | | | 0.15 |
| θ | 8° | 10° | 12° |

Figure 20: PowerFLAT™ 3.3x3.3 recommended footprint (dimensions in mm)



5 Revision history

Table 9: Document revision history

| Date | Revision | Changes |
|-------------|----------|--|
| 31-Jul-2013 | 1 | First release. |
| 05-Dec-2014 | 2 | <p>Document status promoted from preliminary to production data. Modified title, features and description in cover page. Modified: $R_{DS(on)}$ typical and max values in first page and in <i>Table 4: On/off states</i> Modified: <i>Section 4: Package mechanical data</i> Added <i>Section 2.1: Electrical characteristics (curves)</i>.</p> |
| 02-Nov-2017 | 3 | <p>Datasheet promoted from preliminary data to production data. Modified title, silhouette and features table on cover page. Modified <i>Table 2: "Absolute maximum ratings"</i>, <i>Table 4: "Static"</i> and <i>Table 5: "Dynamic"</i>. Modified <i>Figure 8: "Capacitance variations"</i>, <i>Figure 9: "Normalized gate threshold voltage vs temperature"</i>, <i>Figure 10: "Normalized on-resistance vs temperature"</i>, <i>Figure 11: "Normalized $V_{(BR)DSS}$ vs temperature"</i> and <i>Figure 12: "Source-drain diode forward characteristics"</i>. Updated <i>Section 4: "Package information"</i>. Minor text changes.</p> |

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