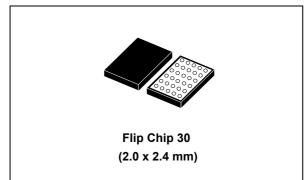


Low voltage high bandwidth quad DPDT switch

Datasheet - production data



Features

- Ultralow power dissipation
 - $I_{CC} = 1 \mu A \text{ (max.) at } T_A = 85 \text{ °C}$
- · Low "ON" resistance
 - R_{ON} = 5.4 Ω (T_A = 25 °C) at V_{CC} = 4.3 V
 - R_{ON} = 6.6 Ω (T_A = 25 °C) at V_{CC} = 3.0 V
- · Wide operating voltage range
 - V_{CC} (OPR.) = 1.65 V to 4.3 V
- 4.3 V tolerant and 1.8 V compatible threshold on digital control input at V_{CC} = 2.3 V to 3.0 V
- · 4 select pins controlling 2 switches each
- Typical bandwidth (-3 dB) at 800 MHz on all channels
- USB (2.0) high speed (480 Mbps) signal switching compliant
- · Integrated fail safe function
- Latch-up performance exceeds 100 mA per JESD 78, Class II
- ESD performance exceeds JESD22 2000-V human body model (A114-A)

Applications

Mobile phones

Description

The STG3820 device is a high-speed CMOS low voltage quad analog DPDT (dual pole dual throw) switch or 2:1 multiplexer/demultiplexer switch fabricated in silicon gate C²MOS technology. It is designed to operate from 1.65 V to 4.3 V, making this device ideal for portable applications.

The SELm-n input is provided to control the switches. The switches nS1 and mS1 are ON (connected to common ports Dn and Dm respectively) when the SELm-n input is held high and OFF (high impedance state exists between the two ports) when the SELm-n is held low. The switches nS2 and mS2 are ON (connected to common port Dn and Dm respectively) when the SELm-n input is held low and OFF (high impedance state exists between the two ports) when the SELm-n is held high.

The STG3820 device has an integrated fail safe function to withstand overvoltage condition when the device is powered off. Additional key features are fast switching speed, break-before-makedelay time and ultralow power consumption. All inputs and outputs are equipped with protection circuits against static discharge, giving them ESD immunity and transient excess voltage.

Table 1. Device summary

Order code	Package	Packing
STG3820BJR	Flip Chip 30 (2.0 x 2.4 mm)	Tape and reel

Contents STG3820

Contents

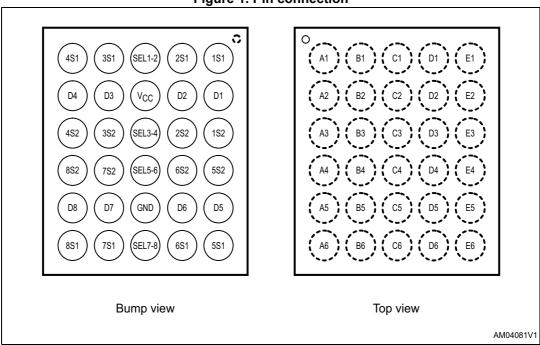
1	Pin settings	. 3
	1.1 Pin connection	. 3
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STG3820 Pin settings

1 Pin settings

1.1 Pin connection

Figure 1. Pin connection



1.2 Pin description

Table 2. Pin assignment

Pin number	Symbol	Name and function
A1	1S1	Independent channel for switch 1
A2	D1	Common channel for switch 1
A3	1S2	Independent channel for switch 1
A4	5S2	Independent channel for switch 5
A5	D5	Common channel for switch 5
A6	5S1	Independent channel for switch 5
B1	2S1	Independent channel for switch 2
B2	D2	Common channel for switch 2
В3	2S2	Independent channel for switch 2
B4	6S2	Independent channel for switch 6
B5	D6	Common channel for switch 6
В6	6S1	Independent channel for switch 6

Pin settings STG3820

Table 2. Pin assignment (continued)

Pin number	Symbol	Name and function
C1	SEL1-2	Switch 1-2 selection control
C2	VCC	Positive supply voltage
C3	SEL3-4	Switch 3-4 selection control
C4	SEL5-6	Switch 5-6 selection control
C5	GND	Ground (0 V)
C6	SEL7-8	Switch 7-8 selection control
D1	3S1	Independent channel for switch 3
D2	D3	Common channel for switch 3
D3	3S2	Independent channel for switch 3
D4	7S2	Independent channel for switch 7
D5	D7	Common channel for switch 7
D6	7S1	Independent channel for switch 7
E1	4S1	Independent channel for switch 4
E2	D4	Common channel for switch 4
E3	4S2	Independent channel for switch 4
E4	8S2	Independent channel for switch 8
E5	D8	Common channel for switch 8
E6	8S1	Independent channel for switch 8

Logic diagram STG3820

Logic diagram 2

Figure 2. Logic equivalent circuit

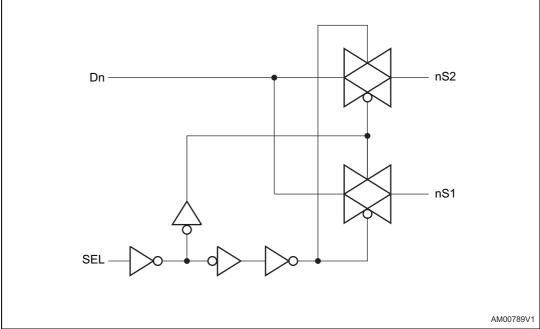


Table 3. Truth table

SEL	Switch nS1	Switch nS2
Н	ON	OFF ⁽¹⁾
L	OFF ⁽¹⁾	ON

^{1.} High impedance.

Maximum ratings STG3820

3 Maximum ratings

Stressing the device above the rating listed in *Table 4: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in *Table 5: Recommended operating conditions* of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{CC}	Supply voltage	-0.5 to 6.0	V
V _I	DC input voltage	-0.5 to V _{CC} + 0.5	V
V _{IC}	DC control input voltage	-0.5 to 5.5	V
V _O	DC output voltage	-0.5 to V _{CC} + 0.5	V
I _{IKC}	DC input diode current on control pin (V _{SEL} < 0 V)	-50	mA
I _{IK}	DC input diode current (V _{SEL} < 0 V)	±50	mA
I _{OK}	DC output diode current	±20	mA
I _O	DC output current	±128	mA
I _{OP}	DC output current peak (pulse at 1 ms, 10% duty cycle)	±300	mA
I _{CC} or I _{GND}	DC V _{CC} or ground current	±100	mA
P _D	Power dissipation at T _A = 70 °C	1120	mW
T _{stg}	Storage temperature	-65 to +150	°C
T _L	Lead temperature (10 sec.)	300	°C

Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Paramet	Value	Unit			
V_{CC}	Supply voltage	Supply voltage				
VI	Input voltage	Input voltage				
V _{IC}	Control input voltage	Control input voltage				
Vo	Output voltage		0 to V _{CC}	V		
T _{op}	Operating temperature		-40 to 85	°C		
dt/dv	Input rise and fall time control	V _L = 1.65 V to 2.7 V	0 to 20	ns/V		
ui/uv	input	0 to 10	115/V			

4 Electrical characteristics

Table 6. DC specifications

						Value			
Symbol	Parameter	V _{CC} (V)	Test conditions		T _A = 25 °C			85 °C	Unit
				Min.	Тур.	Max.	Min.	Max.	
		1.65 – 1.95		0.65 V _{CC}	-	_	0.65 V _{CC}	_	
	High level input	2.3 – 2.5		1.2	_	_	1.2	_	
V _{IH}	voltage	2.7 – 3.0		1.3	_	_	1.3	_	V
		3.3 – 3.6		1.4	_	_	1.4	_	
		4.3		1.6	_	_	1.6	_	
		1.65 – 1.95		_	_	0.25	_	0.25	
V _{IL}		2.3 – 2.5		_	_	0.25	_	0.25	
	Low level input voltage	2.7 – 3.0		_	_	0.25	_	0.25	V
		3.3 – 3.6		_	_	0.30	_	0.30	
		4.3		_	_	0.40	_	0.40	
		1.8	$V_S = 0 \text{ V to } V_{CC}$ $I_S = 8 \text{ mA}$	_	17.0	19.6	_	_	Ω
		2.7		_	7.5	8.7	_	_	
R _{PEAK}	Switch ON peak resistance	3.0		_	6.6	7.6	_	_	
		3.7	3 •	_	5.8	6.7	_	_	
		4.3		_	5.4	6.2	_	_	
	Switch ON	3.0	$V_S = 3 V$ $I_S = 8 \text{ mA}$	_	5.1	5.8	_	_	•
R _{ON}	resistance	3.0	$V_S = 0.4 \text{ V}$ $I_S = 8 \text{ mA}$	_	6.3	7.3	_	_	Ω
		1.8		_	_	_	_	_	
	ON registance	2.7		_	_	_	_	_	Ω
ΔR_{ON}	ON resistance match between	3.0	V _S at R _{ON} MAX I _S = 8 mA	_	0.3	_	_	_	
	channels ⁽¹⁾	3.7	5 0	_	_	_	_	_	
		4.3		_	_	_	_	_	

Electrical characteristics STG3820

Table 6. DC specifications (continued)

					Value					
Symbol	Parameter	V _{CC} (V)	Test conditions	7	T _A = 25 °C			85 °C	Unit	
				Min.	Тур.	Max.	Min.	Max.		
		1.8	$V_S = 0 \text{ V to}$ 0.4 V $I_S = 8 \text{ mA}$	-	4.5	_	_	_		
		1.8		_	9.5	_	_	_		
R _{FLAT}	ON resistance flatness ⁽²⁾	2.7		_	2.2	_	_	_	Ω	
		3.0	$V_S = 0 \text{ V to } V_{CC}$ $I_S = 8 \text{ mA}$	_	1.8	_	_	_		
		3.7		_	1.6	_	_	_		
		4.3		_	1.6	_	_	_		
l _{OFF}	OFF state leakage current (Sn), (D)	4.3	V _S = 0.3 or 4 V	-20	_	20	-100	100	nA	
I _{IN}	Input leakage current	0 to 4.3	V _{SEL} = 0 to 4.3 V	-0.2	_	0.2	-1.0	1.0	μA	
I _{CC}	Quiescent supply current	1.65 to 4.3	V _{SEL} = V _{CC} or GND	-0.2	_	0.2	-1.0	1.0	μA	
	Quiescent supply		V _{SEL} = 1.65 V	_	±37	±50	_	±100		
I _{CCLV}	current for low	4.3	V _{SEL} = 1.80 V	_	±33	±40	_	±50	μΑ	
	voltage driving ⁽³⁾		V _{SEL} = 2.60 V	_	±11	±20	-	±30		

^{1.} ΔR_{ON} = max. |mSN - nSN|, where m = 1 to 8 and n = 1 to 8, N = 1, 2.

^{2.} Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.

^{3.} Measurement is for one SEL pin.

Table 7. AC electrical characteristics (C $_L$ = 35 pF, R $_L$ = 50 $\Omega,\,t_r$ = $t_f~\leq~5$ ns)

						Value			
Symbol	Parameter	V _{CC} (V) Test conditions		7	T _A = 25 °C			85 °C	Unit
				Min.	Тур.	Max.	Min.	Max.	
		1.65 - 1.95		_	0.21	_	_	_	
t t	Propagation	2.3 - 2.7		_	0.15	_	_	_	ns
t _{PLH} , t _{PHL}	delay	3.0 - 3.3		_	0.14	_	_	_	113
		3.6 - 4.3		_	0.13	_	_	_	
		1.65 - 1.95	V _S = 0.8 V	-	36	_	_	_	
t	Turn-on time	2.3 - 2.7		_	20	23	_	26	ne
ON	t _{ON} Turn-on time	3.0 - 3.3	$V_{S} = 1.5 V$	-	15	17	_	20	ns
		3.6 - 4.3		_	13	15	_	17	
		1.65 - 1.95	V _S = 0.8 V	-	29	_	_	_	
t	Turn-off time	2.3 - 2.7		_	19	22	_	25	ns
t _{OFF}	rum-on ume	3.0 - 3.3	$V_{S} = 1.5 V$	_	14	16	_	18	113
		3.6 - 4.3		_	11	13	_	14	
		1.65 - 1.95		_	10	_	_	_	
t_	Break-before-	2.3 - 2.7	$C_L = 35 \text{ pF}$ $R_L = 50 \Omega$	-	7	_	_	_	ne
t _D	make time delay	3.0 - 3.3	$V_{S} = 1.5 \text{ V}$	-	6	_	_	_	ns
		3.6 - 4.3		_	4	_	_	_	
		1.65		-	3.9	_	_	_	
Q	Charge injection	2.3	C _L = 100 pF V _{GEN} = 0 V	_	4.8	_	_	_	pC
Q	Onarge injection	3.0	$R_{GEN} = 0 V$ $R_{GEN} = 0 \Omega$	_	5.2	_	_	_	
		4.3		_	6.4	_	_	_	

Electrical characteristics STG3820

Table 8. AC electrical characteristics (C $_L$ = 5 pF, R $_L$ = 50 $\Omega,$ T $_A$ = 25 $^{\circ}\text{C})$

				Value					
Symbol	Parameter	V _{CC} (V)	Test conditions	Т	A = 25 °	С	-40 to	85 °C	Unit
				Min.	Тур.	Max.	Min.	Max.	
OIDD	40	1.65 – 4.3	$V_S = 1 V_{RMS}$, f = 1 MHz signal = 0 dBm	_	-78	_	_	-	dB
OIRR OFF isolation ⁽¹⁾	OFF Isolation 7	1.05 – 4.3	$V_S = 1 V_{RMS}$, f = 10 MHz signal = 0 dBm	_	-57	_	_	-	ив
Xtalk		1.65 – 4.3	$V_S = 1 V_{RMS}$, f = 1 MHz signal = 0 dBm	_	-78	_	_	-	dB
Aldık	Crosstalk	1.05 – 4.5	$V_S = 1 V_{RMS}$, f = 10 MHz signal = 0 dBm	_	-58	_	_	-	uв
BW	-3dB bandwidth	3.0 – 4.3	$R_L = 50 \Omega$ signal = 0 dBm	-	800	_	_	1	MHz
C _{IN}	Control pin input capacitance		V _{CC} = 0 V	_	2	_	_	_	pF
	Sn port capacitance	3.3	F = 240 MHz, switch is enabled	_	6		_	_	nE
C _{Sn}	Sn port capacitance	3.3	F = 240 MHz, switch is disabled	_	2	_	_	_	pF
C _D	D port capacitance	3.3	F = 240 MHz	_	8	_	_	_	pF

^{1.} Off isolation = 20 Log10 (V_D/V_S), V_D = output, V_S = input to off switch.

Table 9. USB related AC electrical characteristics

Symbol				Value					
	Parameter	V _{CC} (V)	Test conditions	T _A = 25 °C			-40 to 85 °C		Unit
				Min.	Тур.	Max.	Min.	Max.	
t _{SK(0)}	Channel-to- channel skew	3.0 - 3.6	C _L = 10 pF	_	26	-	-	_	ps
t _{SK(P)}	Skew of opposite transition of the same output	3.0 - 3.6	C _L = 10 pF	_	60	_	_	_	ps
TJ	Total jitter	3.0 - 3.6	$R_L = 50 \Omega$ $C_L = 10 \text{ pF}$ $t_R = t_F = 750 \text{ ps}$ at 480 Mbps	ı	130	_	_	_	ps

STG3820 **Test circuits**

Test circuits 5

Figure 3. On-resistance

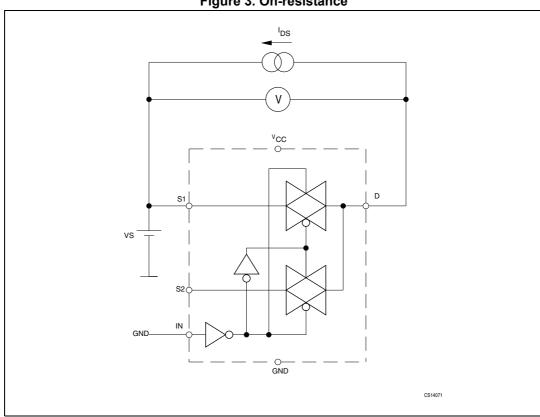
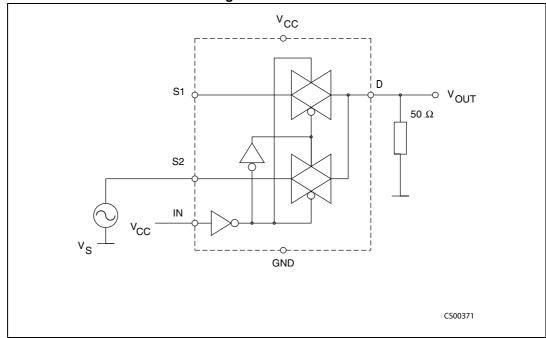


Figure 4. Bandwidth



STG3820 Test circuits

Figure 5. Off leakage

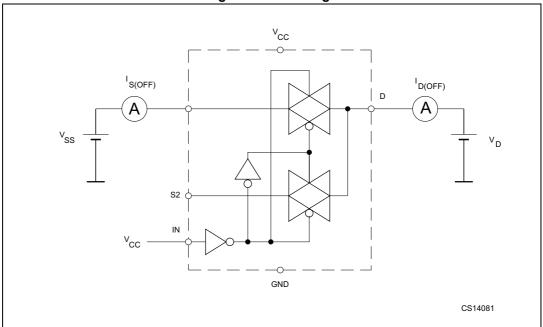
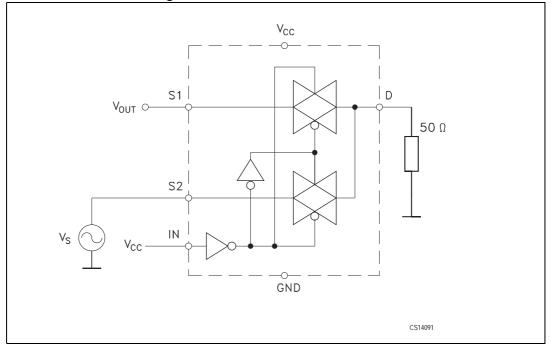


Figure 6. Channel to channel crosstalk



Test circuits STG3820

Figure 7. Off isolation

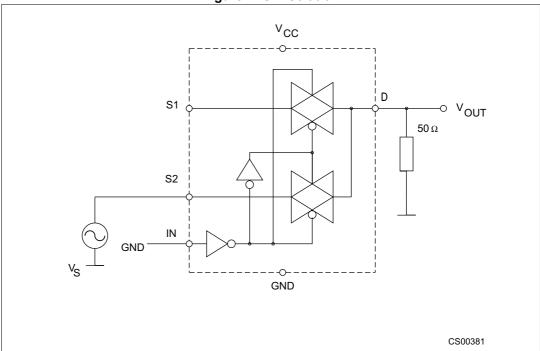
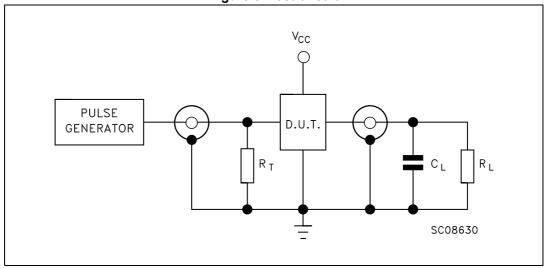


Figure 8. Test circuit



Note:

 C_L = 5/35 pF or equivalent: (includes jig capacitance).

 R_L = 50 Ω or equivalent.

 R_T = Z_{OUT} of pulse generator (typically 50 Ω).

STG3820 Test circuits

Figure 9. Break-before-make time delay

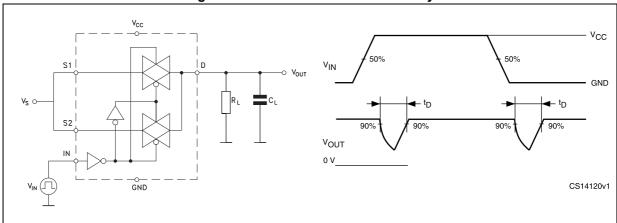


Figure 10. Switching time and charge injection (V_{GEN} = 0 V, R_{GEN} = 0 Ω , R_L = 1 M Ω , C_L = 100 pF)

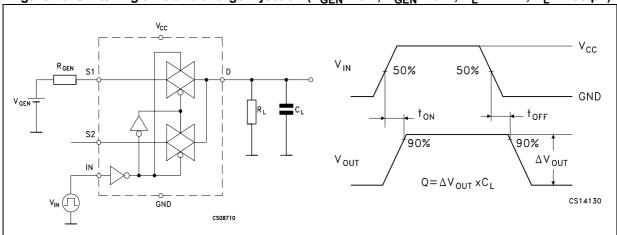
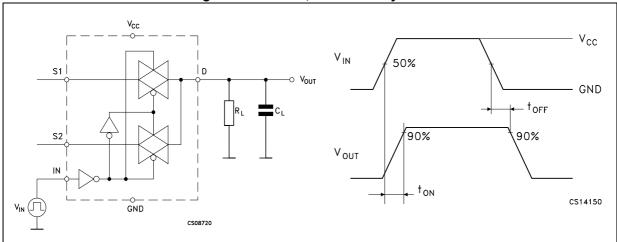


Figure 11. Turn-on, turn-off delay time



Package information STG3820

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Figure 12. Package outline for Flip Chip 30 (2.0 x 2.4 x 0.625 mm) - 0.4 mm pitch D1 ØЬ **BOTTOM VIEW** Ε D **TOP VIEW**

4

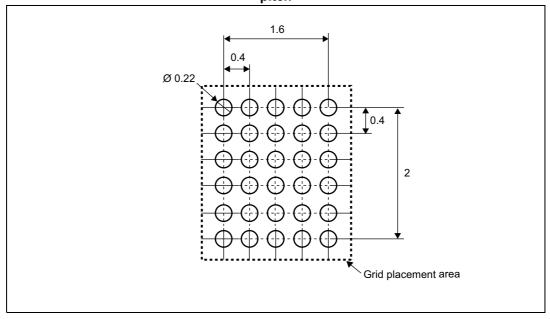
Flip Chip 30

STG3820 Package information

Table 10. Mechanical data for Flip Chip 30 (2.0 x 2.4 x 0.625 mm) - 0.4 mm pitch

Symbol	Dimensions (mm)		
	Min.	Тур.	Max.
Α	0.565	0.625	0.685
A1	0.17	0.205	0.24
A2	0.355	0.375	0.395
b	0.215	0.255	0.295
D	2.1	2.4	2.43
D1	_	2.0	-
E	1.97	2.0	2.03
E1	_	1.6	-
е	0.36	0.4	0.44
f	0.19	0.2	0.21
ccc	_	0.05	-
\$	0.040	0.045	0.05

Figure 13. Footprint recommendations for Flip Chip 30 (2.0 x 2.4 x 0.625 mm) - 0.4 mm pitch

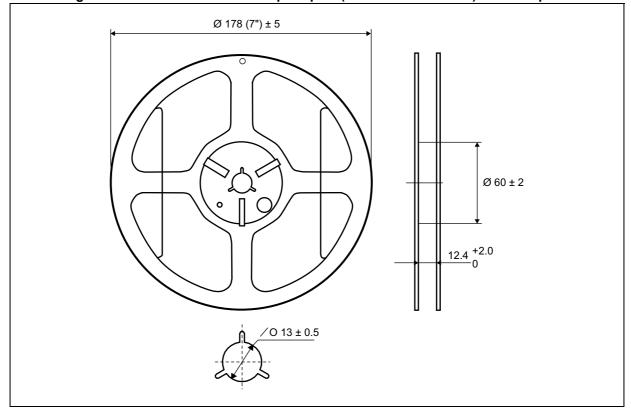


Package information STG3820

 2.00 ± 0.05 4.00 ± 0.10 4.00 ± 0.10 Ø 1.50 ± 0.10 1.75 ± 0.10 + 3.50 ± 0.05 8.00 ^{+0.30} _{-0.10} 0.20 ± 0.02 45° 45° 2.18 ± 0.05 0.73 ± 0.05 2.54 ± 0.05 Αo Во Ko

Figure 14. Tape information for Flip Chip 30 (2.0 x 2.4 x 0.625 mm) - 0.4 mm pitch





STG3820 Revision history

7 Revision history

Table 11. Document revision history

Date	Revision	Changes	
18-Dec-2009	1	Initial release.	
19-Jan-2011	2	Document reformatted, added <i>Contents</i> , updated <i>Figure 12</i> and <i>Figure 13</i> , corrected typo in <i>Features</i> , <i>Table 1</i> , <i>Section 1: Pin settings</i> , <i>Table 2</i> , <i>Table 7</i> , <i>Table 8</i> , notes below <i>Figure 8</i> , title of <i>Figure 11</i> , <i>Figure 12</i> , <i>Table 10</i> , and <i>Figure 13</i> , corrected name of "Table 11" to <i>Figure 13</i> .	
23-Apr-2013	3	Moved <i>Description</i> to page 1. Redrawn <i>Figure 1</i> . Updated <i>Section 3</i> (added/updated cross-references, updated V _{CC} value in <i>Table 4</i>). Redrawn <i>Figure 12</i> to <i>Figure 15</i> . Updated <i>Figure 12</i> (removed superfluous reference to note). Updated title of <i>Figure 14</i> and <i>Figure 15</i> (added "Flip Chip 30 (2.0 x 2.4 x 0.625 mm) - 0.4 mm pitch"). Minor corrections throughout document.	
06-Aug-2013	4	4 Updated <i>Table 8 on page 10</i> (replaced C _{ON} and C _{OFF} symbol by C _{sn} and C _D symbol).	

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