UM0755
User manual

FET driver for 3-phase BLCD motor
L9906 demonstration board

Introduction

The L9906 demonstration board is an evaluation board designed to provide the user with a platform for the evaluation of the L9906. The board provides all the main input/output capabilities needed to drive a BLCD motor properly and to provide diagnostic functionalities.

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1 Hardware description

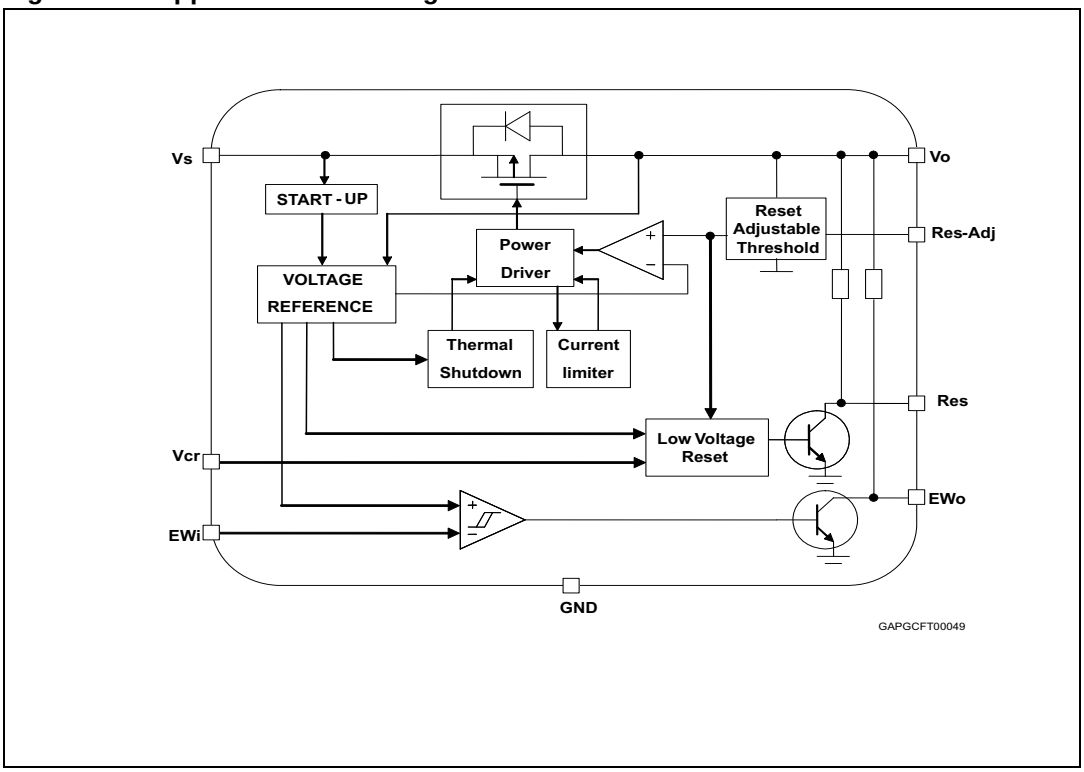
The L9906 demonstration board has been developed for maximum flexibility, giving the user total access to all pins to simplify changing the device as well as the external PowerMOS on the inverter.

Its main features are:

- Total accessibility to all pins.
- Daughterboard approach to simplify changing the device.
- Daughterboard approach for the inverter to simplify changing the external PowerMOS.

1.1 Block diagram

Figure 1. Application block diagram



1.1.1 Microcontroller

- Standard connector for ST10F252 family
- PWM input
- Configuration and diagnostics of L9906 via SPI
- Possibility to connect to other microcontrollers by wire adaptor

1.1.2 Inverter

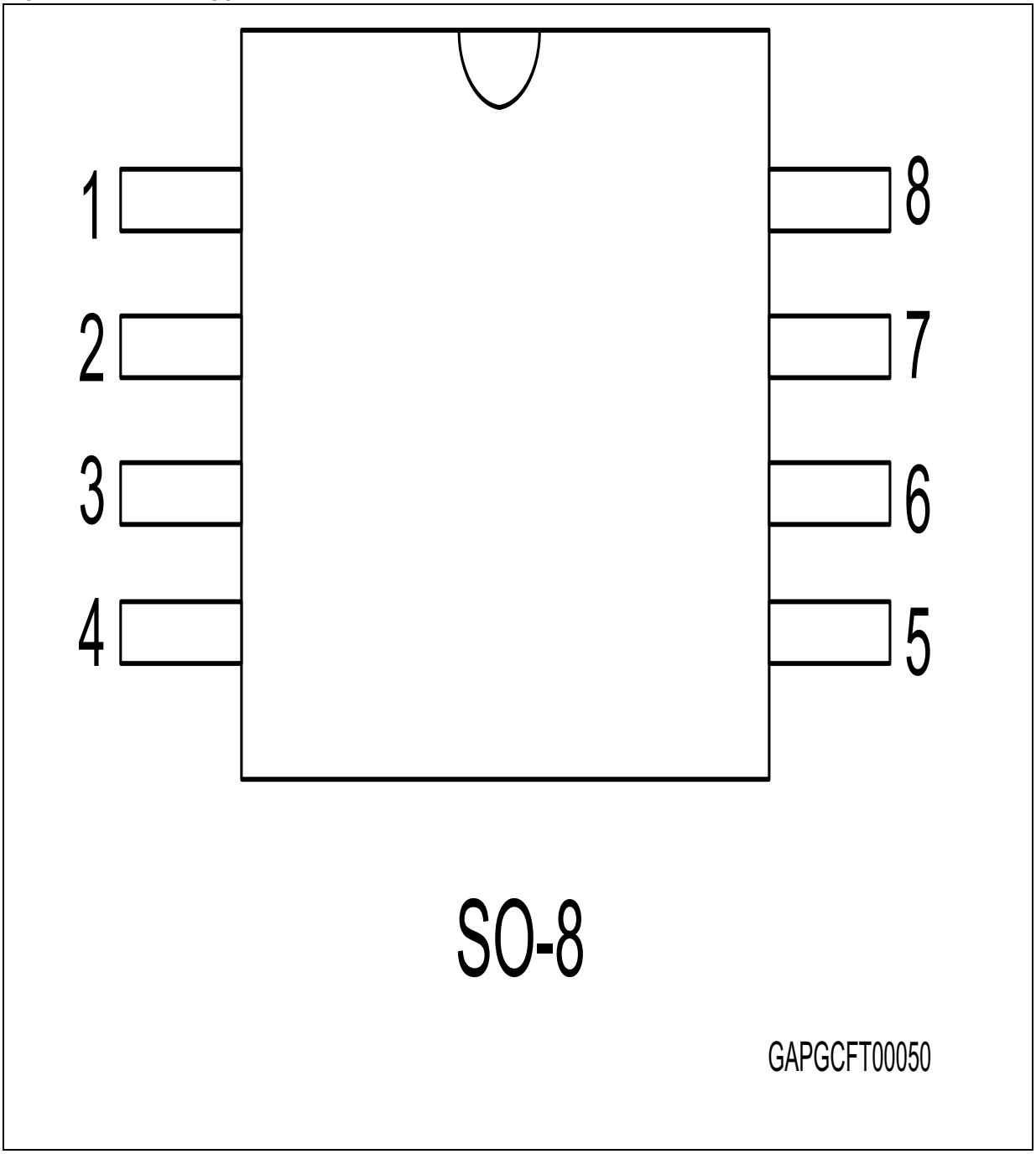
- BLCD motor driver
- Daughterboard approach
- 6 Power Mosfet (ST N-channel PowerMOS 40 V - 4.4 mΩ - 80 A - D2PAK)

1.1.3 USB

- The SPI communication can be controlled also by a PC via an external USB converter changing the jumper configuration.

2 L9906 application circuit

Figure 2. L9906 application circuit



3 L9906 pinout and pin descriptions

Figure 3. L9906 pinout

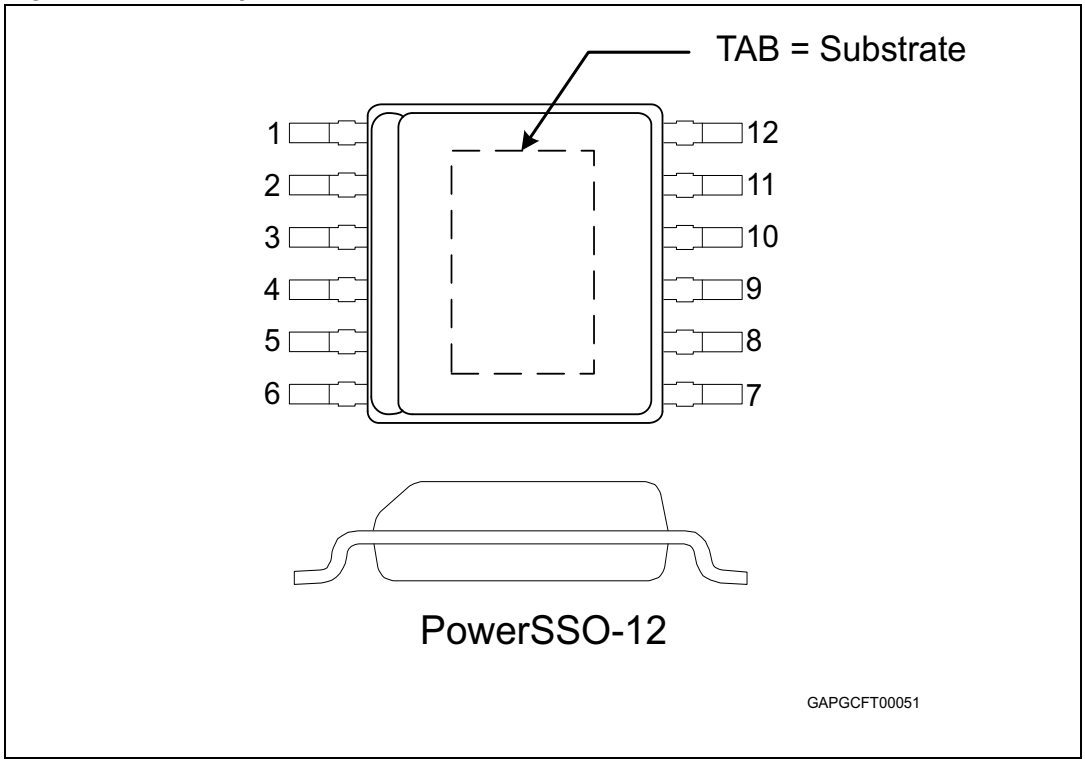


Table 1. L9906 pin descriptions

Pin number	Pin name	Description	I/O type
1	NC	Not connected	-
2	GLS_3	Gate connection for low-side MOSFET, phase 3	O
3	SLS_3	Source connection for low-side MOSFET, phase 3	I
4	NC	Not connected	-
5	GLS_2	Gate connection for low-side MOSFET, phase 2	O
6	SLS_2	Source connection for low-side MOSFET, phase 2	I
7	NC	Not connected	-
8	GLS_1	Gate connection for low-side MOSFET, phase 1	O
9	SLS_1	Source connection for low-side MOSFET, phase 1	I
10	AGND	Analog Ground	GND
11	IS1+	Positive input for current sense amplifier 1	I
12	IS1-	Negative input for current sense amplifier 1	I
13	NC	Not connected	-
14	IB1	Output for current sense amplifier 1 (test mode digital output #1)	O

Table 1. L9906 pin descriptions (continued)

Pin number	Pin name	Description	I/O type
15	IB2	Output for current sense amplifier 2 (test mode digital output #2)	O
16	SGND2	Substrate (and ESD_GND) connection 2	GND
17	IS2-	Negative input for current sense amplifier 2	I
18	IS2+	Positive input for current sense amplifier 2	I
19	NC	Not connected	-
20	CBS_3	Bootstrap capacitor for high-side MOSFET, phase 3	I
21	GHS_3	Gate connection for high-side MOSFET, phase 3	O
22	SHS_3	Source connection for high-side MOSFET, phase 3	I
23	NC	Not connected	-
24	CBS_2	Bootstrap capacitor for high-side MOSFET, phase 2	I
25	GHS_2	Gate connection for high-side MOSFET, phase 2	O
26	SHS_2	Source connection for high-side MOSFET, phase 2	I
27	NC	Not connected	-
28	CBS_1	Bootstrap capacitor for high-side MOSFET, phase 1	I
29	GHS_1	Gate connection for high-side MOSFET, phase 1	O
30	SHS_1	Source connection for high-side MOSFET, phase 1	I
31	NC	Not connected	-
32	NC	Not connected	-
33	TM	Test mode enable input	I
34	PWM_H1	PWM command input for high-side phase 1	I
35	PWM_H2	PWM command input for high-side phase 2	I
36	PWM_H3	PWM command input for high-side phase 3	I
37	FS_FLAG	Fault status flag output	O
38	CS	SPI chip select input	I
39	SCK	SPI serial clock input	I
40	SI	SPI serial data input	I
41	SO	SPI serial data output	O
42	TO3	Test output	O
43	EN2	Enable input 2 (ANDed with EN1 to enable any gate drive output)	I
44	EN1	Enable input 1(ANDed with EN1 to enable any gate drive output)	I
45	PWM_L1	PWM command input for low-side phase 1	I
46	PWM_L2	PWM command input for low-side phase 2	I
47	PWM_L3	PWM command input for low-side phase 3	I
48	SGND1	Substrate (and ESD_GND) connection1	GND
49	VCC	5 V/3.3 V power supply input	I

Table 1. L9906 pin descriptions (continued)

Pin number	Pin name	Description	I/O type
50	NC	Not connected	-
51	GCR	Resistor connection for gate driver current selection	O
52	VDD	3.3 V power supply output	O
53	DGND	Digital ground	GND
54	VB	Protected battery supply	-
55	NC	Not connected	-
56	BST_L	Boost regulator inductance connection	O
57	NC	Not connected	-
58	BGND	Boost ground	GND
59	NC	Not connected	-
60	BST_C	Boost regulator capacitance connection	I
61	NC	Not connected	-
62	VCAP	Decoupling capacitor for low-side drivers power supply	I
63	NC	Not connected	-
64	VDH	High-side drain voltage sense	I

4 Board layout and views and images

Figure 4. Motherboard front layout

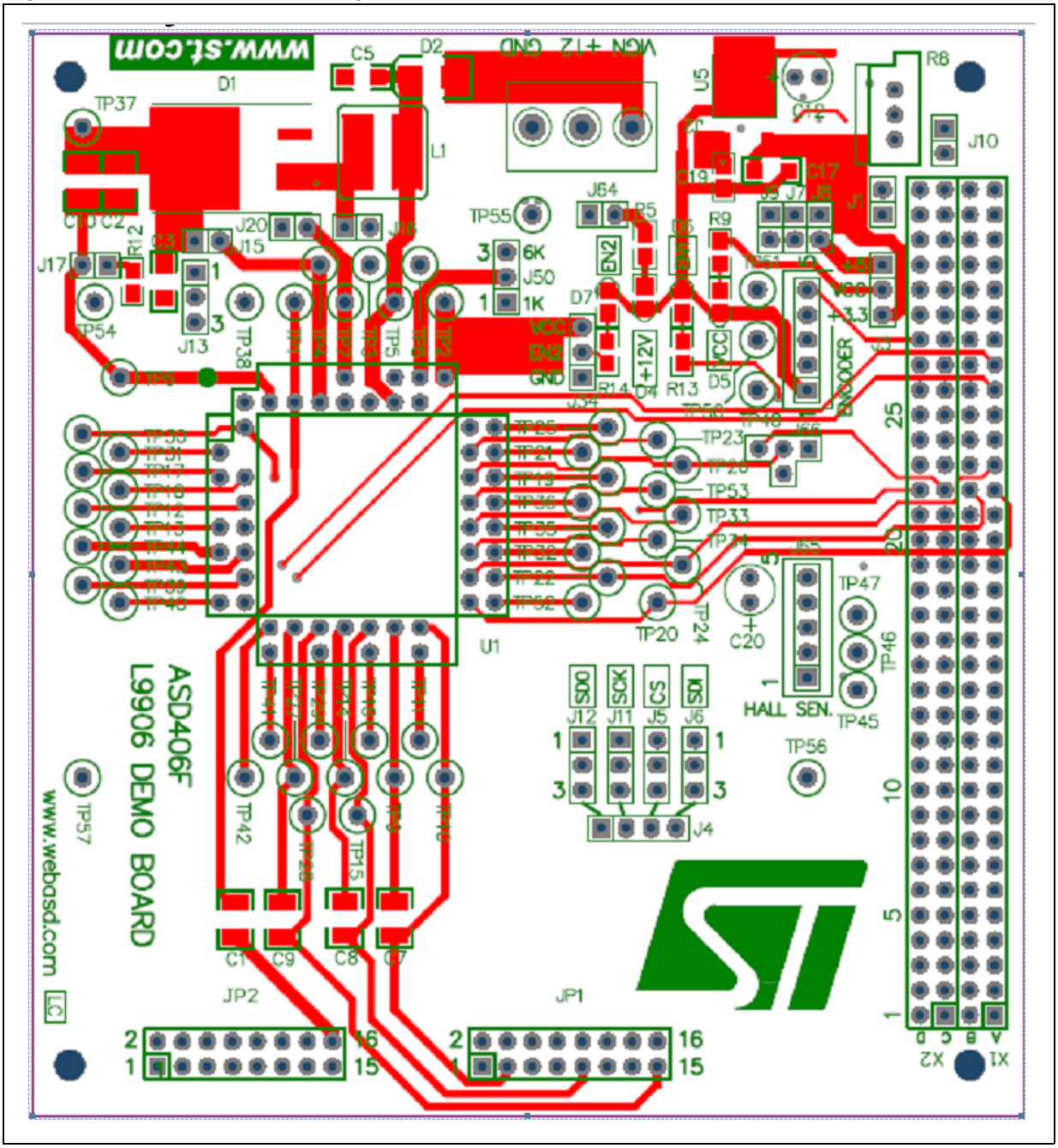


Figure 5. Motherboard back layout

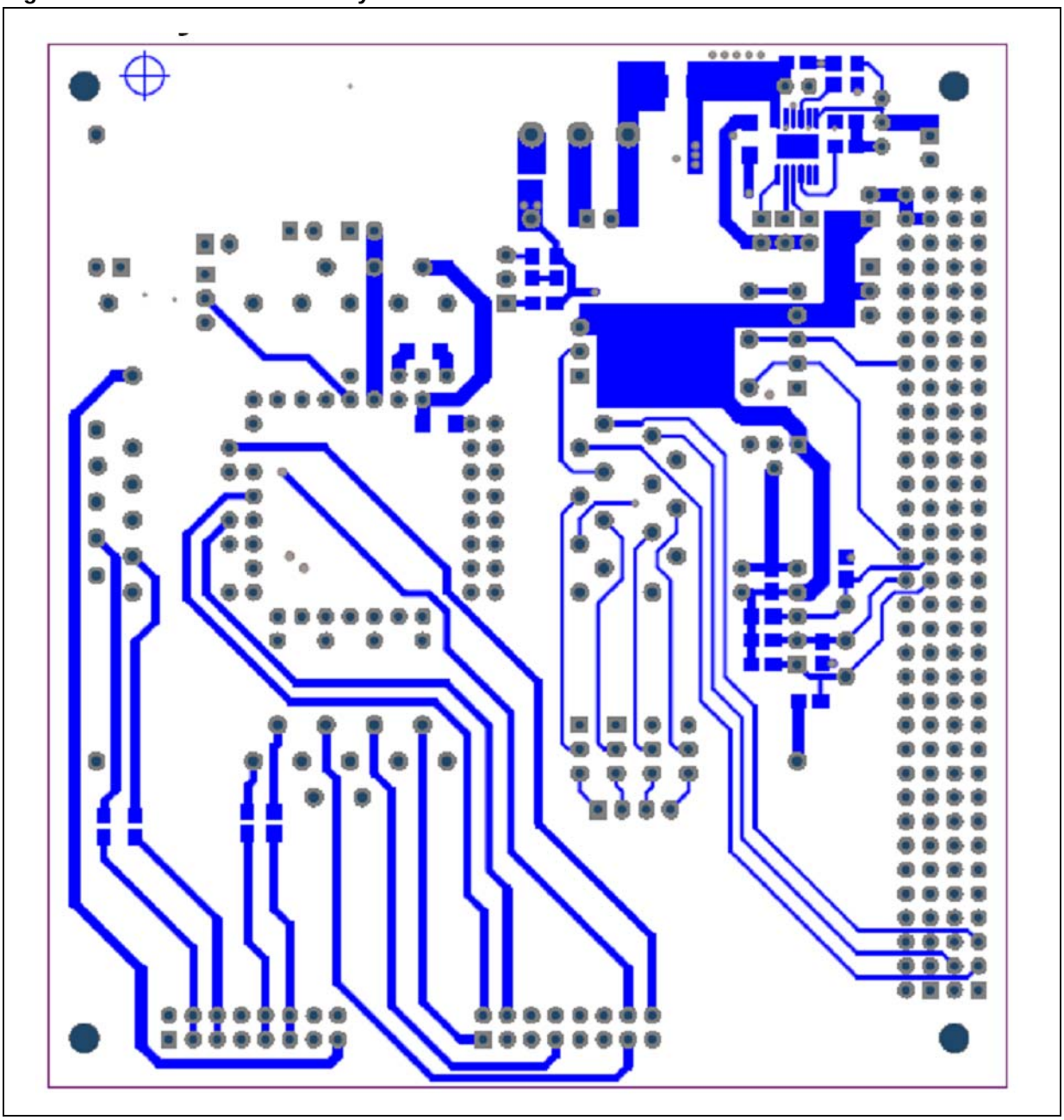


Figure 6. Motherboard front view

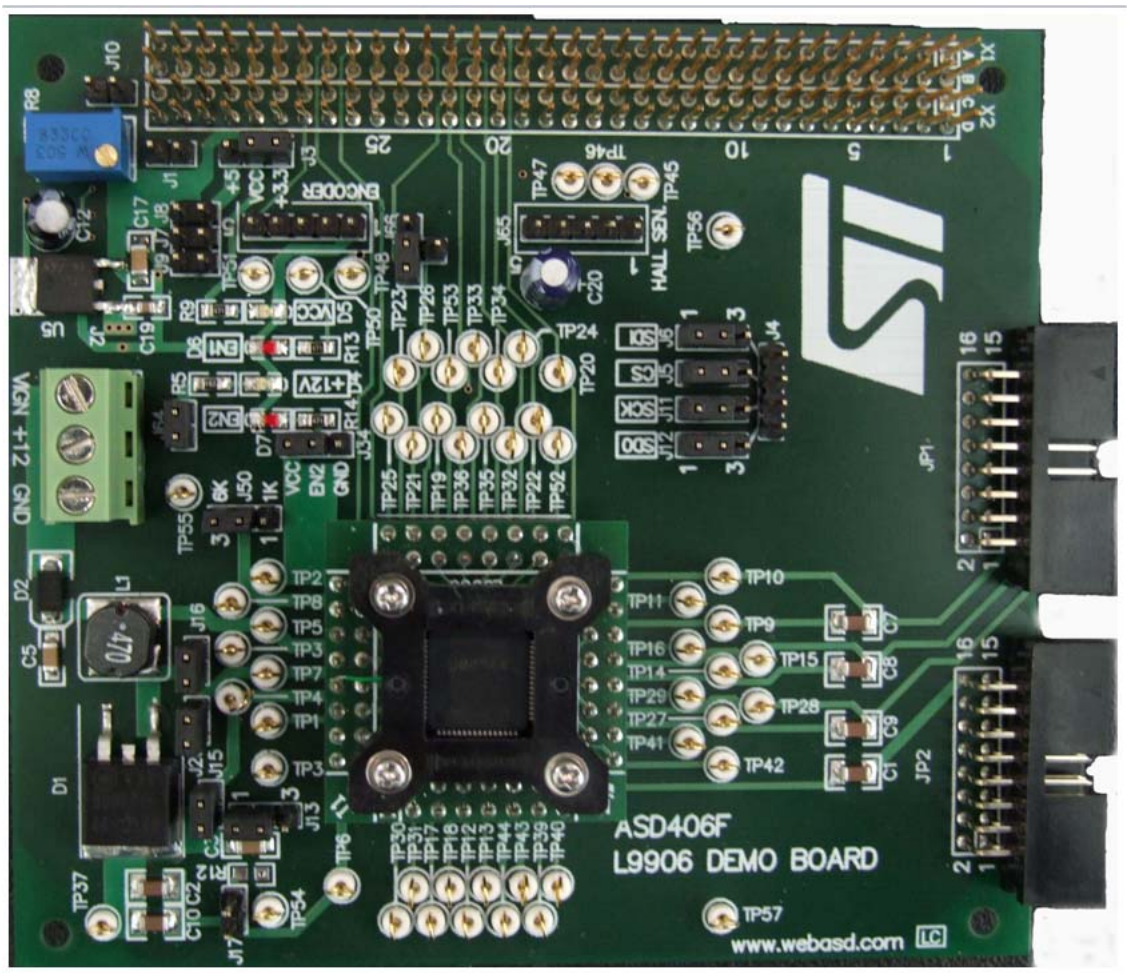


Figure 7. Motherboard back view

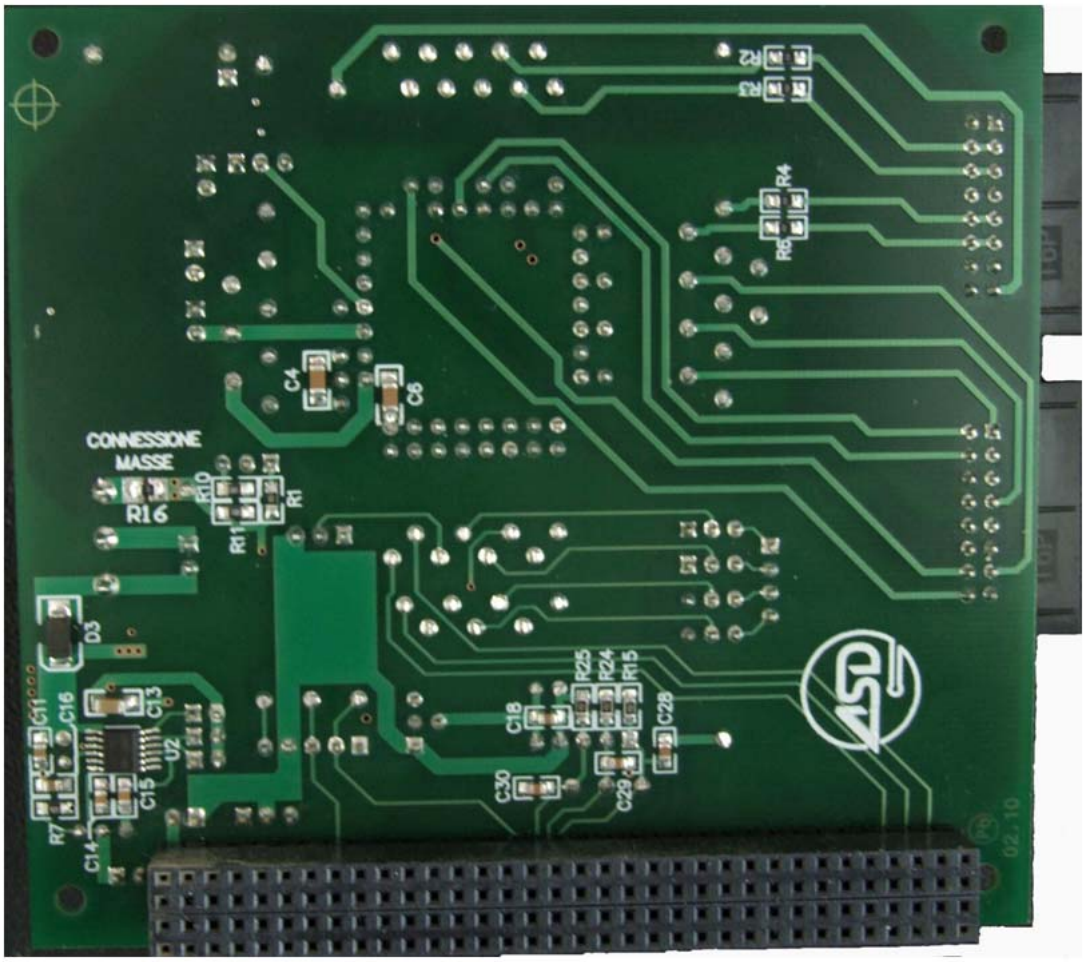


Figure 8. Device daughterboard layout

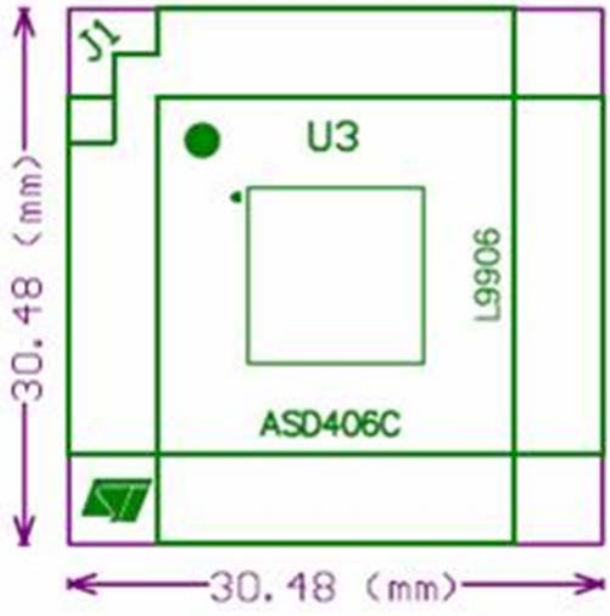


Figure 9. Device daughterboard front view

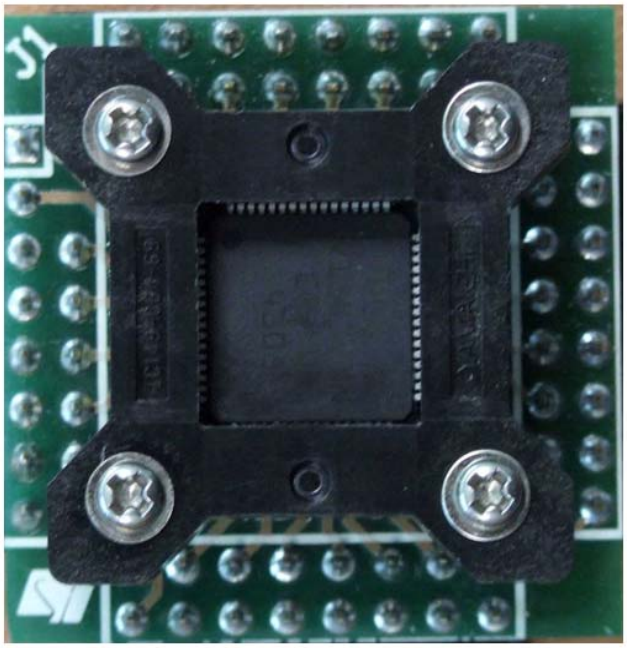


Figure 10. Inverter daughterboard front layout

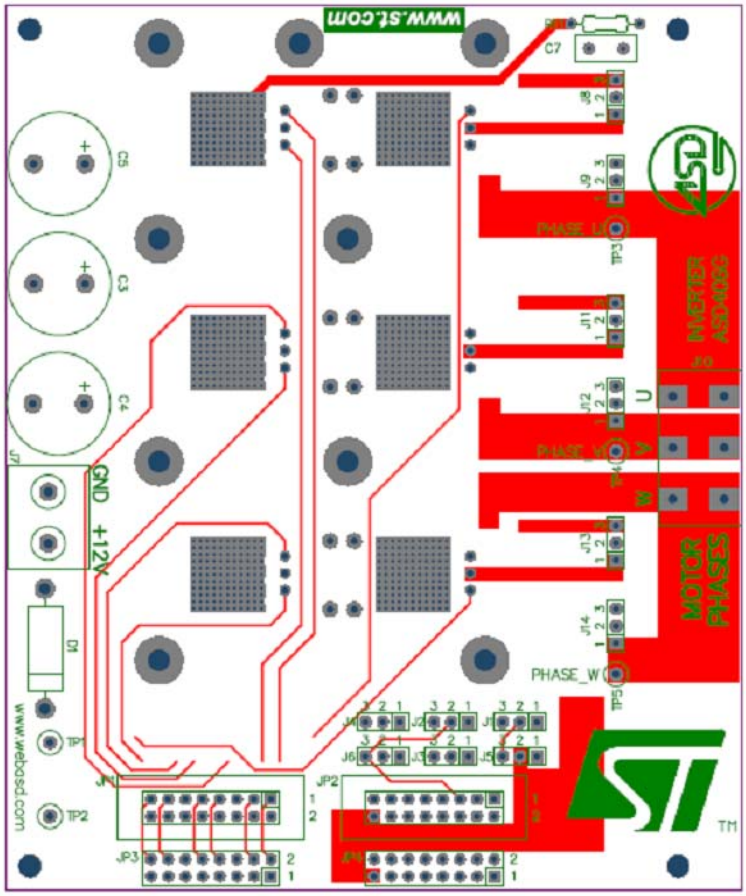


Figure 11. Inverter daughterboard back layout

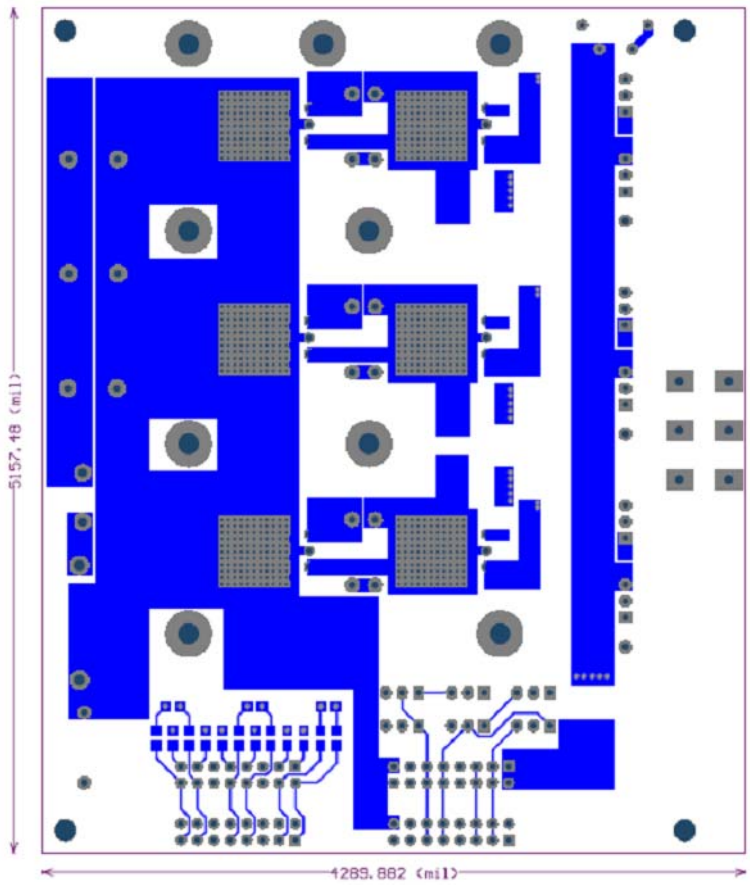


Figure 12. Inverter daughterboard front view

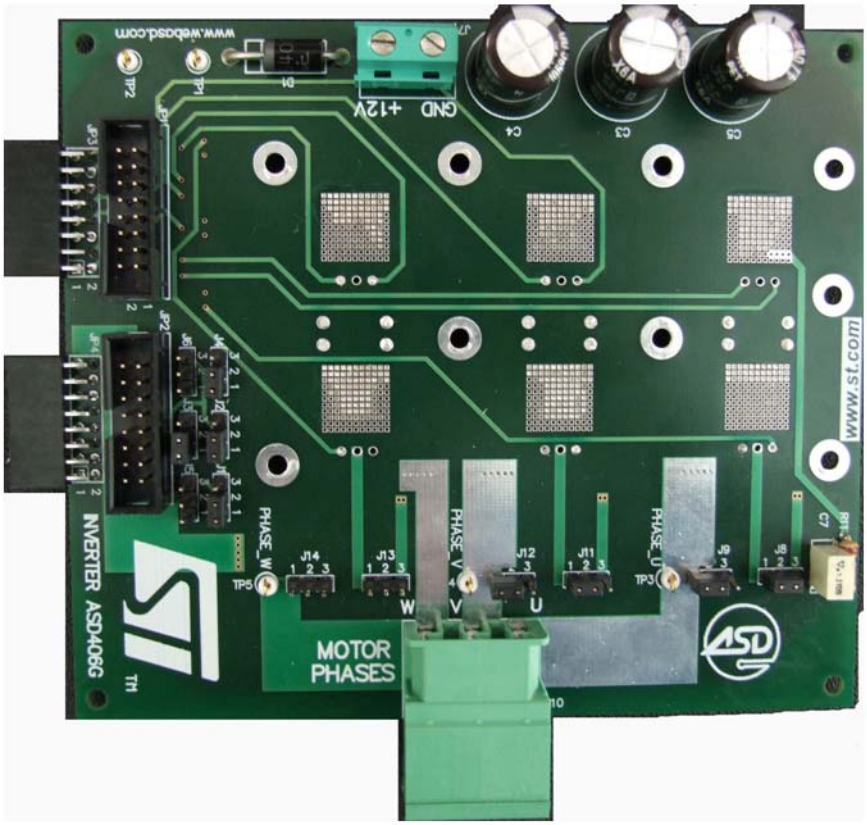
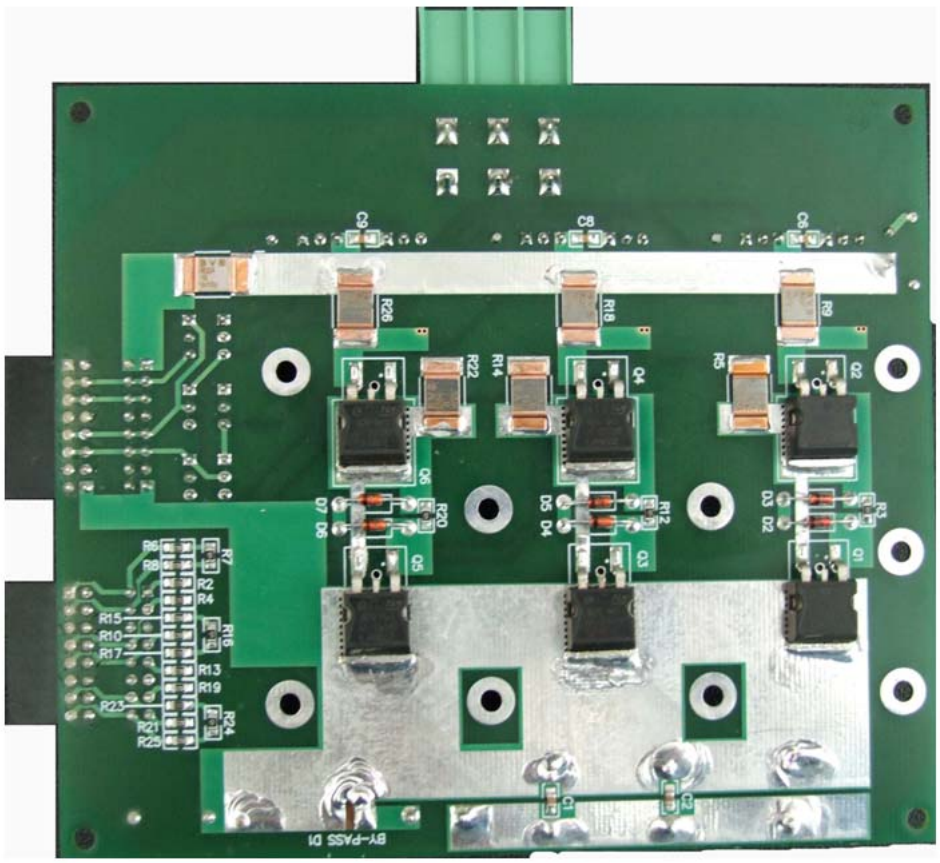
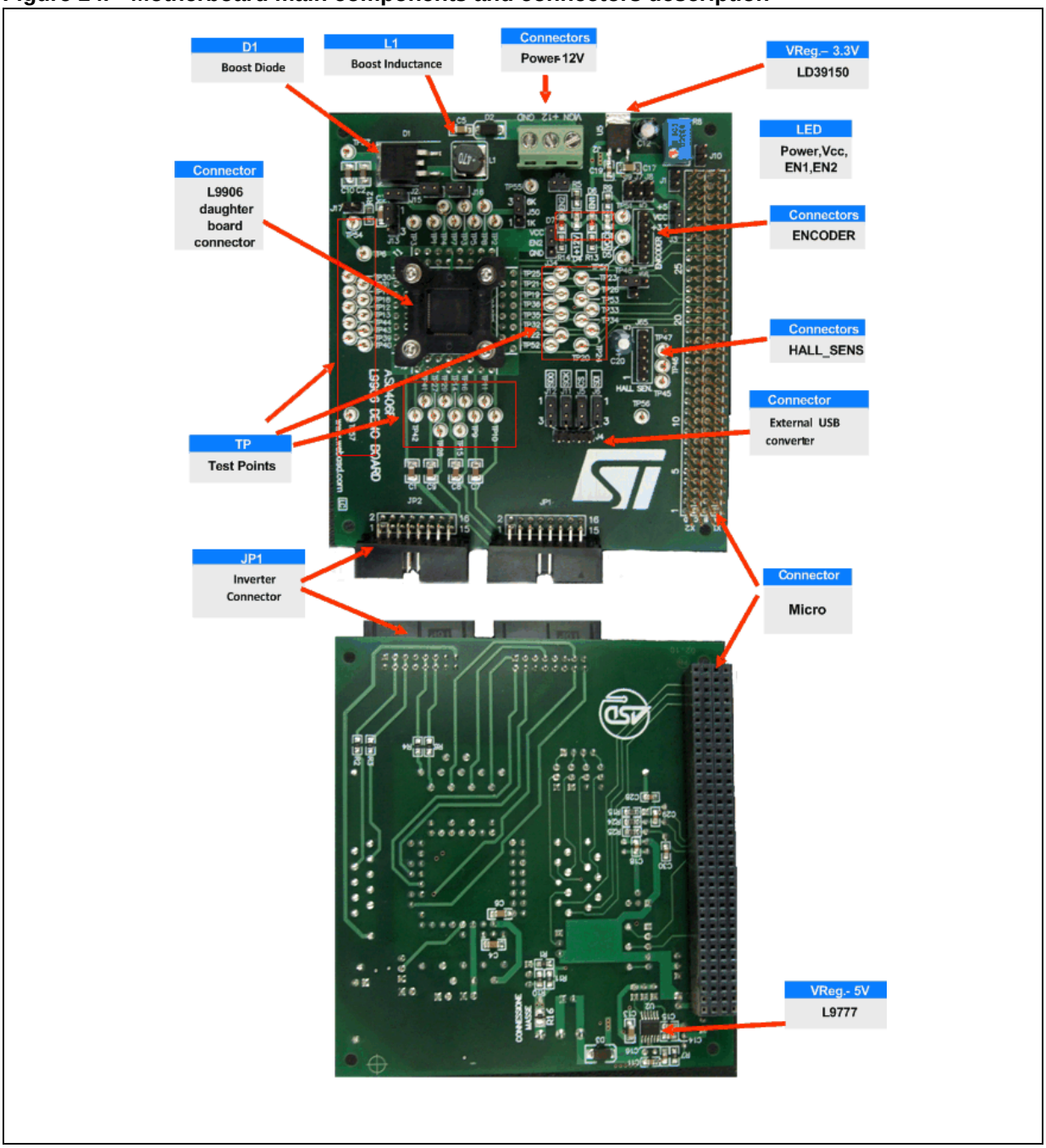


Figure 13. Inverter daughterboard back view



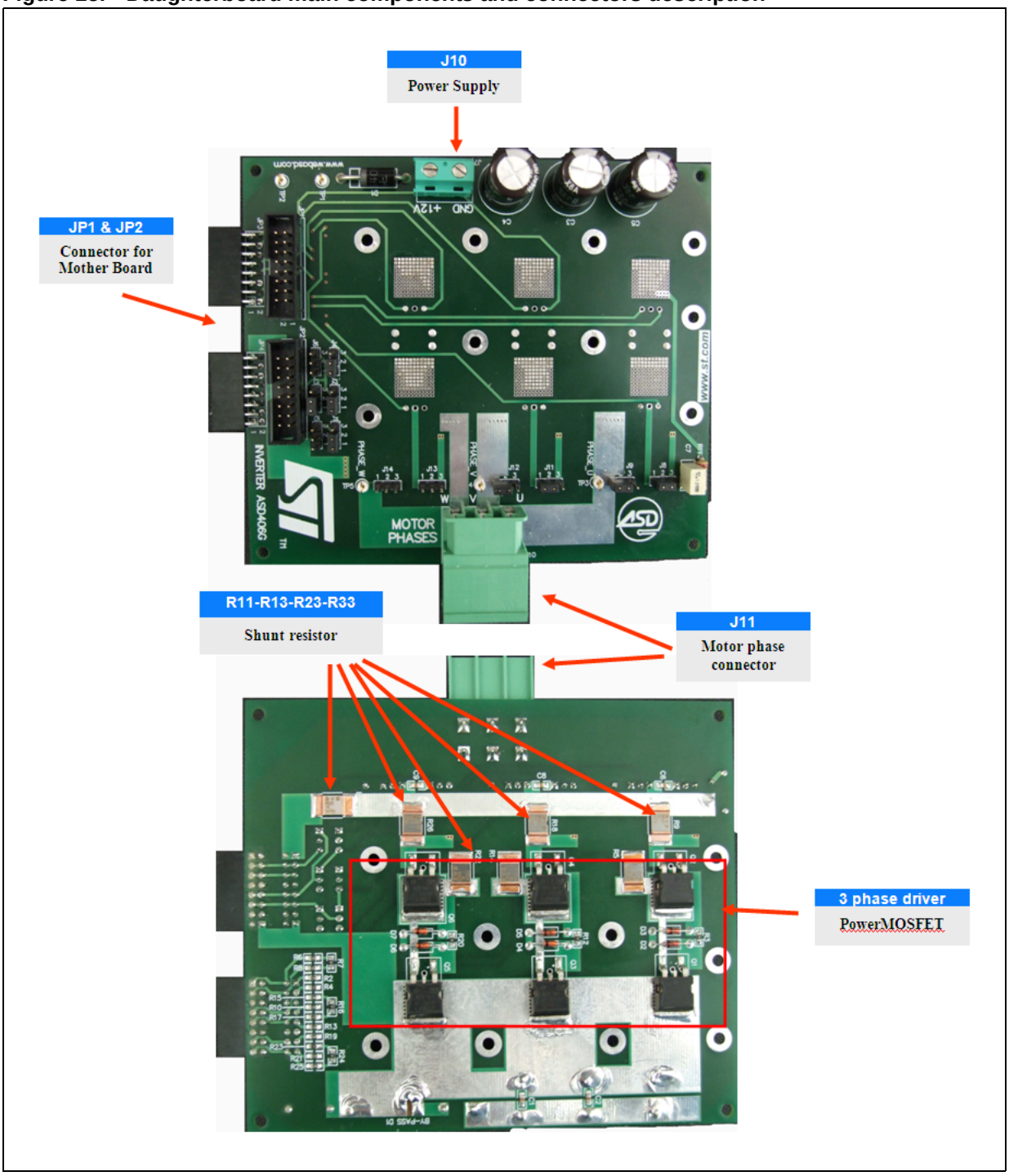
5 Motherboard main components and connectors description

Figure 14. Motherboard main components and connectors description



6 Daughterboard main components and connectors description

Figure 15. Daughterboard main components and connectors description



7 Jumpers and connectors description

7.1 Motherboard jumpers and connectors description

Table 2. Motherboard jumpers and connectors description

Name	Description	Type
J1	V_{CC} source jumper (on = microcontroller, off = J3 conf)	On/off jumper
J2	V_{bat} (ignition switch)	Screw
J3	V_{CC} source jumper (1-2 = 5 V, 2-3 = 3.3 V)	Configurable 2-position jumper
J4	SPI signals connector (CS, SDI, SCK, SDO)	Pins
J5	CS signal source jumper (2-1 = microcontroller, 3-2 = external USB)	Configurable 2-position jumper
J6	SDI signal source jumper (2-1 = microcontroller, 3-2 = external USB)	Configurable 2-position jumper
J7	L9777 WD jumper (on = pin connected, off = pin disconnected)	On/off jumper
J8	L9777 VDD_EN jumper (on = pin connected, off = pin disconnected)	On/off jumper
J9	L9777 WD_EN jumper (on = pin connected, off = pin disconnected)	On/off jumper
J10	L9777 RADJ jumper (on = pin connected to GND, off = pin connected to R8)	On/off jumper
J11	SCK signal source jumper (2-1 = microcontroller, 3-2= external USB)	Configurable 2-position jumper
J12	SDO signal source jumper (2-1 = microcontroller, 3-2= external USB)	Configurable 2 -position jumper
J15	BST_C jumper (on = pin connected, off = pin disconnected)	On/off jumper
J16	BST_L jumper (on = pin connected, off = pin disconnected)	On/off jumper
J20	BGND jumper (on = pin connected, off = pin disconnected)	On/off jumper
J34	EN2 signal source jumper (2-1 = GND, 3-2 = V_{CC})	Configurable 2 position jumper
J50	GCR signal source jumper (2-1 = R1 = 1 KΩ, 3-2 = R10 = 6 KΩ)	Configurable 2 position jumper
J64	Ignition key simulator (on = ignition simulation, off = ignition switch)	On/off jumper
J65	Hall sensor connector	Multipin with guide
J66	Encoder connector	Multipin with guide
JP1	Inverter connector	Multipin with guide

Table 2. Motherboard jumpers and connectors description (continued)

Name	Description	Type
U1	L9906 socket	Multipin
X1	Microcontroller connector	Multipin
X2	Microcontroller connector	Multipin

Figure 16. Microcontroller connector

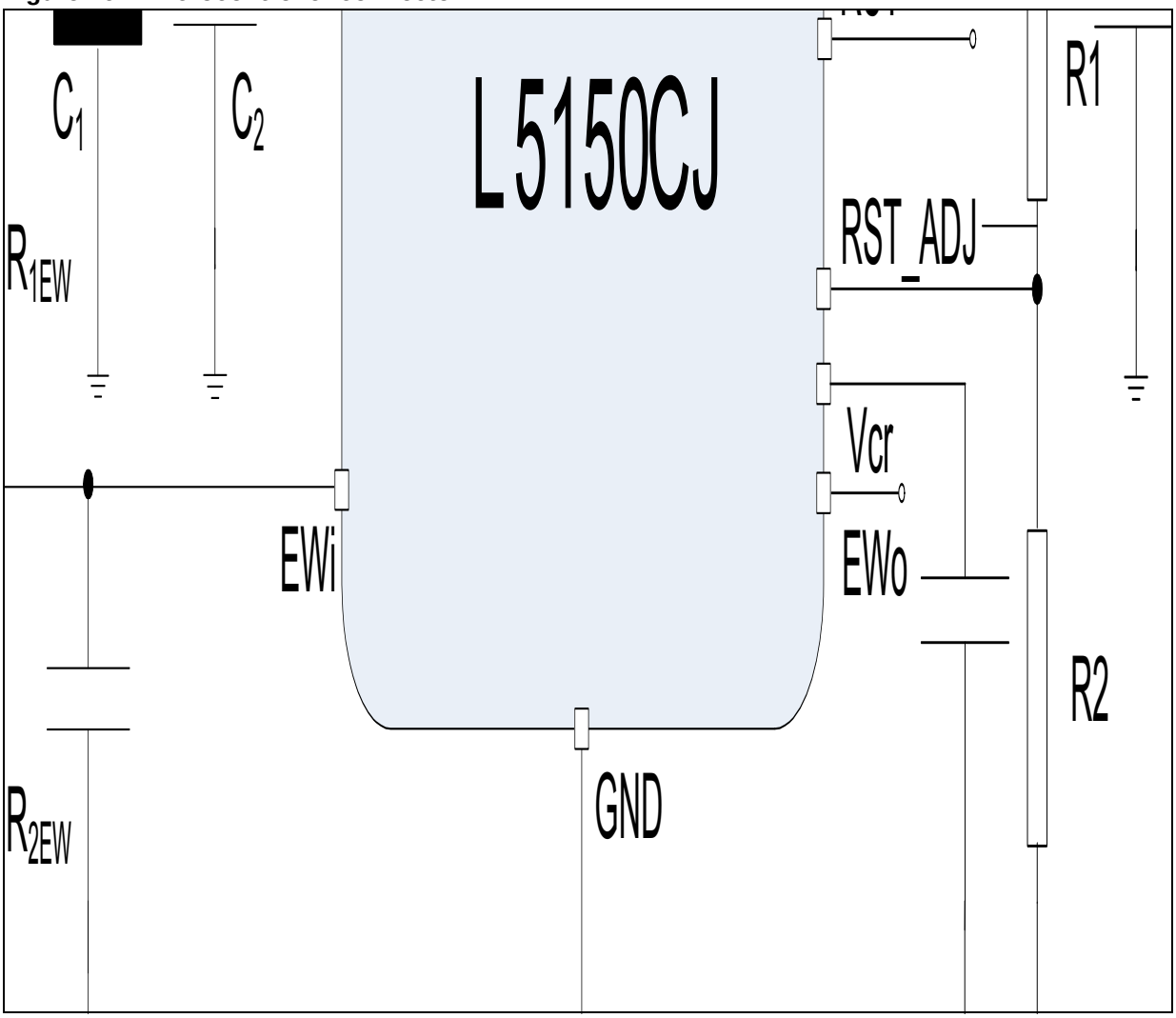
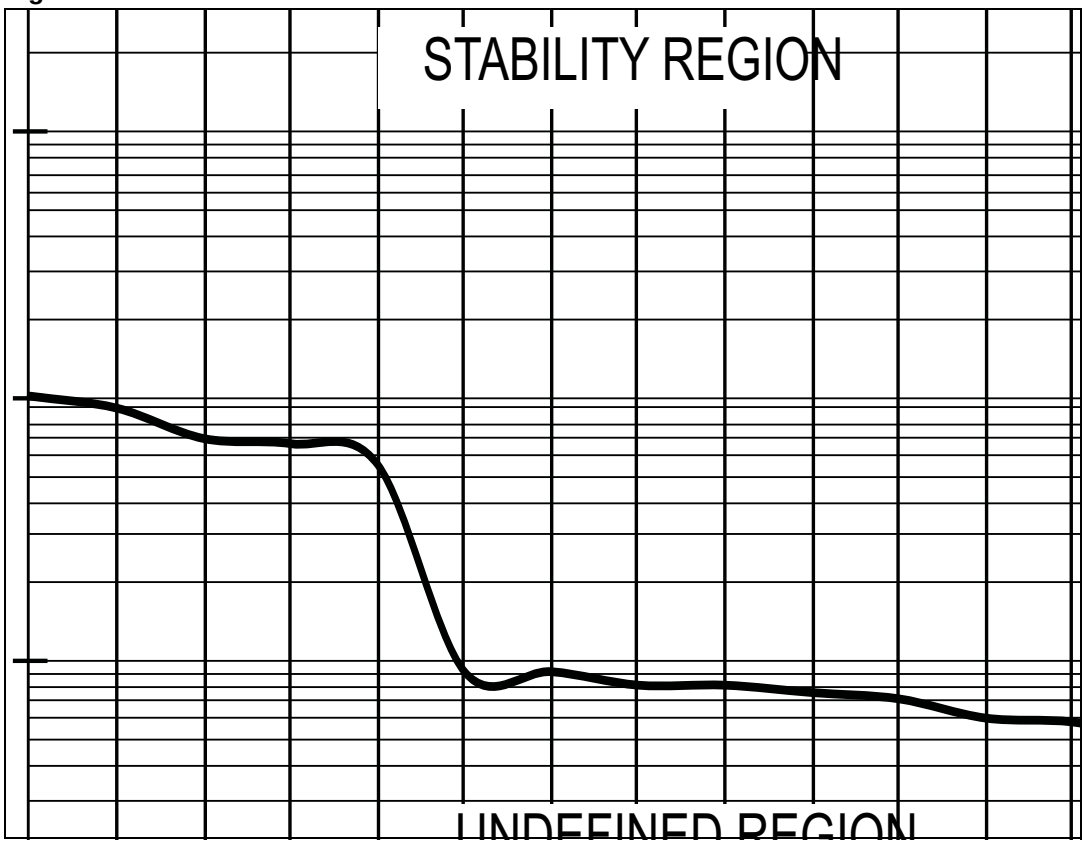


Figure 17. USB connection

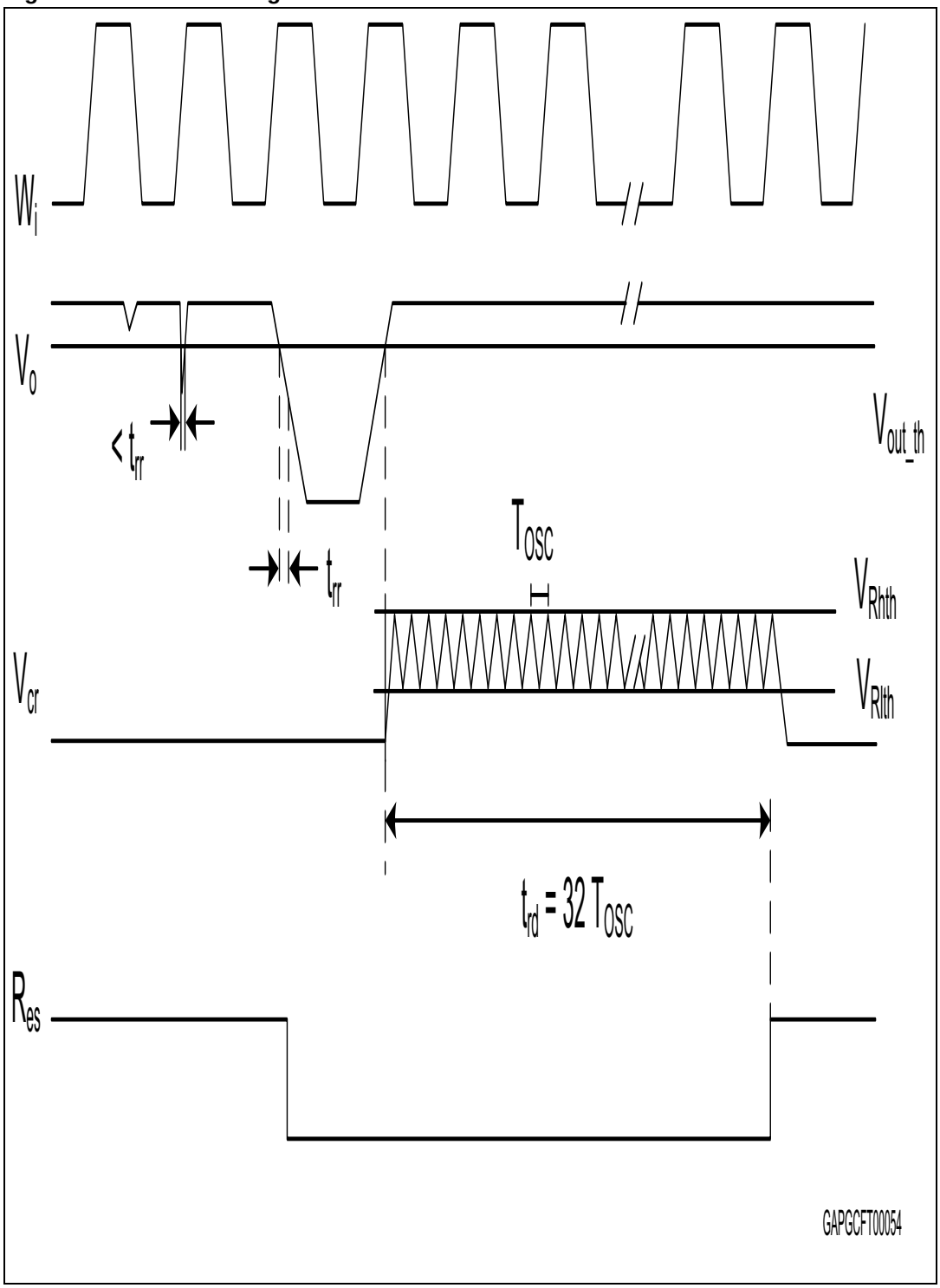


7.2 Inverter daughterboard jumpers and connectors description

Table 3. Inverter daughterboard jumpers and connectors description

Name	Description	Type
J7	Power connector	Screw
J10	Motor phase connector	Screw
JP1	Motherboard male connector for control signals	Multipin with guide
JP2	Motherboard male connector for phase current	Multipin with guide
JP3	Motherboard female connector for control signals	Multipin with guide
JP4	Motherboard female connector for phase current	Multipin with guide
J1,2,3,4,5,6,8,9, 11,12,13,14	Is +/- selector	Configurable 2 position jumper

Figure 18. Inverter daughter connector



8 Test points description

Table 4. Motherboard test points description

TP name	Pin name	Description	I/O type
TP1	VCAP	Decoupling capacitor for power supply of low-side drivers	I
TP2	VCC	5 V / 3.3 V power supply input	I
TP3	BST_L	Boost regulator inductance connection	O
TP4	BST_C	Boost regulator capacitance connection	I
TP5	VB	Protected battery supply	I
TP6	VDH	High-side drain voltage sense	I
TP7	BGND	Boost ground	GND
TP8	VDD	3.3 V Power supply output	O
TP9	CBS_1	Bootstrap capacitor for high-side MOSFET, phase 1	I
TP10	SHS_1	Source connection for high-side MOSFET, phase 1	I
TP11	GHS_1	Gate connection for high-side MOSFET, phase 1	O
TP12	GLS_1	Gate connection for low-side MOSFET, phase 1	O
TP13	SLS_1	Source connection for low-side MOSFET, phase 1	I
TP14	CBS_2	Bootstrap capacitor for high-side MOSFET, phase 2	I
TP15	SHS_2	Source connection for high-side MOSFET, phase 2	I
TP16	GHS_2	Gate connection for high-side MOSFET, phase 2	O
TP17	GLS_2	Gate connection for low-side MOSFET, phase 2	O
TP18	SLS_2	Source connection for low-side MOSFET, phase 2	I
TP19	EN2	Enable input 2 (ANDed with EN1 to enable any gate drive output)	I
TP20	PWM_H1	PWM command input for high-side phase 1	I
TP21	PWM_L1	PWM command input for low-side phase 1	I
TP22	PWM_H2	PWM command input for high-side phase 2	I
TP23	PWM_L2	PWM command input for low-side phase 2	I
TP24	PWM_H3	PWM command input for high-side phase 3	I
TP25	PWM_L3	PWM command input for low-side phase 3	I
TP26	EN1	Enable input 1 (ANDed with EN2 to enable any gate drive output)	EN1 test point
TP27	CBS_3	Bootstrap capacitor for high-side MOSFET, phase 3	Test point
TP28	SHS_3	Source connection for high-side MOSFET, phase 3	I
TP29	GHS_3	Gate connection for high-side MOSFET, phase 3	O
TP30	GLS_3	Gate connection for low-side MOSFET, phase 3	O
TP31	SLS_3	Source connection for low-side MOSFET, phase 3	I
TP32	FS_FLAG	Fault status flag output	O

Table 4. Motherboard test points description (continued)

TP name	Pin name	Description	I/O type
TP33	SI	SPI serial data input	I
TP34	CS	SPI chip select input	I
TP35	SCK	SPI serial clock input	I
TP36	SO	SPI serial data output	O
TP37	VCbst	Boost regulator capacitance voltage	—
TP38	PGND	PGND test point	—
TP39	IB1	Output for current sense amplifier 1 (Test mode digital output #1)	O
TP40	IB2	Output for current sense amplifier 2 (Test mode digital output #2)	O
TP41	IS2-	Negative input for current sense amplifier 2	I
TP42	IS2+	Positive input for current sense amplifier 2	I
TP43	IS1-	Negative input for current sense amplifier 1	I
TP44	IS1+	Positive input for current sense amplifier 1	I
TP45	HALL_1	Hall sensor 1	O
TP46	HALL_2	Hall sensor 2	O
TP47	HALL_3	Hall sensor 3	O
TP48	INDEX	Encoder INDEX	O
TP50	Channel A	Encoder channel A	O
TP51	Channel B	Encoder channel B	O
TP52	TM	Test mode enable input	I
TP53	TO3	Test output	—
TP54	GND	Ground	—
TP55	GND	Ground	—
TP56	GND	Ground	—
TP57	GND	Ground	—

Table 5. Inverter daughterboard test points description

TP Name	Pin Name	Description	I/O type
TP1	—	V_{bat}	I
TP2	—	GND	I
TP3	—	Phase A	I
TP4	—	Phase B	I
TP5	—	Phase C	I

9 Functional description

9.1 Jumper setting using external USB interface for SPI communication

In order to use an external USB interface for SPI communication, the configurable jumpers must be set as indicated in *Table 6*, while all the ON/OFF jumpers type must be ON.

Table 6. Configuration jumpers using external USB interface for SPI

Name	Description	Configuration
J5	CS signal source jumper	3-2
J6	SDI signal source jumper	3-2
J11	SCK signal source jumper	3-2
J12	SDO signal source jumper	3-2
J34	EN2 signal source jumper	3-2 or 2-1(1)
J50	GCR signal source jumper	3-2 or 2-1(2)

1. 2-1 = GND device disabled; 3-2 = V_{CC} device enabled
2. Depending on selected current for gate driver (refer to table Igxx_1/Igxx_2 in device data sheet) setting using microcontroller interface

9.2 Jumper setting using microcontroller interface

In order to use the microcontroller interface for the SPI communication, the configurable jumpers must be set as indicated in *Table 7*, while all the ON/OFF jumpers type must be ON.

Table 7. Configuration jumpers using microcontroller interface for SPI

Name	Description	Configuration
J5	CS Signal source jumper	2-1
J6	SDI Signal source jumper	2-1
J11	SCK Signal source jumper	2-1
J12	SDO Signal source jumper	2-1
J34	EN2 Signal source jumper	3-2 or 2-1(1)
J50	GCR Signal source jumper	3-2 or 2-1(2)

1. 2-1 = GND device disabled; 3-2 = V_{CC} device enabled
2. Depending on selected current for gate driver (refer to table Igxx_1/Igxx_2 in device data sheet)

9.3 Notes at start up

9.3.1 Start up for V_{CC} = 3.3 V

Procedure:

- Set one of the two EN pin to zero by manually changing the jumper configuration of EN2 (J34) or setting EN1 by a microcontroller command
- Apply the V_{bat} and V_{CC}
- Send the SPI frame 0x8000- diagnostic
- Set EN to high (previously set to '0')
- Apply control signal.

9.3.2 Start up for V_{CC} = 5 V

The power-up default value for V_{CC} overvoltage threshold is “10”, corresponding to a V_{CC} = 3.3 V application. Therefore, use the following procedure.

- Set one of the two EN pins to zero by either manually changing the jumper configuration of EN2 (J34) or use a microcontroller command to set EN1.
- Apply the V_{bat} and V_{CC}
- Send this SPI frame in order to reset the fault[(a)]: 0x3409 (0011010000001001)
- Send the SPI frame 0x8000 (1000000000000000) - diagnostic
- Set EN to high (previously set to '0')
- Apply control signal

9.3.3 BOOST check

The BOOST functionality can be verified by measuring the output voltage on pin 60 (BST_C—test point 4). The value should be approximately +10 V with respect to the battery VB.

In general, it is recommended to check the logic level of pin 37 (test point 32) (FS_FLAG, low if any fault is latched) and read out the status of DIAG register to determine the kind of faults reported.

a. The fault is due to the default Power up value that corresponding to V_{CC} = 3.3 V application (for reference, see the SPI bitmap in the device datasheet).

9.4 Notes for current sensing setup

The power board has been designed to give the possibility to choose any combination of current sensing to use as input for the two Operational Amplifier of the L9906.

In *Table 8* are reported all the possible combinations.

Table 8. Jumper setup for the possible combination of current sensing

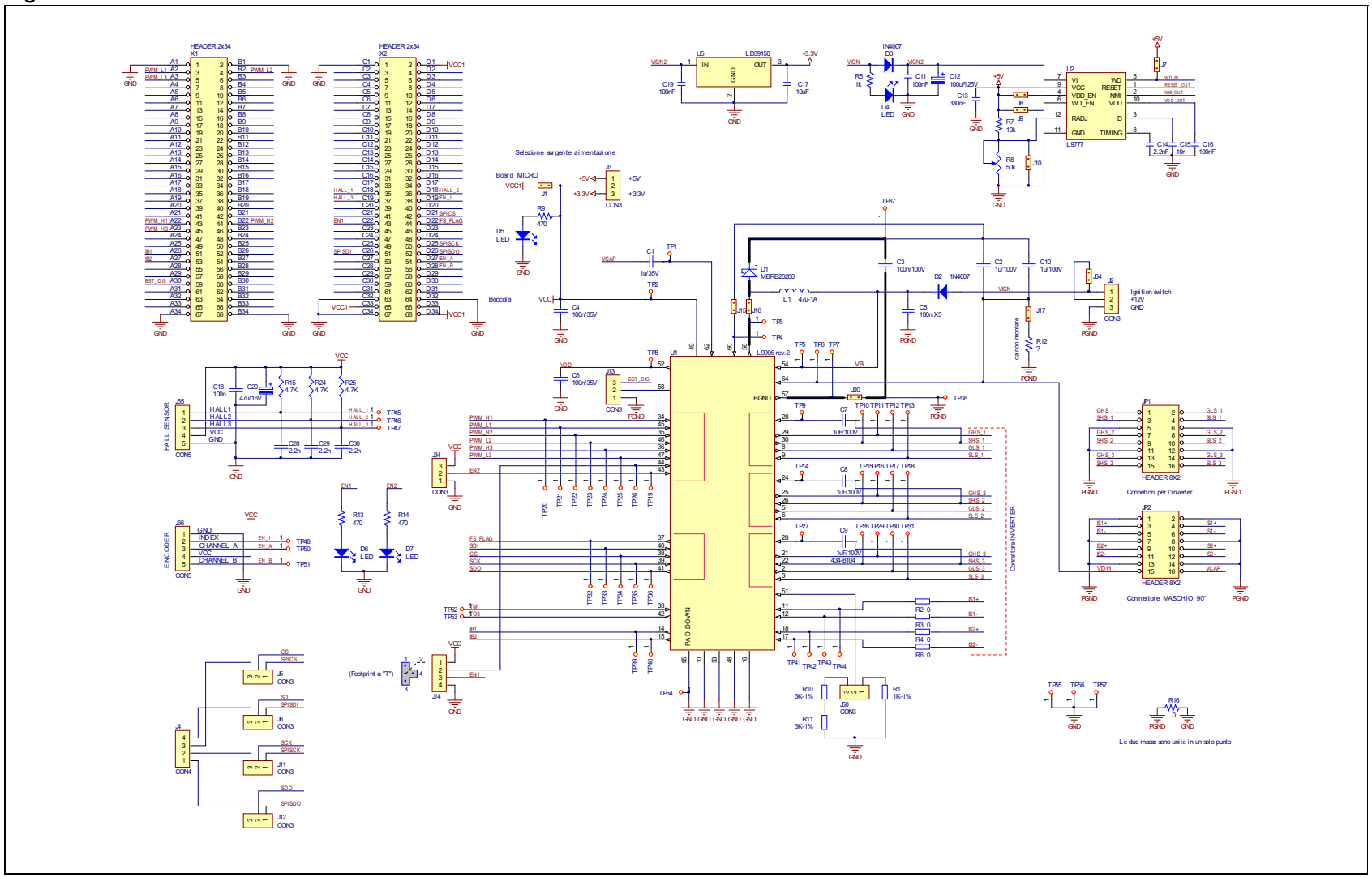
IS1 source selector		IS2 source selector		R1 DC link selector		R5/R9 PhaseU or Brench U selector		R14/R18 PhaseV or Brench V selector		R22/R26 Phase W or BrenchW selector		Is1+ output	Is1- output	Is2+ output	Is2- output
IS1+	IS1-	IS2+	IS2-	DC		U		V		W					
J1	J2	J3	J4	J5	J6	J8	J9	J11	J12	J13	J14				
1-2	1-2	1-2	1-2	off	off	1-2	1-2	1-2	1-2	off	off	PhaseU+	PhaseU-	PhaseV+	PhaseV-
1-2	1-2	2-3	2-3	off	off	1-2	1-2	off	off	1-2	1-2	PhaseU+	PhaseU-	PhaseW+	PhaseW-
1-2	1-2	off	off	1-2	1-2	1-2	1-2	off	off	off	off	PhaseU+	PhaseU-	Tot	Tot
2-3	2-3	2-3	2-3	off	off	off	off	1-2	1-2	1-2	1-2	PhaseV+	PhaseV-	PhaseW+	PhaseW-
2-3	2-3	off	off	1-2	1-2	off	off	1-2	1-2	off	off	PhaseV+	PhaseV-	Tot	Tot
off	off	1-2	1-2	2-3	2-3	off	off	1-2	1-2	off	off	Tot	Tot	PhaseV+	PhaseV-
off	off	2-3	2-3	2-3	2-3	off	off	off	off	1-2	1-2	Tot	Tot	PhaseW+	PhaseW-
1-2	1-2	1-2	1-2	off	off	2-3	2-3	2-3	2-3	off	off	BranchU+	BranchU-	BranchV+	BranchV-
1-2	1-2	2-3	2-3	off	off	2-3	2-3	off	off	2-3	2-3	BranchU+	BranchU-	BranchW+	BranchW-
1-2	1-2	off	off	1-2	1-2	2-3	2-3	off	off	off	off	BranchU+	BranchU-	Tot	Tot
2-3	2-3	2-3	2-3	off	off	off	off	2-3	2-3	2-3	2-3	BranchV+	BranchV-	BranchW+	BranchW-
2-3	2-3	off	off	1-2	1-2	off	off	2-3	2-3	off	off	BranchV+	BranchV-	Tot	Tot
off	off	1-2	1-2	2-3	2-3	off	off	2-3	2-3	off	off	Tot	Tot	BranchV+	BranchV-
off	off	2-3	2-3	2-3	2-3	off	off	off	off	2-3	2-3	Tot	Tot	BranchW+	BranchW-
1-2	1-2	1-2	1-2	off	off	1-2	1-2	2-3	2-3	off	off	PhaseU+	PhaseU-	BranchV-	BranchV+
1-2	1-2	2-3	2-3	off	off	1-2	1-2	off	off	2-3	2-3	PhaseU+	PhaseU-	BranchW-	BranchW+
1-2	1-2	1-2	1-2	off	off	2-3	2-3	1-2	1-2	off	off	PhaseV+	PhaseV-	BranchU-	BranchU+
2-3	2-3	2-3	2-3	off	off	off	off	1-2	1-2	2-3	2-3	PhaseV+	PhaseV-	BranchW-	BranchW+

Table 8. Jumper setup for the possible combination of current sensing (continued)

IS1 source selector		IS2 source selector		R1 DC link selector		R5/R9 PhaseU or Brench U selector		R14/R18 PhaseV or Brench V selector		R22/R26 Phase W or BrenchW selector		Is1+ output	Is1- output	Is2+ output	Is2- output
1-2	1-2	2-3	2-3	off	off	2-3	2-3	off	off	1-2	1-2	PhaseW+	PhaseW-	BranchU-	BranchU+
2-3	2-3	2-3	2-3	off	off	off	off	2-3	2-3	1-2	1-2	PhaseW+	PhaseW-	BranchV-	BranchV+

Appendix A Motherboard schematic

Figure 19. Motherboard schematic



A.1 Motherboard BOM (bill of materials

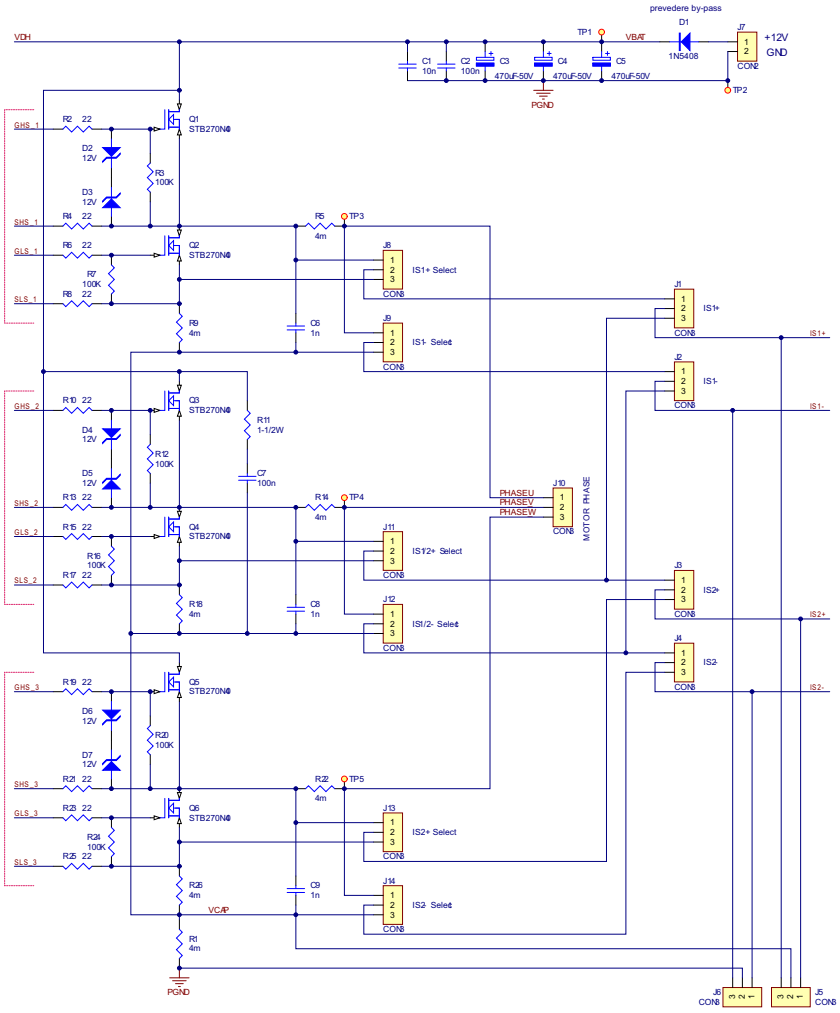
Table 9. Motherboard BOM

Comment	Description	Designator	Footprint	LibRef	Quantity
1 µF/35 V	Capacitor	C1	1210	CAP	1
1 µ/F100 V	Capacitor	C2, C10	1210	CAP	2
100 nF/100 V	Capacitor	C3	1206	CAP	1
100 nF/35 V	Capacitor	C4, C6	1206	CAP	2
100 n X5	Capacitor	C5	1206	CAP	1
1 µF/100 V	Capacitor	C7, C8, C9	1210	CAP	3
100 nF		C11, C16, C19	0805	C	3
100 µF/25 V	Electrolytic capacitor	C12	RB.1/.2	COND EL	1
330 nF		C13	1206	C	1
2.2 nF		C14	0805	C	1
10 nF		C15	0805	C	1
10 µF		C17	1206	C	1
100 nF	Capacitor	C18	0805	CAP	1
47 µF/16 V	Low-side electrolytic capacitor	C20	RB.1/.2	COND EL	1
2.2 nF	Capacitor	C28, C29, C30	0805	CAP	3
MBRB20200	Dual diode schottky	D1	SIP-G3/E14	MBRB20200	1
1N4007	Diode	D2, D3	do-214aa	1N4007	2
LED	LED diode	D4, D5, D6, D7	0805 LED	LED	4
JUMP1	JUMP 2POLI	J1, J7, J8, J9, J10, J15, J16, J20, J64	SIP2	JAMP1	9
CON3		J2	CON3	CON3	1
		J3, J5, J6, J11, J12, J34, J50	SIP3	CON3	7
CON4		J4	SIP4	CON4	1
CON5	5-pin connector - AMPEX model	J65, J66	SIP5	CON5	2
HEADER 17X2		JP1	IDC34	HEADER 17X2	1
47 µH-1 A		L1	WE-PD2 744775147INDUCTOR1		1
1kΩ -1%	Resistor	R1	0805	Res2	1
0	Resistor	R2, R3, R4, R6, R16	0805	R, Res2	5

Table 9. Motherboard BOM (continued)

Comment	Description	Designator	Footprint	LibRef	Quantity
1 kΩ		R5	0805	R	1
10 kΩ		R7	0805	R	1
50 kΩ		R8	VR5	POT	1
470 Ω		R9, R13, R14	0805	R	3
3 kΩ-1%	Resistor	R10, R11	0805	Res2	2
4.7 kΩ	Resistor	R15, R24, R25	0805	RES1	3
TEST POINT	Test point	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20, TP21, TP22, TP23, TP24, TP25, TP26, TP27, TP28, TP29, TP30, TP31, TP32, TP33, TP34, TP35, TP36, TP37, TP38, TP39, TP40, TP41, TP42, TP43, TP44, TP45, TP46, TP47, TP48, TP50, TP51, TP52, TP53, TP54,TP55, TP56, TP57	TEST POINT	TEST POINT	56
L9906	3-phase motor control	U1	QFP-64 ASD ADAPTER	L9906	1
L9777		U2	PWSSO12	L9777	1
LD39150	3.3 V low dropout voltage regulator	U5	TO-252 (DPAK)	LD39150	1
HEADER 2x34		X1, X2	IDC68	HEADER 34X2	2

Appendix B Inverter daughterboard schematic

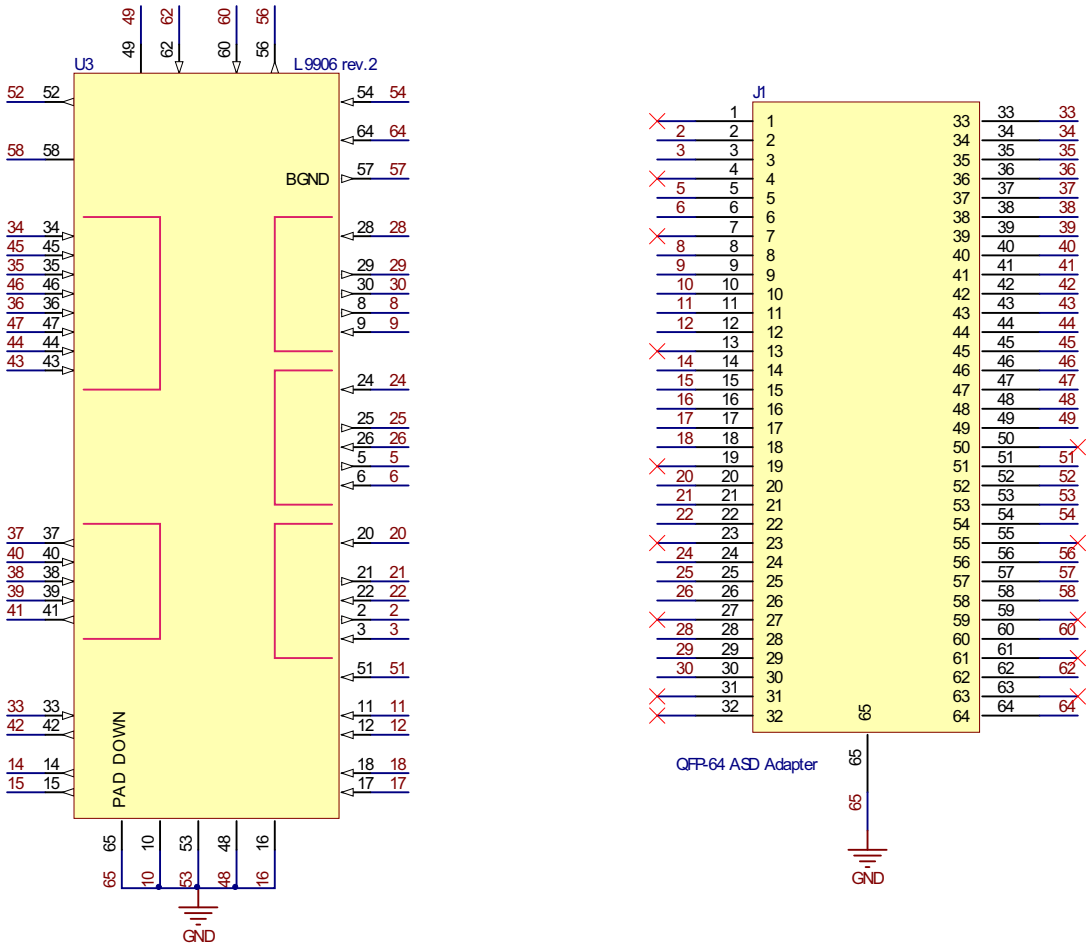


B.1 Inverter daughterboard BOM

Table 10. Inverter daughterboard BOM

Comment	Description	Designator	Footprint	LibRef	Quantity
10 nF	Capacitor	C1	0805	CAP	1
100 nF	Capacitor	C2	0805	CAP	1
470 µF, 50V	Low-side electrolytic capacitor	C5, C52, C56	RB.3/.6	COND EL	3
1nF	Capacitor	C8, C10, C11	0805	CAP	3
100 nF	Capacitor	C9	RAD0.2	CAP	1
CON2	7.62 mm pitch connector	J10	GMKDS 3/2-7.62	CON2	1
CON3	7.62 mm pitch board-to-board connector (RS)	J11	POWER COMBICO 3/7.62	CON3	1
HEADER 17X2		JP1, JP2	IDC34	HEADER 17X2	2
STB270N04		Q1, Q2, Q3, Q4, Q5, Q6	D2PAK STB	MOSFET N	6
4 m	Resistor	R11, R13, R23, R33	BVS	RES1	4
1-1/2 W	Resistor	R21	AXIAL0.4	RES1	1
TEST POINT	Test Point	TP1, TP2, TP3, TP4	TEST POINT	TEST POINT	5

Appendix C Device daughterboard schematic



C.1 Device daughterboard BOM

Table 11. Device daughterboard BOM

Comment	Description	Designator	Footprint	LibRef	Quantity
QFP-64 ASD adapter	QFP-64 ASD adapter	J1	QFP-64 ASD adapter	QFP-64 ASD adapter	1
L9906	3-phase motor control	U3	t-qfp64 (10x10x1.0)	L9906	1

Revision history

Table 12. Document revision history

Date	Revision	Changes
17-Sep-2009	1	Initial release.
04-Jul-2011	2	Removed Section 10 and Section 11. Added Section 9.4.
19-Sep-2013	3	Updated disclaimer.

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