ADBS-A320

Optical Finger Navigation

Data Sheet

Description

The ADBS-A320 sensor is a small form factor (SFF) LED illuminated optical finger navigation system.

The ADBS-A320 is a low-power optical finger navigation sensor. It has a new, low-power architecture and automatic power management modes, making it ideal for battery- and power-sensitive applications such as mobile phones.

The ADBS-A320 is capable of high-speed motion detection – up to 15ips. In addition, it has an on-chip oscillator and integrated LED to minimize external components.

There are no moving parts which means high reliability and less maintenance for the end user. In addition, precision optical alignment is not required, facilitating high volume assembly.

The sensor is programmed via registers through either a serial peripheral interface or a two wire interface port. It is packaged in a 28 I/O surface mountable package.

The ADBS-A320 is designed for use with ADBL-A321 lens. The ADBL-A321 lens is the optical component necessary for proper operation of the sensor.

Theory of Operation

The ADBS-A320 is based on Optical Finger Navigation (OFN) Technology, which measures changes in position by optically acquiring sequential surface images (frames) and mathematically determining the direction and magnitude of movement.

The ADBS-A320 contains an Image Acquisition System (IAS), a Digital Signal Processor (DSP), and a communication system.

The IAS acquires microscopic surface images via the lens and illumination system. These images are processed by the DSP to determine the direction and distance of motion. The DSP calculates the Δx and Δy relative displacement values.

The host reads the Δx and Δy information from the sensor serial port if a motion interrupt is published. The microcontroller then translates the data into cursor navigation, rocker switch, scrolling or other system dependent navigation data.

Features

- Low power architecture
- Surface mount technology (SMT) device
- Self-adjusting power-saving modes for longer battery life
- High speed motion detection up to 15ips
- Self-adjusting frame rate for optimum performance
- Motion detect pin output
- Finger detect pin output
- Internal oscillator – no clock input needed
- Selectable 250, 500, 750, 1000 and 1250 cpi resolution
- Dual 2.8V/1.8V or single 2.8V supply options
- Selectable Input/Output voltage at 2.8V or 1.8V nominal
- Serial peripheral interface (SPI) or Two wire interface (TWI)
- Integrated chip-on-board LED with wavelength of 870nm

Applications

- Finger input devices
- Mobile devices
- Integrated input devices
- Battery-powered input device

Avago customers purchasing the ADBS-A320 OFN product are eligible to receive a royalty free license to our US patents 6977645, 6621483, 6950094, 6172354 and 7289649, for use in their end products.

***CAUTION:** It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

Pinout of ADBS-A320 Optical Sensor

Pin	Name	Description	Input/Output pin	Function
1	GND	Ground		
2	XY_LED	XY LED driver connection		Must connect to LED- (see schematics fig 7a,7b)
3	MOTION	Motion Detect (active low output)	O (CMOS output)	Open when not used Default active low signal, can be changed in Motion_Control register 0x1d
4	GPIO	General Purpose Input / Output for FPD function	O (CMOS output)	Pin indicate Finger Presence Detection, OFN engine 0x60 must be enabled (see application note OFN A320 firmware design guide). Open when not used
5	VDDIO	Voltage supply for I/O		Sets I/O voltage but not for nDREG_EN
6	IO_MOSI_A0	TWI address set or Master Out Slave In	I (Schmitt trigger input)	SPI : MOSI (Master Out Slave In) signal TWI : address select 0 Open when not used
7	IO_CLK	Serial clock input	I (Schmitt trigger input)	Serial clock signal
8	IO_MISO_SDA	TWI serial data or Master In Slave Out	In SPI – CMOS output. In TWI – open drain I/O	SPI : MISO (Master Input Slave Out) signal TWI : serial data signal
9	IO_NCS_A1	TWI address set or Chip Select	I (Schmitt trigger input)	SPI : NCS (chip select) signal TWI : address select 1 Open when not used Active low signal
10	NRST	Hardware Chip Reset	I (Schmitt trigger input)	Set to high when not used Active low signal
11	GND	Ground		
12	ORIENT	Sensor orientation input	I (Schmitt trigger input)	Set to high when not used
13	SHTDWN	Shutdown (active high input)	I (Schmitt trigger input)	Set to low when not used Active high signal
14	VDDIO	Voltage supply for I/O		Sets I/O voltage but not for nDREG_EN
15	IO_SELECT	SPI / TWI Select	I (Schmitt trigger input)	TWI : GND or SPI : High
16	DVDD	Digital Supply voltage or Regulator Output voltage		In regulator disabled, supply 1.8V. In regulator enabled, do not supply 1.8V.
17	nDREG_EN	Digital Regulator enable signal	I (Schmitt trigger input)	Tie to VDDA to disable internal regulator or GND to supply 1.8V to DVDD
18	NC	No Connect		No Connection
19	NC	No Connect		No Connection
20	VDDA	Analog Voltage input		
21	GND	Ground		
22	GND	Ground		
23	NC	No Connect		No connection
24	LED-	LED Cathode		Must connect to XY_LED
25	LED-	LED Cathode		Must connect to XY_LED
26	LED-	LED Cathode		Must connect to XY_LED
27	LED+	LED Anode		Provide 2.8V supply voltage
28	GND	Ground		

Note when A0, A1 is in NC, the sensor will drive the pin to 0 or low.

Overview of Optical Sensor Assembly

Avago Technologies provides an IGES file drawing describing the cover plate molding features.

The components interlock as they are mounted onto defined features on the cover plate.

The ADBS-A320 sensor is designed for surface mounting on a PCB, looking up. There is an aperture stop and features on the package that align to the lens.

The lens provides optics for the imaging of the surface as well as illumination of the surface at the optimum angle. Features on the lens align it to the sensor and cover plate. Contamination must be kept away from the lens. During assembly process, it is recommended to use a minimum of a 10K clean room environment or equivalent laminar flow workbench. See Application note OFN A320 Assembly Guide for more details on process flow.

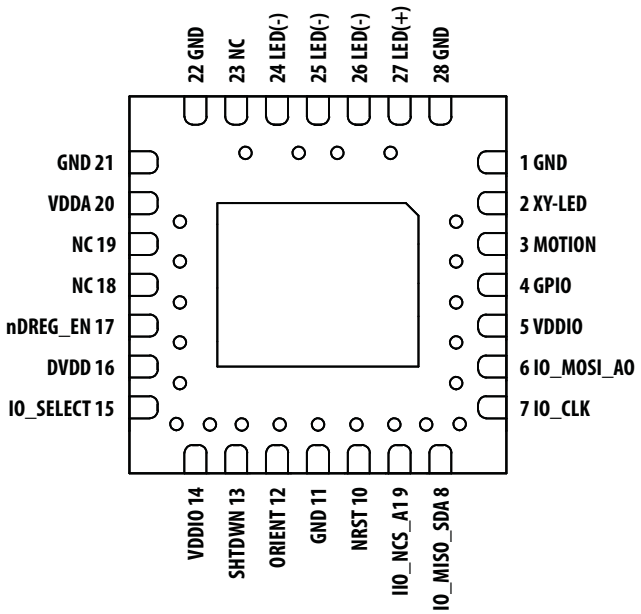


Figure 1a. Package outline drawing (bottom view)

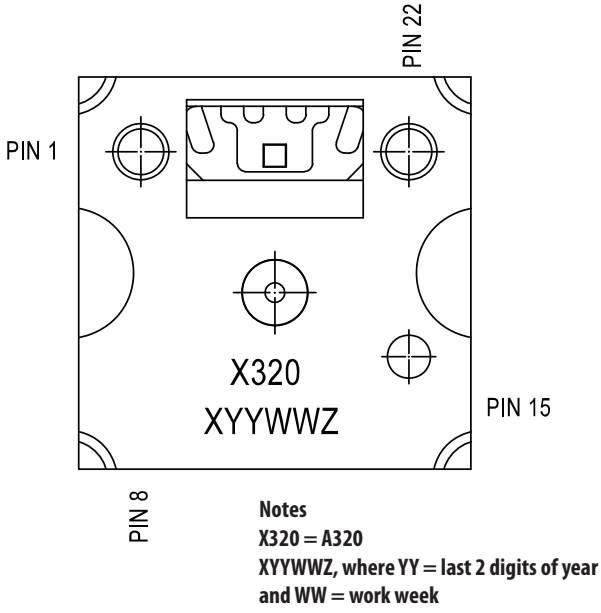
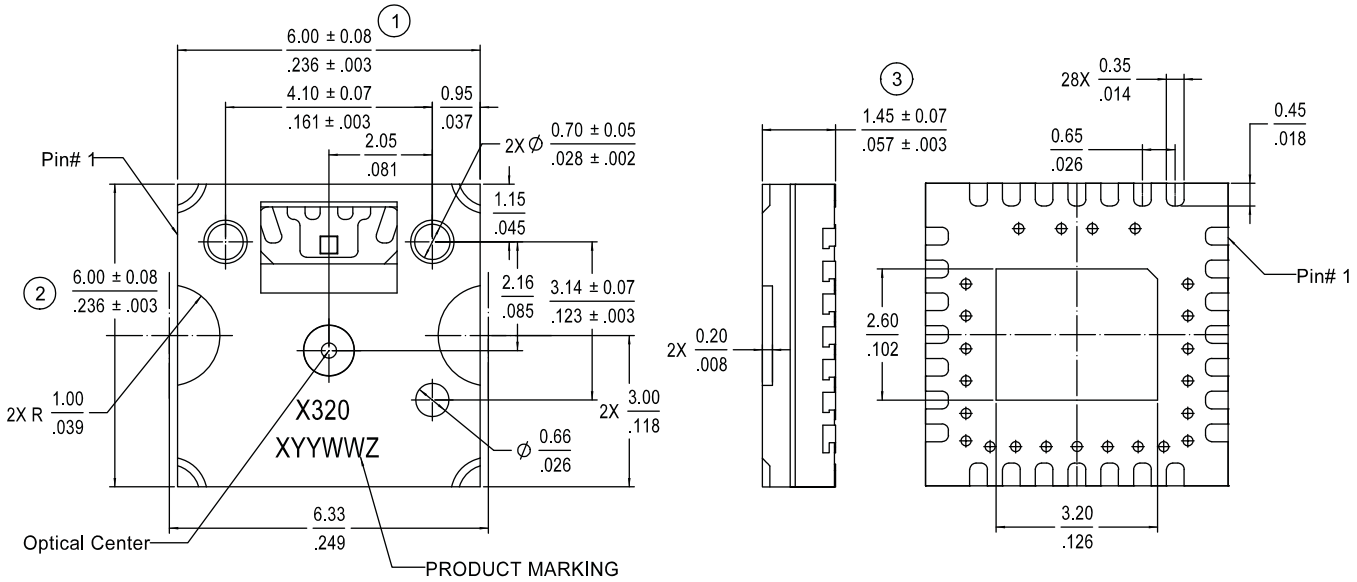


Figure 1b. Package outline drawing (top view)



Note:
1. Dimension in millimeters/inches
2. Coplanarity of pads : 0.08mm
3. Non Cumulative Pad pitch tolerance : ± 0.10mm
4. Maximum flash : ± 0.2mm
5. Dimensional tolerance (unless otherwise stated) : ± 0.10mm
6. All critical dimensions are indicated by number enclosed in a circle.

Figure 2. Package outline drawing

PCB Assembly Considerations

1. Surface mount the sensor and all other electrical components into PCB.
2. Reflow the entire assembly in a no-wash solder process.
3. Remove the protective kapton tape from optical aperture of the sensor and LED. Care must be taken to keep contaminants from entering the aperture. Recommend not to place the PCB facing up during the entire assembly process. Recommend to hold the PCB first vertically for the kapton removal process.
4. Press fit the lens onto the sensor until there is no gap between the lens and sensor, with force up to a maximum 2.2kgf. Care must be taken to avoid contaminating or staining the lens. The lens piece has alignment posts which will mate with the alignment holes on the sensor package.
5. Place and secure the optical navigation cover onto the lens to ensure the sensor and lens components are always interlocked to the correct vertical height. The cover design has a foolproof feature to avoid wrong orientation of the cover.
6. The optical position reference for the PCB is set by the navigation cover and lens.
7. Install device top casing. There MUST be a feature in either top casing or bottom casing to press onto the sensor to ensure the sensor and lens components are always interlocked to the correct vertical height.

Soldering Profile Information

Max rising slope	0.0°C/sec to 3°C/sec
Preheat time 150 – 200° C, ts	60 – 90 sec
Time above Reflow (T_L = 220° C)	50 – 100 sec
Peak Temperature	225 – 260° C

The recommended soldering profile is shown below.

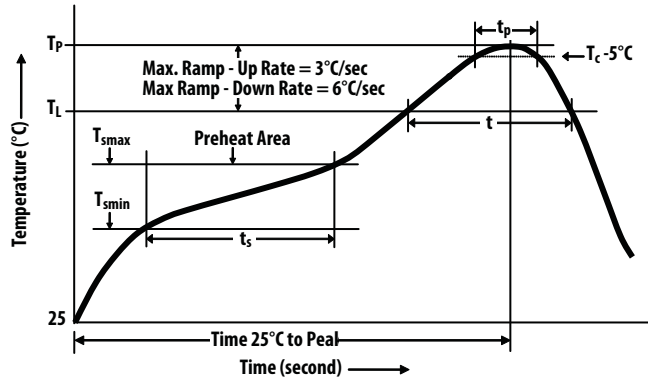
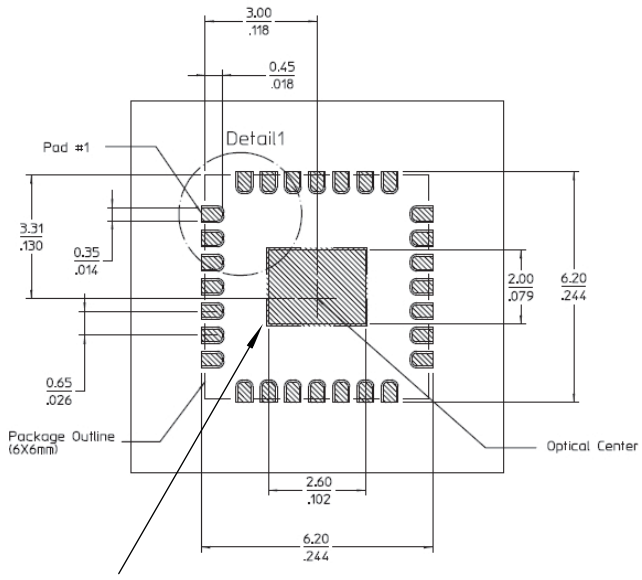


Figure 3a. Recommended reflow profile



Note: Rectangular shape pad on PCB or FPC should match in size (1:1) to sensor center GND pad

Figure 3b. Recommended Customer's PCB PADOUT and spacing

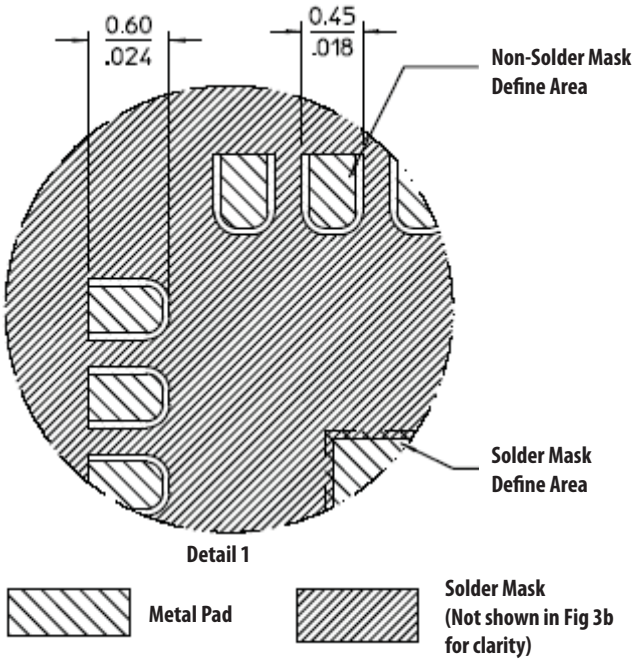


Figure 3c. Recommended Customer's PCB PADOUT and spacing

As ADBS-A320 is a QFN package, it is meant to be a contact-down package. The critical area for soldering ADBS-A320 is on the terminal undersides, while the terminal sides are deemed as non-critical area, and thus not intended to be wet-table. The non-wetting of the terminal sides is due to exposed copper on the package side (which is expected and accepted), occurred after the singulation step, which is a standard process in QFN assembly. This is in line with the Industry Standard (for more information, please refer to IPC-A-610D: Acceptability of Electronics Assemblies).

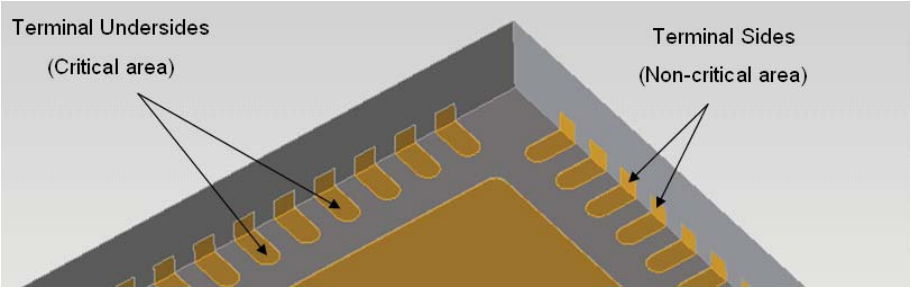


Figure 3d. Bottom view of A320 (QFN package)

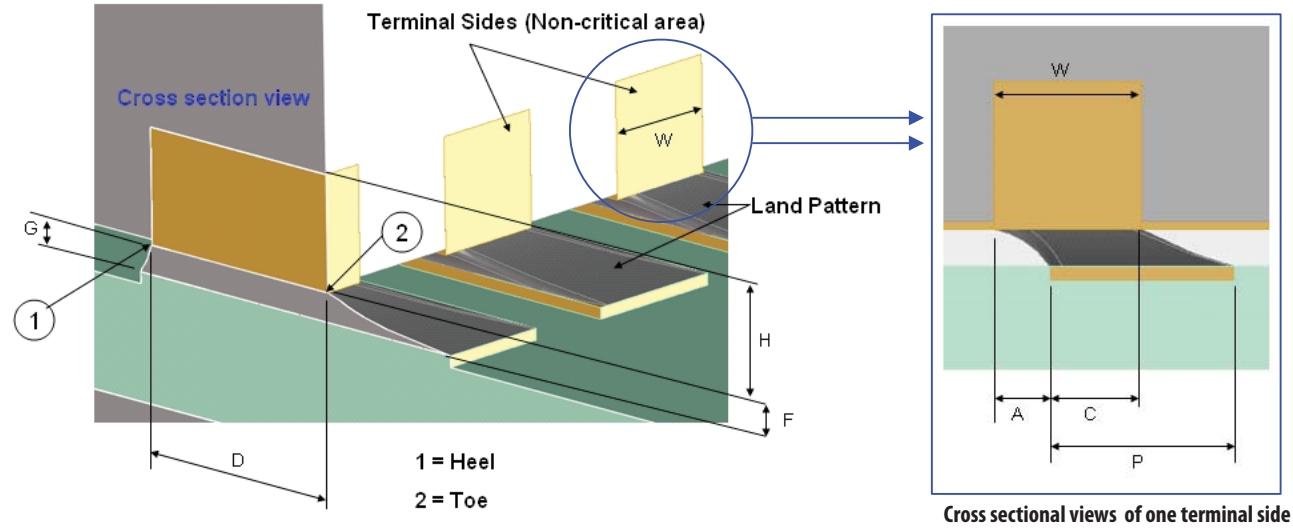


Figure 3e. Cross sectional views of A320

Critical and Non-critical areas of QFN soldering in Figure 3d and 3e

Feature	Dimension	Class 1	Class 2	Class 3
Maximum Side Overhang	A	50% W, Note 1	25% W, Note 1	25% W, Note 1
Minimum End Joint Width	C	50% W	75% W	75% W
Minimum Side Joint Length	D	Note 4	Note 4	Note 4
Minimum Fillet Height	F	Notes 2, 5	Notes 2, 5	Notes 2, 5
Solder Fillet Thickness	G	Note 3	Note 3	Note 3
Termination Height	H	Note 5	Note 5	Note 5
Land Width	P	Note 2	Note 2	Note 2
Termination Width	W	Note 2	Note 2	Note 2

Notes
1. Should not violate minimum electrical clearance.
2. Unspecified parameter. Variable in size as determined by design.
3. Good wetting is evident.
4. Is not a visual attribute for inspection.
5. Terminal sides are not required to be solderable. Toe fillets are not required.

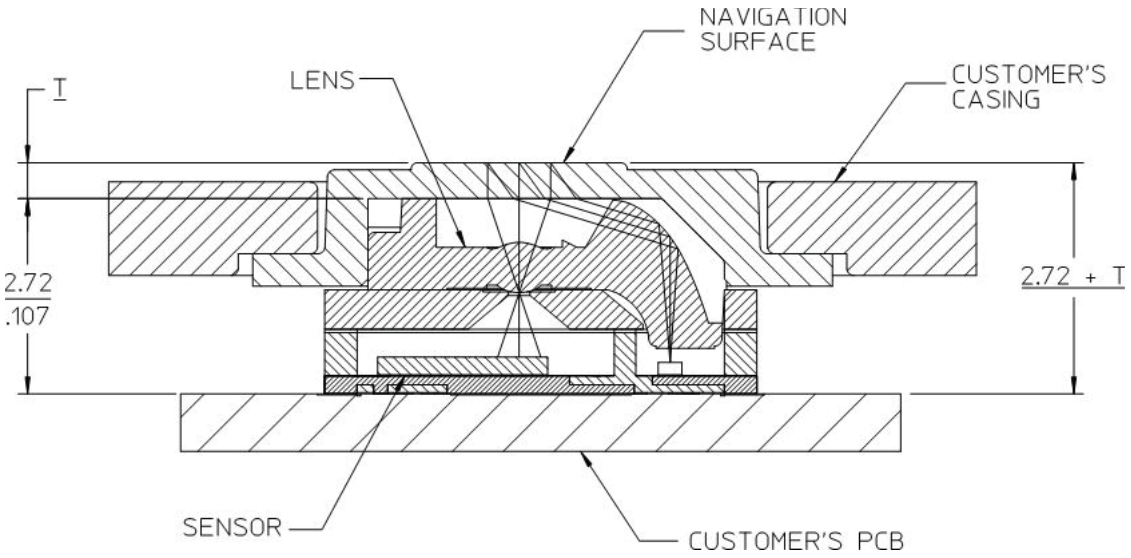


Figure 4. 2D Assembly drawing of ADBS-A320

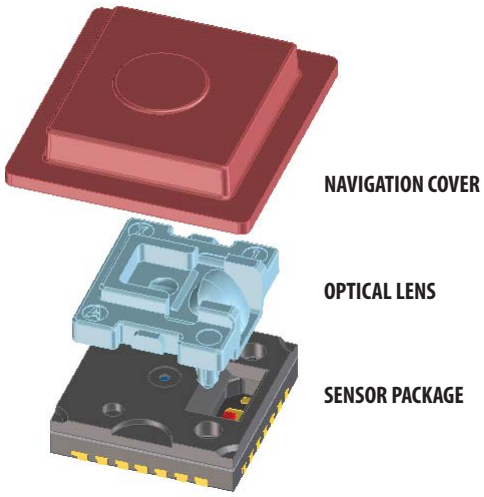


Figure 5a. Exploded Top view

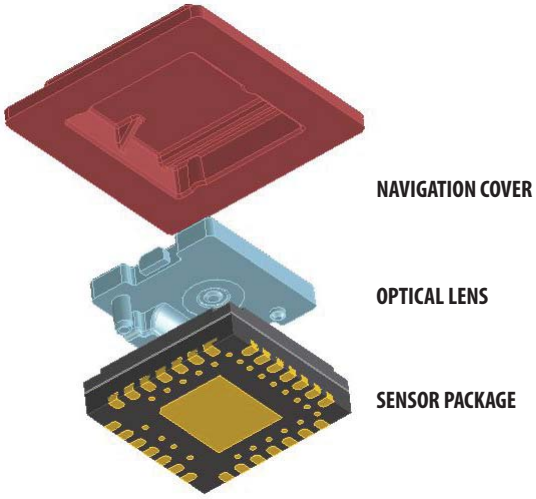
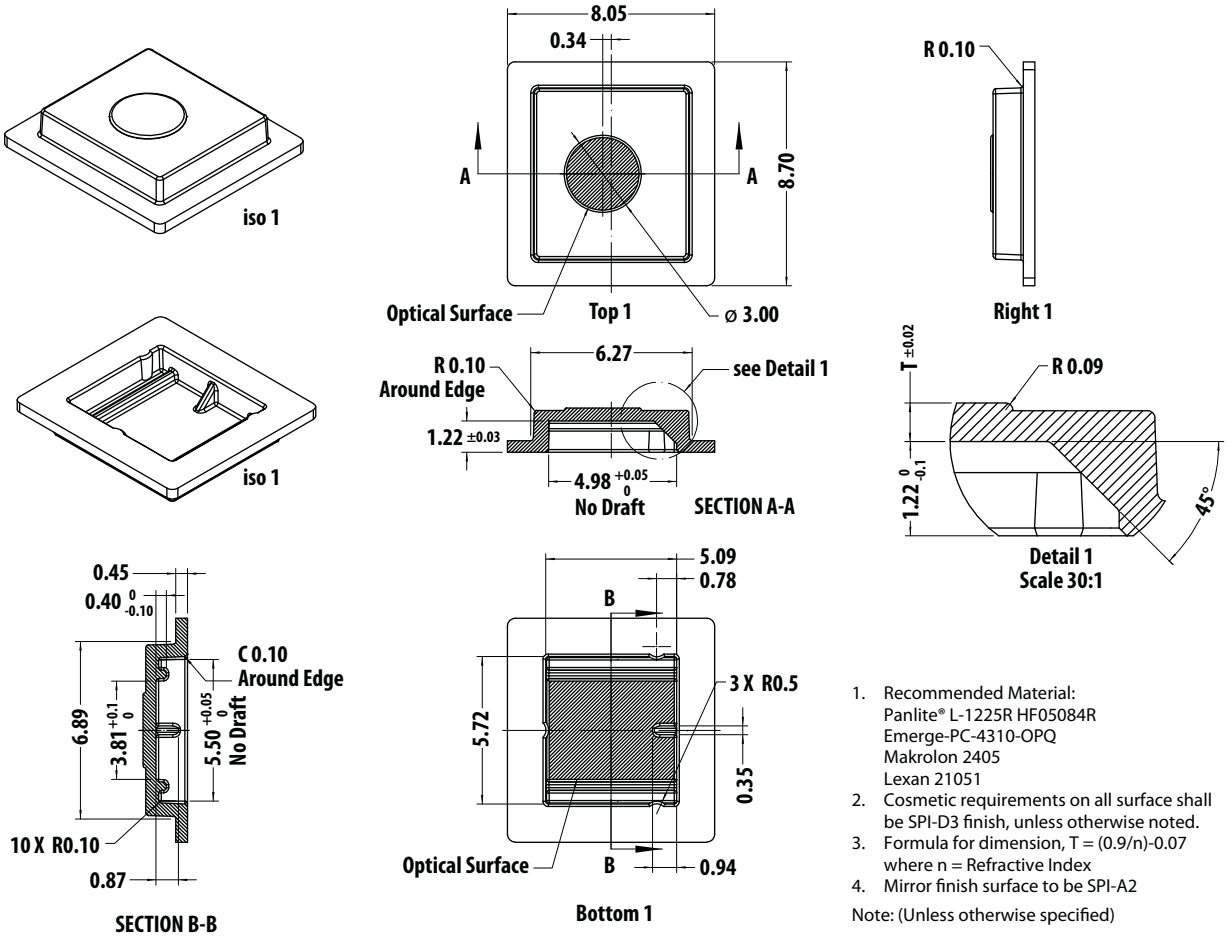


Figure 5b. Exploded Bottom view



1. Recommended Material:
   Panlite® L-1225R HF05084R
   Emerge-PC-4310-OPQ
   Makrolon 2405
   Lexan 21051
2. Cosmetic requirements on all surface shall be SPI-D3 finish, unless otherwise noted.
3. Formula for dimension, T = (0.9/n)-0.07 where n = Refractive Index
4. Mirror finish surface to be SPI-A2

Note: (Unless otherwise specified)

Figure 6a. Top cover drawing design

Important notes for top cover designs:

1. The recommended transmissivity of top cover window is between 86%-92% from 800nm to 940nm with worst case minimum of 80% and maximum of 97% across this range of light spectrum.
2. The Assert/ Deassert thresholds must be recalculated and set in the sensor accordingly during initialization to address variation of surface reflection and transmissivity for custom cover designs. (See OFN firmware application note and OFN mechanical guide application note for further details).

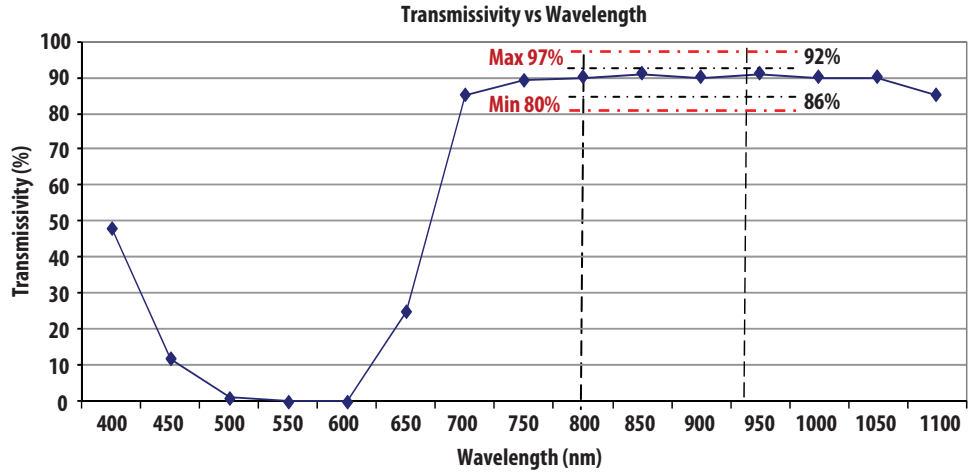
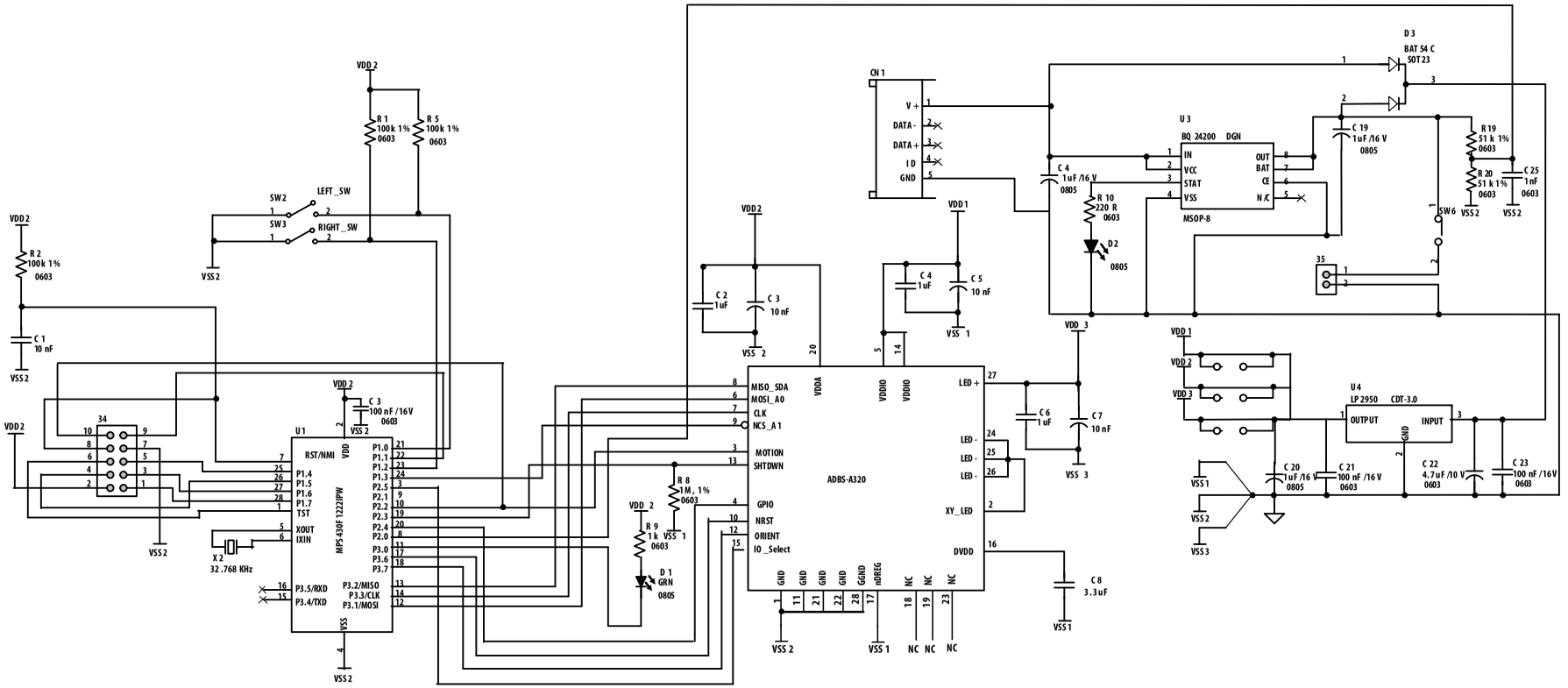
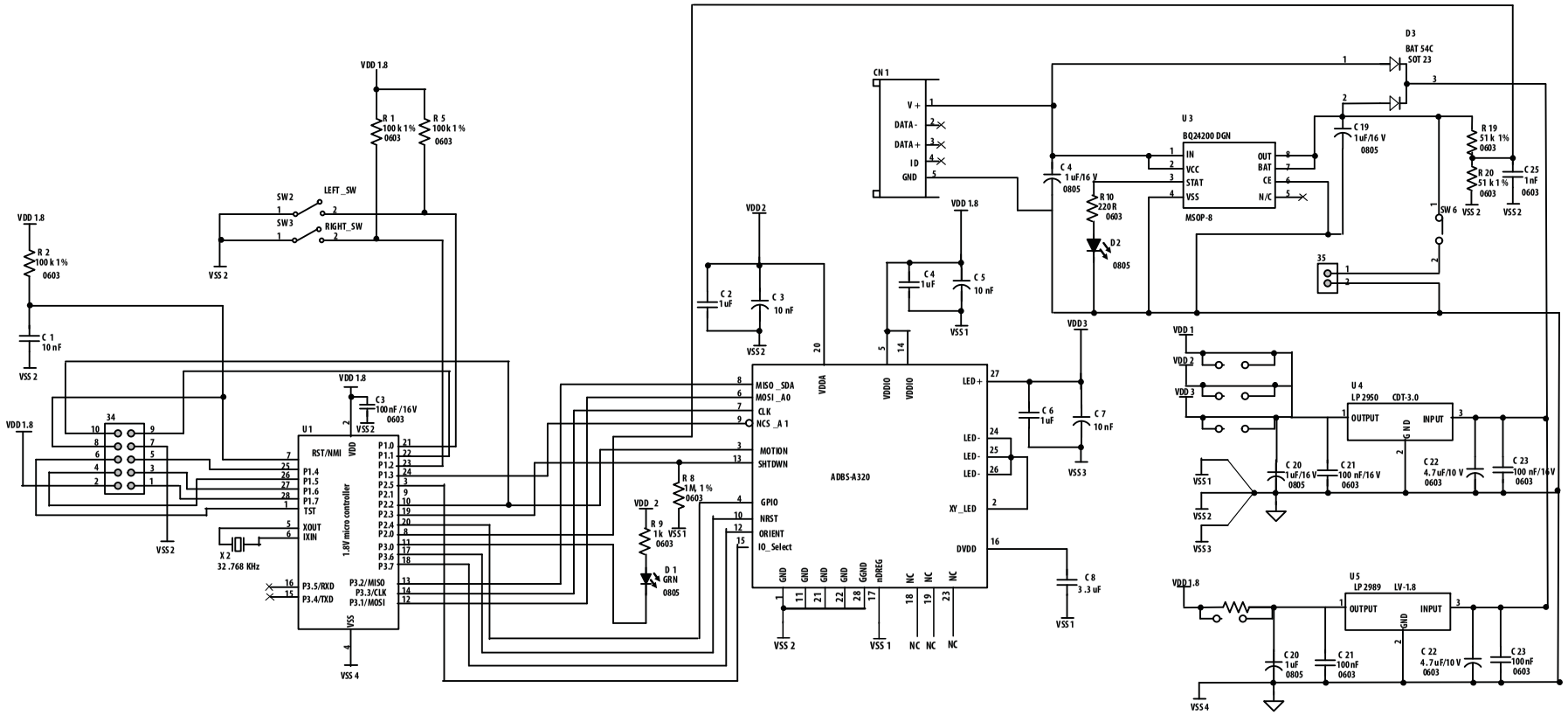


Figure 6b. Example of Transmissivity vs. Wavelength curve for standard Avago cover material



Note :- Dome + must be connected to MCU to detect button change state and Dome – can be connected to GND

Figure 7a. Schematic diagram for interface between ADBS-A320 and 3V microcontroller via SPI with internal Regulator 1.8V enabled



Note :- Dome + must be connected to MCU to detect button change state and Dome – can be connected to GND.

Figure 7b. Schematic diagram for interface between ADBS-A320 and 1.8V microcontroller via SPI with internal Regulator 1.8V enabled

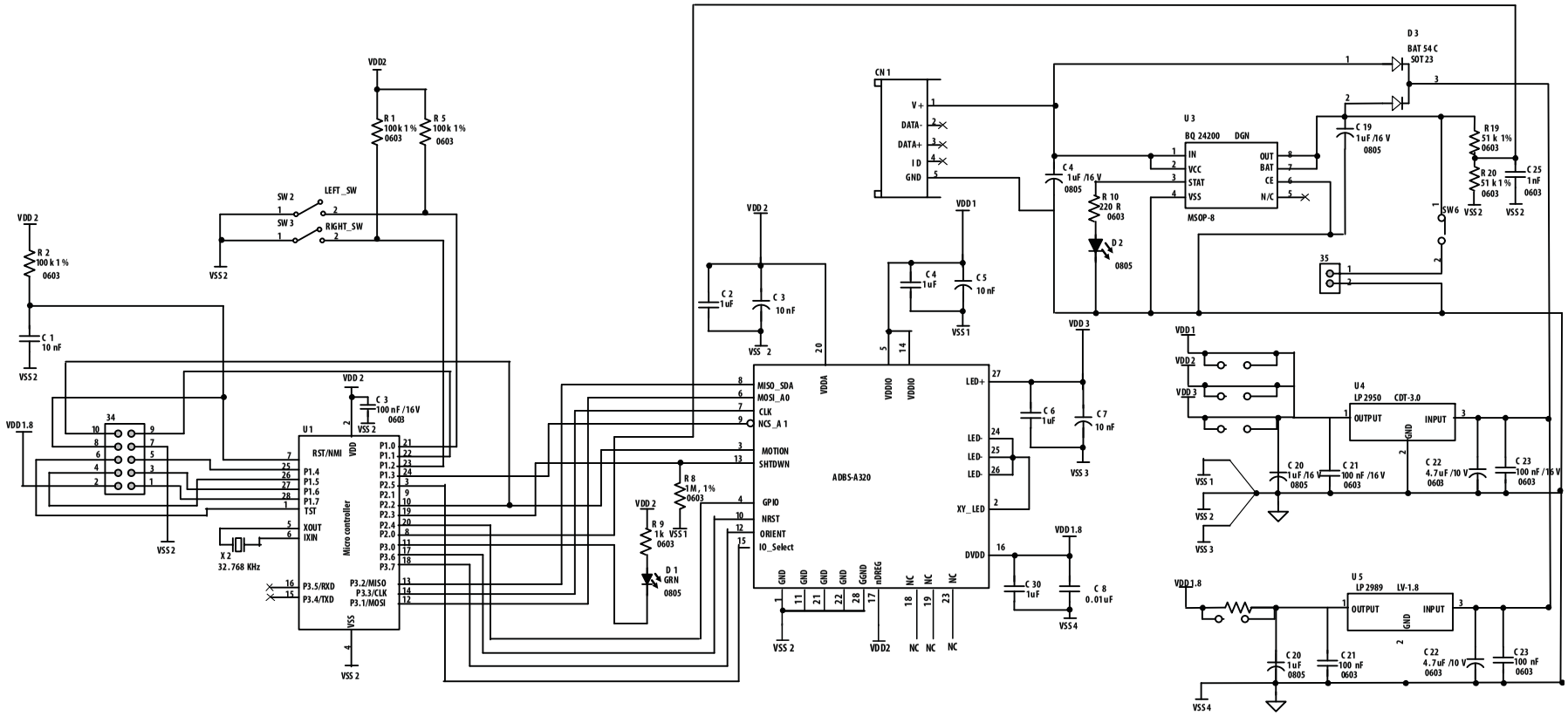
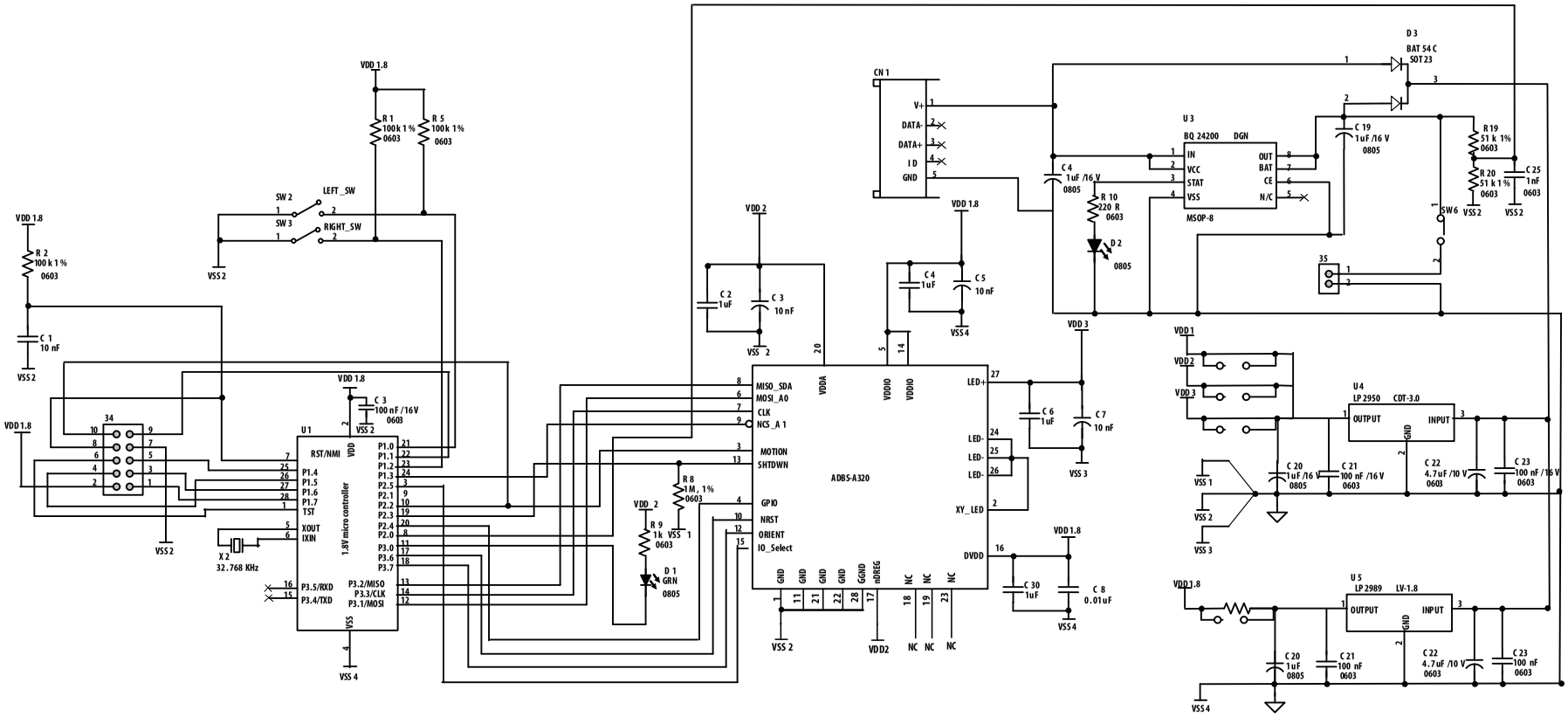


Figure 7c. Schematic diagram for interface between ADBS-A320 and 3V microcontroller via SPI with internal Regulator 1.8V disabled



Note :- Dome + must be connected to MCU to detect button change state and Dome – can be connected to GND.

Figure 7d. Schematic diagram for interface between ADBS-A320 and 1.8V microcontroller via SPI with internal Regulator 1.8V disabled

I/O Voltage options (values listed are typical)

Internal regulator status	nDREG pin	V_{DDA}	DV_{DD}	V_{DDIO}	I/O pin interface voltage	Notes for DV_{DD}	Notes for pin18 & 19 connection
Enabled	GND (Fig 7a)	2.8V	Output 1.8V with bypass capacitor 3.3uF	External 1.8V or V_{DDA}	1.8V or 2.8V	Do not use internal regulator output voltage as supply to other circuits.	MUST be No Connect (NC)
Disabled	V_{DDA} (Fig 7b)	2.8V	Input of 1.8V with 0.01uF and 1uF	External 1.8V or V_{DDA}	1.8V or 2.8V	Require external voltage supply.	Prefer if No Connect. Optional connection to GND allowed

Regulatory Requirements

- Passes FCC B and worldwide analogous emission limits when assembled following Avago Technologies recommendations.
- Passes IEC-55024 or CISPR 24 radiated susceptibility level when assembled following Avago Technologies recommendations.

Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_S	-40	85	°C	
Lead Solder Temp			260	°C	For 1.4 seconds
Moisture Sensitivity Level	MSL		1		Referring to JEDEC-J-STD-020.
Analog Supply Voltage	V_{DDA}	-0.5	3.6	V	
I/O Supply Voltage	V_{DDIO}	-0.5	3.6	V	
Digital Supply Voltage	DV_{DD}	-0.5	2	V	
LED supply voltage	V_{LED+}	-0.5	3.6	V	
ESD (sensor only)			2	kV	All pins, human body model JESD22-A114-E
Input Voltage	V_{IN}	-0.5	V_{DDA}+0.5 V_{DDIO}+0.5	V	nDREG_EN pin All pins except nDREG_EN pin
Latchup Current	Iout		20	mA	All Pins

Note - Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are the stress ratings only and functional operation of the device at these or any other condition beyond those indicated may affect device reliability.

At power up, if DV_{DD} is powered up before V_{DDA}, DV_{DD} should never exceed V_{DDA} by more than 0.7V to avoid high inrush current. If DV_{DD} is powered up before V_{DDA}, then V_{DDA} must ramp up to stable voltage in less than 1.5seconds. In this case high inrush current of up to 180mA can be observed at DV_{DD}.

At power down, if V_{DDA} is powered down before DV_{DD} and V_{DDIO}, then DV_{DD} must ramp down to 0V in less than 1.5seconds. In this case high inrush current of up to 180mA can be observed at DV_{DD}.

Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Operating Temperature	T_A	-20		60	°C	
Analog supply voltage	V_{DDA}	2.6	2.8	3.3	Volts	Including V_{NA} noise.
I/O supply voltage	V_{DDIO}	1.65	1.8 or 2.8	3.3	Volts	Including V_{NA} noise. Sets I/O voltages but not for nDREG_EN. See fig 7a, 7b.
Digital supply voltage	DV_{DD}	1.65	1.8	1.95	Volts	Input voltage supply when nDREG pin is high. Input voltage supply not required when nDREG is GND
LED supply voltage	V_{LED+}	2.6	2.8	3.3	Volts	Including V_{NA} noise.
Power supply rise time	t_{VRT}	0.001		100	ms	0 to 2.8V
Supply noise (Sinusoidal)	V_{NA}			100	mV p-p	10kHz-50MHz
Speed	S			15	in/sec	Using prosthetic finger as surface

AC Electrical Specifications

Electrical Characteristics at 25°C, V_{DDA}=2.8V, DV_{DD}=1.8V.

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Motion delay after reset	$t_{MOT-RST}$	3.5		23	ms	From Hard or Soft_RESET register write to valid register write/read and motion, assuming motion is present
Shutdown	t_{SHTDWN}			50	ms	From SHTDWN pin active to low current
Wake from shutdown	t_{WAKEUP}	100			ms	From SHTDWN pin inactive to valid motion. Refer to section "Notes on Shutdown", also note $t_{MOT-RST}$
MOTION rise time	$t_{r-MOTION}$		150	300	ns	C_L = 100pF
MOTION fall time	$t_{f-MOTION}$		150	300	ns	C_L = 100pF
SHTDWN pulse width	$t_{P-SHTDWN}$	150			ms	
NRST pulse width	t_{NRST}	20			us	From edge of valid NRST pulse
Reset wait time after stable supply voltage	$t_{VRT-NRST}$	100			ms	
Transient Supply Current	I_{DDT}			75	mA	Max supply current for 500 usec for each supply voltages ramp from 0 to 3.3V

DC Electrical Specifications

Electrical Characteristics at 25°C, V_{DDA}=3.3V, DV_{DD}=1.95V at default LED setting 13mA.

		Internal regulator Enabled		Internal regulator Disabled			
Parameter		**Typical**	**Max**	**Typical**	**Max**	**Units**	**Notes**
DC average supply current in Run mode	I V_{DDA}	1.80	2.50	0.90	1.10	mA	GPIO=SHTDWN=pull low, IO_MISO=NRST=ORIENT=pull high.
	IDD_LED+	1.30	1.80	1.30	1.80	mA	GPIO=SHTDWN=pull low, IO_MISO=NRST=ORIENT=pull high.
	I DV_{DD}	0	0	0.90	1.40	mA	GPIO=SHTDWN=pull low, IO_MISO=NRST=ORIENT=pull high.
	Total	3.10	4.30	3.10	4.30	mA	
DC average supply current in Rest1 mode	I V_{DDA}	0.20	0.30	0.10	0.15	mA	GPIO=SHTDWN=pull low, IO_MISO=NRST=ORIENT=pull high.
	IDD_LED+	0.20	0.40	0.20	0.40	mA	GPIO=SHTDWN=pull low, IO_MISO=NRST=ORIENT=pull high.
	I DV_{DD}	0	0	0.10	0.15	mA	GPIO=SHTDWN=pull low, IO_MISO=NRST=ORIENT=pull high.
	Total	0.40	0.70	0.40	0.70	mA	
DC average supply current in Rest2 mode	I V_{DDA}	0.06	0.12	0.03	0.07	mA	GPIO=SHTDWN=pull low, IO_MISO=NRST=ORIENT=pull high.
	IDD_LED+	0.04	0.08	0.04	0.08	mA	GPIO=SHTDWN=pull low, IO_MISO=NRST=ORIENT=pull high.
	I DV_{DD}	0	0	0.03	0.05	mA	GPIO=SHTDWN=pull low, IO_MISO=NRST=ORIENT=pull high.
	Total	0.10	0.20	0.10	0.20	mA	
DC average supply current in Rest3 mode	I V_{DDA}	0.03	0.12	0.02	0.06	mA	GPIO=SHTDWN=pull low, IO_MISO=NRST=ORIENT=pull high.
	IDD_LED+	0.01	0.03	0.01	0.03	mA	GPIO=SHTDWN=pull low, IO_MISO=NRST=ORIENT=pull high.
	I DV_{DD}	0	0	0.01	0.06	mA	GPIO=SHTDWN=pull low, IO_MISO=NRST=ORIENT=pull high.
	Total	0.04	0.15	0.04	0.15	mA	
Analog shutdown supply current	$I_{DDSHTDWN}$ V_{DDA}	17	44.3	0	2	µA	GPIO=pull low, SHTDWN= IO_MISO=NRST=ORIENT=pull high.
Analog shutdown supply current	$I_{DDSHTDWN}$ VLED+	0	0.7	0	0.7	µA	GPIO=pull low, SHTDWN= IO_MISO=NRST=ORIENT=pull high.
Digital shutdown supply current	$I_{DDSHTDWN}$ DV_{DD}	0	0	3	15	µA	GPIO=pull low, SHTDWN= IO_MISO=NRST=ORIENT=pull high.

DC Electrical Specifications

Electrical Characteristics at 25°C, V_{DDA}=3.3V, DV_{DD}=1.95V at default LED setting 13mA.

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
V_{DDIO} DC Supply Current	I V_{DDIO}			10	uA	Average current V_{DDIO}.
Analog peak supply current	I_{PEAK} V_{DDA}			2.5	mA	At LED register setting of 40mA.
LED+ peak supply current	I_{PEAK} LED+			49.5	mA	At LED register setting of 40mA.
Digital Peak supply current	I_{PEAK} DV_{DD}			1.5	mA	At LED register setting of 40mA.
Input Low Voltage	V_{IL}	-0.05	0	V_{DDIO}*0.35	V	IO_MOSI_A0, IO_CLK, IO_MISO_SDA, IO_NCS_A1, NRST, ORIENT, SHTDWN, IO_SELECT
Input High Voltage	V_{IH}	V_{DDIO} * 0.7	V_{DDIO}	V_{DDIO}+0.05	V	IO_MOSI_A0, IO_CLK, IO_MISO_SDA, IO_NCS_A1, NRST, ORIENT, SHTDWN, IO_SELECT
Input hysteresis	V_{HYS}	100			mV	
Input leakage current	I_{leak}		±1	±10	µA	IO_MOSI_A0, IO_CLK, IO_MISO_SDA, IO_NCS_A1, NRST, ORIENT, SHTDWN, IO_SELECT
Output Low Voltage	V_{OL}			0.2	V	I_{out}=1.2mA
Output High Voltage	V_{OH}	V_{DDIO}-0.2	V_{DDIO}-0.1		V	I_{out}=600uA
Input Capacitance	C_{in}			10	pF	MOSI, NCS, SCLK, SHTDWN

Notes on Power-up

The ADBS-A320 does not perform an internal power up self-reset; the NRST pin must be toggled every time power is applied. The appropriate sequence is as follows:

1. Apply power. See Notes on Power Up sequence below.
2. Set NCS pin high if using SPI. If TWI, then NCS_A1 will follow TWI address. Set Shutdown pin low and Orient. Set IO_Select pin to low (for TWI) or high (for SPI).
3. If in TWI mode, set A0 and A1 according to the Table TWI slave address in datasheet. This step is skipped if SPI mode is used.
4. In TWI, drive NRST low then high. This is optional for SPI. TWI slave address will only be selected after a NRST toggle is applied when A0 and A1 is set.
5. If in SPI mode, wait until sensor valid power up by reading Product ID register. If in TWI mode, skip this step.
6. If in SPI mode, perform soft reset by writing 0x5A to address 0x3a. In TWI mode, this is not required.
7. Write 0xE4 to address 0x60.
8. Set Speed Switching, write 0x62 with 0x12, 0x63 with 0x0E.
9. Check registers 0x64 with 0x08, 0x65 with 0x06, 0x66 with 0x40, 0x67 with 0x08, 0x68 with 0x48, 0x69 with 0x0a, 0x6a with 0x50, 0x6b with 0x48.
10. Check Assert/De-assert registers, 0x6d with 0xc4, 0x6e with 0x34, 0x6f with 0x3c, 0x70 with 0x18, 0x71 with 0x20.
11. Check Finger Presence Detect register, 0x75 with 0x50.
12. IF XY Quantization is used, check 0x73 with 0x99 and 0x74 with 0x02.
13. Write 0x10 to register 0x1C. This will activate burst mode. If burst mode not used then skip this step.
14. Read from registers 0x02, 0x03 and 0x04 (or read these same 3 bytes from burst motion) one time regardless the state of the motion pin.
15. Check 0x1a with 0x00 to set LED drive current to 13mA.
16. At power down, see Notes on Power Down sequence below.

Note on register settings

Please refer to the OFN A320 firmware design guide for tuning best Speed Switching, Assert/Deassert, Finger Presence Detect and XY Quantisation register settings.

Notes on Power Up sequence

When internal regulator is enabled, nDREG_EN = Ground, apply V_{DDA} and V_{DDIO} in any order.

When internal regulator is disabled, nDREG_EN = High, V_{DDA} must be applied prior to DV_{DD}. The sensor must power up from V_{DDA} first to a stable voltage. Then apply DV_{DD}. V_{DDIO} can be applied in any order.

See Absolute Maximum Rating for other condition.

If V_{DDIO} is applied before V_{DDA} in internal regulator enabled or V_{DDIO} is applied before V_{DDA} and DV_{DD} in internal regulator disabled, while all sensor I/O pins are at high or low, then a small leakage current of 1uA can be expected at V_{DDIO}.

If V_{DDIO} is applied before V_{DDA} in internal regulator enabled or V_{DDIO} is applied before V_{DDA} and DV_{DD} in internal regulator disabled, while all sensor I/O pins are floating, then a leakage current of up to 1mA can be expected at V_{DDIO}.

If V_{DDIO} is Grounded, then the TWI line will be pulled down and rendered not operational. V_{DDIO} must be applied for I/O pins to be functional.

Notes on Power Down sequence

During power down and internal regulator disabled, it is a MUST to ramp down DV_{DD} first then followed by V_{DDA} to 0V or all at the same time. Do not power down V_{DDA} before power down DV_{DD}.

If V_{DDA} is powered down before DV_{DD}, DV_{DD} should never exceed V_{DDA} by more than 0.7V to avoid high inrush current.

During power-up there will be a period of time after the power supply is high but before any clocks are available. See power sequence chart below reference to "Notes on Power up" steps.

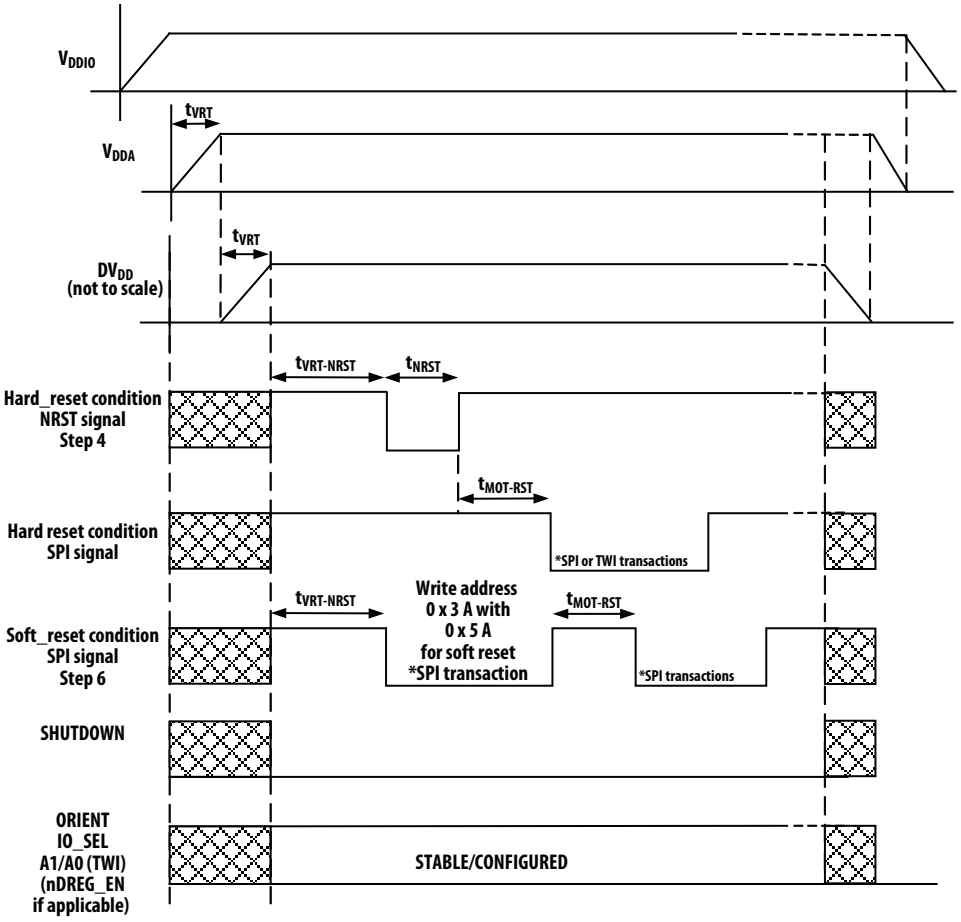


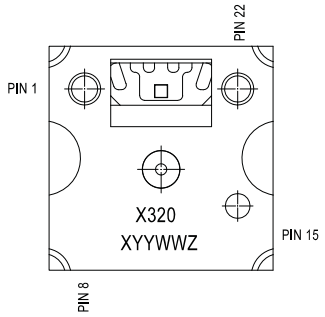
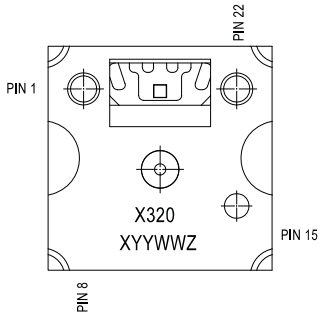
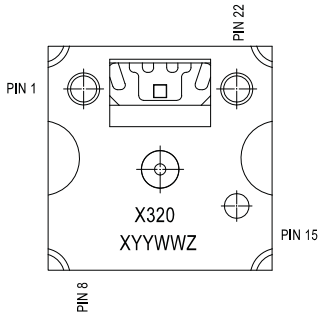
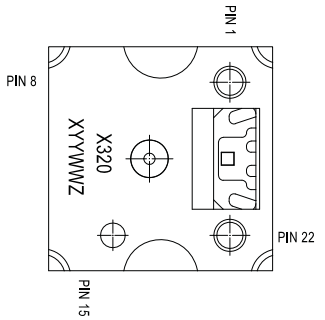
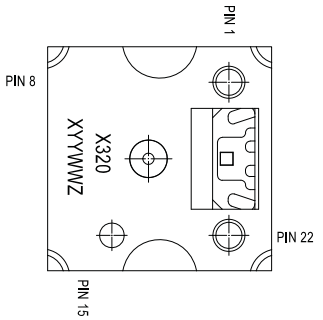
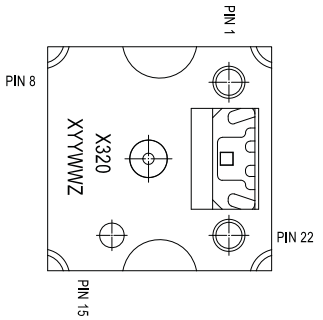
Figure 8. Power up and down sequence

As in step 4, in TWI mode, the sensor must be toggle with hard reset. The hard reset via toggling NRST pin high to low then high again must observe $t_{VRT-NRST}$ and t_{NRST}. Then a time of $t_{MOT-RST}$ must be observed before accessing the sensor registers via SPI or TWI ports. See two graphs for Hard reset condition.

If SPI mode is used, then hard reset is not required. Instead a soft reset can be employed. Note that time $t_{VRT-NRST}$ and $t_{MOT-RST}$ must be observed before accessing SPI ports.

The Shutdown, Orient, IO_Select and TWI ports are stable after proper power up procedures.

The table below shows the state of the various pins during power-up and reset.

State of Signal Pins After V_{DDA} is Valid			
Pin	**NCS high before reset**	**NCS Low before reset**	**After Reset**
NCS	High	Low	Functional
MISO	Undefined	Functional	Depends on NCS
SCLK	Ignored	Functional	Depends on NCS
MOSI	Ignored	Functional	Depends on NCS
XY_LED	Undefined	Undefined	Functional
MOTION	Undefined	Undefined	Functional
SHTDWN	Must be low	Must be low	Functional
NRST	High	High	High
IO_Select	SPI: High, TWI:Low	SPI: High, TWI:Low	SPI: High, TWI:Low
ORIENT Top view	High 	High 	High 
ORIENT Top view	Low 	Low 	Low 
GPIO	Undefined	Undefined	Undefined

Notes on Shutdown and Reset

The ADBS-A320 can be set in Shutdown mode by asserting or setting SHTDWN pin high. During the shutdown state, supply voltages V_{DDIO} and DV_{DD} must be maintained above the minimum level. If these conditions are not met, then the sensor must be restarted by powering down then powering up again for proper operation. Any register settings must then be reloaded.

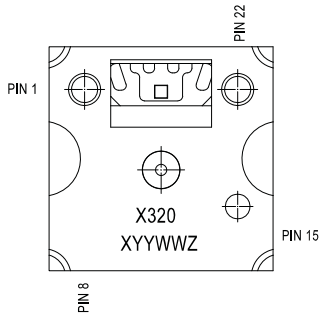
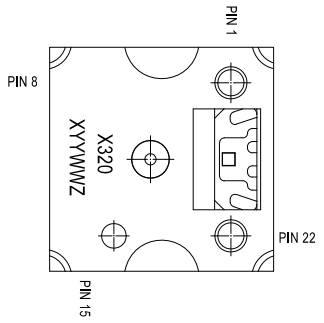
During the shutdown state, supply voltages V_{DDIO} and DV_{DD} must be maintained above the minimum level. For proper operation, SHTDWN pulse width must be at least $t_{P\text{-}SHTDWN}$. Shorter pulse widths may cause the chip to enter an undefined state. In addition, the SPI or TWI port should not be accessed when SHTDWN is asserted. (Other ICs on the same SPI bus can be accessed, as long as the sensor's NCS pin is not asserted.) The table below shows the state of various pins during shutdown. After deasserting SHTDWN, wait t_{WAKEUP} before accessing the SPI port. Reinitializing the sensor from shutdown state will retain all register data that were written to the sensor prior to shutdown (see register table page 34 for list of registers). If the internal regulator is disabled and V_{DDA} is removed but DV_{DD} is retained, reinitializing the sensor from shutdown state will retain all register data that were written to the sensor prior to shutdown. See register table page 34 for list of registers.

The reset of the sensor via Soft_RESET register or through the NRST pin would reset all registers to the default value. Any register settings must then be reloaded.

Power management modes

The ADBS-A320 has three power-saving modes. Each mode has a different motion detection period, affecting response time to sensor motion (Response Time). The sensor automatically changes to the appropriate mode, depending on the time since the last reported motion (Downshift Time). The parameters of each mode are shown in the following table.

Mode	Response Time (nominal)	Downshift Time (nominal)
Rest 1	19.5 ms	250 ms
Rest 2	96 ms	9.5 s
Rest 3	482 ms	582 s

Pin	SHTDWN active
NCS	Functional*
MISO	Undefined
SCLK	Undefined
MOSI	Undefined
XY_LED	Low current
MOTION	Undefined
NRST	High
IO_Select	SPI:High, TWI:Low
ORIENT Top view	High 
ORIENT Top view	Low 
GPIO	Undefined

*In Regulator disabled mode, NCS pin must be held to 1 (high) if SPI bus is shared with other devices.

Note: There are long wakeup times from shutdown. These features should not be used for power management during normal sensor motion.

Motion Pin Timing

The motion pin is a level-sensitive output that signals the micro-controller when motion has occurred. The motion pin is lowered whenever the motion bit is set; in other words, whenever there is data in the Delta_X or Delta_Y registers. Clearing the motion bit (by reading Delta_Y and Delta_X, or writing to the Motion register) will put the motion pin high.

LED Mode

For power savings, the LED will not be continuously on. ADBS-A320 will flash the LED only when needed.

Serial Peripheral Interface (SPI)

AC Electrical Specifications

Electrical Characteristics at 25°C, V_{DDA}=2.8V, DV_{DD}=1.8V.

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Serial Port Clock Frequency	f_{sclk}			1	MHz	Active drive, 50% duty cycle
MISO rise time	tr-MISO		150	300	ns	CL = 100pF
MISO fall time	tf-MISO		150	300	ns	CL = 100pF
MISO delay after SCLK	tDLY-MISO			120	ns	From SCLK falling edge to MISO data valid, no load conditions
MISO hold time	thold-MISO	0.5		1/fSCLK	µs	Data held until next falling SCLK edge
MOSI hold time	thold-MOSI	200			ns	Amount of time data is valid after SCLK rising edge
MOSI setup time	tsetup-MOSI	120			ns	From data valid to SCLK rising edge
SPI time between write commands	tSWW	30			µs	From rising SCLK for last bit of the first data byte, to rising SCLK for last bit of the second data byte.
SPI time between write and read commands	tSWR	20			µs	From rising SCLK for last bit of the first data byte, to rising SCLK for last bit of the second address byte.
SPI time between read and subsequent commands	tSRW tSRR	500			ns	From rising SCLK for last bit of the first data byte, to falling SCLK for the first bit of the address byte of the next command.
SPI read address-data delay	tSRAD	4			µs	From rising SCLK for last bit of the address byte, to falling SCLK for first bit of data being read.
NCS inactive after motion burst	tBEXIT	500			ns	Minimum NCS inactive time after motion burst before next SPI usage
NCS to SCLK active	tNCS-SCLK	120			ns	From NCS falling edge to first SCLK falling edge
SCLK to NCS inactive (for read operation)	tSCLK-NCS	120			ns	From last SCLK rising edge to NCS rising edge, for valid MISO data transfer
SCLK to NCS inactive (for write operation)	tSCLK-NCS	20			us	From last SCLK rising edge to NCS rising edge, for valid MOSI data transfer
NCS to MISO high-Z	tNCS-MISO			500	ns	From NCS rising edge to MISO high-Z state

The synchronous serial port is used to set and read parameters in the ADBS-A320, and to read out the motion information.

The port is a four wire serial port. The host micro-controller always initiates communication; the ADBS-A320 never initiates data transfers. SCLK, MOSI, and NCS may be driven directly by a micro-controller. The port pins may be shared with other SPI slave devices. When the NCS pin is high, the inputs are ignored and the output is tri-stated.

The lines that comprise the SPI port:

SCLK: Clock input. It is always generated by the master (the micro-controller).

MOSI: Input data. (Master Out/Slave In)

MISO: Output data. (Master In/Slave Out)

NCS: Chip select input (active low). NCS needs to be low to activate the serial port; otherwise, MISO will be high Z, and MOSI & SCLK will be ignored. NCS can also be used to reset the serial port in case of an error.

Chip Select Operation

The serial port is activated after NCS goes low. If NCS is raised during a transaction, the entire transaction is aborted and the serial port will be reset. This is true for all transactions. After a transaction is aborted, the normal address-to-data or transaction-to-transaction delay is still required before beginning the next transaction. To improve communication reliability, all serial transactions should be framed by NCS. In other words, the port should not remain enabled during periods of non-use because ESD events could be interpreted as serial communication and put the chip into an unknown state. In addition, NCS must be raised after each burst-mode transaction is complete to terminate burst-mode. The port is not available for further use until burst-mode is terminated.

Write Operation

Write operation, defined as data going from the micro-controller to the ADBS-A320, is always initiated by the micro-controller and consists of two bytes. The first byte contains the address (seven bits) and has a "1" as its MSB to indicate data direction. The second byte contains the data. The ADBS-A320 reads MOSI on rising edges of SCLK.

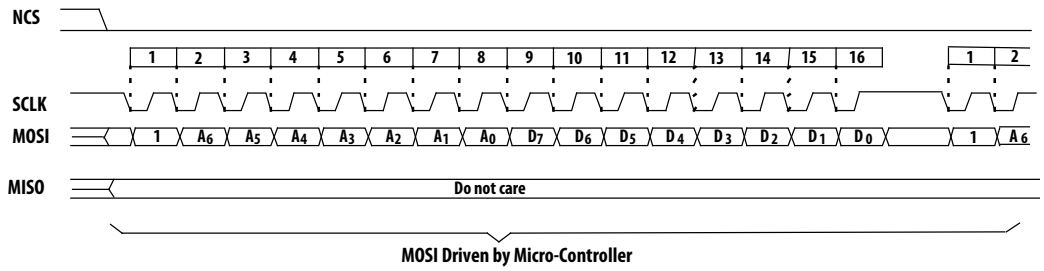


Figure 9. Write Operation

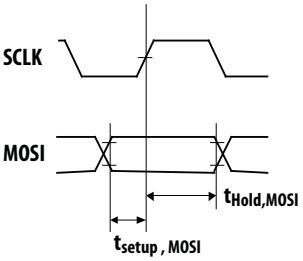


Figure 10. MOSI Setup and Hold Time

Read Operation

A read operation, defined as data going from the ADBS-A320 to the micro-controller, is always initiated by the micro-controller and consists of two bytes. The first byte contains the address, is sent by the micro-controller over MOSI, and has a "0" as its MSB to indicate data direction. The second byte contains the data and is driven by the ADBS-A320 over MISO. The sensor outputs MISO bits on falling edges of SCLK and samples MOSI bits on every rising edge of SCLK.

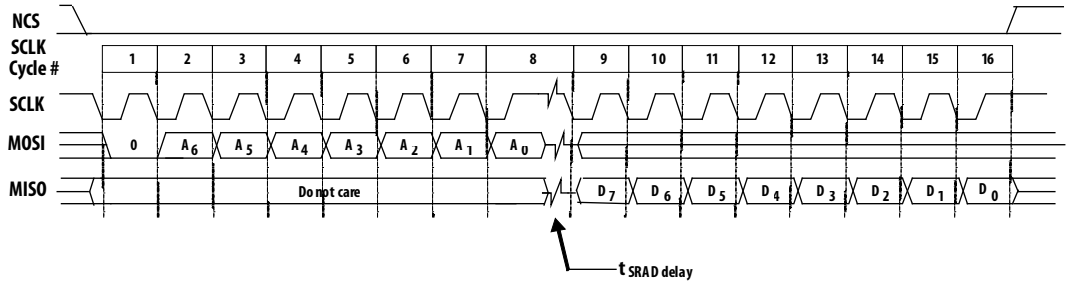
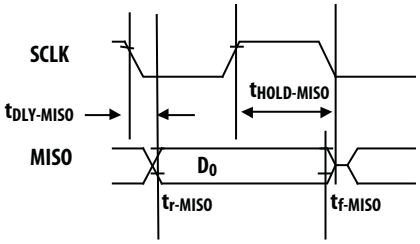


Figure 11. Read Operation



NOTE: The $0.5/f_{SCLK}$ minimum high state of SCLK is also the minimum MISO data hold time of the ADBS-A320. Since the falling edge of SCLK is actually the start of the next read or write command, the ADBS-A320 will hold the state of data on MISO until the falling edge of SCLK.

Figure 12. MISO Delay and Hold Time

Required timing between Read and Write Commands

There are minimum timing requirements between read and write commands on the serial port.

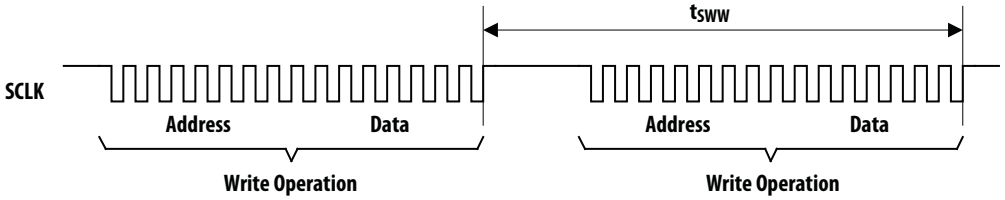


Figure 13. Timing between two write commands

If the rising edge of the SCLK for the last data bit of the second write command occurs before the required delay (t_{SWW}), then the first write command may not complete correctly.

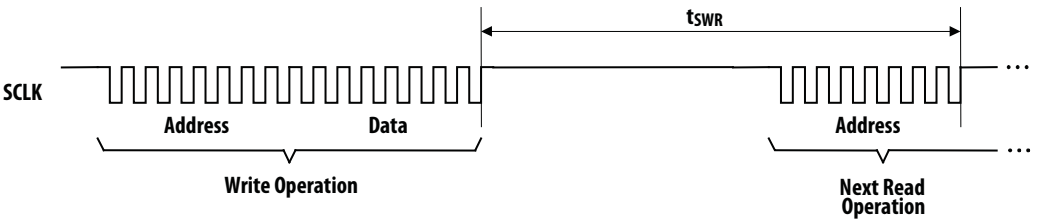


Figure 14. Timing between write and read commands

If the rising edge of SCLK for the last address bit of the read command occurs before the required delay (t_{SWR}), the write command may not complete correctly.

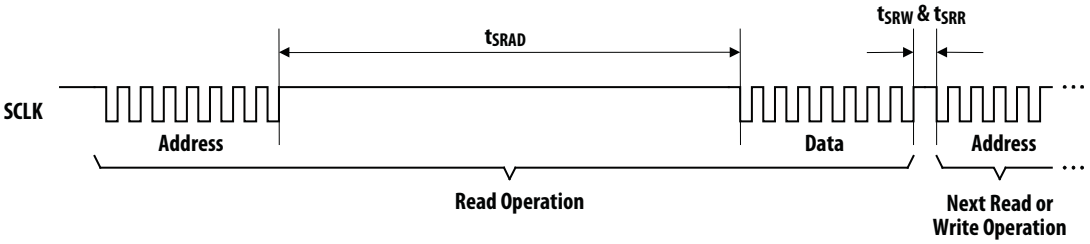


Figure 15. Timing between read and either write or subsequent read commands

During a read operation SCLK should be delayed at least t_{SRAD} after the last address data bit to ensure that the ADBS-A320 has time to prepare the requested data. The falling edge of SCLK for the first address bit of either the read or write command must be at least t_{SRR} or t_{SRW} after the last SCLK rising edge of the last data bit of the previous read operation.

Burst Mode Operation

Burst mode is a special serial port operation mode that may be used to reduce the serial transaction time for a motion read. The speed improvement is achieved by continuous data clocking from multiple registers without the need to specify the register address, and by not requiring the normal delay period between data bytes.

Burst mode is activated by writing 0x10 to register 0x1c IO_MODE. Then the burst mode data can be read by reading the Motion register 0x02. The ADBS-A320 will respond with the contents of the Motion, Delta_Y, Delta_X, SQUAL, Shutter_Upper, Shutter_Lower and Maximum_Pixel registers in that order. The burst transaction can be terminated after the first 3 bytes of the sequence are read by bringing the NCS pin high. After sending the register address, the micro-controller must wait t_{SRAD} and then begin reading data. All data bits can be read with no delay between bytes by driving SCLK at the normal rate. The data is latched into the output buffer after the last address bit is received. After the burst transmission is complete, the micro-controller must raise the NCS line for at least t_{BEXIT} to terminate burst mode. The serial port is not available for use until it is reset with NCS, even for a second burst transmission.

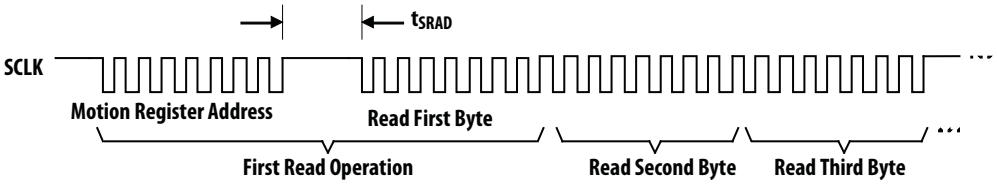


Figure 16. Motion Burst Timing

Two – Wire Interface (TWI)

ADBS-A320 uses a two-wire serial control interface compatible with I2C. The parameters are listed below.

Electrical Characteristics at 25°C, V_{DDA}=2.8V, DV_{DD}=1.8V.

Parameter	Symbol	Minimum	Maximum	Units	Notes
SCL clock frequency	fscl		400	kHz	
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	0.6	–	µs	
LOW period of the SCL clock	t_{LOW}	1.0	–	µs	
HIGH period of the SCL clock	t_{HIGH}	0.6	–	µs	
Set up time for a repeated START condition	$t_{SU;STA}$	0.6	–	µs	
Data hold time	$t_{HD;DAT}$	0(2)	0.9(3)	µs	
Data set-up time	$t_{SU;DAT}$	100	–	ns	
Rise time of both SDA and SCL signals	t_r	20+0.1C_b(4)	300	ns	
Fall time of both SDA and SCL signals	t_f	20+0.1C_b(4)	300	ns	
Set up time for STOP condition	$t_{SU;STO}$	0.6	–	µs	
Bus free time between a STOP and START condition	t_{BUF}	1.3	–	µs	
Capacitive load for each bus line	C_b	–	400	pF	
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	0.1 VDDA	–	V	
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	0.2 V_{DDA}		V	

Notes:
1. All values referred to V_{IHMIN} and V_{ILMAX} levels.
2. A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum has $t_{HD;DAT}$ only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
4. C_B = total capacitance of one bus line in pF.

The ADBS-A320 responds to one of the following selectable slave device addresses depending on the IO_A0 and IO_A1 input pin state. These pins should be set to avoid conflict with any other devices that might be sharing the bus.

Table 1. TWI slave address

A0	A1	Slave Address (Hex)
0	0	33
0	1	37
0	NC	3b
1	0	53
1	1	57
1	NC	5b
NC	0	63
NC	1	67
NC	NC	6b

Serial Transfer Clock and Serial Data signals

The serial control interface uses two signals: a serial transfer clock (SCL) signal and a serial data (SDA) signal. Always driven by the master, SCL synchronizes the serial transmission of data bits on SDA. The frequency of SCL may vary throughout a transfer, as long as the timing is greater than the minimum timing.

SDA is bi-directional. The host (master) can read from or write to the ADBS-A320. The host (typically a microcontroller) drives SCL and SDA in a write operation or requesting information from the ADBS-A320. The ADBS-A320 drives the SDA only under two conditions. First, when responding with an acknowledge (ACK) bit after receiving data from the host, or second, when sending data to the host at the host's request. Data is sent in Eight-bit packets.

Start and Stop of Synchronous Operation

The host initiates and terminates all data transfers. Data transfers are initiated by driving SDA from high to low while holding SCL high. Data transfers are terminated by driving SDA from low to high while SCL is held high.

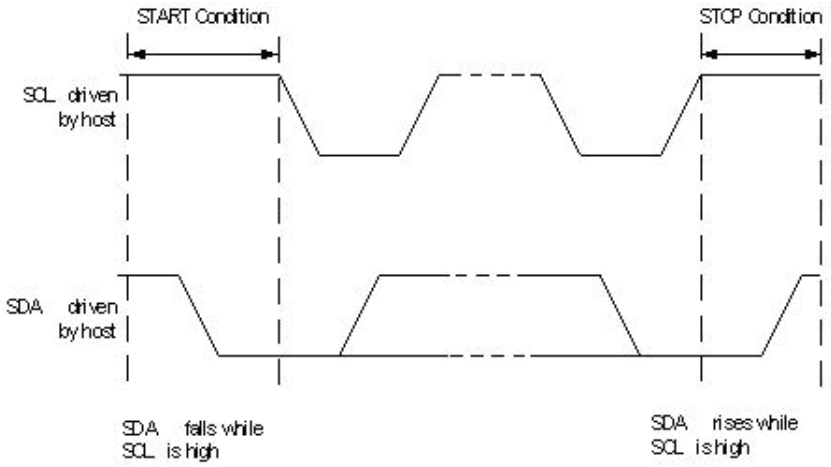


Figure 17. TWI Start and Stop operation

Acknowledge/Not Acknowledge Bit

After a start condition, a single acknowledge/not acknowledge bit follows each Eight-bit data packet. The device receiving the data drives the acknowledge/not acknowledge signal on SDA. Acknowledge (ACK) is defined as 0 and not acknowledge (NAK) is defined as 1.

Packet Formats

Read and write operations between the host and the ADBS-A320 use three types of host driven packets and one type of ADBS-A320 driven packet. All packets are eight bits long with the most significant bit first, followed by an acknowledge bit.

Slave Device Address (DA)

Command packets contain a 7-bit ADBS-A320 device address and an active low read/write bit (R/W).

First bit of packet							Last bit of packet
Device Address							R/$\overline{W}$
DA[6]	DA[5]	DA[4]	DA[3]	DA[2]	DA[1]	DA[0]	Write = 0 Read = 1

Register Address Packets (RA)

The address packets contain an auto-increment (ai) bit and a 7-bit address. If the 'ai' bit is set, the slave will process data from successive addresses in successive bytes. For example, registers 0x01, 0x02, and 0x03 can be written by setting the 'ai' bit to one with address 0x01. The host would send three bytes of data, and the host would terminate with a P condition.

First bit of packet							Last bit of packet
Auto increment	Register Address						
Auto increment=1, No increment=0	RA[6]	RA[5]	RA[4]	RA[3]	RA[2]	RA[1]	RA[0]

Data Packet (DP)

Contains 8 data bits and may be sent by the host or the ADBS-A320.

First bit of packet							Last bit of packet
Data							
DP[7]	DP[6]	DP[5]	DP[4]	DP[3]	DP[2]	DP[1]	DP[0]

Host Driven Packets

The host initiates all data transmission with a START condition. Next, slave address and register address packets are sent. If there is a device address match, the ADBS-A320 then responds to each Eight-bit data transmission with an acknowledge signal (SDA = 0). Data is transmitted with the most significant bit first.

To terminate the transfer of host driven packets, the host follows the ADBS-A320's ACK with a STOP condition. The host can also issue a START condition after the ADBS-A320's ACK if it wants to start a new data transfer.

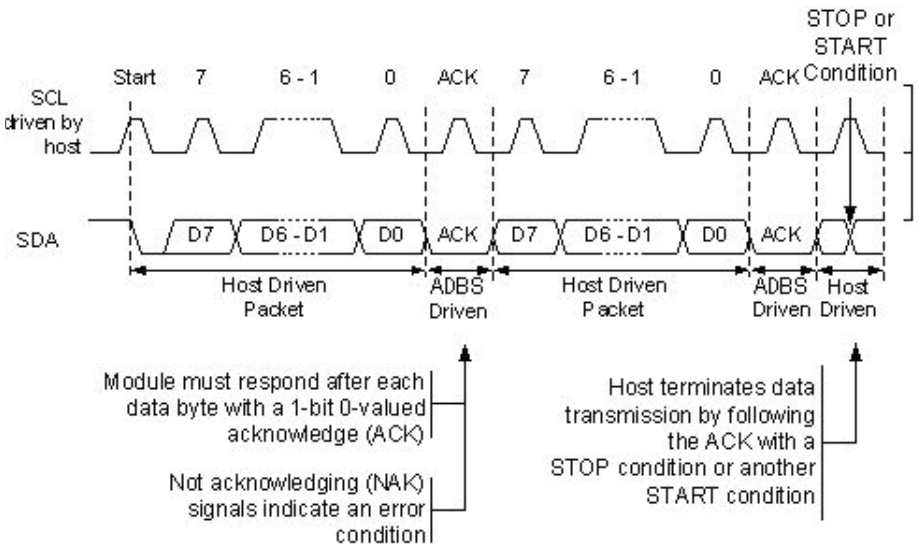


Figure 18. Host packets

ADBS-A320 Driven Packets

By request of the host, the ADBS-A320 acknowledges a read request and then outputs a data byte transmitting the most significant bit (7) first. If the host intends to continue the data transfer, the host acknowledges the ADBS-A320. If the host intends to terminate the transfer, it responds with not acknowledge (SDA = 1), and then drives SDA to generate a STOP condition. The host can also drive a START condition if it wants to begin a new data transfer with the same ADBS-A320.

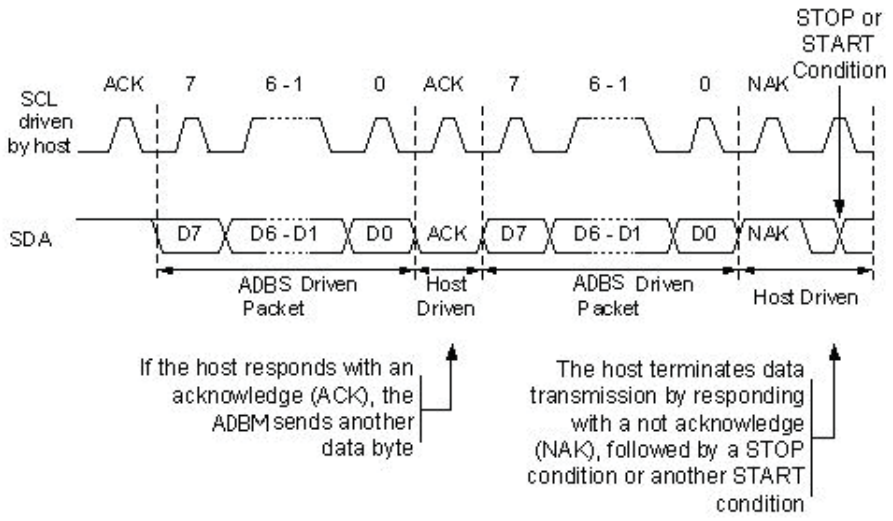


Figure 19. Sensor packets

Example: Writing Data to Sensor Registers

The host writes a value of 0x02 to address 0x07 in the following illustration.

The example ADBS-A320 address is 0x57.

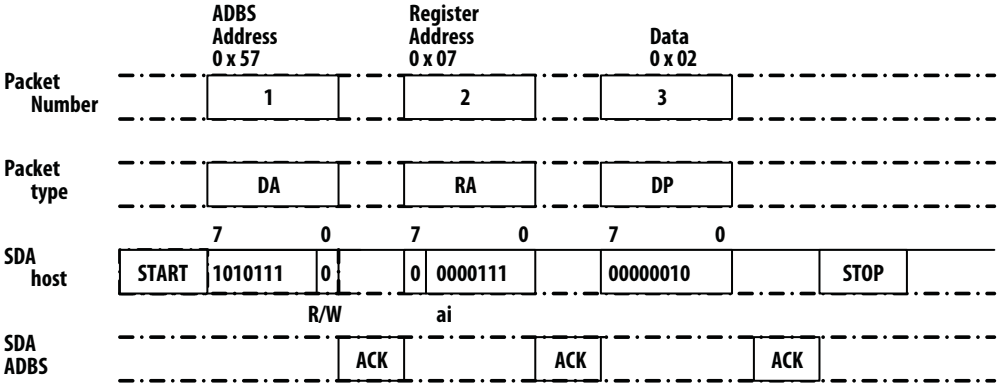


Figure 20. TWI write

Example: Single Byte Read from Sensor Register

The sensor reads a value 0x01from the register address 0x02 in the following illustration. Again, the example ADBS-A320 address is 0x57.

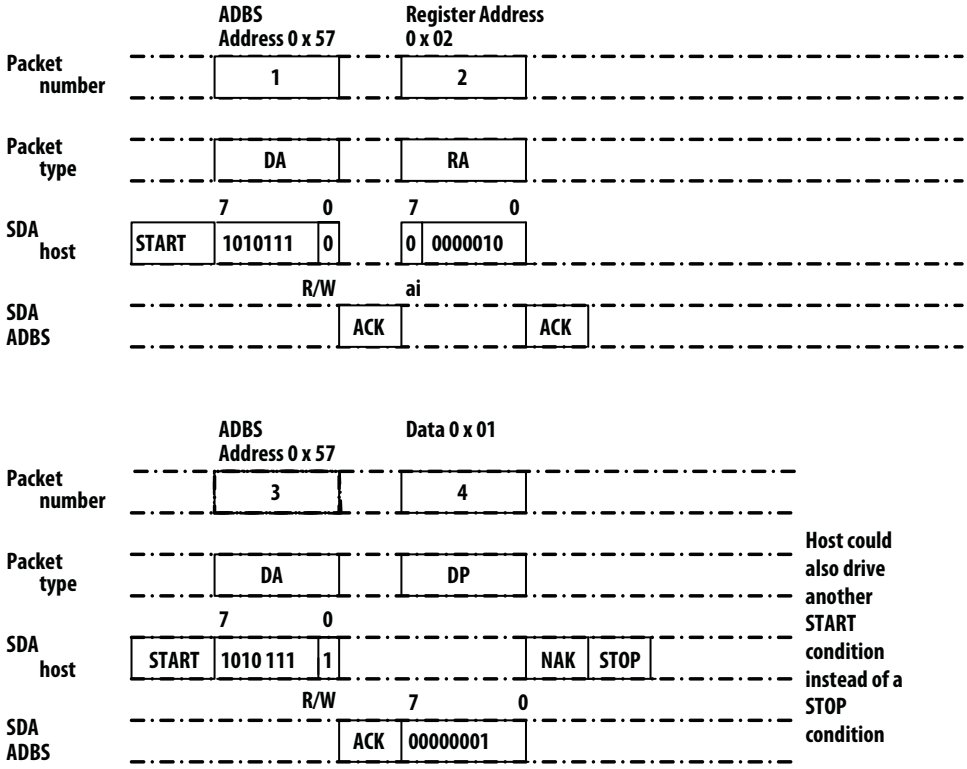


Figure 21. TWI single byte read

Example: Polling of Status register (X-Y Motion Bit and Button bits)

To poll the STATUS register, the following structure can be used:

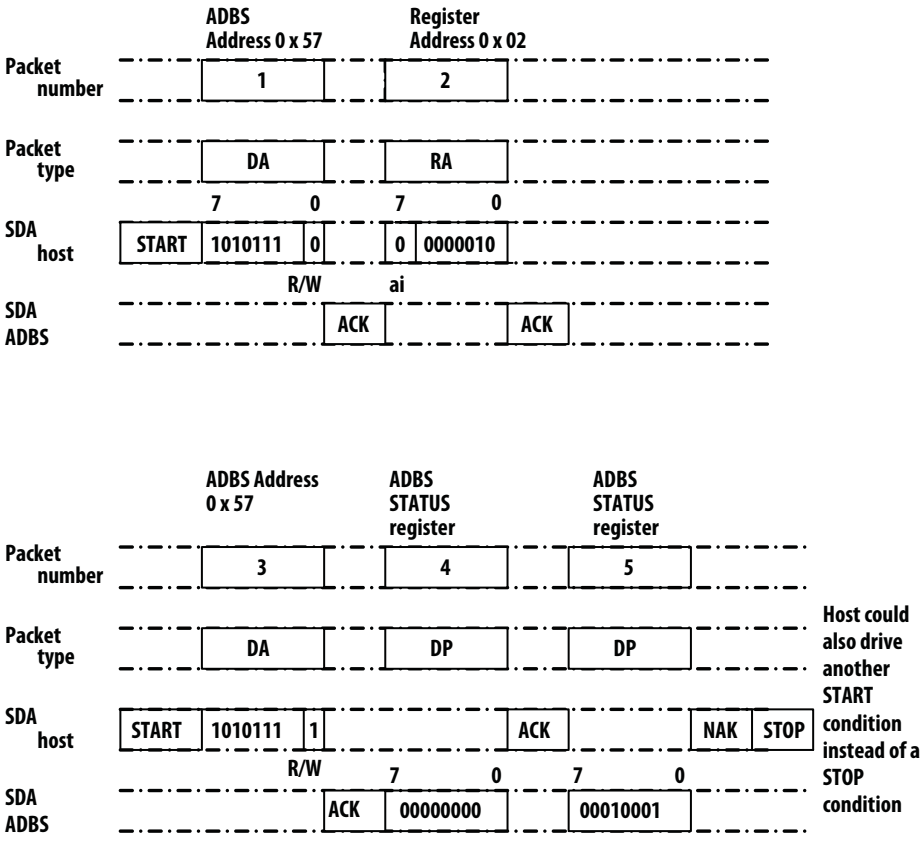


Figure 22. TWI polling

In this case, the host read ADBS-A320 data packets until the update bit (bit 4). Then the host could read successive registers using the ai bit example below.

Note: polling the Status register rather than using the DATA_RDY pin increases power consumption

Example: Multiple-Byte Read from Sensor Register using 'ai' bit

The ai is a useful feature, especially in the case of reading Delta_X, Delta_Y, and Delta_HI in succession once either the DATA_RDY interrupt pin and/or update bit in the STATUS register bit are set.

Once the ai bit is set, the slave will deliver data packets from successive addresses until the 'STOP' condition from the host.

In the example below, 3 bytes are read successively from registers 0x03, 0x04, and 0x05.

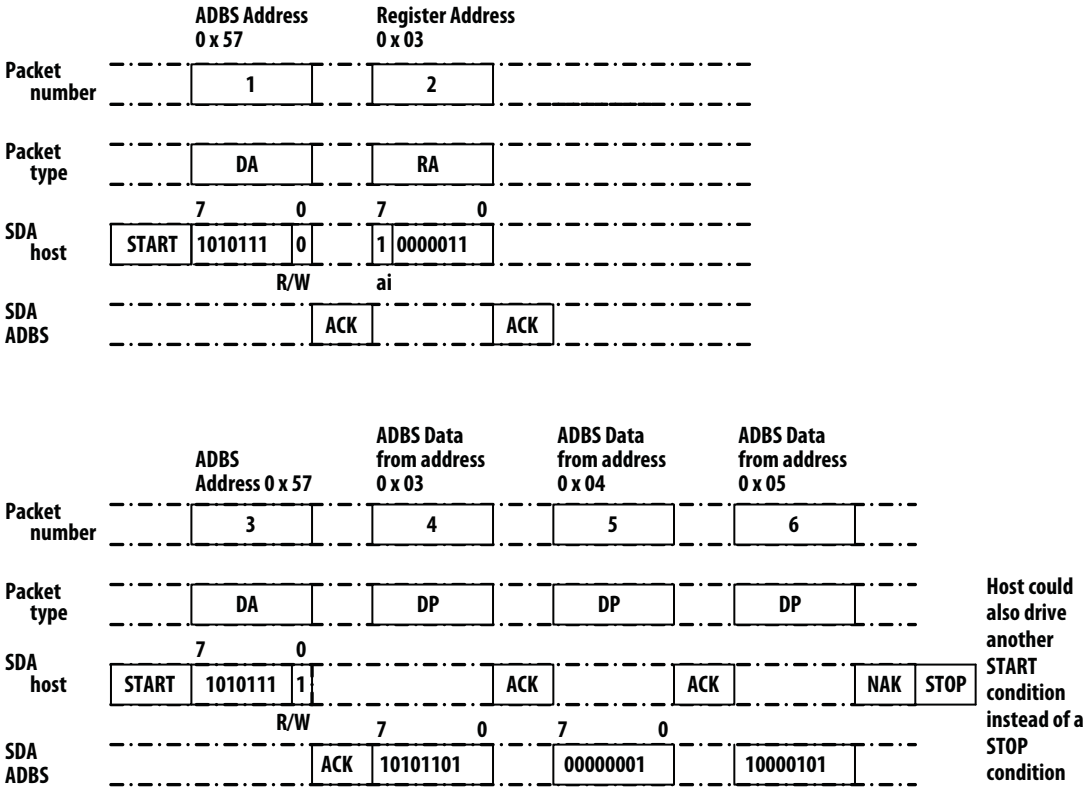


Figure 23. TWI ai bit

SCL and SDA Timing

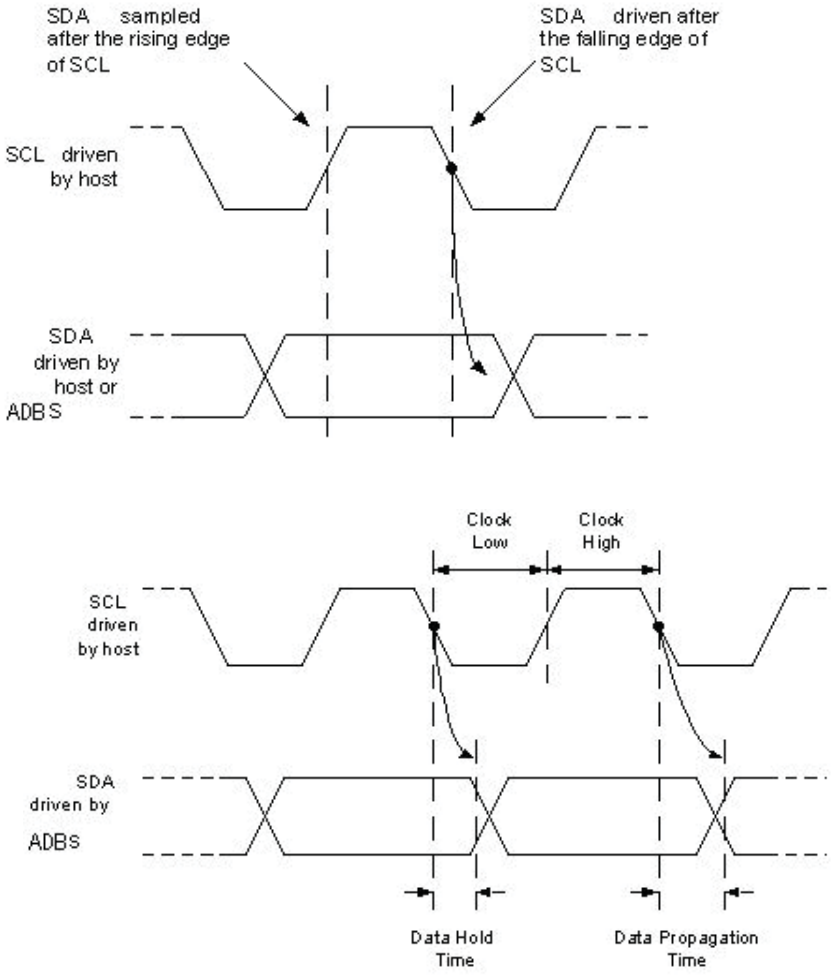


Figure 24. TWI SCL and SDA Timing

ADBS-A320 driven SDA

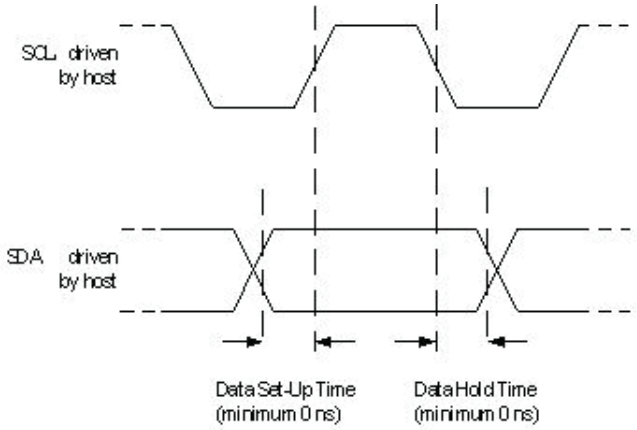


Figure 25. Sensor driven SDA

ADBS-A320 I2C communication requirement

There are several I2C timing sequences which must be observed for OFN sensors. They are listed below.

I2C during hard reset

During I2C communication and sensor hard reset via NRST, it is suggested to have I2C idle time of 5usec before and after NRST is released. The I2C lines, IO_MISO_SDA and IO_CLK has to be quiet 5usec before and after NRST is pulled high to ensure normal operation of the I2C lines. Any I2C communication before and after the I2C quiet time of 5usec period can continue on the I2C bus. See figure26 for timing diagram.

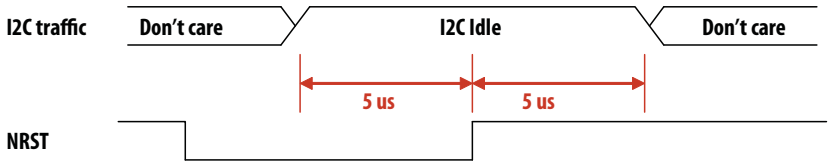


Figure 26. I2C quiet time during NRST

I2C during shutdown after hard reset

I2C quiet time must be observed if shutdown is used after a hard reset is initiated. When hard reset or NRST is initiated, figure 26 requirements must be observed where 5usec I2C quiet time must be observed before and after NRST is set to high. Then if a shutdown is pulled high after NRST is high, another 5usec I2C quiet time is required before I2C bus line can continue communication. See figure 27 for the timing diagram.

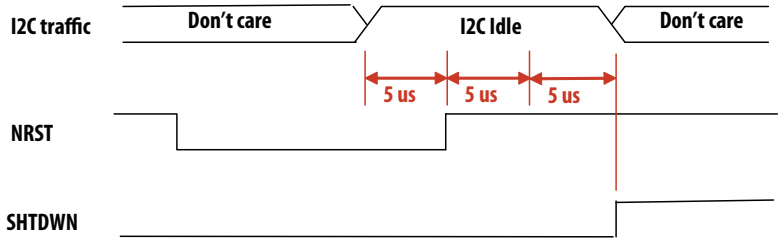


Figure 27. I2C quiet time for shutdown after hard reset

I2C during hard reset after shutdown

An I2C quiet time must be observed when a hard reset NRST is initiated after a valid shutdown. The I2C quiet time requirement for this condition is specified in this section although this operating condition is very unlikely to be used in most applications as it is not necessary to initiate hard reset after recovery from shutdown.

If NRST is pulled high within or after shutdown, an additional I2C quiet time of 275usec for internal regulator enabled or 490usec for internal regulator disabled, from shutdown being pulled low is needed on top of the 5usec before and after NRST being pulled high as mentioned earlier in figure 26. See figure 28 and Table for complete timing requirements.

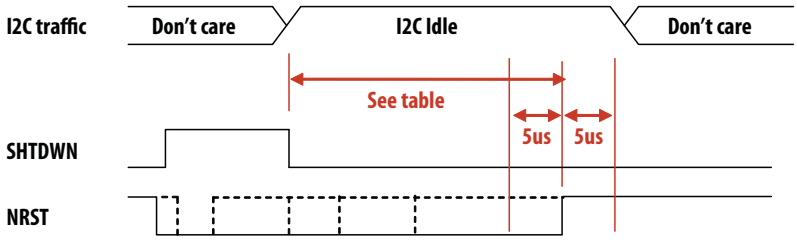


Figure 28. I2C quiet time for hard reset after shutdown

	Internal regulator enabled	Internal regulator disabled
Time (usec)	275	490

Registers

The ADBS-A320 registers are accessible via the serial port. The registers are used to read motion data and status as well as to set the device configuration.

Address	Register	Read/ Write	Default Value	Address	Register	Read/ Write	Default Value
0x00	Product_ID*	R	0x83	0x40-0x5f	Reserved		
0x01	Revision_ID*	R	0x01	0x60	OFN_Engine*	R/W	0x00
0x02	Motion	R/W	Any	0x61	Reserved		
0x03	Delta_X	R	Any	0x62	OFN_Resolution*	R/W	0x1a
0x04	Delta_Y	R	Any	0x63	OFN_Speed_Control*	R/W	0x04
0x05	SQUAL	R	Any	0x64	OFN_Speed_ST12*	R/W	0x08
0x06	Shutter_Upper	R	Any	0x65	OFN_Speed_ST21*	R/W	0x06
0x07	Shutter_Lower	R	Any	0x66	OFN_Speed_ST23*	R/W	0x40
0x08	Maximum_Pixel	R	Any	0x67	OFN_Speed_ST32*	R/W	0x08
0x09	Pixel_Sum	R	Any	0x68	OFN_Speed_ST34*	R/W	0x48
0x0a	Minimum_Pixel	R	Any	0x69	OFN_Speed_ST43*	R/W	0x0a
0x0b	Pixel_Grab	R/W	Any	0x6a	OFN_Speed_ST45*	R/W	0x50
0x0c	CRC0*	R	0x00	0x6b	OFN_Speed_ST54*	R/W	0x48
0x0d	CRC1*	R	0x00	0x6c	Reserved		
0x0e	CRC2*	R	0x00	0x6d	OFN_AD_CTRL*	R/W	0xc4
0x0f	CRC3*	R	0x00	0x6e	OFN_AD_ATH_HIGH*	R/W	0x34
0x10	Self_Test	W	0x00	0x6f	OFN_AD_DTH_HIGH*	R/W	0x3c
0x11	Configuration_Bits*	R/W	0x00	0x70	OFN_AD_ATH_LOW*	R/W	0x18
0x12-0x19	Reserved			0x71	OFN_AD_DTH_LOW*	R/W	0x20
0x1a	LED_Control*	R/W	0x00	0x72	Reserved		
0x1b	Reserved			0x73	OFN_Quantize_CTRL*	R/W	0x99
0x1c	IO_Mode*	R/W	0x00	0x74	OFN_XYQ_THRESH*	R/W	0x02
0x1d	Motion_Control	W	0x00	0x75	OFN_FPD_CTRL*	R/W	0x50
0x1e-0x2d	Reserved			0x76	Reserved		
0x2e	Observation	R/W	Any	0x77	OFN_Orientation_CTRL*	R/W	0x01
0x2f-0x39	Reserved						
0x3a	Soft_RESET	W	0x00				
0x3b	Shutter_Max_Hi*	R/W	0x0b				
0x3c	Shutter_Max_Lo*	R/W	0x71				
0x3d	Reserved						
0x3e	Inverse_Revision_ID*	R	0xFE				
0x3f	Inverse_Product_ID*	R	0x7C				

* Note - Registers with * will retain the same register values before and after shutdown if the supply voltages remain above their minimum values. In any case where there is a need to disable VDDA during shutdown, it is advisable that the register values are reloaded after VDDA is enabled to prevent any loss in register settings during VDDA cycling.

Product_ID Address: 0x00
Access: Read Reset Value: 0x83

Bit	7	6	5	4	3	2	1	0
Field	PID_7	PID_6	PID_5	PID_4	PID_3	PID_2	PID_1	PID_0

Data Type: 8-Bit unsigned integer.

USAGE: This register contains a unique identification assigned to the ADBS-A320. The value in this register does not change; it can be used to verify that the serial communications link is functional.

Revision_ID Address: 0x01
Access: Read Reset Value: 0x01

Bit	7	6	5	4	3	2	1	0
Field	RID_7	RID_6	RID_5	RID_4	RID_3	RID_2	RID_1	RID_0

Data Type: 8-Bit unsigned integer.

USAGE: This register contains the IC revision. It is subject to change when new IC versions are released.

Motion			Address: 0x02					
Access: Read/Write			Reset Value: Any					
Bit	7	6	5	4	3	2	1	0
Field	MOT	PIXRDY	PIXFIRST	OVF	Reserved	Reserved	Reserved	GPIO

Data Type: Bit field.

USAGE: Register 0x02 allows the user to determine if motion has occurred since the last time it was read. If the MOT bit is set, then the user should read registers 0x03 and 0x04 to get the accumulated motion. Read this register before reading the Delta_Y and Delta_X registers.

Writing anything to this register clears the MOT and OVF bits, Delta_Y and Delta_X registers. The written data byte is not saved.

Internal buffers can accumulate more than eight bits of motion for X or Y. If either one of the internal buffers overflows, then absolute path data is lost and the OVF bit is set. This bit is cleared once some motion has been read from the Delta_X and Delta_Y registers, and if the buffers are not at full scale. Since more data is present in the buffers, the cycle of reading the Motion, Delta_X and Delta_Y registers should be repeated until the motion bit (MOT) is cleared. Until MOT is cleared, either the Delta_X or Delta_Y registers will read either positive or negative full scale. If the motion register has not been read for long time, at 500 cpi it may take up to 16 read cycles to clear the buffers, at 1000 cpi, up to 32 cycles. To clear an overflow, write anything to this register.

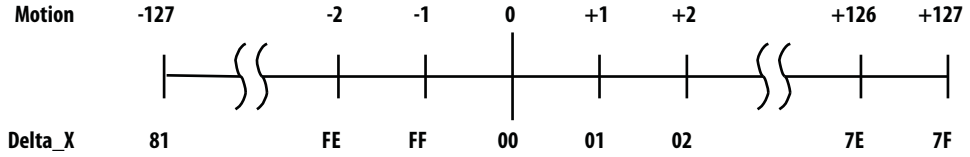
The PIXRDY bit will be set whenever a valid pixel data byte is available in the Pixel_Dump register. Check that this bit is set before reading from Pixel_Dump. To ensure that the Pixel_Grab pointer has been reset to pixel 0,0 on the initial write to Pixel_Grab, check to see if PIXFIRST is set to high.

Field Name	Description
MOT	Motion since last report **0 = No motion** 1 = Motion occurred, data ready for reading in Delta_X and Delta_Y registers
PIXRDY	Pixel Dump data byte is available in Pixel_Dump register **0 = data not available** 1 = data available
PIXFIRST	This bit is set when the Pixel_Grab register is written to or when the complete pixel array has been read, initiating an increment to pixel 0,0. **0 = Pixel_Grab data not from pixel 0,0** 1 = Pixel_Grab data is from pixel 0,0
OVF	Motion overflow, ΔY and/or ΔX buffer has overflowed since last report **0 = no overflow** 1 = Overflow has occurred
GPIO	Reports GPIO status (read only) 0 = low 1 = high

Delta_X			Address: 0x03					
Access: Read			Reset Value: Any					
Bit	7	6	5	4	3	2	1	0
Field	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0

Data Type: Eight bit 2's complement number.

USAGE: X movement is counts since last report. Absolute value is determined by resolution. Reading clears the register.



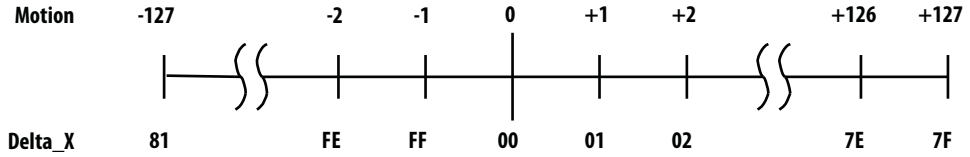
		Delta X
ORIENT PIN HIGH	Maximum	+127
	Minimum	-127
ORIENT PIN LOW	Maximum	+127
	Minimum	-127

NOTES: Avago RECOMMENDS that registers 0x03 and 0x04 be read sequentially.

Delta_Y			Address: 0x04					
Access: Read			Reset Value: Any					
Bit	7	6	5	4	3	2	1	0
Field	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0

Data Type: Eight bit 2's complement number.

USAGE: Y movement is counts since last report. Absolute value is determined by resolution. Reading clears the register.



		Delta Y
ORIENT PIN HIGH	Maximum	+127
	Minimum	-127
ORIENT PIN LOW	Maximum	+127
	Minimum	-128

NOTES: Avago RECOMMENDS that registers 0x03 and 0x04 be read sequentially.

SQUAL Address: 0x05
Access: Read Reset Value: Any

Bit	7	6	5	4	3	2	1	0
Field	SQ_7	SQ_6	SQ_5	SQ_4	SQ_3	SQ_2	SQ_1	SQ_0

Data Type: Upper 8 bits of a 9-bit unsigned integer.

USAGE: SQUAL (Surface Quality) is a measure of the number of valid features visible by the sensor in the current frame. The maximum SQUAL register value is 167. Since small changes in the current frame can result in changes in SQUAL, variations in SQUAL when looking at a surface are expected.

Shutter_Upper Address: 0x06
Access: Read Reset Value: Any

Bit	7	6	5	4	3	2	1	0
Field	S_{15}	S_{14}	S_{13}	S_{12}	S_{11}	S_{10}	S_9	S_8

Shutter_Lower Address: 0x07
Access: Read Reset Value: Undefined

Bit	7	6	5	4	3	2	1	0
Field	S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0

Data Type: Sixteen bit unsigned integer.

USAGE: Units are clock cycles. Read Shutter_Upper first, then Shutter_Lower. They should be read consecutively. The shutter is adjusted to keep the average and maximum pixel values within normal operating ranges. The shutter value is automatically adjusted.

Maximum_Pixel Address: 0x08
Access: Read Reset Value: Any

Bit	7	6	5	4	3	2	1	0
Field	MP_7	MP_6	MP_5	MP_4	MP_3	MP_2	MP_1	MP_0

Data Type: Eight-bit number.

USAGE: Maximum Pixel value in current frame. Minimum value = 0, maximum value = 254. The maximum pixel value can vary with every frame.

Pixel_Sum Address: 0x09
Access: Read Reset Value: Any

Bit	7	6	5	4	3	2	1	0
Field	AP_7	AP_6	AP_5	AP_4	AP_3	AP_2	AP_1	AP_0

Data Type: High 8 bits of an unsigned 17-bit integer.

USAGE: This register is used to find the average pixel value. It reports the seven bits of a 16-bit counter, which sums all pixels in the current frame. It may be described as the full sum divided by 512. To find the average pixel value, use the following formula:

Average Pixel = Register Value * 128/121 = Register Value * 1.06

The maximum register value is 240. The minimum is 0. The pixel sum value can change every frame.

Minimum_Pixel Address: 0x0a
Access: Read Reset Value: Any

Bit	7	6	5	4	3	2	1	0
Field	MP_7	MP_6	MP_5	MP_4	MP_3	MP_2	MP_1	MP_0

Data Type: Eight-bit number.

USAGE: Minimum Pixel value in current frame. Minimum value = 0, maximum value = 254. The minimum pixel value can vary with every frame.

Pixel_Grab Address: 0x0b
Access: Read/Write Reset Value: Any

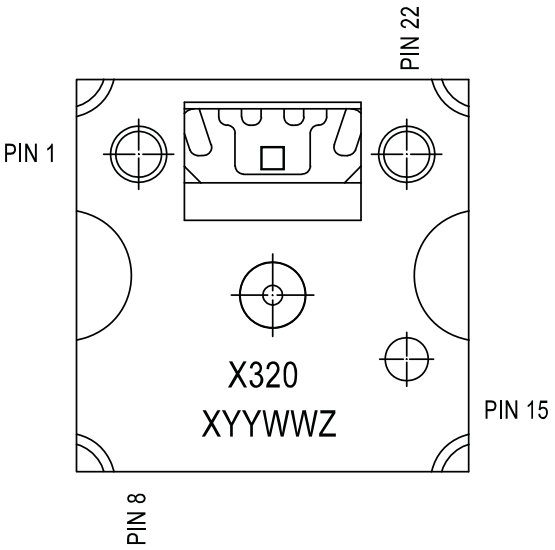
Bit	7	6	5	4	3	2	1	0
Field	PD_7	PD_6	PD_5	PD_4	PD_3	PD_2	PD_1	PD_0

Data Type: Eight-bit word.

USAGE: For test purposes, the sensor will read out the contents of the pixel array, one pixel per frame. To start a pixel grab, write anything to this register to reset the pointer to pixel 0,0. Then read the PIXRDY bit in the Motion register. When the PIXRDY bit is set, there is valid data in this register to read out. After the data in this register is read, the pointer will automatically increment to the next pixel. Reading may continue indefinitely; once a complete frame's worth of pixels has been read, PIXFIRST will be set to high to indicate the start of the first pixel and the address pointer will start at the beginning location again. The pixel map address and corresponding sensor orientation is shown below.

18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19
56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38
75	74	73	72	71	70	69	68	67	66	65	64	63	62	61	60	59	58	57
94	93	92	91	90	89	88	87	86	85	84	83	82	81	80	79	78	77	76
113	112	111	110	109	108	107	106	105	104	103	102	101	100	99	98	97	96	95
132	131	130	129	128	127	126	125	124	123	122	121	120	119	118	117	116	115	114
151	150	149	148	147	146	145	144	143	142	141	140	139	138	137	136	135	134	133
170	169	168	167	166	165	164	163	162	161	160	159	158	157	156	155	154	153	152
189	188	187	186	185	184	183	182	181	180	179	178	177	176	175	174	173	172	171
208	207	206	205	204	203	202	201	200	199	198	197	196	195	194	193	192	191	190
227	226	225	224	223	222	221	220	219	218	217	216	215	214	213	212	211	210	209
246	245	244	243	242	241	240	239	238	237	236	235	234	233	232	231	230	229	228
265	264	263	262	261	260	259	258	257	256	255	254	253	252	251	250	249	248	247
284	283	282	281	280	279	278	277	276	275	274	273	272	271	270	269	268	267	266
303	302	301	300	299	298	297	296	295	294	293	292	291	290	289	288	287	286	285
322	321	320	319	318	317	316	315	314	313	312	311	310	309	308	307	306	305	304
341	340	339	338	337	336	335	334	333	332	331	330	329	328	327	326	325	324	323
360	359	358	357	356	355	354	353	352	351	350	349	348	347	346	345	344	343	342

Figure 29. Top view of pixel map address without lens



Sensor orientation mounted without lens

342	343	344	345	346	347	348	349	350	351	352	353	354	355	356	357	358	359	360
323	324	325	326	327	328	329	330	331	332	333	334	335	336	337	338	339	340	341
304	305	306	307	308	309	310	311	312	313	314	315	316	317	318	319	320	321	322
285	286	287	288	289	290	291	292	293	294	295	296	297	298	299	300	301	302	303
266	267	268	269	270	271	272	273	274	275	276	277	278	279	280	281	282	283	284
247	248	249	250	251	252	253	254	255	256	257	258	259	260	261	262	263	264	265
228	229	230	231	232	233	234	235	236	237	238	239	240	241	242	243	244	245	246
209	210	211	212	213	214	215	216	217	218	219	220	221	222	223	224	225	226	227
190	191	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207	208
171	172	173	174	175	176	177	178	179	180	181	182	183	184	185	186	187	188	189
152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167	168	169	170
133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149	150	151
114	115	116	117	118	119	120	121	122	123	124	125	126	127	128	129	130	131	132
95	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113
76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94
57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75
38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56
19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18

Figure 30. Top view of pixel map address with lens

CRC0			Address: 0x0c					
Access: Read			Reset Value: 0x00					
Bit	7	6	5	4	3	2	1	0
Field	$CRC0_7$	$CRC0_6$	$CRC0_5$	$CRC0_4$	$CRC0_3$	$CRC0_2$	$CRC0_1$	$CRC0_0$

Data Type: Eight-bit number

USAGE: Register 0x0c reports the first byte of the system self test results. See Self Test register 0x10.

CRC1			Address: 0x0d					
Access: Read			Reset Value: 0x00					
Bit	7	6	5	4	3	2	1	0
Field	$CRC1_7$	$CRC1_6$	$CRC1_5$	$CRC1_4$	$CRC1_3$	$CRC1_2$	$CRC1_1$	$CRC1_0$

Data Type: Eight-bit number

USAGE: Register 0x0d reports the second byte of the system self test results. See Self Test register 0x10.

CRC2			Address: 0x0e					
Access: Read			Reset Value: 0x00					
Bit	7	6	5	4	3	2	1	0
Field	$CRC2_7$	$CRC2_6$	$CRC2_5$	$CRC2_4$	$CRC2_3$	$CRC2_2$	$CRC2_1$	$CRC2_0$

Data Type: Eight-bit number

USAGE: Register 0x0e reports the third byte of the system self test results. See Self Test register 0x10.

CRC3			Address: 0x0f					
Access: Read			Reset Value: 0x00					
Bit	7	6	5	4	3	2	1	0
Field	$CRC3_7$	$CRC3_6$	$CRC3_5$	$CRC3_4$	$CRC3_3$	$CRC3_2$	$CRC3_1$	$CRC3_0$

Data Type: Eight-bit number

USAGE: Register 0x0f reports the fourth byte of the system self test results. See Self Test register 0x10.

Self_Test Address: 0x10
Access: Write Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	TESTEN

Data Type: Bit field

USAGE: Set the TESTEN bit in register 0x10 to start the system self-test. The test takes 250ms. During this time, do not write or read through the SPI port. Results are available in the CRC0-3 registers. After self-test, reset the chip to start normal operation.

The procedure to start self test is as follows:-

1. Write 0x5a to register 0x3a to initiate soft reset. Do not load OFN registers.
2. Write data 0xF6 to register 0x60.
3. Write data 0xAA to register 0x73.
4. Write data 0xC4 to register 0x63.
5. Write 0x01 to register 0x10 to initiate self test.
6. Wait 250ms.
7. Read from CRC0 from address 0x0c, CRC1 from address 0x0d, CRC2 from address 0x0e, CRC3 from address 0x0f.

The results are as follows.

CRC#	**Orient = 1**	**Orient = 0**
CRC0	0x36	0x33
CRC1	0x72	0x8E
CRC2	0x7F	0x24
CRC3	0xD6	0x6C

Field Name	**Description**
TESTEN	Enable System Self Test **0 = Disable** 1 = Enable

Configuration_bits Address: 0x11
Access: Read/Write Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	RES	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Data Type: Bit field

USAGE: Register 0x11 allows the user to change the configuration of the sensor. The RES bit allows selection between 500 and 1000 cpi resolution.

Field Name	**Description**
RES	Sets resolution **0 = 500** 1 = 1000

Reserved Address: 0x12-0x19

LED_Control Address: 0x1a
Access: Read/Write Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	Reserved	Reserved	Reserved	Reserved	Reserved	LED2	LED1	LED0

Data Type: Bit field

USAGE: Register 0x1a allows the user to change the LED drive current of the sensor.

Field Name	Description
LED2:0	**0x00 = 13mA** 0x03 = 40mA 0x05 = 9.6mA

Reserved Address: 0x1b

IO_Mode Address: 0x1c
Access: Read/Write Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	Reserved	Reserved	Reserved	Burst	Reserved	SPI	Reserved	TWI

Data Type: Bit field

USAGE: Register 0x1c allows the user to read the Input or Output mode of the sensor.

Field Name	Description
Burst	Burst mode **0 = not in burst mode** 1 = In Burst mode
SPI	SPI mode **0 = not in SPI mode** 1 = In SPI mode
TWI	TWI mode **0 = not in TWI mode** 1 = In TWI mode

Motion_Control Address: 0x1d
Access: Write Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	Control	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Data Type: Bit field

USAGE: Register 0x1d allows the user to control and read the Motion pin state.

Field Name	Description
Control	Motion control pin **0 = set Motion pin active low. Motion pin will go low when motion is present.** 1 = set Motion pin active high

Reserved Address: 0x1e-0x2d

Observation Address: 0x2e
Access: Read/Write Reset Value: Any

Bit	7	6	5	4	3	2	1	0
Field	$MODE_1$	$MODE_0$	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Data Type: Bit field

USAGE: Register 0x2e provides bits that are set every frame. It can be used during ESD testing to check that the chip is running correctly. Writing anything to this register will clear the bits.

Field Name	Description
$MODE_{1-0}$	Mode Status: Reports which mode the sensor is in. 00 = Run 01 = Rest1 10 = Rest2 11 = Rest3

Reserved Address: 0x2f-0x39

Soft_RESET Address: 0x3a
Access: Write Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	RST_7	RST_6	RST_5	RST_4	RST_3	RST_2	RST_1	RST_0

Data Type: 8-bit integer

USAGE: Write 0x5A to this register to reset the chip. All settings will revert to default values.

Shutter_Max_Hi Address: 0x3b
Access: Read/Write Reset Value: 0x0b

Bit	7	6	5	4	3	2	1	0
Field	SMH_7	SMH_6	SMH_5	SMH_4	SMH_3	SMH_2	SMH_1	SMH_0

Data Type: 8-Bit integer

USAGE: This value is the upper 8-bit of shutter maximum open time. Shutter value represents pixel array exposure time in multiples of internal clock cycles with maximum value at 2929decimal.

Shutter_Max_Lo Address: 0x3c
Access: Read/Write Reset Value: 0x71

Bit	7	6	5	4	3	2	1	0
Field	SML_7	SML_6	SML_5	SML_4	SML_3	SML_2	SML_1	SML_0

Data Type: 8-Bit integer

USAGE: This value is the lower 8-bit of shutter maximum open time. Shutter value represents pixel array exposure time in multiples of internal clock cycles.

Reserved Address: 0x3d

Inverse_Revision_ID Address: 0x3e
Access: Read Reset Value: 0xFE

Bit	7	6	5	4	3	2	1	0
Field	$NRID_7$	$NRID_6$	$NRID_5$	$NRID_4$	$NRID_3$	$NRID_2$	$NRID_1$	$NRID_0$

Data Type: Inverse 8-Bit unsigned integer

USAGE: This value is the inverse of the Revision_ID. It can be used to test the SPI port.

Inverse_Product_ID Address: 0x3f
Access: Read Reset Value: 0x7C

Bit	7	6	5	4	3	2	1	0
Field	$NPID_7$	$NPID_6$	$NPID_5$	$NPID_4$	$NPID_3$	$NPID_2$	$NPID_1$	$NPID_0$

Data Type: Inverse 8-Bit unsigned integer

USAGE: This value is the inverse of the Product_ID. It can be used to test the SPI port.

Reserved Address: 0x40-0x5f

OFN_Engine Address: 0x60
Access: Read/Write Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	Engine	Speed	Assert/ Deassert	XYQ	Reserved	Finger	XY_Scale	Reserved

Data Type: Bit field

USAGE: This register is used to set several properties of the sensor.

Field Name	Description
Engine	Sets optical finger navigation properties. 0 = Disable properties 1 = Enable properties
Speed	Sets speed switching 0 = Disable speed switching 1 = Enable speed switching
Assert/Deassert	Sets Assert/Deassert mode 0 = Disable Assert/Deassert 1 = Enable Assert/Deassert
XY Q	Sets XY quantization 0 = Disable quantization 1 = Enable quantization
Finger	Sets finger presence detection 0 = Disable finger presence detection 1 = Enable finger presence detection
XY_Scale	Sets scaling factor for XY 0 = Disable scaling 1 = Enable scaling

Reserved Address: 0x61

OFN_Resolution Address: 0x62
Access: Read/Write Reset Value: 0x1a

Bit	7	6	5	4	3	2	1	0
Field	Reserved	Reserved	$WakeRES_2$	$WakeRES_1$	$WakeRES_0$	RES_2	RES_1	RES_0

Data Type: Bit field

USAGE: This register is used to set several properties of the sensor.

Field Name	Description
$WakeRES_{2:0}$	Sets resolution when sensor wakes up from rest modes. Effective is speed switching is enabled. 0x01 : 250cpi 0x02 : 500cpi 0x03 : 750cpi 0x04 : 1000cpi 0x05 : 1250cpi
$RES_{2:0}$	Reads resolution of sensor 0x01 : 250cpi 0x02 : 500cpi 0x03 : 750cpi 0x04 : 1000cpi 0x05 : 1250cpi

OFN_Speed_Control Address: 0x63
Access: Read/Write Reset Value: 0x04

Bit	7	6	5	4	3	2	1	0
Field	Y_scale	X_scale	Reserved	Reserved	SP_IntVal1	SP_IntVal0	Low_cpi	Hi_cpi

Data Type: Bit field

USAGE: This register is used to set several properties of the sensor.

Field Name	Description
Y_scale	Sets scaling factor for Y axis 0 = Disable 1 = Enable scale of Y * 2
X_scale	Sets scaling factor for X axis 0 = Disable 1 = Enable scale of X * 2
SPIntVal 1:0	Speed switching checking interval 0x00: 4ms **0x01: 8ms (default)** 0x02: 12ms 0x03: 16ms
Low_cpi	Sets low cpi when in speed switching mode 0 = Disable 1 = Enable 250cpi
Hi_cpi	Sets high cpi when in speed switching mode 0 = Disable 1 = Enable 1250cpi

OFN_Speed_ST12 Address: 0x64
Access: Read/Write Reset Value: 0x08

Bit	7	6	5	4	3	2	1	0
Field	ST	ST	ST	ST	ST	ST	ST	ST

Data Type: Bit field

USAGE: This register is used to set several speed switching properties of the sensor.

Field Name	Description
ST 7:0	Sets resolution switching from step 1 to 2. Write in hexadecimal value. Formula (in decimal) = Velocity (inch per second) * 8

OFN_Speed_ST21 Address: 0x65
Access: Read/Write Reset Value: 0x06

Bit	7	6	5	4	3	2	1	0
Field	ST	ST	ST	ST	ST	ST	ST	ST

Data Type: Bit field

USAGE: This register is used to set several speed switching properties of the sensor.

Field Name	Description
ST 7:0	Sets resolution switching from step 2 to 1. Write in hexadecimal value. Formula (in decimal) = Velocity (inch per second) * 8

OFN_Speed_ST23 Address: 0x66
Access: Read/Write Reset Value: 0x40

Bit	7	6	5	4	3	2	1	0
Field	ST	ST	ST	ST	ST	ST	ST	ST

Data Type: Bit field

USAGE: This register is used to set several speed switching properties of the sensor.

Field Name	Description
ST 7:0	Sets resolution switching from step 2 to 3. Write in hexadecimal value. Formula (in decimal) = Velocity (inch per second) * 8

OFN_Speed_ST32 Address: 0x67
Access: Read/Write Reset Value: 0x08

Bit	7	6	5	4	3	2	1	0
Field	ST	ST	ST	ST	ST	ST	ST	ST

Data Type: Bit field

USAGE: This register is used to set several speed switching properties of the sensor.

Field Name	Description
ST 7:0	Sets resolution switching from step 3 to 2. Write in hexadecimal value. Formula (in decimal) = Velocity (inch per second) * 8

OFN_Speed_ST34
Access: Read/Write

Address: 0x68
Reset Value: 0x48

Bit	7	6	5	4	3	2	1	0
Field	ST	ST	ST	ST	ST	ST	ST	ST

Data Type: Bit field

USAGE: This register is used to set several speed switching properties of the sensor.

Field Name	Description
ST 7:0	Sets resolution switching from step 3 to 4. Write in hexadecimal value. Formula (in decimal) = Velocity (inch per second) * 8

OFN_Speed_ST43
Access: Read/Write

Address: 0x69
Reset Value: 0x0a

Bit	7	6	5	4	3	2	1	0
Field	ST	ST	ST	ST	ST	ST	ST	ST

Data Type: Bit field

USAGE: This register is used to set several speed switching properties of the sensor.

Field Name	Description
ST 7:0	Sets resolution switching from step 4 to 3. Write in hexadecimal value. Formula (in decimal) = Velocity (inch per second) * 8

OFN_Speed_ST45
Access: Read/Write

Address: 0x6a
Reset Value: 0x50

Bit	7	6	5	4	3	2	1	0
Field	ST	ST	ST	ST	ST	ST	ST	ST

Data Type: Bit field

USAGE: This register is used to set several speed switching properties of the sensor.

Field Name	Description
ST 7:0	Sets resolution switching from step 4 to 5. Write in hexadecimal value. Formula (in decimal) = Velocity (inch per second) * 8

OFN_Speed_ST54 Address: 0x6b
Access: Read/Write Reset Value: 0x48

Bit	7	6	5	4	3	2	1	0
Field	ST	ST	ST	ST	ST	ST	ST	ST

Data Type: Bit field

USAGE: This register is used to set several speed switching properties of the sensor.

Field Name	Description
ST 7:0	Sets resolution switching from step 5 to 4. Write in hexadecimal value. Formula (in decimal) = Velocity (inch per second) * 8

Reserved Address: 0x6c

OFN_AD_CTRL Address: 0x6d
Access: Read/Write Reset Value: 0xc4

Bit	7	6	5	4	3	2	1	0
Field	1	1	Reserved	Reserved	Reserved	ST_HIGH_2	ST_HIGH_1	ST_HIGH_0

Data Type: Bit field

USAGE: This register is used to set Assert De-assert control. Must write 1 to bit 7 and 6.

Field Name	Description
$ST\_HIGH_{2:0}$	0x01 = lowest cpi setting (if lowest resolution is on then is 250cpi or else 500cpi) 0x02 = low cpi setting 0x03 = middle cpi setting **0x04 = higher cpi setting (default)** 0x05 = highest cpi seting (if highest resolution is on then is 1250cpi or else 1000cpi)

OFN_AD_ATH_HIGH Address: 0x6e
Access: Read/Write Reset Value: 0x34

Bit	7	6	5	4	3	2	1	0
Field	ATH_H	ATH_H	ATH_H	ATH_H	ATH_H	ATH_H	ATH_H	ATH_H

Data Type: Bit field

USAGE: This register is used to set HIGH speed Assert shutter threshold.

Field Name	Description
ATH_H 7:0	Sets HIGH speed assert threshold. Write in hexadecimal value. Formula (in decimal) = Shutter value / 8. It is recommended to have hysteresis of 60 to 100 between assert and de-assert threshold.

OFN_AD_DTH_HIGH Address: 0x6f
Access: Read/Write Reset Value: 0x3c

Bit	7	6	5	4	3	2	1	0
Field	DTH_H	DTH_H	DTH_H	DTH_H	DTH_H	DTH_H	DTH_H	DTH_H

Data Type: Bit field

USAGE: This register is used to set HIGH speed De-assert shutter threshold.

Field Name	Description
DTH_H 7:0	Sets HIGH speed de-assert threshold. Write in hexadecimal value. Formula (in decimal) = Shutter value / 8. It is recommended to have hysteresis of 60 to 100 between assert and de-assert threshold.

OFN_AD_ATH_LOW Address: 0x70
Access: Read/Write Reset Value: 0x18

Bit	7	6	5	4	3	2	1	0
Field	ATH_L	ATH_L	ATH_L	ATH_L	ATH_L	ATH_L	ATH_L	ATH_L

Data Type: Bit field

USAGE: This register is used to set LOW speed Assert shutter threshold.

Field Name	Description
ATH_L 7:0	Sets LOW speed assert threshold. Write in hexadecimal value. Formula (in decimal) = Shutter value / 8. It is recommended to have hysteresis of 60 to 100 between assert and de-assert threshold.

OFN_AD_DTH_LOW Address: 0x71
Access: Read/Write Reset Value: 0x20

Bit	7	6	5	4	3	2	1	0
Field	DTH_L	DTH_L	DTH_L	DTH_L	DTH_L	DTH_L	DTH_L	DTH_L

Data Type: Bit field

USAGE: This register is used to set LOW speed De-assert shutter threshold.

Field Name	Description
DTH_L 7:0	Sets LOW speed de-assert threshold. Write in hexadecimal value. Formula (in decimal) = Shutter value / 8. It is recommended to have hysteresis of 60 to 100 between assert and de-assert threshold.

Reserved Address: 0x72

OFN_QUANTIZE_CTRL Address: 0x73
Access: Read/Write Reset Value: 0x99

Bit	7	6	5	4	3	2	1	0
Field	YQ_ON	YQ_DIV_6	YQ_DIV_5	YQ_DIV_4	XQ_ON	XQ_DIV_2	XQ_DIV_1	XQ_DIV_0

Data Type: Bit field

USAGE: This register is used to set quatization for DeltaX and DeltaY. If both X and Y quantization modes are on, then only largest quantized X or Y will be reported.

Field Name	**Description**
YQ_ON	0 = Y quantization off 1 = Y quantization On
$YQ\_DIV_{6:4}$	Quantization factor 2^{YQ_DIV} . Reported YQ = DY / 2^{YQ_DIV} .
XQ_ON	0 = X quantization off 1 = X quantization On
$XQ\_DIV_{2:0}$	Quantization factor 2^{XQ_DIV} . Reported XQ = DX / 2^{XQ_DIV} .

OFN_XYQ_THRESH Address: 0x74
Access: Read/Write Reset Value: 0x02

Bit	7	6	5	4	3	2	1	0
Field	Reserved	Reserved	Reserved	Reserved	Reserved	XYQ_M	XYQ_C_1	XYQ_C_0

Data Type: Bit field

USAGE: This register is used to set quatization gradient for DeltaX and DeltaY.

Field Name	**Description**
XYQ_M	Gradient of linear region 0 = Gradient 1 1 = Gradient 2
$XYQ\_C_{1:0}$	Indicates the offset of linear region (max of C = 3 or 0x03)

OFN_FPD_CTRL Address: 0x75
Access: Read/Write Reset Value: 0x50

Bit	7	6	5	4	3	2	1	0
Field	Reserved	FPD_POL	FPD_TH	FPD_TH	FPD_TH	FPD_TH	FPD_TH	FPD_TH

Data Type: Bit field

USAGE: This register is used to set finger presence detection control.

Field Name	Description
FPD_POL	0 = GPIO is active LOW 1 = GPIO is active HIGH (default)
$FPD\_TH_{5:0}$	Sets FPD threshold based on shutter value. Write in hexadecimal value. Formula (in decimal):- Shutter value / 32.

Reserved Address: 0x76

OFN_ORIENTATION_CTRL Address: 0x77
Access: Read/Write Reset Value: 0x01

Bit	7	6	5	4	3	2	1	0
Field	XY_SWAP	Y_INV	X_INV	Reserved	Reserved	Reserved	$ORIENT_1$	$ORIENT_0$

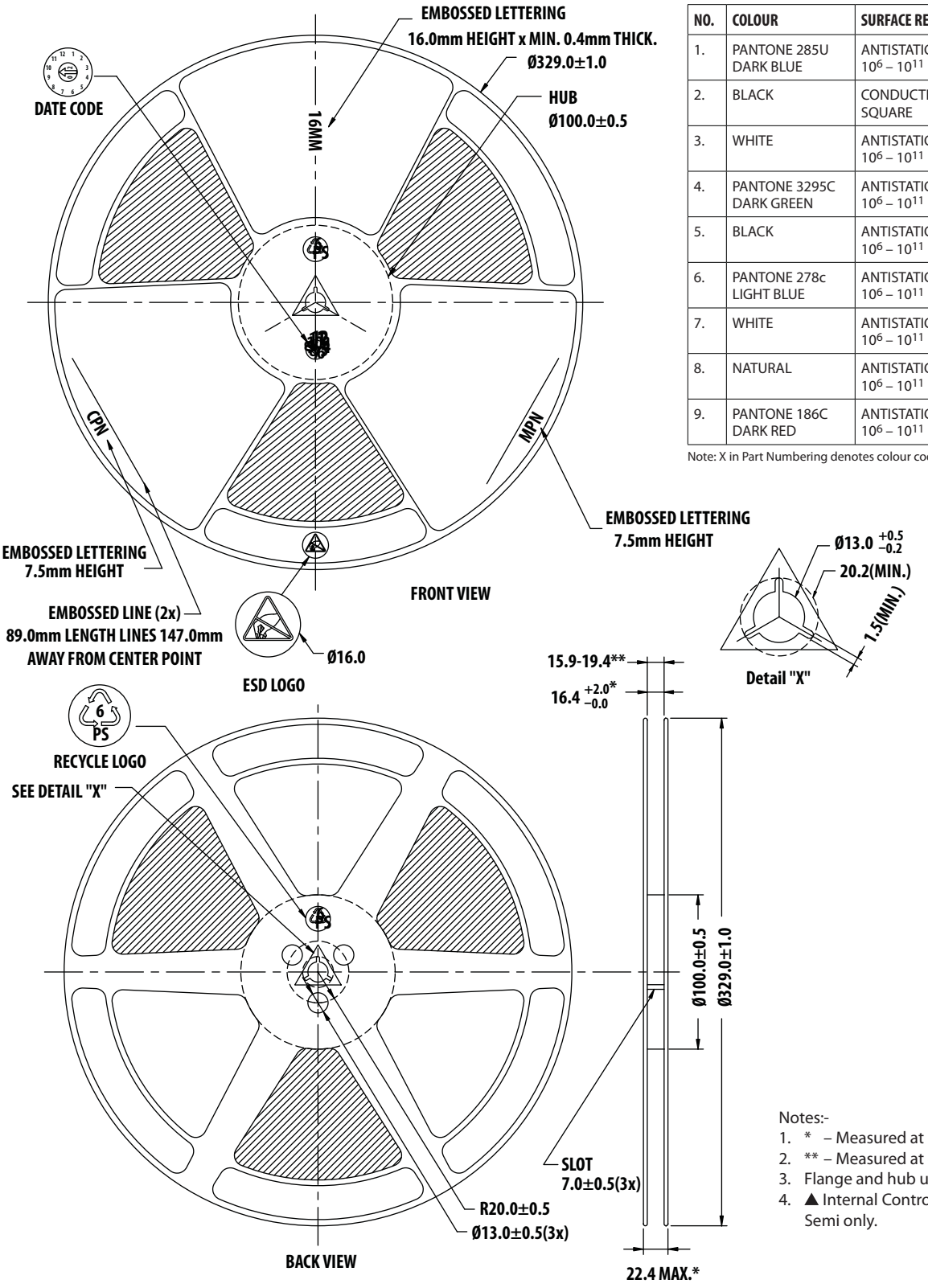
Data Type: Bit field

USAGE: This register is used to set sensor orientation control after ORIENT pin is set.

Field Name	Description
XY_SWAP	**0 = Normal sensor reporting of DX, DY. (default)** 1 = Swap data of DX to DY and DY to DX.
Y_INV	**0 = Normal sensor reporting of DY. (default)** 1 = Invert data of DY only.
X_INV	**0 = Normal sensor reporting of DX. (default)** 1 = Invert data of DX only.
ORIENT1:0	Read only bits of Orient pin state 0x00 = mounted 90deg clockwise (Orient pin is low) **0x01 = mounted 0deg (default, Orient pin is high, Figure 27)**

Packing information

Packaging tape, reel and packing information.

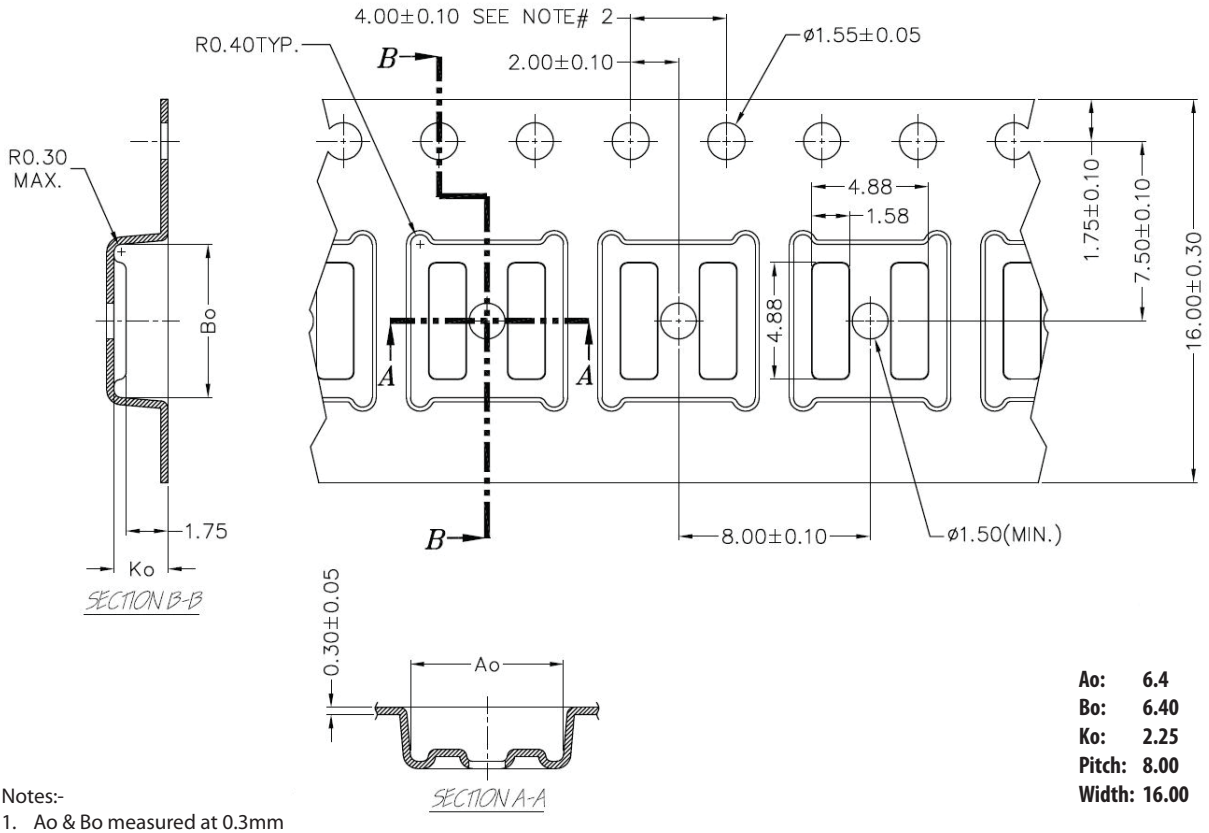


NO.	COLOUR	SURFACE RESISTIVITY
1.	PANTONE 285U DARK BLUE	ANTISTATIC COATED 10^6 – 10^{11} PER OHMS SQUARE
2.	BLACK	CONDUCTIVE <10^6 PER OHMS SQUARE
3.	WHITE	ANTISTATIC COATED 10^6 – 10^{11} PER OHMS SQUARE
4.	PANTONE 3295C DARK GREEN	ANTISTATIC COATED 10^6 – 10^{11} PER OHMS SQUARE
5.	BLACK	ANTISTATIC COATED 10^6 – 10^{11} PER OHMS SQUARE
6.	PANTONE 278c LIGHT BLUE	ANTISTATIC COATED 10^6 – 10^{11} PER OHMS SQUARE
7.	WHITE	ANTISTATIC COATED 10^6 – 10^{11} PER OHMS SQUARE
8.	NATURAL	ANTISTATIC COATED 10^6 – 10^{11} PER OHMS SQUARE
9.	PANTONE 186C DARK RED	ANTISTATIC COATED 10^6 – 10^{11} PER OHMS SQUARE

Note: X in Part Numbering denotes colour code.

Notes:-
1. * – Measured at hub area.
2. ** – Measured at outer edge.
3. Flange and hub ultrasonic welded.
4. ▲ Internal Control ø13.0±0.2 for ON Semi only.

Reel information



Ao:	**6.4**
Bo:	**6.40**
Ko:	**2.25**
Pitch:	**8.00**
Width:	**16.00**

Notes:-
1. Ao & Bo measured at 0.3mm above base of pocket.
2. 10 pitches cumulative tol. ±0.2mm.
3. ( ) Reference dimensions only.

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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