Operational Amplifiers

Input/Output Full Swing Low Voltage Operation High Speed CMOS Operational Amplifiers

BU7255HFV BU7255SHFV

General Description
BU7255HFV and BU7255SHFV are low-voltage CMOS operational amplifiers. BU7255SHFV has a wider operating temperature range. These have features of low supply current, high slew rate, and low input bias current. These are suitable for mobile equipment and sensor amplifiers.

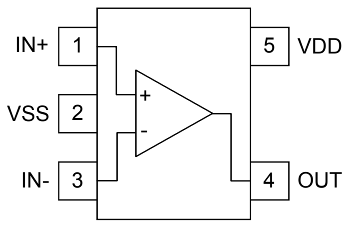
Features
- Low Operating Supply Voltage
- Input/Output Full Swing
- High Slew Rate
- Wide Operating Temperature Range (BU7255SHFV)
- Low Input Bias Current

Applications
- Buffer
- Active Filter
- Sensor Amplifier
- Mobile Equipment

Key Specifications
- Operating Supply Voltage (single supply): +2.4V to +5.5V
- Slew Rate: 3.4V/μs(Typ)
- Temperature Range:
  - BU7255HFV -40°C to +85°C
  - BU7255SHFV -40°C to +105°C
- Input Offset Current: 1pA(Typ)
- Input Bias Current: 1pA(Typ)

Package
Package	W(Typ) x D(Typ) x H(Max)
HVSOF5	1.60mm x 1.60mm x 0.60mm

Pin Configuration
BU7255HFV, BU7255SHFV : HVSOF5



Pin No.	Pin Name
1	IN+
2	VSS
3	IN-
4	OUT
5	VDD

Package
HVSOF5
BU7255HFV BU7255SHFV

Ordering Information
B U 7 2 5 5 x x x x - T R

Part Number	Package	Packaging and forming specification
BU7255HFV BU7255SHFV	HFV : HVSOF5	TR: Embossed tape and reel

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays.

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Line-up

Topr	Package		Orderable Part Number
-40°C to +85°C	HVSOF5	Reel of 3000	BU7255HFV-TR
-40°C to +105°C	HVSOF5	Reel of 3000	BU7255SHFV-TR

Absolute Maximum Ratings (T_A=25°C)

Parameter	Symbol	Rating		Unit
		BU7255HFV	BU7255SHFV	
Supply Voltage	VDD-VSS	+7		V
Power Dissipation	P_D	0.53 (Note 1,2)		W
Differential Input Voltage (Note 3)	V_{ID}	VDD - VSS		V
Input Common-mode Voltage Range	V_{ICM}	(VSS-0.3) to (VDD+0.3)		V
Input Current (Note 4)	I_I	±10		mA
Operating Supply Voltage	V_{opr}	+2.4 to +5.5		V
Operating Temperature	T_{opr}	-40 to +85	-40 to +105	°C
Storage Temperature	T_{stg}	-55 to +125		°C
Maximum Junction Temperature	T_{Jmax}	+125		°C

(Note 1) To use at temperature above T_A=25°C reduce 5.35mW.
(Note 2) Mounted on a FR4 glass epoxy PCB 70mm×70mm×1.6mm (Copper foil area less than 3%)
(Note 3) The voltage difference between inverting input and non-inverting input is the differential input voltage.
Then input terminal voltage is set to more than VSS.
(Note 4) An excessive input current will flow when input voltages of more than VDD+0.6V or less than VSS-0.6V are applied.
The input current can be set to less than the rated current by adding a limiting resistor.
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

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Electrical Characteristics:

○BU7255HFV, BU7255SHFV (Unless otherwise specified VDD=+3V, VSS=0V, T_A=25°C)

Parameter	Symbol	Temperature Range	Limit			Unit	Conditions
			Min	Typ	Max		
Input Offset Voltage (Note 5)	V_{IO}	25°C	-	1	9	mV	-
Input Offset Current (Note 5)	I_{IO}	25°C	-	1	-	pA	-
Input Bias Current (Note 5)	I_B	25°C	-	1	-	pA	-
Supply Current (Note 6)	I_{DD}	25°C	-	540	900	µA	R_L=∞ A_V=0dB, IN+=1.5V
		Full Range	-	-	1200		
Maximum Output Voltage(High)	V_{OH}	25°C	VDD-0.1	-	-	V	R_L=10kΩ
Maximum Output Voltage(Low)	V_{OL}	25°C	-	-	VSS+0.1	V	R_L=10kΩ
Large Signal Voltage Gain	A_V	25°C	60	105	-	dB	R_L=10kΩ
Input Common-mode Voltage Range	V_{ICM}	25°C	0	-	3	V	VSS to VDD
Common-mode Rejection Ratio	CMRR	25°C	40	60	-	dB	-
Power Supply Rejection Ratio	PSRR	25°C	45	80	-	dB	-
Output Source Current (Note 7)	I_{SOURCE}	25°C	2	4	-	mA	OUT=VDD - 0.4V
Output Sink Current (Note 7)	I_{SINK}	25°C	4	8	-	mA	OUT=VSS + 0.4V
Slew Rate	SR	25°C	-	3.4	-	V/µs	C_L=25pF
Unity Gain Frequency	f_T	25°C	-	4	-	MHz	C_L=25pF, A_V=40dB
Phase Margin	θ	25°C	-	40	-	deg	C_L=25pF, A_V=40dB

(Note 5) Absolute value

(Note 6) Full range BU7255: T_A=-40°C to +85°C BU7255S: T_A=-40°C to +105°C

(Note 7) Consider the power dissipation of the IC under high temperature environment when selecting the output current value.
There may be a case where the output current value is reduced due to the rise in IC temperature caused by the heat generated inside the IC.

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Description of Electrical Characteristics

Described below are descriptions of the relevant electrical terms used in this datasheet. Items and symbols used are also shown. Note that item name and symbol and their meaning may differ from those on another manufacturer's document or general document.

1. Absolute maximum ratings

Absolute maximum rating items indicate the condition which must not be exceeded. Application of voltage in excess of absolute maximum rating or use out of absolute maximum rated temperature environment may cause deterioration of characteristics.

(1) Supply Voltage (VDD/VSS)
Indicates the maximum voltage that can be applied between the VDD terminal and VSS terminal without deterioration or destruction of characteristics of internal circuit.

(2) Differential Input Voltage (V_{ID})
Indicates the maximum voltage that can be applied between non-inverting and inverting terminals without damaging the IC.

(3) Input Common-mode Voltage Range (V_{ICM})
Indicates the maximum voltage that can be applied to the non-inverting and inverting terminals without deterioration or destruction of electrical characteristics. Input common-mode voltage range of the maximum ratings does not assure normal operation of IC. For normal operation, use the IC within the input common-mode voltage range characteristics.

(4) Power Dissipation (P_D)
Indicates the power that can be consumed by the IC when mounted on a specific board at the ambient temperature 25°C (normal temperature). As for package product, P_D is determined by the temperature that can be permitted by the IC in the package (maximum junction temperature) and the thermal resistance of the package.

2. Electrical characteristics

(1) Input Offset Voltage (V_{IO})
Indicates the voltage difference between non-inverting terminal and inverting terminals. It can be translated into the input voltage difference required for setting the output voltage at 0 V.

(2) Input Offset Current (I_{IO})
Indicates the difference of input bias current between the non-inverting and inverting terminals.

(3) Input Bias Current (I_B)
Indicates the current that flows into or out of the input terminal. It is defined by the average of input bias currents at the non-inverting and inverting terminals.

(4) Supply Current (I_{DD})
Indicates the current that flows within the IC under specified no-load conditions.

(5) Maximum Output Voltage(High) / Maximum Output Voltage(Low) (V_{OH}/V_{OL})
Indicates the voltage range of the output under specified load condition. It is typically divided into maximum output voltage High and low. Maximum output voltage high indicates the upper limit of output voltage. Maximum output voltage low indicates the lower limit.

(6) Large Signal Voltage Gain (A_V)
Indicates the amplifying rate (gain) of output voltage against the voltage difference between non-inverting terminal and inverting terminal. It is normally the amplifying rate (gain) with reference to DC voltage.
Av = (Output voltage) / (Differential Input voltage)

(7) Input Common-mode Voltage Range (V_{ICM})
Indicates the input voltage range where IC normally operates.

(8) Common-mode Rejection Ratio (CMRR)
Indicates the ratio of fluctuation of input offset voltage when the input common mode voltage is changed. It is normally the fluctuation of DC.
CMRR = (Change of Input common-mode voltage)/(Input offset voltage fluctuation)

(9) Power Supply Rejection Ratio (PSRR)
Indicates the ratio of fluctuation of input offset voltage when supply voltage is changed.
It is normally the fluctuation of DC.
PSRR= (Change of power supply voltage)/(Input offset voltage fluctuation)

(10) Output Source Current/ Output Sink Current (I_{SOURCE} / I_{SINK})
The maximum current that can be output from the IC under specific output conditions. The output source current indicates the current flowing out from the IC, and the output sink current indicates the current flowing into the IC.

(11) Slew Rate (SR)
Indicates the ratio of the change in output voltage with time when a step input signal is applied.

(12) Unity Gain Frequency (f_T)
Indicates a frequency where the voltage gain of operational amplifier is 1.

(13) Phase Margin (θ)
Indicates the margin of phase from 180 degree phase lag at unity gain frequency.

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Typical Performance Curves

○ BU7255HFV, BU7255SHFV

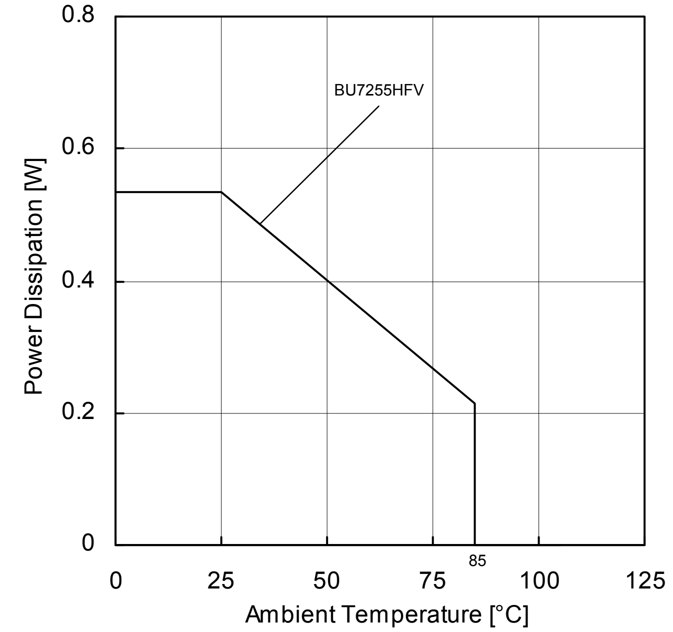

Figure 1.
Power Dissipation vs Ambient Temperature
(Derating Curve)

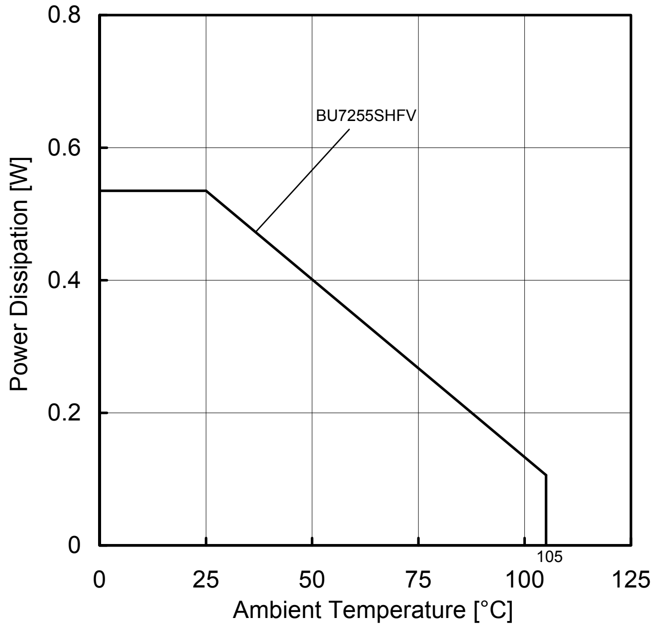

Figure 2.
Power Dissipation vs Ambient Temperature
(Derating Curve)

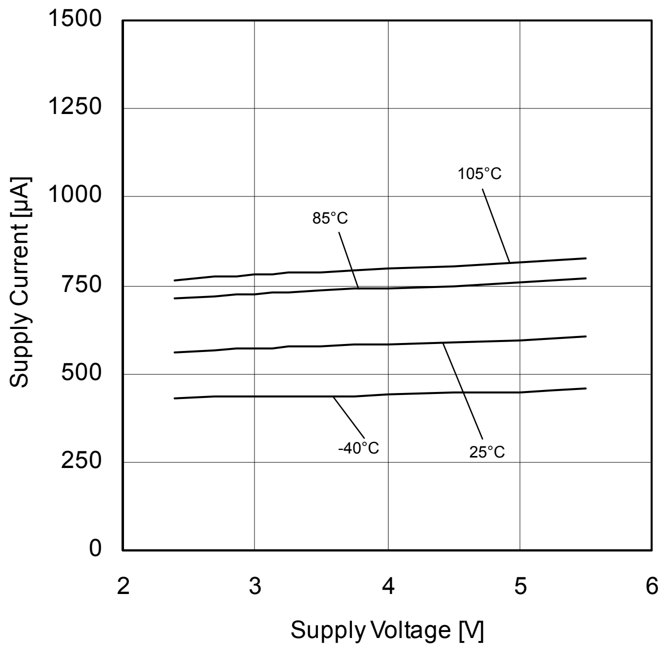

Figure 3.
Supply Current vs Supply Voltage

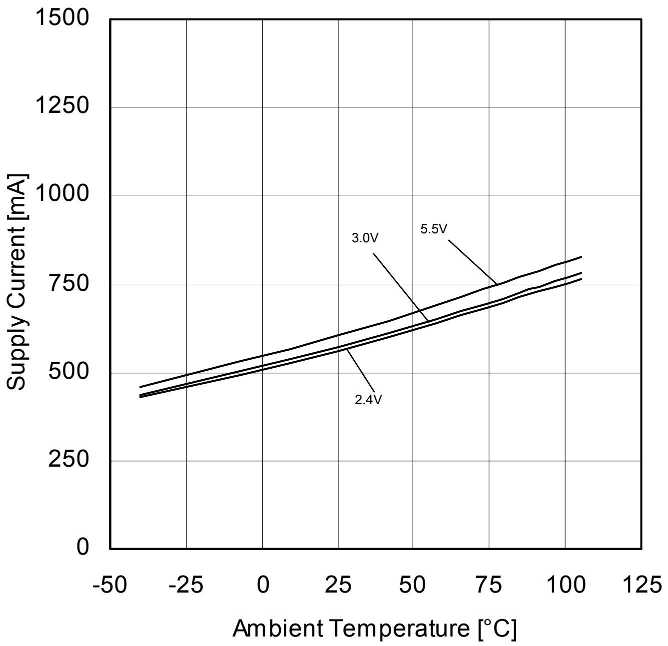

Figure 4.
Supply Current vs Ambient Temperature

(*)The above characteristics are measurements of typical sample, they are not guaranteed.
BU7255HFV: -40°C to +85°C BU7255SHFV: -40°C to +105°C

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Typical Performance Curves – Continued
○ BU7255HFV, BU7255SHFV

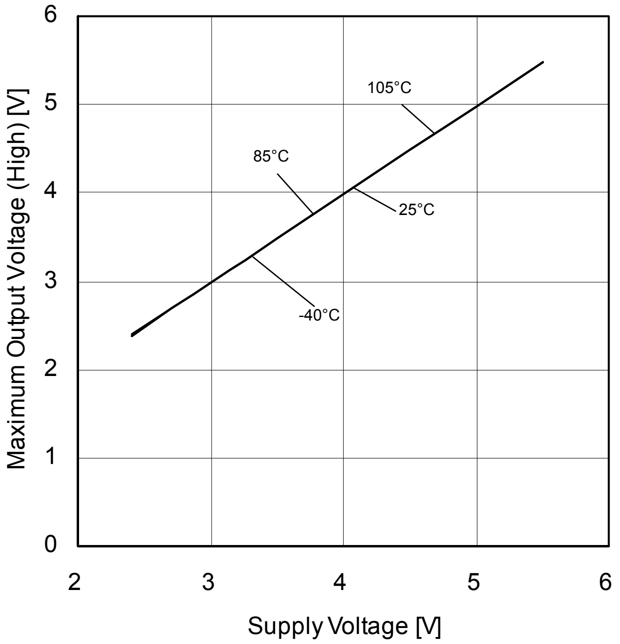

Figure 5.
Maximum Output Voltage (High) vs Supply Voltage
(R_L=10 kΩ)

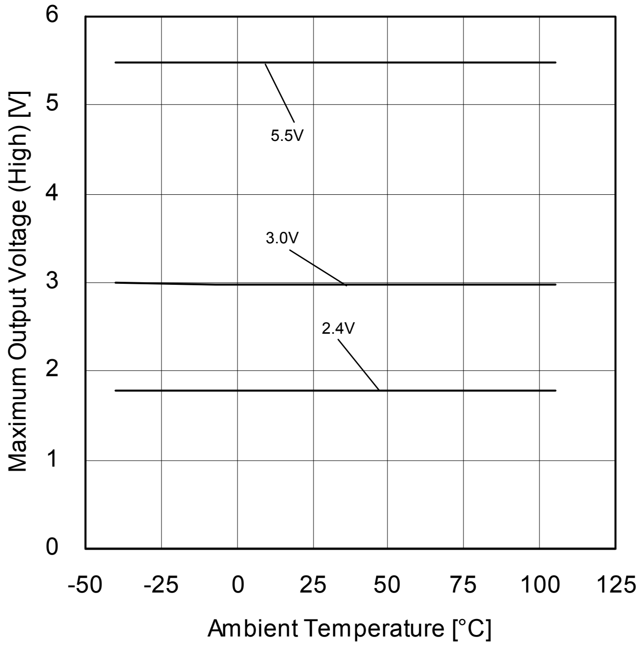

Figure 6.
Maximum Output Voltage (High) vs Ambient Temperature
(R_L=10 kΩ)

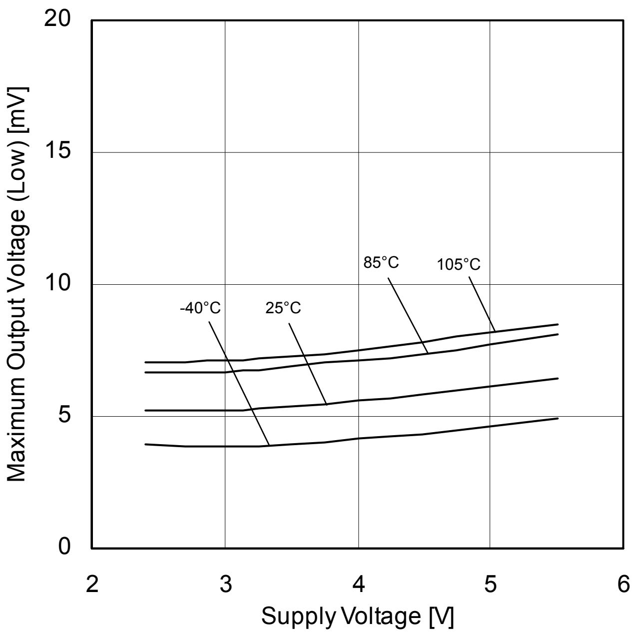

Figure 7.
Maximum Output Voltage (Low) vs Supply Voltage
(R_L=10 kΩ)

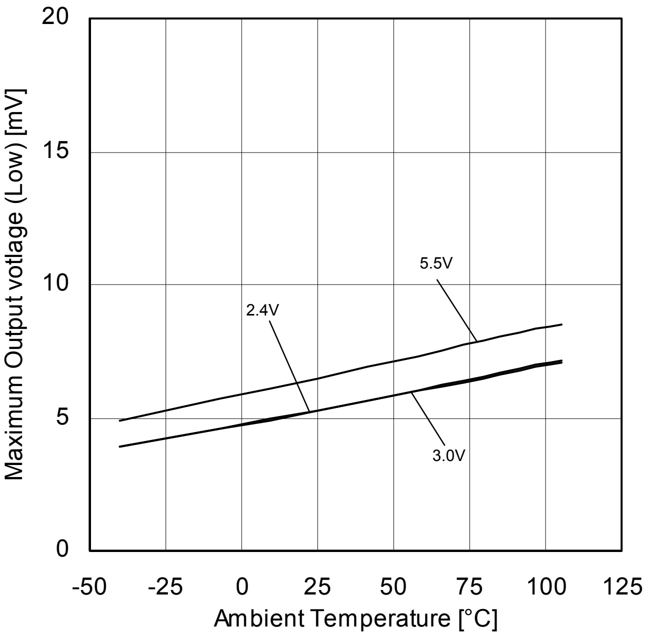

Figure 8.
Maximum Output Voltage (Low) vs Ambient Temperature
(R_L=10 kΩ)

(*)The above characteristics are measurements of typical sample, they are not guaranteed.
BU7255HFV: -40°C to +85°C　BU7255SHFV: -40°C to +105°C

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Typical Performance Curves – Continued

○ BU7255HFV, BU7255SHFV

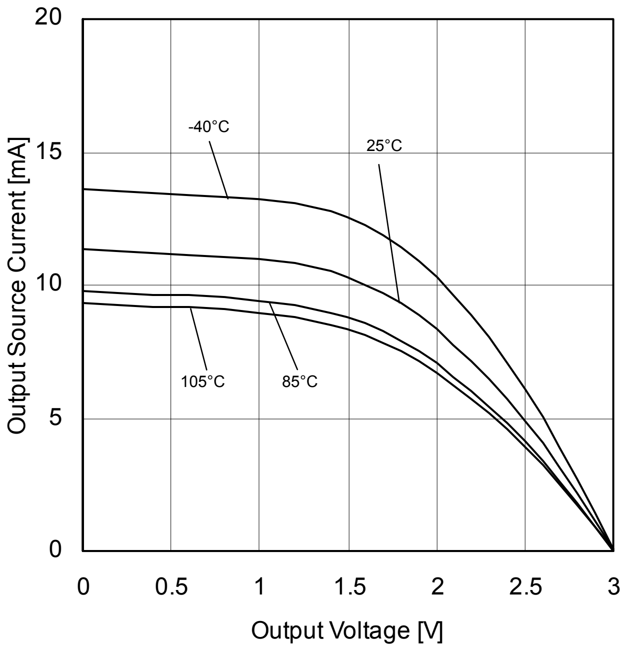

Figure 9.
Output Source Current vs Output Voltage
(VDD=3V)

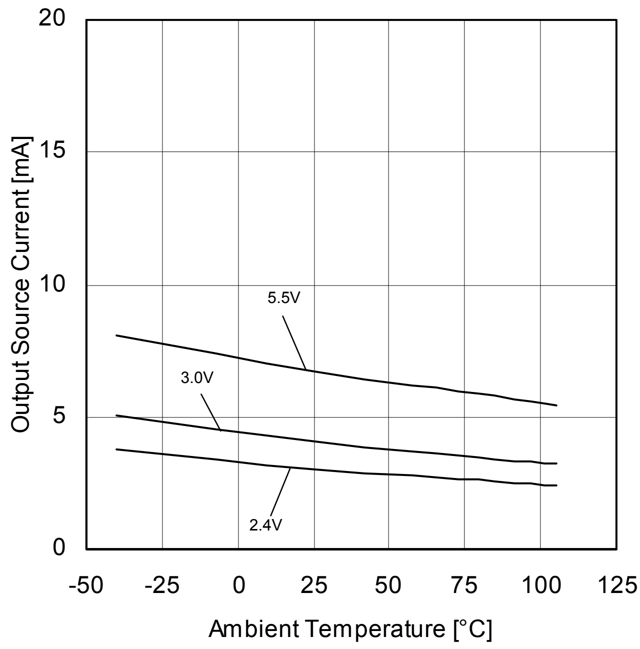

Figure 10.
Output Source Current vs Ambient Temperature
(OUT=VDD-0.4V)

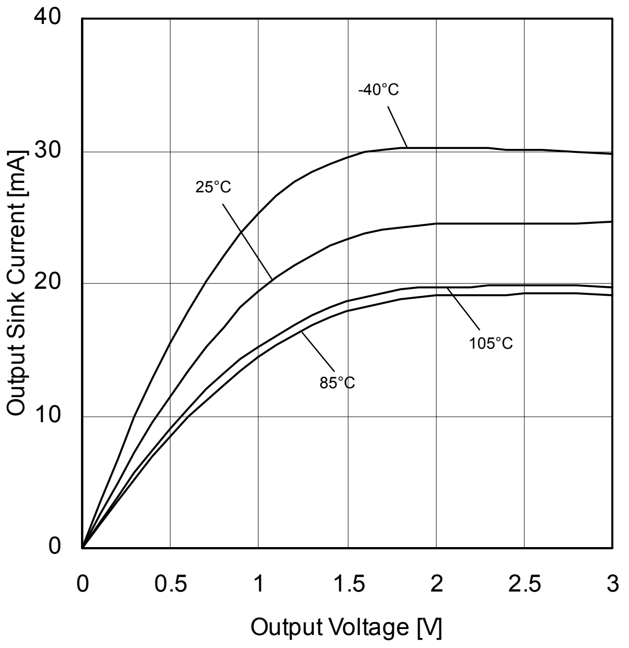

Figure 11.
Output Sink Current vs Output Voltage
(VDD=3V)

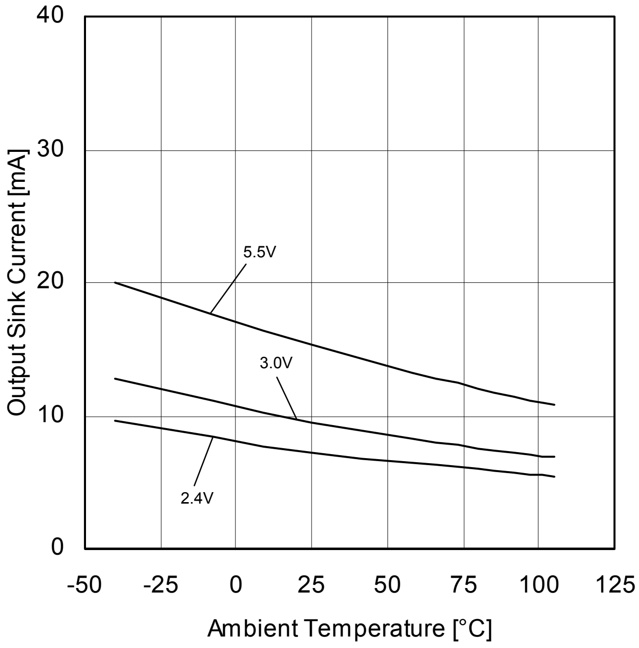

Figure 12.
Output Sink Current vs Ambient Temperature
(OUT=VSS+0.4V)

(*)The above characteristics are measurements of typical sample, they are not guaranteed.
BU7255HFV: -40°C to +85°C BU7255SHFV: -40°C to +105°C

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Typical Performance Curves – Continued

○ BU7255HFV, BU7255SHFV

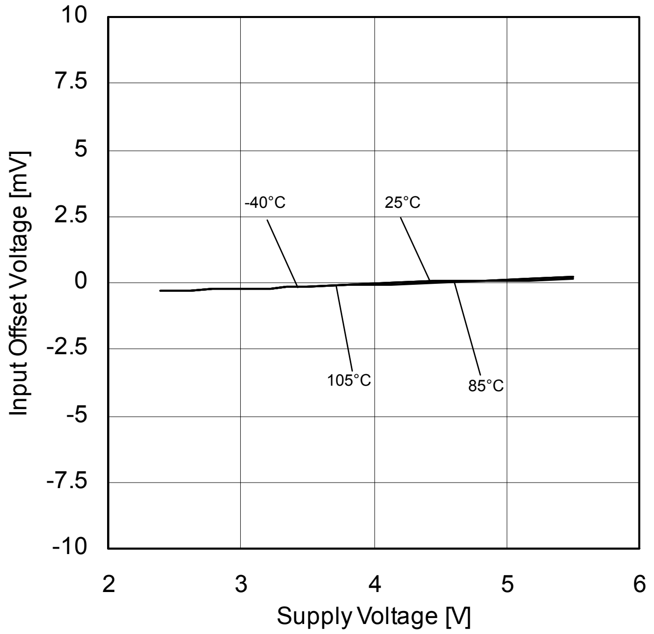

Figure 13.
Input Offset Voltage vs Supply Voltage
(V_{ICM}=VDD,　E_K=-VDD/2)

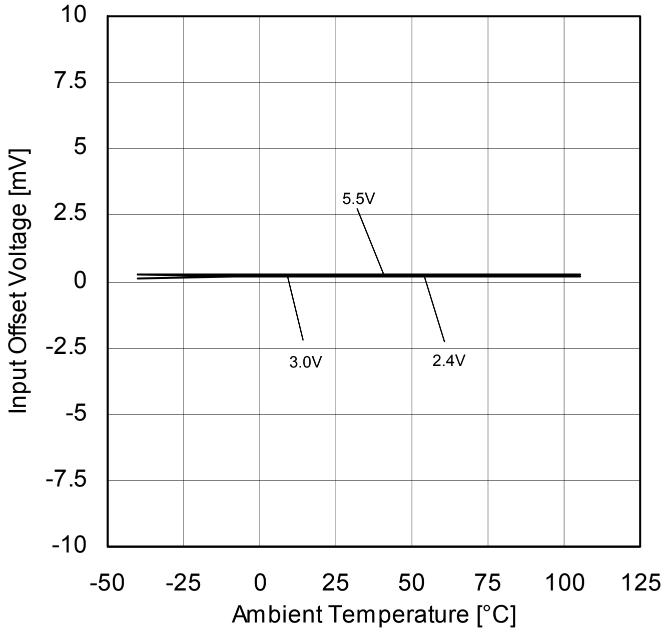

Figure 14.
Input Offset Voltage vs Ambient Temperature
(V_{ICM}=VDD,　E_K=-VDD/2)

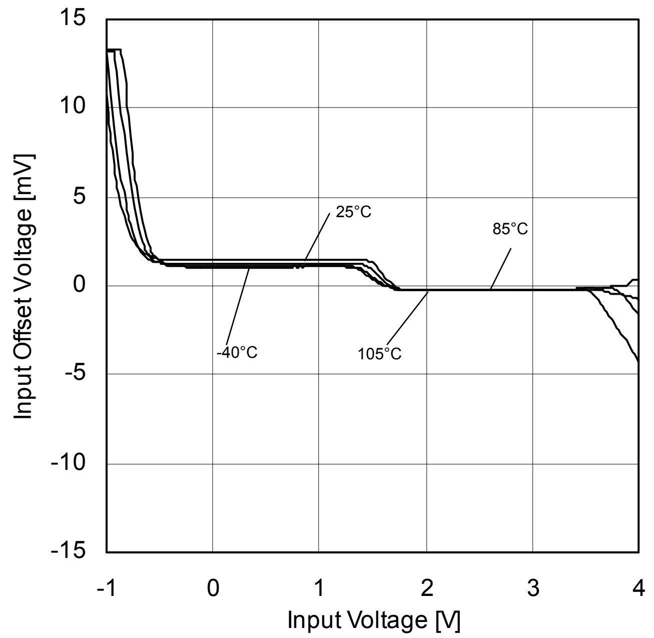

Figure 15.
Input Offset Voltage vs Input Voltage
(VDD=3V)

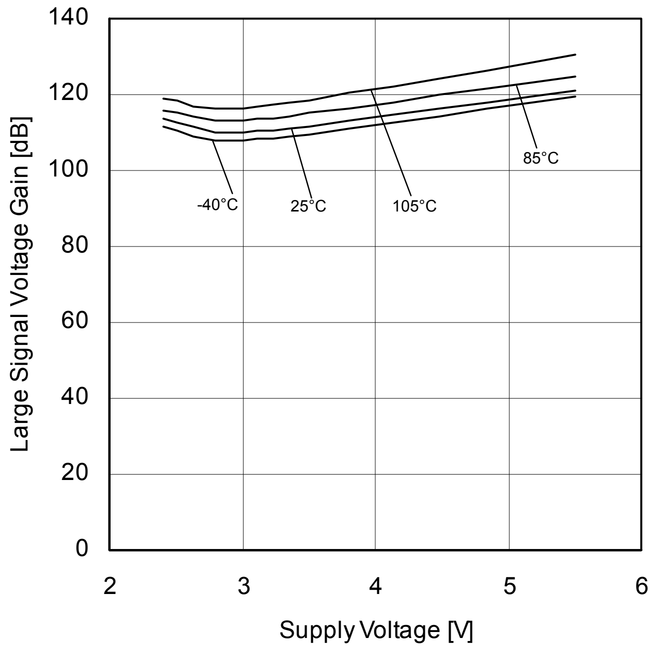

Figure 16.
Large Signal Voltage Gain vs Supply Voltage

(*)The above characteristics are measurements of typical sample, they are not guaranteed.
BU7255HFV: -40°C to +85°C　BU7255SHFV: -40°C to +105°C

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Typical Performance Curves – Continued

○ BU7255HFV, BU7255SHFV

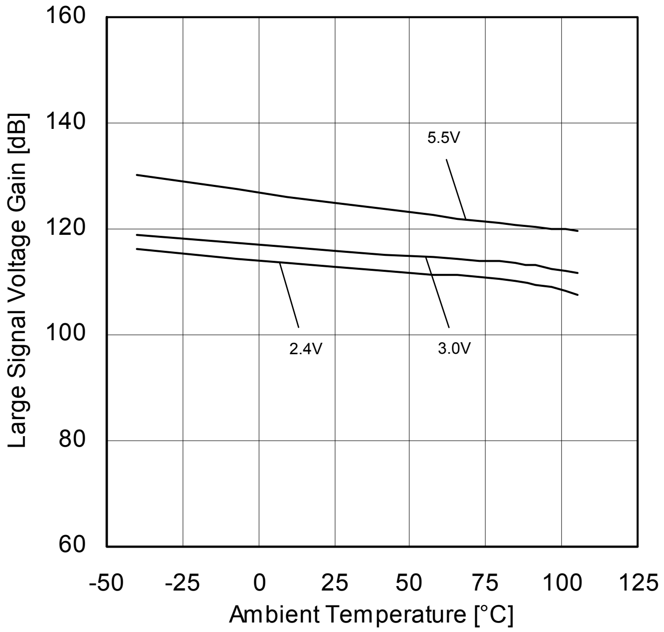

Figure 17.
Large Signal Voltage Gain vs Ambient Temperature

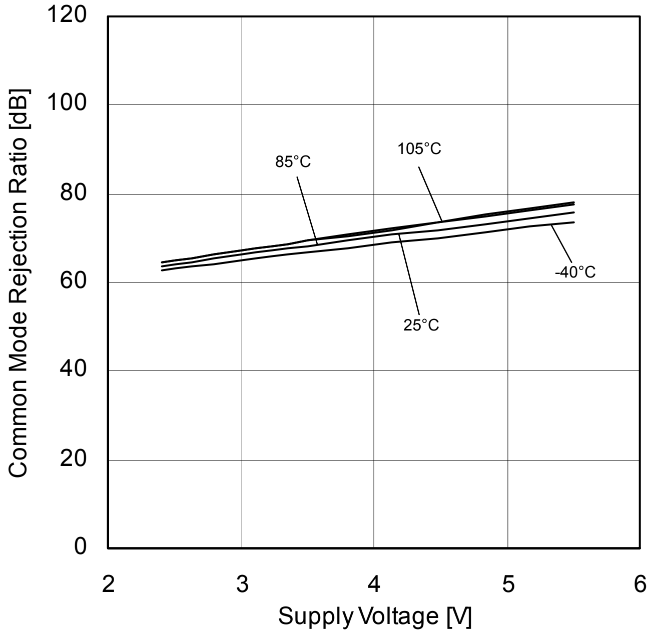

Figure 18.
Common Mode Rejection Ratio vs Supply Voltage

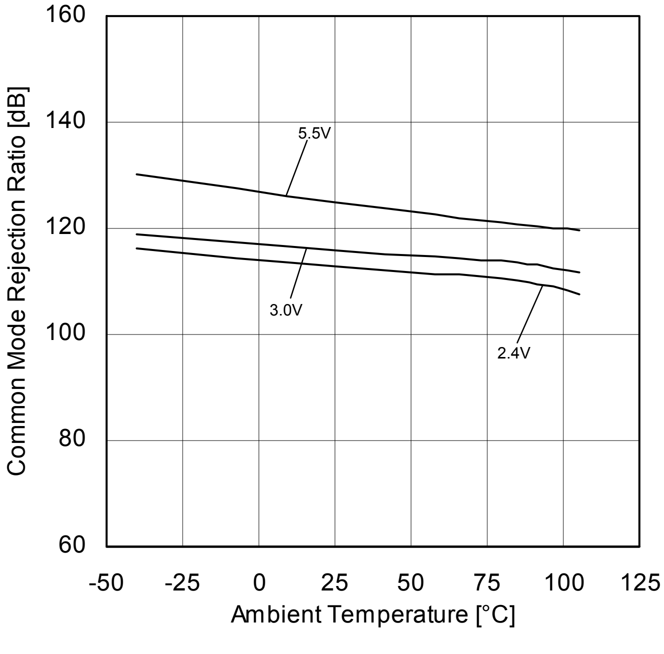

Figure 19.
Common Mode Rejection Ratio vs Ambient Temperature

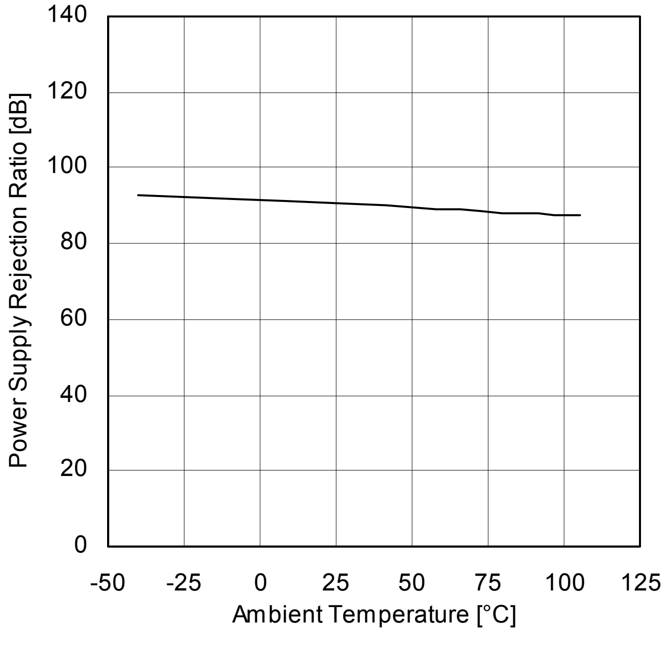

Figure 20.
Power Supply Rejection Ratio vs Ambient Temperature

(*)The above characteristics are measurements of typical sample, they are not guaranteed.
BU7255HFV: -40°C to +85°C BU7255SHFV: -40°C to +105°C

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Typical Performance Curves – Continued

○ BU7255HFV, BU7255SHFV

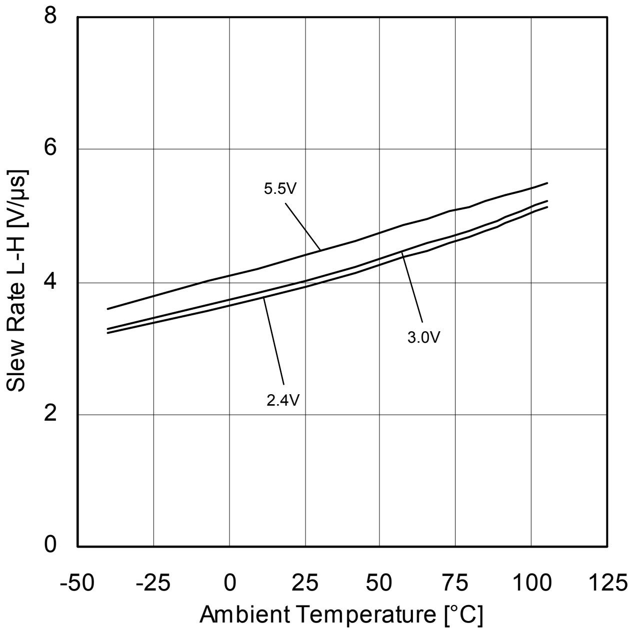

Figure 21.
Slew Rate L-H vs Ambient Temperature

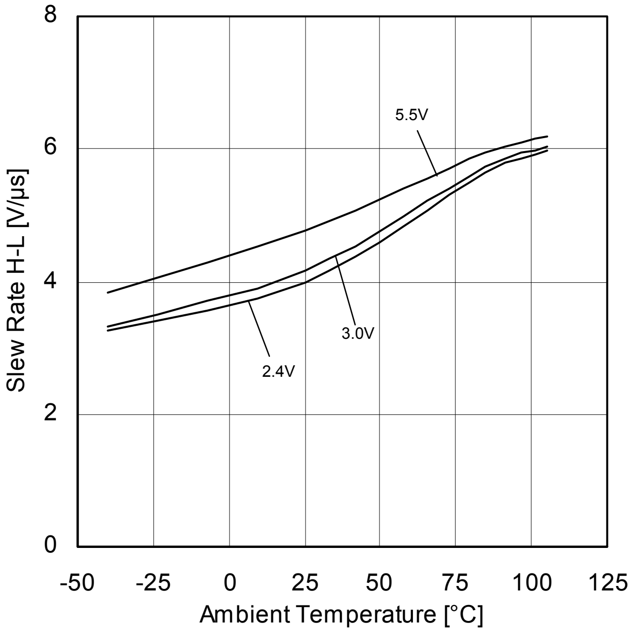

Figure 22.
Slew Rate H-L vs Ambient Temperature

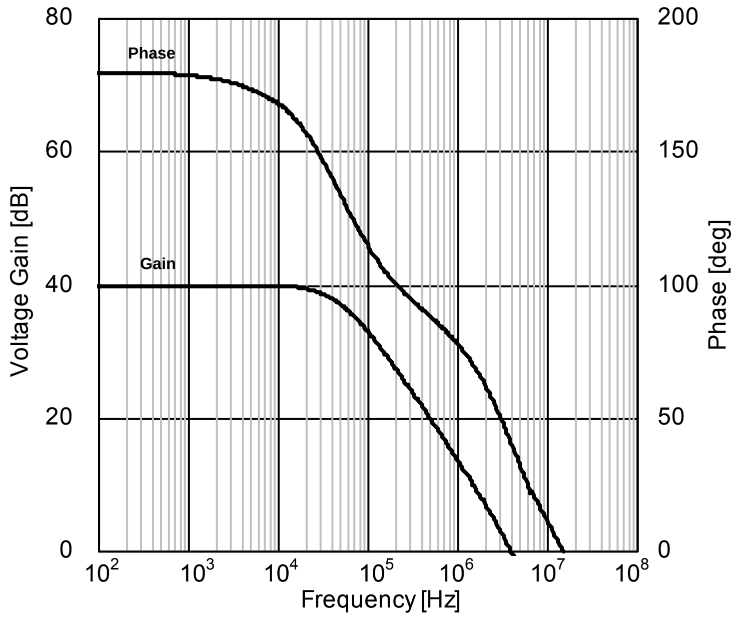

Figure 23.
Voltage Gain・Phase vs Frequency
(VDD=+3V, VSS=0V, T_A=25°C)

(*)The above characteristics are measurements of typical sample, they are not guaranteed.
BU7255HFV: -40°C to +85°C　BU7255SHFV: -40°C to +105°C

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Application Information

NULL method condition for Test Circuit 1

VDD, VSS, E_K, V_{ICM}, V_{RL} Unit:V, R_L Unit:ohms

Parameter	V_F	SW1	SW2	SW3	VDD	VSS	E_K	V_{ICM}	V_{RL}	R_L	Calculation
Input Offset Voltage	V_{F1}	ON	ON	OFF	3	0	-1.5	3	-	-	1
Large Signal Voltage Gain	V_{F2}	ON	ON	ON	3	0	-0.5	1.5	1.5	10k	2
	V_{F3}						-2.5				
Common-mode Rejection Ratio (Input Common-mode Voltage Range)	V_{F4}	ON	ON	OFF	3	0	-1.5	0	-	-	3
	V_{F5}							3			
Power Supply Rejection Ratio	V_{F6}	ON	ON	OFF	2.4	0	-1.2	0	-	-	4
	V_{F7}				5.5						

- Calculation –

1. Input Offset Voltage (V_{IO})

$$V_{IO} = \frac{|V_{F1}|}{1 + R_F/R_S} \quad [V]$$

2. Large Signal Voltage Gain (A_V)

$$Av = 20Log \frac{\Delta E_K \times (1+R_F/R_S)}{|V_{F3} - V_{F2}|} \quad [dB]$$

3. Common-Mode Rejection Ratio (CMRR)

$$CMRR = 20Log \frac{\Delta V_{ICM} \times (1+R_F/R_S)}{|V_{F5} - V_{F4}|} \quad [dB]$$

4. Power Supply Rejection Ratio (PSRR)

$$PSRR = 20Log \frac{\Delta VDD \times (1+ R_F/R_S)}{|V_{F7} - V_{F6}|} \quad [dB]$$

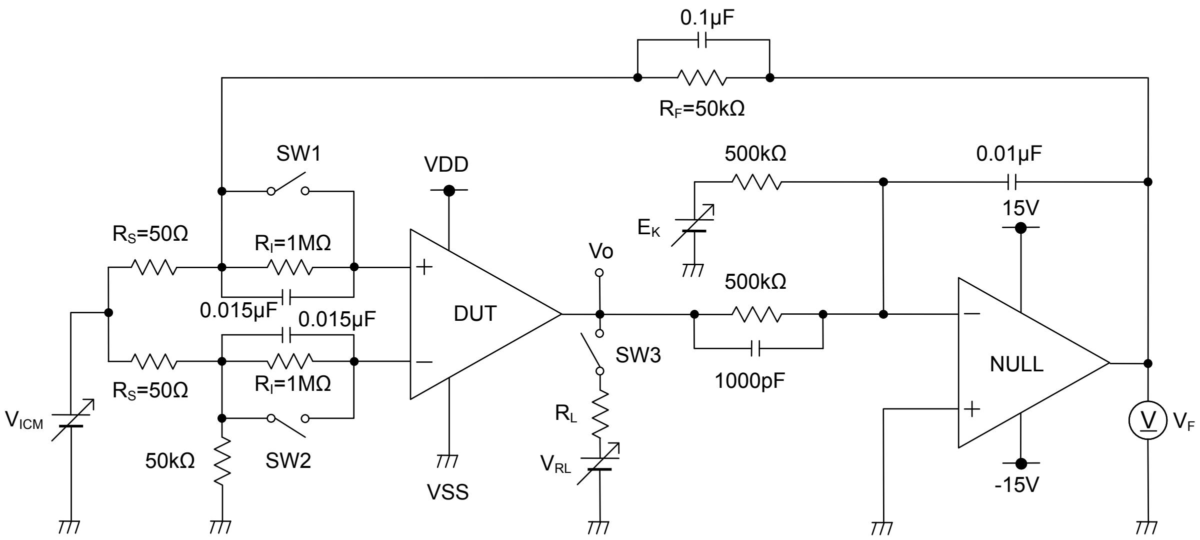

Figure 24. Test Circuit 1

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Application Information – continued

Switch Condition for Test Circuit 2

Parameter	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	SW9	SW10	SW11	SW12
Supply Current	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF
Maximum Output Voltage (R_L=10kΩ)	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF
Output Current	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF
Slew Rate	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	ON
Maximum Frequency	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	ON	OFF	OFF	ON

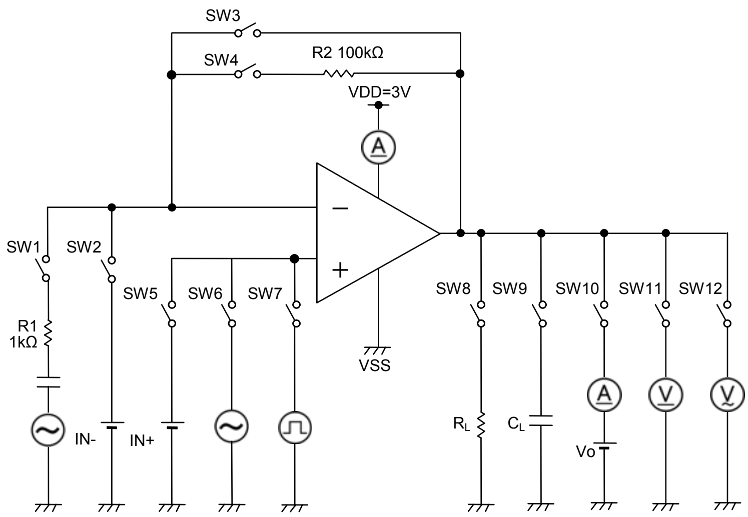

Figure 25. Test Circuit 2

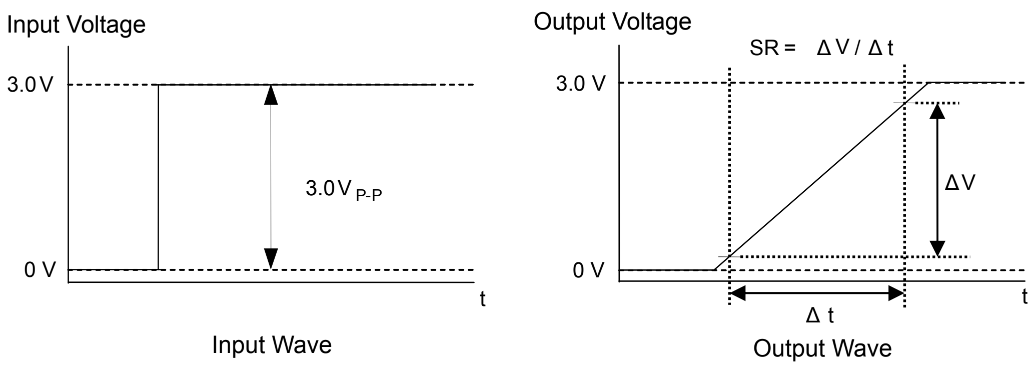

Figure 26. Slew Rate Input and Output Wave

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Examples of Circuit

○Voltage Follower

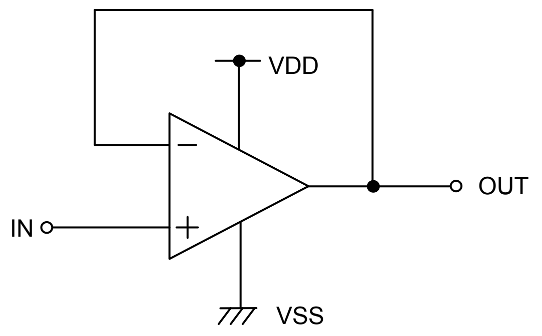

Figure 27. Voltage Follower Circuit

Voltage gain is 0dB.

Using this circuit, the output voltage (OUT) is configured to be equal to the input voltage (IN). This circuit also stabilizes the output voltage (OUT) due to high input impedance and low output impedance. Computation for output voltage (OUT) is shown below.

OUT=IN

○Inverting Amplifier

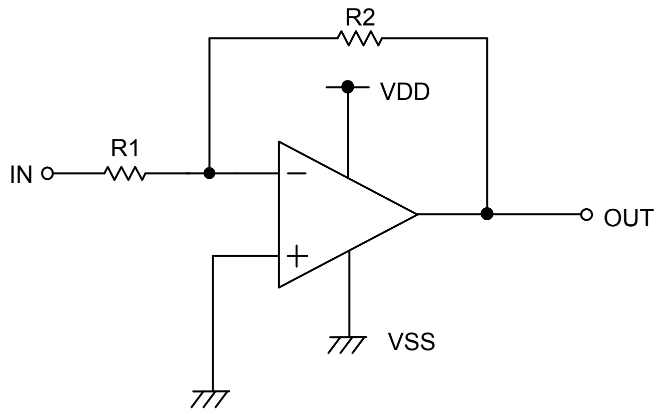

Figure 28. Inverting Amplifier Circuit

For inverting amplifier, input voltage (IN) is amplified by a voltage gain and depends on the ratio of R1 and R2. The out-of-phase output voltage is shown in the next expression

OUT=-(R2/R1)・IN

This circuit has input impedance equal to R1.

○Non-inverting Amplifier

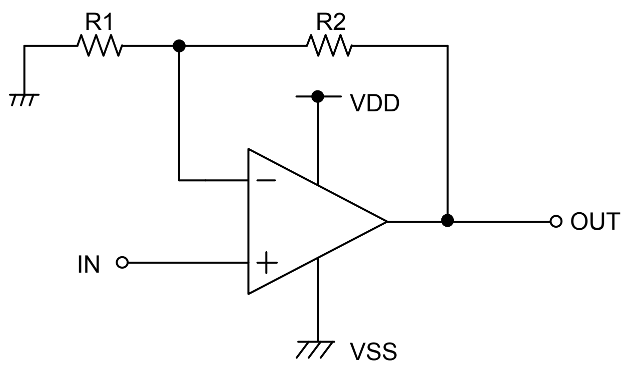

Figure 29. Non-inverting Amplifier Circuit

For non-inverting amplifier, input voltage (IN) is amplified by a voltage gain, which depends on the ratio of R1 and R2. The output voltage (OUT) is in-phase with the input voltage (IN) and is shown in the next expression.

OUT=(1 + R2/R1)・IN

Effectively, this circuit has high input impedance since its input side is the same as that of the operational amplifier.

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Power Dissipation

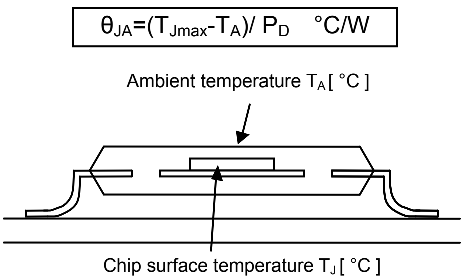
Power dissipation (total loss) indicates the power that the IC can consume at T_A=25°C (normal temperature). As the IC consumes power, it heats up, causing its temperature to be higher than the ambient temperature. The allowable temperature that the IC can accept is limited. This depends on the circuit configuration, manufacturing process, and consumable power.

Power dissipation is determined by the allowable temperature within the IC (maximum junction temperature) and the thermal resistance of the package used (heat dissipation capability). Maximum junction temperature is typically equal to the maximum storage temperature. The heat generated through the consumption of power by the IC radiates from the mold resin or lead frame of the package. Thermal resistance, represented by the symbol θ_{JA}°C/W, indicates this heat dissipation capability. Similarly, the temperature of an IC inside its package can be estimated by thermal resistance.

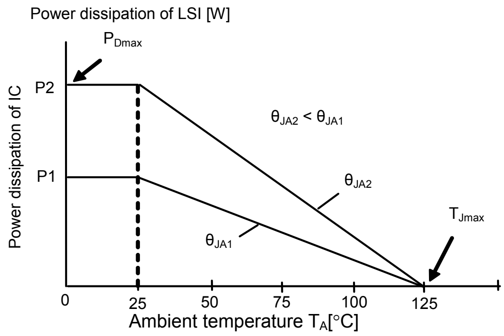
Figure 30(a) shows the model of the thermal resistance of a package. The equation below shows how to compute for the Thermal resistance (θ_{JA}), given the ambient temperature (T_A), maximum junction temperature (T_{Jmax}), and power dissipation (P_D):

$$\theta_{JA} = (T_{Jmax} - T_A) / P_D \quad °C/W$$

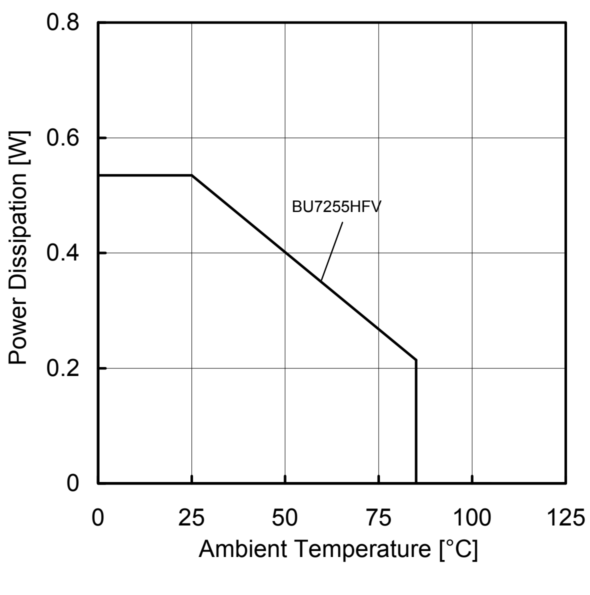
The Derating curve in Figure 30(b) indicates the power that the IC can consume with reference to ambient temperature. Power consumption of the IC begins to attenuate at certain temperatures. This gradient is determined by Thermal resistance (θ_{JA}), which depends on the chip size, power consumption, package, ambient temperature, package condition, wind velocity, etc. This may also vary even when the same of package is used. Thermal reduction curve indicates a reference value measured at a specified condition. Figure 30(c) to (d) shows an example of the derating curve for BU7255HFV, and BU7255SHFV.



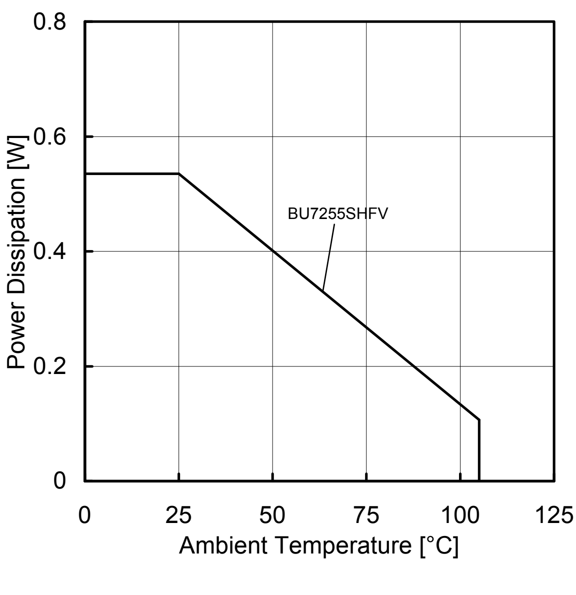
(a) Thermal Resistance



(b) Derating Curve



(c) BU7255HFV



(d) BU7255SHFV

5.3	mW/℃

When using the unit above T_A=25°C, subtract the value above per Celsius degree. Power dissipation is the value when FR4 glass epoxy board 70mm×70mm×1.6mm (copper foil area below 3%) is mounted

Figure 30. Thermal Resistance and Derating Curve

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the P_D stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the P_D rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. **Regarding the Input Pin of the IC**
    In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

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Operational Notes – continued

12. **Input Voltage**
Applying (VSS-0.3) to (VDD+0.3) to the input terminal is possible without causing deterioration of the electrical characteristics or destruction, regardless of the supply voltage. However, this does not ensure normal circuit operation. Please note that the circuit operates normally only when the input voltage is within the common mode input voltage range of the electric characteristics.

13. **Power Supply(single/dual)**
The op-amp operates when the voltage supplied is between VDD and VSS. Therefore, the single supply op-amp can be used as dual supply op-amp as well.

14. **Output Capacitor**
If a large capacitor is connected between the output pin and VSS pin, current from the charged capacitor will flow into the output pin and may destroy the IC when the VDD pin is shorted to ground or pulled down to 0V. Use a capacitor smaller than 0.1uF between output pin and VSS pin.

15. **Oscillation by Output Capacitor**
Please pay attention to the oscillation by output capacitor and in designing an application of negative feedback loop circuit with these Ics.

16. **Latch up**
Be careful of input voltage that exceed the VDD and VSS. When CMOS device have sometimes occur latch up and protect the IC from abnormaly noise.

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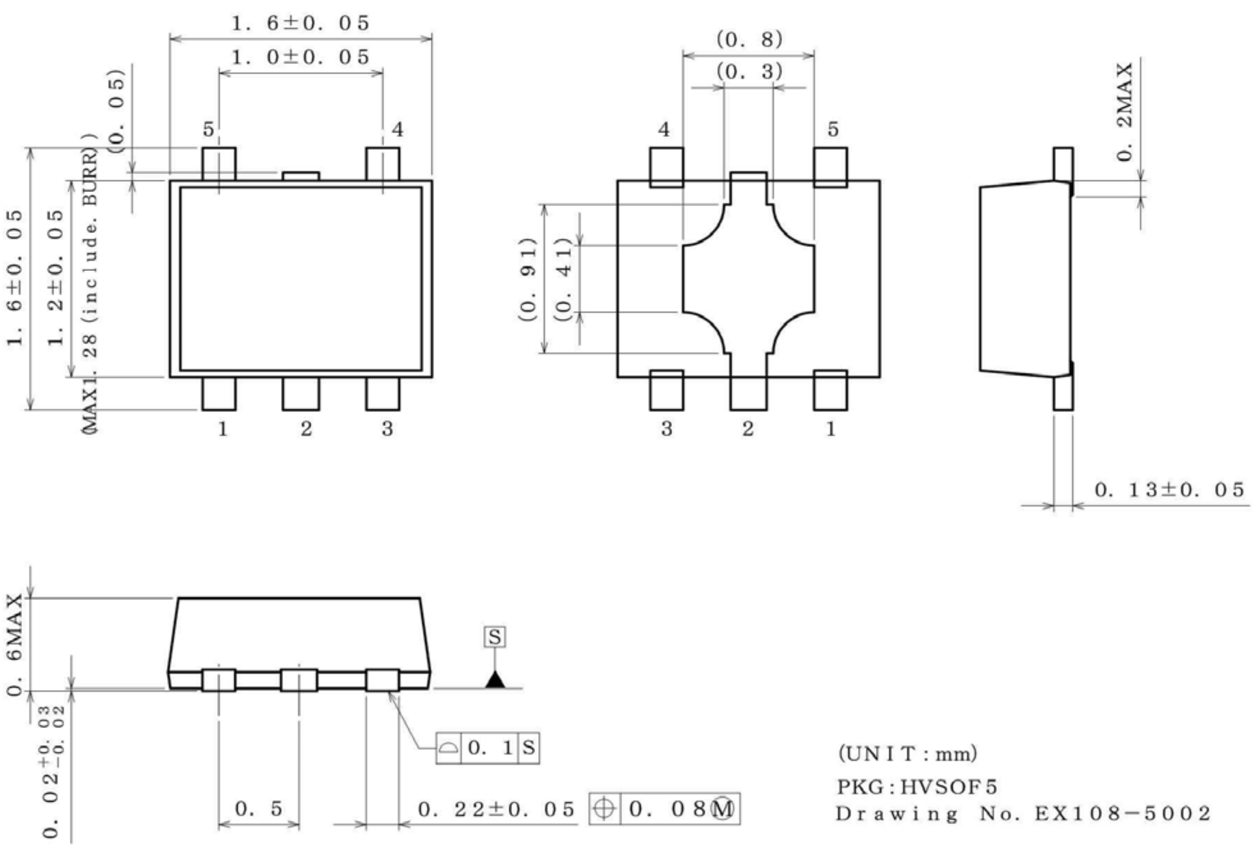
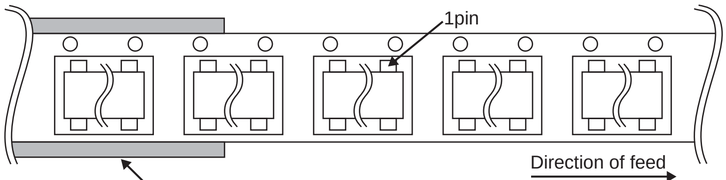
Physical Dimension, Tape and Reel Information

Package Name	HVSOF5



<Tape and Reel information>

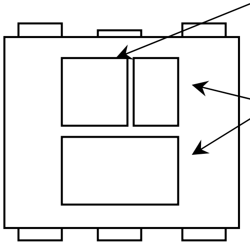
Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Marking Diagram

HVSOF5 (TOP VIEW)



Product Name	Package Type	Marking
BU7255HFV	HVSOF5	A4
BU7255SHFV		B4

Revision History

Date	Revision	Changes
08.Jan.2014	001	New Release
06.Mar.2015	002	Add the measuring condition (Page.10　Figure 23)
21.Oct.2016	003	P.1…Add (Typ) for Slew Rate P.4…Corrected Input offset fluctuation→Input offset voltage fluctuation P.9…Corrected Large Signal Voltage Gain→Common Mode Rejection Ratio at Figure 19 P.11…Corrected S1～S3→SW1～SW3, Add Condition of V_{RL}, R_L P.12…Corrected SW No.→Parameter P.15…Corrected Operational Notes 2, 13 P.18…Delete Land Pattern Data

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

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