InnoSwitch5-Pro Family

Digitally Controllable Off-Line CV/CC ZVS Flyback Switcher IC with 750 V and 900 V PowiGaN Switch, Synchronous Rectification and FluxLink Feedback

Product Highlights

New in InnoSwitch5-Pro

- Zero voltage switching (ZVS) using advanced SR FET control – no active clamp required
- Supports very wide output voltage range 3 V to 30 V
- Native support for 28 V USB PD Extended Power Range (EPR)
- Lossless input line voltage sensing on the secondary-side for adaptive DCM/CCM/ZVS control
- Enables <2% CC accuracy for UFCS protocol

Highly Integrated, Compact Footprint

- Robust 750 V and 900 V PowiGaN™ primary switch options
- Steady-state switching frequency up to 140 kHz minimizes transformer size
- Synchronous rectification driver and secondary-side sensing
- Integrated FluxLink™, HIPOT-isolated, feedback link
- Drives low-cost N-channel FET series load switch
- Integrated 3.6 V supply for external MCU

Digitally Controlled via I²C Interface

- Precise CV, CC, CP Control
- Dynamic adjustment of power supply voltage and current
- Selectable DCM-only operation to reduce SR FET voltage stress
- Optimized command set to reduce I²C traffic
- Telemetry for power supply status and fault monitoring

EcoSmart™ – Energy Efficient

- Enables >95% efficiency
- Less than 30 mW no-load including line sense and MCU

Advanced Protection / Safety Features

- Series load switch short-circuit protection
- Disable output fault response
- Fast input line UV/OV protection
- Programmable output OV/UV fault detection and response
- Open SR FET gate detection
- Hysteretic thermal shutdown
- Programmable watchdog timer for system faults

Full Safety and Regulatory Compliance

- Reinforced isolation >4000 VAC
- 100% production HIPOT testing
- UL1577 isolation voltage 4000 VAC (max) safety approved. TUV (EN62368-1) and CQC (GB4943.1) safety pending

Green Package

- Halogen free and RoHS compliant

Applications

- High density power adapters
- Multiprotocol adapters including USB PD + PPS, 28 V USB PD EPR, QC, VOOC, VFC, SCP, UFCS
- Direct-charge mobile device chargers
- Multi-chemistry tool and general purpose battery chargers
- Adjustable CV and CC LED ballast

Description

The InnoSwitch™5-Pro family of ICs substantially reduces the size of power adapters. Switching frequency of up to 140 kHz and a very high level of integration combine to reduce the component volume and PCB board area required by a typical adapter implementation.

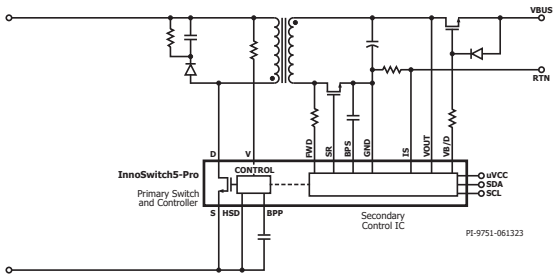


Figure 1. Typical Application schematic.

Figure 2. High Creepage, Safety-Compliant InSOP-T28D Package.

Output Power Table[1]

Product[4,5]	750 V PowiGaN Switch			
	230 VAC ±15%		85-264 VAC	
	Adapter[2]	**Open Frame[3]**	**Adapter[2]**	**Open Frame[3]**
INN5375F	90 W	100 W	75 W	90 W
INN5376F	115 W	125 W	80 W	115 W
INN5377F	135 W	145 W	90 W	135 W
Product[4,5]	900 V PowiGaN Switch			
INN5396F	115 W	125 W	80 W	115 W
Product[4,5]	750 PowiGaN Switch			
	230 VAC ±15%		385 VDC (PFC Input)	
	Adapter[2]	**Open Frame[3]**	**Adapter[2]**	**Open Frame[3]**
INN5475F	105 W	130 W	160 W	180 W
INN5476F	140 W	160 W	180 W	200 W
INN5477F	170 W	190 W	200 W	220 W
Product[4,5]	900 V PowiGaN Switch			
INN5496F	140 W	160 W	180 W	200 W

Table 1. Output Power Table.

Notes:
1. Maximum output power is dependent on the design, with maximum IC package temperature kept <125 °C.
2. Minimum continuous power in a typical non-ventilated enclosed typical size adapter measured at 40 °C ambient.
3. Minimum peak power capability.
4. F Package: InSOP-T28D.
5. INN53xx series optimized for universal AC input designs. INN54xx series optimized for peak power designs with PFC input.

InnoSwitch5-Pro ICs achieve zero voltage switching in discontinuous conduction mode using advanced SR FET control. Overall system efficiency exceeds 95%, allowing designers to eliminate heat sinks, spreaders and potting materials for thermal management, further reducing size, component cost and manufacturing complexity. The integration of PowiGaN primary switch and controller, isolated feedback and secondary controller with an I²C interface simplifies the development and manufacturing of fully programmable, highly efficient power supplies.

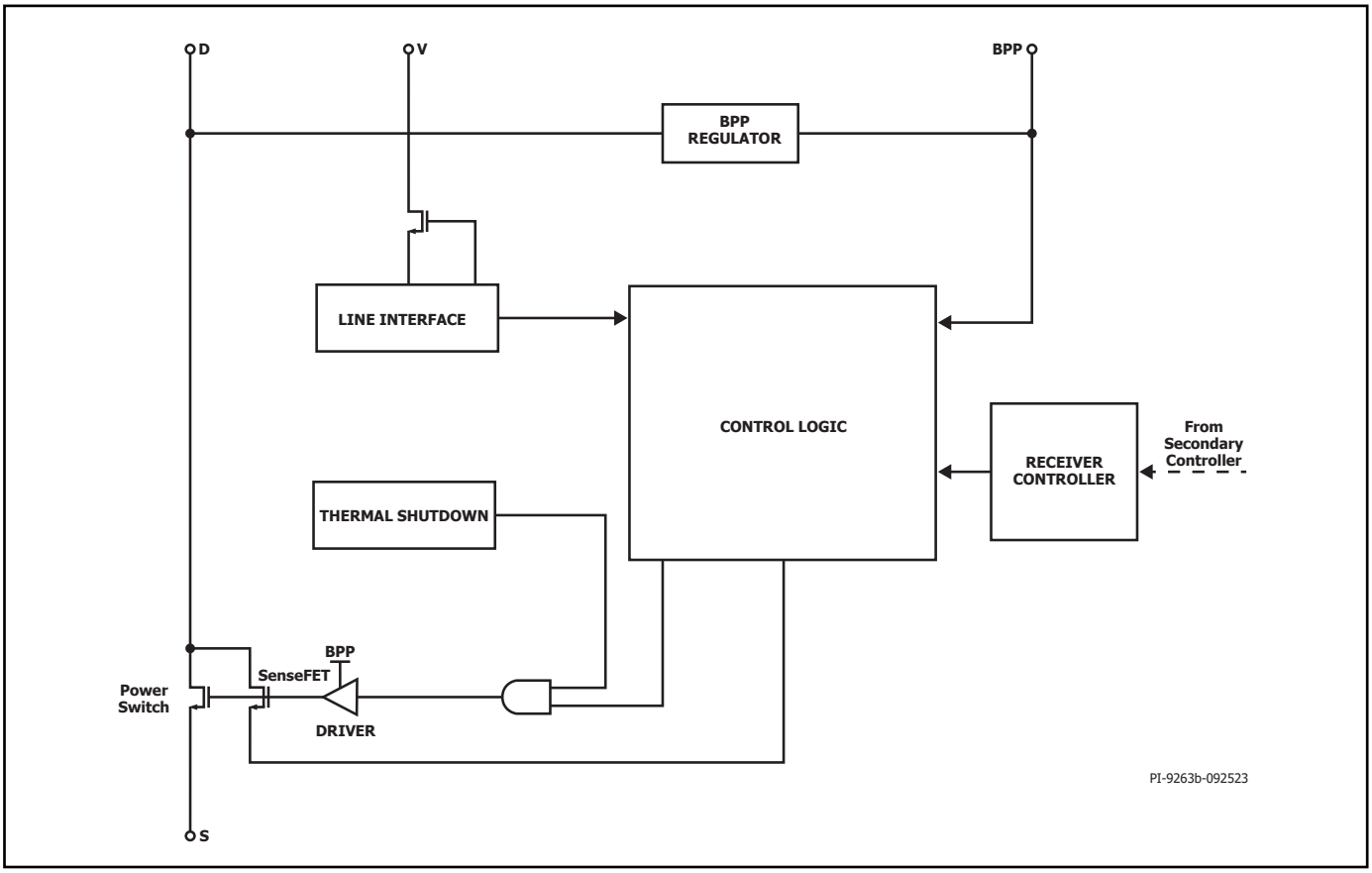


Figure 3. Primary Controller Block Diagram.

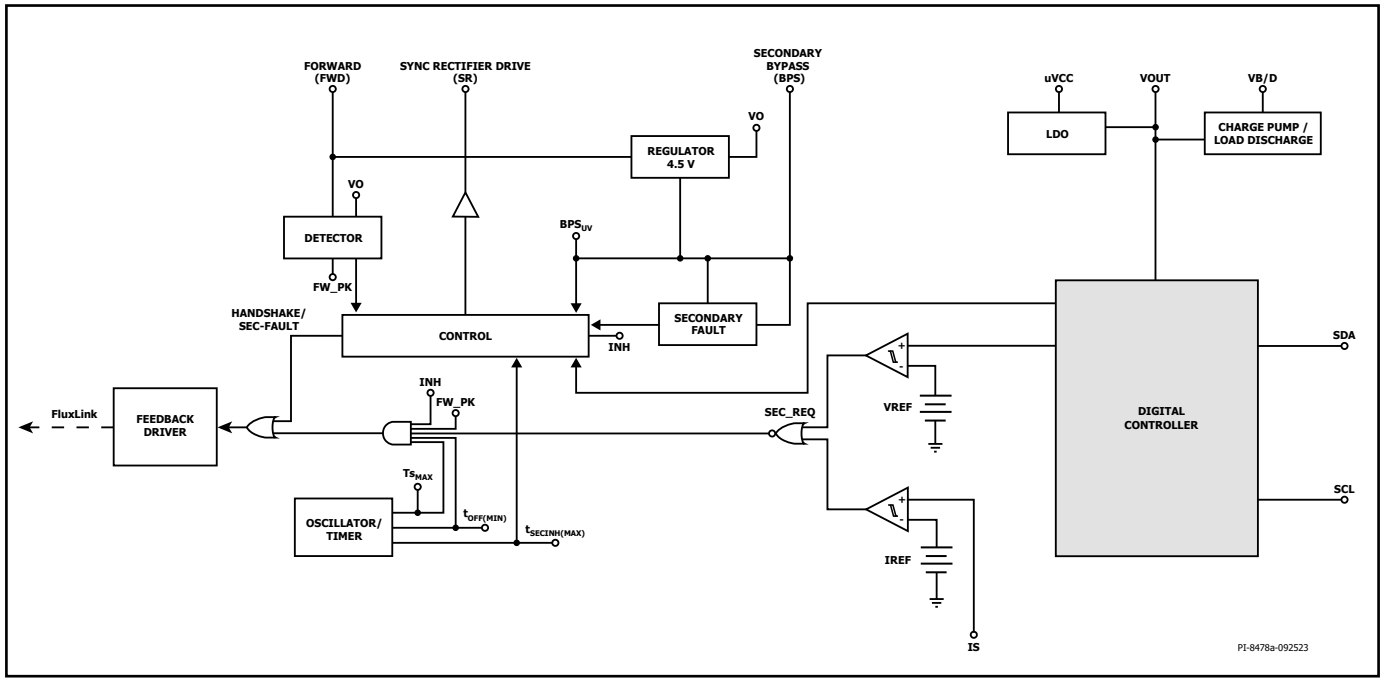


Figure 4. Secondary Controller Block Diagram.

Pin Functional Description

ISENSE (IS) Pin (Pin 1)
Connection to the power supply return output terminals. An external current sense resistor should be connected between this and the SECONDARY GROUND pin.

SECONDARY GROUND (GND) (Pin 2)
Ground reference for the secondary IC. Note this is not the power supply output ground due to the presence of the sense resistor between this and the ISENSE pin.

NC Pin (Pin 3)
Leave it open. Should not be connected to any other pins.

SECONDARY BYPASS (BPS) Pin (Pin 4)
It is the connection point for an external bypass capacitor for the secondary IC supply.

I²C CLOCK (SCL) Pin (Pin 5)
I²C serial communication protocol clock line sourced by the bus master.

I²C SERIAL DATA (SDA) Pin (Pin 6)
I²C serial communication protocol data line sourced by the bus master.

EXTERNAL VCC SUPPLY (uVCC) Pin (Pin 7)
This is 3.6 V supply for an external controller.

VBUS SERIES SWITCH DRIVE AND LOAD DISCHARGE (VB/D) Pin (Pin 8)
V_{BUS} enable and driver for NMOS gate for V_{OUT} to V_{BUS} series pass FET(s). This pin is also used to discharge output load voltage (V_{BUS}).

SYNCHRONOUS RECTIFIER DRIVE (SR) Pin (Pin 9)
Gate driver output and connection to external SR FET gate.

OUTPUT VOLTAGE (VOUT) Pin (Pin 10)
Connected directly to the output voltage providing current for the secondary IC and sense for output voltage regulation. This pin also has an active/programmable pull-down current source.

FORWARD (FWD) Pin (Pin 11)
The connection point to the switching node of the transformer output winding provides information on the primary switch timing plus providing power for the secondary IC when V_{OUT} is below a threshold value.

NC Pin (Pin 12-14)
Leave it open. Should not be connected to any other pins.

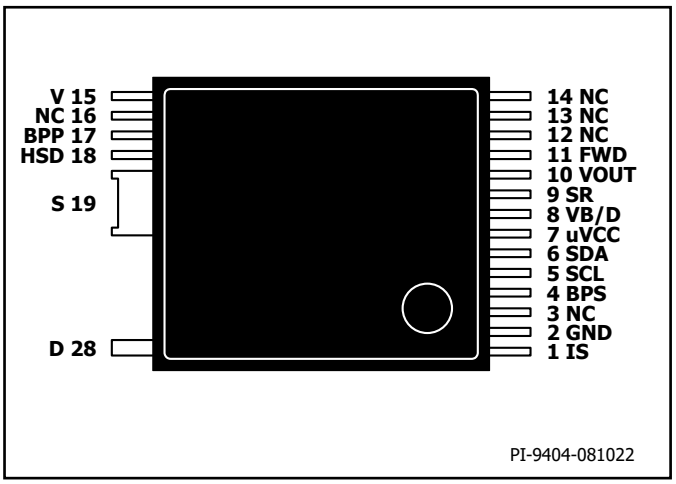


Figure 5. Pin Configuration.

UNDER/OVER INPUT VOLTAGE (V) Pin (Pin 15)
A high-voltage pin connected to the AC or DC side of the input bridge for detecting under and overvoltage conditions at the power supply input. When connected to the AC side of the bridge, a high-voltage switch is opened when not sensing to reduce power consumption. This pin should be tied to GND to disable UV/OV protection.

NC Pin (Pin 16)
Leave open or connect to SOURCE pin or BPP pin.

PRIMARY BYPASS (BPP) Pin (Pin 17)
The connection point for an external bypass capacitor for the primary IC supply. This is also the I_{LIM} selection pin for choosing standard I_{LIM} or I_{LIM+1}.

HSD Pin (Pin 18)
HSD pin should be tied to ground.

SOURCE (S) Pin (Pin 19)
These pins are the power switch source connection. It is also ground reference for primary BYPASS pin.

DRAIN (D) Pin (Pin 28)
This pin is the power switch drain connection.

InnoSwitch5-Pro Functional Description

The InnoSwitch5-Pro combines a high-voltage power switch, along with both primary-side and secondary-side controllers in one device.

The architecture incorporates a novel inductive coupling feedback scheme (FluxLink) using the package lead frame and bond wires to provide a safe, reliable, and cost-effective means to transmit accurate, output voltage and current information from the secondary controller to the primary controller.

The InnoSwitch5-Pro secondary controller consists of a transmitter circuit that is magnetically coupled to the primary receiver, an I^2C interface to control power supply parameters and telemetry functions, a 4.5 V regulator on the SECONDARY BYPASS pin, synchronous rectifier FET driver, oscillator and timing functions, and a host of integrated protection features.

The primary controller on lnnoSwitch5-Pro is a quasi-resonant (QR) flyback controller that has the ability to operate in continuous conduction mode (CCM). The controller uses both variable frequency and variable current limit control schemes. The primary controller consists of a frequency jitter oscillator, a receiver circuit magnetically coupled to the secondary controller, a current limit controller, 5 V regulator on the PRIMARY BYPASS pin, bypass overvoltage detection circuit, a lossless input line sensing circuit, current limit selection circuitry, over-temperature protection and leading edge blanking.

Figure 3 and Figure 4 show the functional block diagrams of the primary and secondary controller with the most important features.

Primary Controller

InnoSwitch5-Pro IC is a variable frequency controller allowing CCM/ CrM/DCM operation for enhanced efficiency and extended output power
capability.

PRIMARY BYPASS Pin Regulator
The PRIMARY BYPASS pin has an internal regulator that charges the PRIMARY BYPASS pin capacitor to V_{BPP} by drawing current from the DRAIN pin whenever the power switch is off. The PRIMARY BYPASS pin is the internal supply voltage node. When the power switch is on, the device operates from the energy stored in the PRIMARY BYPASS pin capacitor.

In addition, a shunt regulator clamps the PRIMARY BYPASS pin voltage to V_{SHUNT} when current is provided to the PRIMARY BYPASS pin through an external resistor. This allows the InnoSwitch5-Pro IC to be powered externally through a bias winding, decreasing the no-load consumption to less than 30 mW in a 5 V output design.

Primary Bypass I_{LIM} Programming
InnoSwitch5-Pro ICs allows the user to adjust current limit (I_{LIM}) settings through the selection of the PRIMARY BYPASS pin capacitor value. A ceramic capacitor can be used.

There are 2 selectable capacitor sizes – 0.47 µF and 4.7 µF for setting standard and increased I_{LIM} settings respectively.

Primary Bypass Undervoltage Threshold
The PRIMARY BYPASS pin undervoltage circuitry disables the power switch when the PRIMARY BYPASS pin voltage drops below ~4.5 V ($V_{BPP} – V_{BPP(H)}$) in steady-state operation. Once the PRIMARY BYPASS pin voltage falls below this threshold, it must rise to V_{SHUNT} to re-enable turn-on of the power switch.

PRIMARY BYPASS Pin Overvoltage Function
The PRIMARY BYPASS pin has an optional latching OV protection feature. A Zener diode in parallel with the resistor in series with the PRIMARY BYPASS pin capacitor is typically used to detect an overvoltage on the primary bias winding and activate the protection mechanism. In the event that the current into the PRIMARY BYPASS pin exceeds I_{SD}, the device will latch-off or disable the power switch switching for a time $t_{AR(OFF)}$, after which time the controller will restart and attempt to return to regulation.

V_{OUT} OV protection is also included as an integrated feature on the secondary controller (see Output Voltage Protection).

Over-Temperature Protection
The thermal shutdown circuitry senses the primary switch die temperature. The threshold is set to T_{SD} with either a hysteretic or latch-off response.

Hysteretic response: If the die temperature rises above the threshold, the power switch is disabled and remains disabled until the die temperature falls by $T_{SD(H)}$ at which point switching is re-enabled. A large amount of hysteresis is provided to prevent over-heating of the PCB due to a continuous fault condition.

Latch-off response: If the die temperature rises above the threshold the power switch is disabled. The latching condition is reset by bringing the PRIMARY BYPASS pin below $V_{BPP(RESET)}$ or by going below the UNDER/OVER INPUT VOLTAGE pin UV (I_{UV-}) threshold.

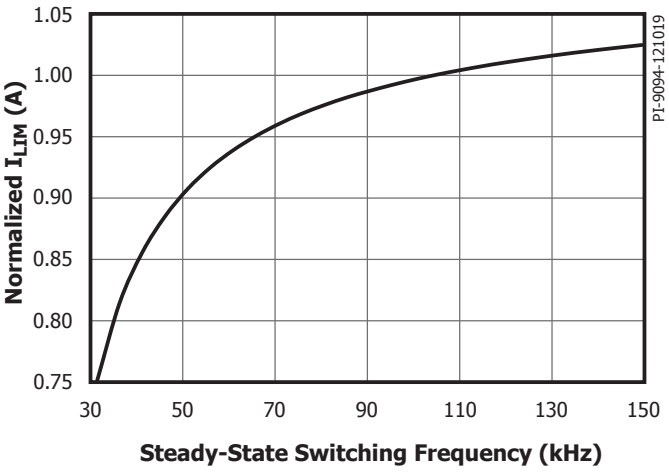


Figure 6. Normalized Primary Current vs. Frequency.

Current Limit Operation
The primary-side controller has a current limit threshold ramp that is inversely proportional to the time from the end of the previous primary switching cycle (i.e. from the time the primary switch turns off at the end of a switching cycle).

This characteristic produces a primary current limit that increases as the switching frequency (load) increases (Figure 6).

This algorithm enables the most efficient use of the primary switch with the benefit that this algorithm responds to digital feedback information immediately when a feedback switching cycle request is received.

At full load, switching cycles have a maximum current approaching 100% I_{LIMIT}. This gradually reduces to 30% of the full current limit as load decreases. Once 30% current limit is reached, there is no further reduction in current limit (since this is low enough to avoid audible noise). The time between switching cycles will continue to increase as load reduces.

Jitter

The normalized current limit is modulated between 100% and 95% at a modulation frequency of f_M this results in a frequency jitter of ~7 kHz with average frequency of ~100 kHz.

Auto-Restart

In the event a fault condition occurs (such as an output overload, output short-circuit, or external component/pin fault), the InnoSwitch5-Pro IC enters auto-restart (AR) or latches off. The latching condition is reset by bringing the PRIMARY BYPASS pin below $V_{BPP(RESET)}$ or by going below the UNDER/OVER INPUT VOLTAGE pin UV (I_{UV-}) threshold.

In auto-restart, switching of the power switch is disabled for $t_{AR(OFF)}$. There are 2 ways to enter auto-restart:

1. Continuous secondary requests at above the overload detection frequency f_{OVL} for longer than 82 ms (t_{AR}).
2. No requests for switching cycles from the secondary for > $t_{AR(SK)}$.

The second is included to ensure that if communication is lost, the primary tries to restart. Although this should never be the case in normal operation, it can be useful when system ESD events (for example) causes a loss of communication due to noise disturbing the secondary controller. The issue is resolved when the primary restarts after an auto-restart off-time.

The auto-restart is reset as soon as an AC reset occurs.

SOA Protection

In the event that there are two consecutive cycles where 110% I_{LIMIT} is reached within ~500 ns (the blanking time + current limit delay time), the controller will skip 2.5 cycles or ~25 µs. This provides sufficient time for the transformer to reset with large capacitive loads without extending the start-up time.

Input Line Voltage Monitoring

The UNDER/OVER INPUT VOLTAGE pin is used for input undervoltage and overvoltage sensing and protection.

A sense resistor is tied between the high-voltage DC bulk capacitor after the bridge (or to the AC side of the bridge rectifier for fast AC reset) and the UNDER/OVER INPUT VOLTAGE pin to enable this functionality. This function can be disabled by shorting the UNDER/OVER INPUT VOLTAGE pin to primary GND.

At power-up, after the primary bypass capacitor is charged and the I_{LIM} state is latched, and prior to switching, the state of the UNDER/OVER INPUT VOLTAGE pin is checked to confirm that it is above the brown-in and below the overvoltage shutdown thresholds.

In normal operation, if the UNDER/OVER INPUT VOLTAGE pin current falls below the brown-out threshold and remains below brown-out for longer than t_{UV-}, the controller enters auto-restart. Switching will only resume once the UNDER/OVER INPUT VOLTAGE pin current is above the brown-in threshold.

In the event that the UNDER/OVER INPUT VOLTAGE pin current is above the overvoltage threshold, the controller will also enter auto-restart. Again, switching will only resume once the UNDER/OVER INPUT VOLTAGE pin current has returned to within its normal operating range.

The input line UV/OV function makes use of a internal high-voltage MOSFET on the UNDER/OVER INPUT VOLTAGE pin to reduce power consumption. If the cycle off-time t_{OFF} is greater than 50 µs, the internal high-voltage MOSFET will disconnect the external sense resistor from the internal IC to eliminate current drawn through the sense resistor. The line sensing function will activate again at the beginning of the next switching cycle.

Primary-Secondary Handshake

At start-up, the primary-side initially switches without any feedback information (this is very similar to the operation of a standard TOPSwitch™, TinySwitch™ or LinkSwitch™ controllers).

If no feedback signals are received during the auto-restart on-time (t_{AR}), the primary goes into auto-restart mode. Under normal conditions, the secondary controller will power-up via the FORWARD pin or from the OUTPUT VOLTAGE pin and take over control. From this point onwards, the secondary controls switching.

If the primary controller stops switching or does not respond to cycle requests from the secondary during normal operation (when the secondary has control), the handshake protocol is initiated to ensure that the secondary is ready to assume control once the primary begins to switch again. An additional handshake is also triggered if the secondary detects that the primary is providing more cycles than were requested.

The most likely event that could require an additional handshake is when the primary stops switching as the result of a momentary line brown-out event. When the primary resumes operation, it will default to a start-up condition and attempt to detect handshake pulses from the secondary.

If secondary does not detect that the primary responds to switching requests for 8 consecutive cycles, or if the secondary detects that the primary is switching without cycle requests for 4 or more consecutive cycles, the secondary controller will initiate a second handshake sequence. This provides additional protection against cross-conduction of the SR FET while the primary is switching. This protection mode also prevents an output overvoltage condition in the event that the primary is reset while the secondary is still in control.

Wait and Listen

When the primary resumes switching after initial power-up recovery from an input line voltage fault (UV or OV) or an auto-restart event, it will assume control and require a successful handshake to relinquish control to the secondary controller.

As an additional safety measure the primary will pause for an auto-restart on-time period, t_{AR} (~82 ms), before switching. During this "wait" time, the primary will "listen" for secondary requests. If it sees two consecutive secondary requests, separated by ~30 µs, the primary will infer secondary control and begin switching in slave mode. If no pulses occurs during the t_{AR} "wait" period, the primary will begin switching under primary control until handshake pulses are received.

Secondary Controller

As shown in the block diagram in Figure 4, the IC is powered by a 4.5 V (V_{BPS}) regulator which is supplied by either VOUT or FWD pins. The SECONDARY BYPASS pin is connected to an external decoupling capacitor and fed internally from the regulator block.

The FORWARD pin also connects to the negative edge detection block used for both handshaking and timing to turn on the SR FET connected to the SYNCHRONOUS RECTIFIER DRIVE pin. The FORWARD pin voltage is used to determine when to turn off the SR FET in discontinuous mode operation. This is when the voltage across the $R_{DS(ON)}$ of the SR FET drops below zero volts.

In continuous conduction mode (CCM) the SR FET is turned off before the pulse request is sent to the primary to demand the next switching cycle, providing excellent synchronous operation, free of any overlap for the FET turn-off.

The output voltage is regulated on the VOUT pin and defaults to 5 V at start-up.

The external current sense resistor connected between ISENSE and SECONDARY GROUND pins is used to regulate the output current in constant current regulation mode.

Programmable Voltage and Current

The operating voltage and current set points are set fully programmable through I^2C interface. The output voltage is fully user programmable with a range from 3 V to 30 V. The fast response feedback loop of the IC features 10 mV (ΔV_{OUT}) voltage change resolution. The programmable current set point features 15% to 100% operating range, with a programming step size of 0.52% of full scale current. Below 5 V and for load current less than 50 mA, voltage command step size of 10 mV may result in non-montonicity since operating frequency is very low.

Minimum Off-Time

The secondary controller initiates a cycle request using the FluxLink connection to the primary. The maximum frequency of secondary-cycle requests is limited by a minimum cycle off-time of $t_{OFF(MIN)}$. This is in order to ensure that there is sufficient reset time after primary conduction to deliver energy to the load.

Maximum Switching Frequency

The maximum switch-request frequency of the secondary controller is f_{SREQ}.

Internal uVCC Generation, Bus Switch Driver and Discharge

The internal LDO generates 3.6 V uVCC for MCU which simplifies the system design. InnoSwitch5-Pro also has an internal driver that guarantees turn-on of an n-channel FET series bus switch with source voltage as high as 30 V. The VB/D pin which enables the bus switch is also configurable as the discharge path for the load.

Programmable Protections

User programmable protection features include output undervoltage (UV) and overvoltage (OV) protection and over-temperature protection.

The UV/OV thresholds are dynamically programmable. Users can program four responses to these protections, including auto-restart, latch-off, disable output, and no-response. An auto-restart (AR) or latch-off (LO) response does not inherently open the series bus switch. The I^2C master must send a command to open it if this is the desired behavior.

The secondary controller also features generation of an interrupt signal if one or more of the faults is detected. The SCL pin is pulled down for ~55 µs to generate an interrupt for MCU.

In the case when the MCU loses communication with the secondary controller, a watchdog timer triggers a reset to reassert a safe 5 V condition and opens the series bus switch.

Telemetry Feature

The controller communicates to the MCU to report back the status of the power supply. Output voltage and current is measured by internal ADC and available to MCU through I^2C. The telemetry features also covers CV, CC and constant power set points, OV/UV thresholds, all protection settings, interrupt status, and complete fault status.

Frequency Soft-Start
At start-up the primary controller is limited to a maximum switching frequency of f_{SW} and 75% of the maximum programmed current limit at the switch-request frequency of 100 kHz.

After handshake is completed the secondary controller linearly ramps up the switching frequency from f_{SW} to f_{SREQ} over the ~10 ms time period.

In the event of a short-circuit or overload at start-up, the device will move directly into CC (constant-current) mode. The device will go into auto-restart (AR), if the output voltage does not rise above the 3.6 V before the expiration of the soft-start timer after handshake has occurred.

If the output voltage reaches regulation within the soft-start time period, the frequency ramp is immediately aborted and the secondary controller is permitted to go full frequency. This will allow the controller to maintain regulation in the event of a sudden transient loading soon after regulation is achieved. The frequency ramp will only be aborted if quasi-resonant-detection programming has already occurred.

Maximum Secondary Inhibit Period
Secondary requests to initiate primary switching are inhibited to maintain operation below maximum frequency and ensure minimum off-time. Besides these constraints, secondary-cycle requests are also inhibited during the "ON" time cycle of the primary switch (time between the cycle request and detection of FORWARD pin falling edge). The maximum time-out in the event that a FORWARD pin falling edge is not detected after a cycle requested is ~30 µs.

SR Disable Protection
In eahch cycle SR is only engaged if a set cycle was requested by the secondary controller and the negative edge is detected on the FORWARD pin. In the event that the voltage on the ISENSE pin exceeds approximately 3 times the CC threshold, the SR FET drive is disabled until the surge current has diminished to nominal levels.

In SRZVS mode of operation, it is recommended to write 0x0E09 into the command register address 0x38 (with parity) to disable SR gate drive under any circumstances of primary switching without any cycle request from the secondary controller or cross conduction detection event. The detection is based on the signal on FORWARD pin and if the signal FORWARD pin has rings going below ground (<0 V, during DCM mode of operation), this can result in SR gate drive being disabled in the subsequent switching cycles. It is recommended to improve the FORWARD pin signal to not have any DCV ringing going below ground during normal operation to avoid SR gate drive disable protection to trigger. In such designs, bit[2:0] of the command above can be incremented in steps of 1b'1 to avoid this protection feature to trigger under normal operation conditions.

When the SR gate drive is disabled due to this protection feature, quasi-resonant switching also gets disable and both SR gate drive and quasi-resonant switching get reinstated automatically once the fault condition is cleared. If this protection feature interferes with normal operation at certain conditions, and of not desirable, it can be disabled by writing 0x0201 into 0x38 (with parity) command register.

In non-SRZVS mode of opeation, it is recommended to write 0x0A09 into the command register address 0x38 (with parity) to enable this protection feature. To disable the protection feature write 0x0201 into the same command register.

SR Static Pull-Down
To ensure that the SR gate is held low when the secondary is not in control, the SYNCHRONOUS RECTIFIER DRIVE pin has internal nominally "ON" device to pull the pin low and reduce any voltage on the SR gate due to capacitive coupling from the FORWARD pin.

Open SR Protection
In order to protect against an open SYNCHRONOUS RECTIFIER DRIVE pin system fault the secondary controller has a protection mode to ensure the SYNCHRONOUS RECTIFIER DRIVE pin is connected to an external FET. If the external capacitance on the SYNCHRONOUS RECTIFIER DRIVE pin is below ~200 pF, the device will assume the SYNCHRONOUS RECTIFIER DRIVE pin is "open" and there is no FET to drive. If the pin capacitance detected is above ~200 pF, the controller will assume an SR FET is connected.

In the event the SYNCHRONOUS RECTIFIER DRIVE pin is detected to be open, the secondary controller will stop requesting pulses from the primary to initiate auto-restart.

If the SYNCHRONOUS RECTIFIER DRIVE pin is tied to ground at start-up, the SR drive function is disabled and the open SYNCHRONOUS RECTIFIER DRIVE pin protection mode is also disabled.

Dynamically Programmable ZVS Operation in DCM Mode using Synchronous Rectifier
In order to improve the conversion efficiency and eliminate switching losses, the InnoSwitch5-Pro IC features a means of achieving zero voltage switching of the primary switch by enabling the synchronous rectifier for short period before sending the switching request in DCM mode of operation. During this time magnetizing current is charged in negative direction at the rate determined by the reflected output voltage on the primary. At the end of SR conduction time, the magnetizing energy will start discharging the drain node capacitance on the primary switch to force the voltage across the primary power switch to zero before every conduction cycle. This mode of operation is available only in the Discontinuous Conduction Mode and the feature gets disabled automatically when there is a CCM switching request. Power converter can be enforced to operate in DCM only mode by sending I^2C command. Enabling SR-ZVS mode benefits the SR FET as well by limiting the peak voltage across the SR FET when primary switch turns ON. See Figure 7.

Rather than detecting the magnetizing ring peak on the primary-side, the valley voltage of the FORWARD pin voltage as it falls below the output voltage is used to initiate the SR-ZVS operation. The details of I^2C programming commands for this mode are provided in the command register section of the data sheet.

SRZVS mode of operation uses output energy to achieve the zero-voltage switching of the primary power switch. It is beneficial when used at high input line condition and higher load conditions with sufficient reflected output voltage to charge the magnetizing current in negative direction in short period.

In SR-ZVS mode, a TVS diode in the primary clamp circuit is required to limit the peak drain voltage of InnoSwitch5-Pro primary switch during abnormal transient events such as ESD and EFT.

Intelligent Quasi-Resonant Mode Switching
In order to improve conversion efficiency and reduce switching losses, the lnnoSwitch5-Pro IC features a means to force switching when the voltage across the primary switch is near its minimum voltage when the converter operates in discontinuous conduction mode (DCM). This mode of operation is automatically engaged in DCM and disabled once the converter moves to continuous conduction mode (CCM). See Figure 8.

Rather than detecting the magnetizing ring valley on the primary-side, the peak voltage of the FORWARD pin voltage as it rises above the output voltage level is used to gate secondary requests to initiate the switch "ON" cycle in the primary controller.

The secondary controller detects when the controller enters in discontinuous-mode and opens secondary cycle request windows corresponding to minimum switching voltage across the primary power switch.

Quasi-resonant (QR) mode is enabled for ~20 µs after DCM is detected. QR switching is disabled after ~20 µs, at which point switching may occur at any time a secondary request is initiated. The secondary controller includes blanking of ~1 µs to prevent false detection of primary "ON" cycle when the FORWARD pin rings below ground.

ZVS and QR Switching Window Optimization

The InnoSwitch5-Pro IC allows for optimization of switching to achieve QR / Valley switching as close to the peak / minimum FORWARD pin voltage respectively. Command register 0x02 = 0x1F is recommended for optimal switching.

Default value is 0x01.

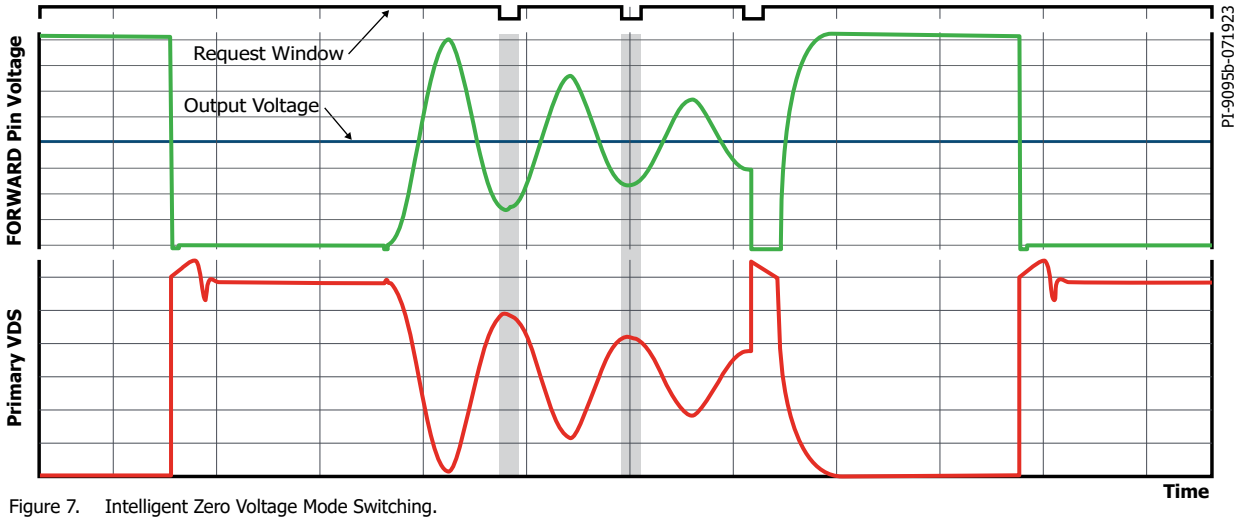


Figure 7. Intelligent Zero Voltage Mode Switching.

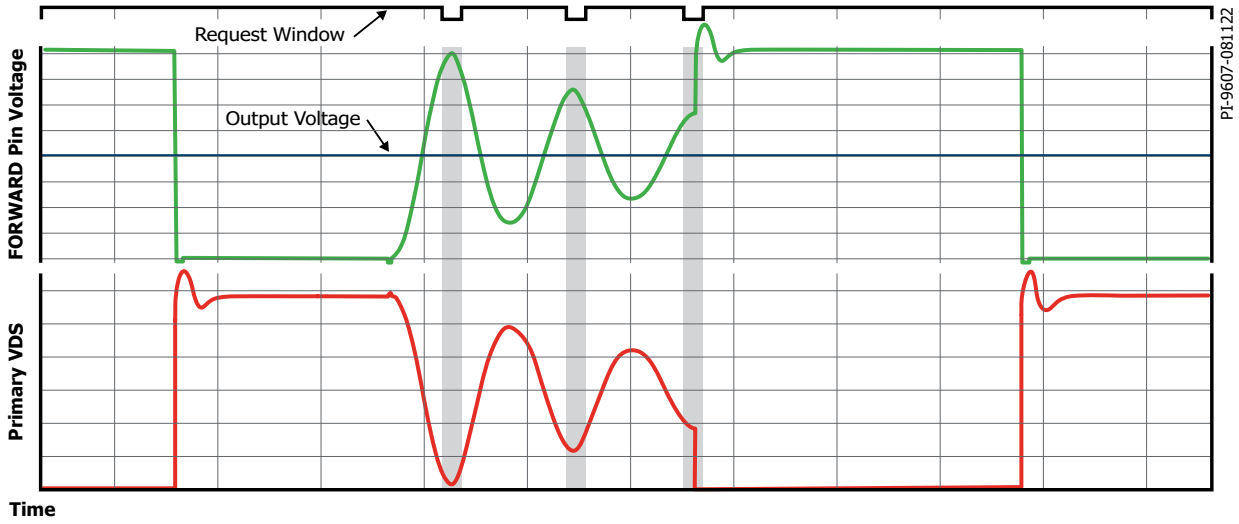


Figure 8. Intelligent Quasi-Resonant Mode Switching.

Register Definition

I²C Slave Address

The InnoSwitch5-Pro 7-bit slave address is 0x18 (7'b001 1000).

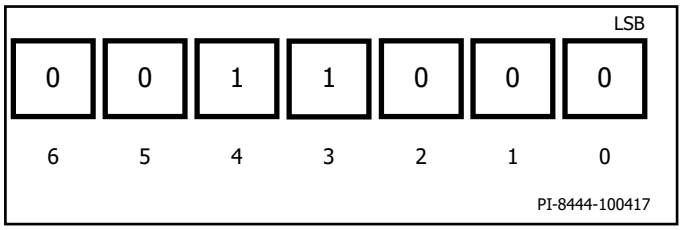


Figure 9. PI Slave Address.

I²C Protocol Format is 3-Byte Write Command

Write commands:
[PI_SLAVE_ADDRESS][W][A][PI_COMMAND][A][Byte][A] or
[PI_SLAVE_ADDRESS][W][A][PI_COMMAND][A][Low Byte][A][High Byte][A]

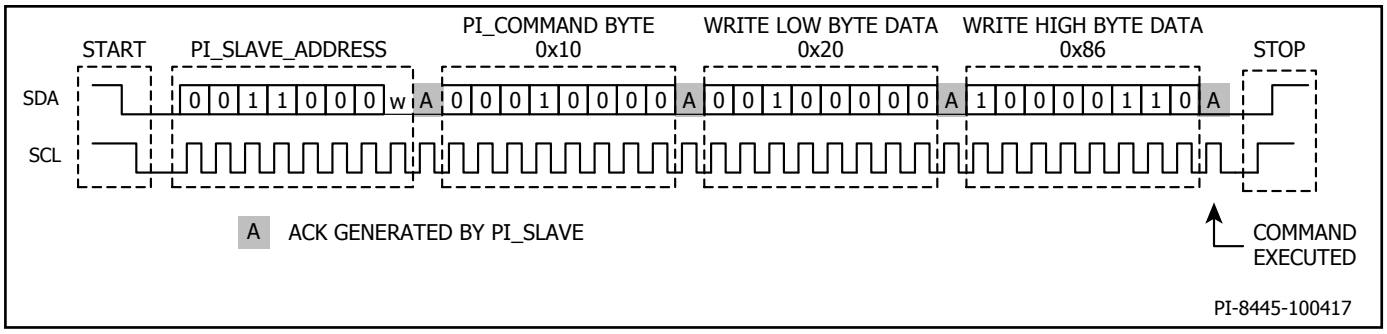


Figure 10. Example Register Write Command Sequence (CV set to 8 V).

I²C Protocol Format is 2-Byte Read Command

Word Read transaction:
[PI_SLAVE_ADDRESS][W][A][PI_COMMAND][A][START_TELEMETRY_REGISTER_ADDRESS]
[A][END_TELEMETRY_REGISTER_ADDRESS [A]
[PI_SLAVE_ADDRESS] [r][A]{PI Slave responds Low Byte}[a]{PI Slave responds High Byte}[na]

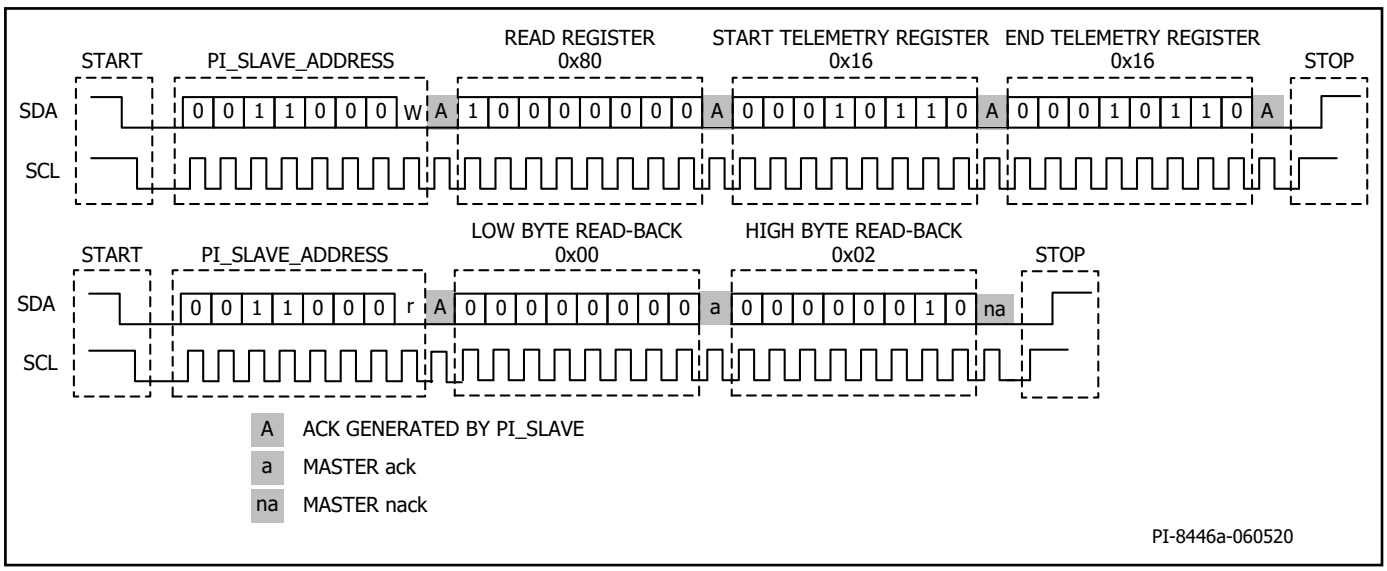


Figure 11. Example Read Register Sequence (Read Fault Register READ11). Note: START and END TELEMETRY Register Addresses Does Not Have to Point to Same Register to Read multiple Registers in Single Command.

Write and Read Command I²C Protocol

[A] denotes a Slave Acknowledgement
[a] denotes a Master Acknowledgement
[na] denotes a Master nack
[W] denotes Write (1'b0)
[r] denotes Read (1'b1)
[PI_SLAVE_ADDRESS] = 0x18 (7'b001 1000)
[PI_COMMAND] (see PI COMMAND Register Address Assignments, Description and Control Range Section)
[TELEMETRY_REGISTER_ADDRESS] (see Telemetry (Read-Back) Registers Address Assignment and Description Section)

Every I²C transaction should have a minimum of 150 µsec delay between commands. If this delay is not provided, commands may be ignored. The InnoSwitch5-Pro does not support clock stretching.

PI COMMAND Register Address Assignments, Description and Control Range

All command register addresses in InnoSwitch5-Pro IC are odd-parity addressing. Some select registers (some highlighted below) also employ odd parity error bit to the high and low bytes of data.

Name	Function	Adjustment Range	Register Address		Type	Default	Description		
			Address	Address with Odd Parity					
VBEN	Series Bus Switch Control	Enable or Disabled	0x04		W_Byte	0x0	bit[7]	Parity	
							bit[1:0]	{11} Enable VBEN/Disable VDIS {01} Disable VBEN/No Reset {00} Disable VBEN/Reset	
BLEEDER[B]	Activate Bleeder (V_{OUT}) Function	Enable or Disabled	0x06	0x86	W_Byte	0xD0	bit[2]	{0}: Auto disable when VOUT<10PCT {1}: Auto disable when VOUT<4PCT	
							bit[1:0]	{00}: Disabled {11}: Enabled with auto disable OTP clears this register	
VDIS	Load (VBUS) Discharge	Enable or Disabled	0x08		W_Byte	0x0	bit[7]	Parity	
							bit[3:0]	{0011} Enable Discharge/ Disable VBEN/Reset {0010} Enable Discharge/ Disable VBEN No Reset {1110} Disable Discharge	
Turn-Off PSU	Latch-Off Device	Enable or Disabled	0x0A	0x8A	W_Byte	0x0	bit[0]	{0}: Disabled {1}: Enabled	
Fast VI Command	Speed of CV/CC Update	10 ms Update Limit or No Speed Limit	0x0C	0x8C	W_Byte	0x0	bit[0]	{1}: Disable 10 msec update limit	
CVO	Constant-Voltage Only	Only CV Mode	0x0E		W_Byte	0x04	bit[4:3]	{11}: 64 ms {10}: 32 ms {01}: 16 ms {00}: 8 ms	
							bit[2:1]	{11}: Disable-Output[A] {10}: Auto-Restart {01}: Latch-Off {00}: No Response	
							bit[0]	{1}: CV Only Mode/No CC Regulation	
CV	Output Voltage	3 V to 30 V (10 mV/step)	0x10		W_Word	500 (5 V)	bit[15]	High Byte Parity	Range {300 to 3000} 10 mV/LSB
							bit[12:8]	Output Voltage	
							bit[7]	Low Byte Parity	
							bit[6:0]	Output Voltage	

Table 2. Command Register Assignments.

Name	Function	Adjustment Range	Register Address		Type	Default	Description		
			Address	Address with Odd Parity					
OVA	Overvoltage Programming	3.3 V to 40 V (100 mV/step)	0x12	0x92	W_Word	Auto-Restart 96 (9.6 V)	bit[15]	High Byte Parity	Range {33 to 400} 100 mV/LSB
							bit[11:10]	{11}: Disable-Output[A] {10}: Auto-Restart {01}: Latch-Off {00}: No Response	
							bit[9:8]	Threshold	
							bit[7]	Low Byte Parity	
							bit[6:0]	Threshold	
UVA	Undervoltage Threshold	2.7 V to 40 V (100 mV/step)	0x14	0x94	W_Word	64 ms Auto-Restart 36 (3.6 V)	bit[15]	High Byte Parity	Range {27 to 400} 100 mV/LSB
							bit[14]	0: Enable UVL timer 1: Disable UVL timer	
							bit[13:12]	{11}: 64ms {10}: 32ms {01}: 16ms {00}: 8ms	
							bit[11:10]	{11}: Disable-Output[A] {10}: Auto-Restart {01}: Latch-Off {00}: No Response	
							bit[9:8]	Threshold	
							bit[7]	Low Byte Parity	
							bit[6:0]	Threshold	
CDC	Cable Drop Compensation	0 mV to 600 mV (50 mV/step)	0x16		W_Word	0 (0 V)	bit[3:0]	Range {0 to 12} 50 mV/LSB	
CC	Constant Current Regulation	15% to 100% of CC, (0.17 mV/step/Rs)	0x18	0x98	W_Word	192 (100%)	bit[15]	High Byte Parity	Range {29 (15%) to 192 (100%)}
							bit[8]		
							bit[7]	Low Byte Parity	
							bit[6:0]		
V_{KP}	Constant Output Power Knee Voltage	5.3 V to 30 V (100 mV/step)	0x1A		W_Word	300 (30 V)	bit[15]	High Byte Parity	Range {53 to 300} 100 mV/LSB
							bit[8]		
							bit[7]	Low Byte Parity	
							bit[6:0]		
LS	Line Sense	Enable	0x1C		W_Byte	0x00	bit[0]	{1}: Line sense trigger, auto reset to 0	
CCSC	Output Short-Circuit Fault Detection	AR, Latch-off or No Response	0x20		W_Byte	0x02	bit[1:0]	{10}: Auto-Restart {01}: Latch-Off {00}: No Response	

Table 3. Command Register Assignments (cont.)

Name	Function	Adjustment Range	Register Address		Type	Default	Description	
			Address	Address with Odd Parity				
ISSC	IS pin Short Fault Response and Detection Frequency Threshold	Disable Output, AR, Latch-off or No Response	0x22	0xA2	W_Byte	0x32	bit[1:0]	{11}: Disable-Output[A] {10}: Auto-Restart {01}: Latch-Off {00}: No Response
		Frequency (30kHz/60kHz/ 90kHz/120kHz)					bit[3:2]	Frequency Detection Threshold {00}: 60 kHz {01}: 30 kHz {10}: 90 kHz {11}: 120 kHz
		Threshold for Current Limit					bit[6:4]	{001}: d'16 {010}: d'32 {011}: d'48 {100}: d'64 {101}: d'80 {110}: d'96 {111}: d'112
Watchdog Time	Communication Rate Monitor	Disable/0.5 s/1 s/2 s	0x26		W_Byte	0x01 (0.5 sec)	bit[1:0]	{00}: No Watch-Dog {01}: 0.5 sec {10}: 1 sec {11}: 2 sec
Interrupt	Interrupt Mask	Writing a non-zero value enables interrupt	0x2C		WR_Byte	0x00	bit[8]	Operating Mode Flag (OMF)
							bit[7]	Series Bus Switch Short
							bit[6]	Control Secondary
		Interrupt is automatically disabled after one interrupt pulse sent out					bit[5]	BPS Current Latch-off
							bit[4]	CVO Mode Peak load timer
							bit[3]	IS pin Short
							bit[2]	Output Short-Circuit
							bit[1]	VOUTUV)
							bit[0]	VOUT(OV)
VBUSSC	Series BUS Switch Short-Circuit Fault	Threshold for Current Sense	0x36	0xB6	W_Byte	0x02	bit[5:4]	{11}: d'72 {10}: d'64 {01}: d'32 {00}: d'48
		Number of Current Sense Samples					bit[3:2]	{11}: 4 samples {10}: 3 samples {01}: 2 samples {00}: 1 sample
		AR, Latch-off or No Response					bit[1:0]	{10}: Auto-Restart {01}: Latch-Off {00}: No Response
DCM-only	Discontinuous Conduction Mode Only	Enable or Disabled	0x3A	0xBA	W_Byte	0x00	bit[2]	{0}: Disable {1}: Enable

Table 4. Command Register Assignments (cont).

Name	Function	Adjustment Range	Register Address		Type	Default	Description
			Address	Address with Odd Parity			
SRZVS	SR based ZVS Mode	Disabled	0x3E		W_Byte	bit[11]	{1}: Enable FWD Valley Switching {0}: Disable FWD Valley Switching
						bit[10]	{1}: Enable SRZVS mode {0}: Disabled SRZVS mode
						bit[7:5]	SR-ZVS Delay Count[C]
						bit[4:0]	SR-ZVS ON Count[C]

Table 5. Command Registers Assignments (cont).

Notes:
A. Disable Output Fault Response Disables VBEN with Reset at fault. Reset may trigger AR depending on the operating conditions.
B. Disable the weak bleeder by writing 0x0x into 0x86 at power-on to reduce no-load power.
C. The minimum values for SR-ZVS ON count and Delay count should be >= d'3 to observe the change of ~85 ns with each step.

Telemetry (Read-Back) Registers Address Assignment and Description

	Name	Register Name	Register Address	Type	Register Bit Assignments		
Command Register Read-Back	READ1	Output Voltage Set-Point	0x02	R_Word	bit[15]	High Byte Parity	{Reg_CV}
					bit[12:8]		
					bit[7]	Low Byte Parity	
					bit[6:0]		
	READ2	Output Current Set-Point	0x04	R_Word	bit[15]	High Byte Parity	{Reg_CC}
					bit[8]		
					bit[7]	Low Byte Parity	
					bit[6:0]		
	READ3	Overvoltage Threshold	0x06	R_Word	bit[15]	High Byte Parity	{Reg_OVA} (10 mV/LSB)
					bit[12:8]		
					bit[7]	Low Byte Parity	
					bit[6:0]		
	READ4	Undervoltage Threshold	0x08	R_Word	bit[15]	High Byte Parity	{Reg_UVA} (10 mV/LSB)
					bit[12:8]		
					bit[7]	Low Byte Parity	
					bit[6:0]		
	READ5	Constant Power Threshold	0x0A	R_Word	bit[8:0]	{Reg_VKP}	
	READ6	Overvoltage Fault	0x0C	R_Word	bit[15:14]	{Reg_OVA_Response}	
		Undervoltage Fault			bit[13:12]	{Reg_UVA_Response}	
		Output Short-Circuit			bit[11:10]	{Reg_CCSC_Response}	
		IS pin Short			bit[9:8]	{Reg_ISSC_Response}	
		Undervoltage Time Out			bit[7:6]	{Reg_UVA_TIMER}	
		Watchdog Time Out			bit[5:4]	{Reg_WD_TIMER}	
		CV Mode			bit[3:2]	{Reg_CVO_Response}	
		CV Mode Timer			bit[1:0]	{Reg_CVO_TIMER}	
	READ7	VBUS Switch Enable	0x0E	R_Word	bit[14]	{Reg_VBEN}	
		Minimum Load			bit[13]	{Reg_BLEEDER}	
		Turn PSU Off			bit[12]	{Reg_PSUOFF}	
		Fast VI Commands			bit[11]	{Reg_FSTVIC}	
		Constant-Voltage Mode Only			bit[10]	{Reg_CVO}	
		Over-Temperature Fault Hysteresis			bit[9]	{Reg_OTP_HYS}	
		Cable Drop Compensation			bit[3:0]	{Reg_CDC}	
Measurement	READ8	Measured Output Current	0x10	R_Word	bit[15]	High Byte Parity	{Reg_ MEASURED_I}
					bit[8]		
					bit[7]	Low Byte Parity	
					bit[6:0]		
	READ9	Measured Output Voltage	0x12	R_Word	bit[15:12]	4'b0	
						Vout Range	Report-back resolution
						3 - 4 V	20 mV
						4 - 8 V	40 mV
						8 - 16 V	80 mV
						16 - 32 V	160 mV

Table 6. Telemetry (Read-Back) Register Assignments.

Name	Description	Register Address	Type	Register Name	
READ10 (Instanta-neous)	Interrupt Enable	0x14	R_Word	bit[15]	{Reg_INTERRUPT_EN}
	System Ready Signal			bit[14]	{Reg_CONTROL_S}
	Output Discharge			bit[13]	{Reg_VDIS}
	Line Sense Reporting Ready			bit[12]	{Reg_Line_Sense}
	Allow to Enter CV command			bit[10]	{Reg_CV_EN}
	Over-Temperature Protection Fault			bit[9]	{Reg_OTP}
	VOUT_ADC > 1.04*VOUT			bit[5]	{Reg_VOUT4PCT}
	VOUT_ADC > 1.1*VOUT			bit[4]	{Reg_VOUT10PCT}
	IS pin Short-Circuit Detected			bit[3]	{Reg_ISSC}
	Output Short-Circuit Detected			bit[2]	{Reg_CCSC}
	Output Voltage UV Fault Comparator			bit[1]	{Reg_VOUT_UV}
	Output Voltage OV Fault Comparator			bit[0]	{Reg_VOUT_OV}
READ11	Operating Mode Flag (OMF)	0x16	R_Word	bit[2]	CC Mode
				bit[1]	CP Mode
				bit[0]	CV Mode
READ12	Average Output Current	0x18	R_Word	bit[15:8]	8b'0
				bit[7:0]	16 sample average of READ 8
READ13	Average Output Voltage	0x1A	R_Word	bit[15:12]	4b'0
				bit[11:0]	16 sample average of READ 9
READ14	Voltage DAC	0x1C	R_Word	bit[15:8]	DAC_100mV
				bit[7:0]	DAC_10mV
READ15	CVO Mode DO	0x1E	R_Word	bit[6]	{Reg_DO_CVO}
	IS pin Short-Circuit DO			bit[4]	{Reg_DO_ISSC}
	Output Voltage OV DO			bit[2]	{Reg_DO_VOUT_OV}
	Output Voltage UV DO			bit[1]	{Reg_DO_VOUT_UV}
	Watchdog triggered			bit[0]	{Reg_Watchdog}
READ16	CVO Mode AR	0x20		bit[14]	{Reg_ar_CVO}
	Bus switch Short-Circuit AR			bit[13]	{Reg_ar_VBUSSC}
	IS pin Short-Circuit AR			bit[12]	{Reg_ar_ISSC}
	Output Short-Circuit AR			bit[11]	{Reg_ar_CCSC}
	Output Voltage OV AR			bit[10]	{Reg_ar_VOUT_OV}
	Output Voltage UV AR			bit[9]	{Reg_ar_VOUT_UV}
	PSU turn OFF command received			bit[7]	{Reg_Lo_CMD}
	CVO Mode LO			bit[6]	{Reg_Lo_CVO}
	Bus switch Short-Circuit LO			bit[5]	{Reg_Lo_VBUSSC}
	IS-pin Short-Circuit LO			bit[4]	{Reg_Lo_ISSC}
	Output Short-Circuit LO			bit[3]	{Reg_Lo_CCSC}
	Output Voltage OV LO			bit[2]	{Reg_Lo_VOUT_OV}
	Output Voltage UV LO			bit[1]	{Reg_Lo_VOUT_UV}
	BPS pin LO			bit[0]	{Reg_BPS_OV}

Table 7. Telemetry (Read-Back) Register Assignments (cont.)

Name	Description	Register Address	Type	Register Name		
READ17	Interrupts	0x22	R_Word	Mask	Status	
					bit[8]	{Reg_OMF}
					bit[7]	{Reg_VBUSSC}
				bit[15]	bit[6]	{Reg_~CONTROL_S}
				bit[14]	bit[5]	{Reg_LO_Fault}
				bit[13]	bit[4]	{Reg_CVO_AR}
				bit[12]	bit[3]	{Reg_ISSC}
				bit[11]	bit[2]	{Reg_CCSC}
				bit[10]	bit[1]	{Reg_VOUT_UV}
				bit[9]	bit[0]	{Reg_VOUT_OV}
READ21	Line Sense TON report	0x2A	R_Word	bit[15:12]		4b'0
				bit[11:0]		16 sample accumulated value of ~ primary switch ON time
READ22	Line Sense TOFF report	0x2C	R_Word	bit[15:0]		16 sample accumulated value of ~ SR switch ON time
READ23	End of Line Calibration	0x2E	R_Word	bit[3]		{0}: Positive offset {1}: Negative offset
				bit[2:0]		Constant Current regulation offset

Table 8. Telemetry (Read-Back) Register Assignments (cont.)

Command Registers

System Ready Status Register

The system ready bit {Reg_control_s} must be read prior to the start of any I²C transactions and after the InnoSwitch5-Pro has entered into a reset state resulting from auto-restart (AR), latch-off (LO), Disable Output (DO) or initial power-up.

When the {Reg_control_s} bit is set to "1", it means InnoSwitch5-Pro is ready to receive I²C commands.

To read the {Reg_control_s} bit, write the READ10 sub address 0x14 into the 0x80 address. Then read High Byte data back from address 0x80. The bit 14 is {Reg_control_s}.

Constant current regulation is based on the average current measurement register (READ12).

For a 5 A CC threshold, the current sense resistor is 6.4 mΩ. The current limit step size for this example is ~26 mA/step.

Example: For a power supply with maximum CC of 5 A (R_S = 6.4 mΩ), the following demonstrates changing the CC set point from 5 A to 2.5 A. This corresponds to change in CC from 100% (0xC0) to 50% (0x60) – with odd parity this becomes 0x80E0:

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	CC Register (0x98)
Low Byte:	0xE0 (8'b0100 0000)
High Byte:	0x80 (8'b1000 0000)

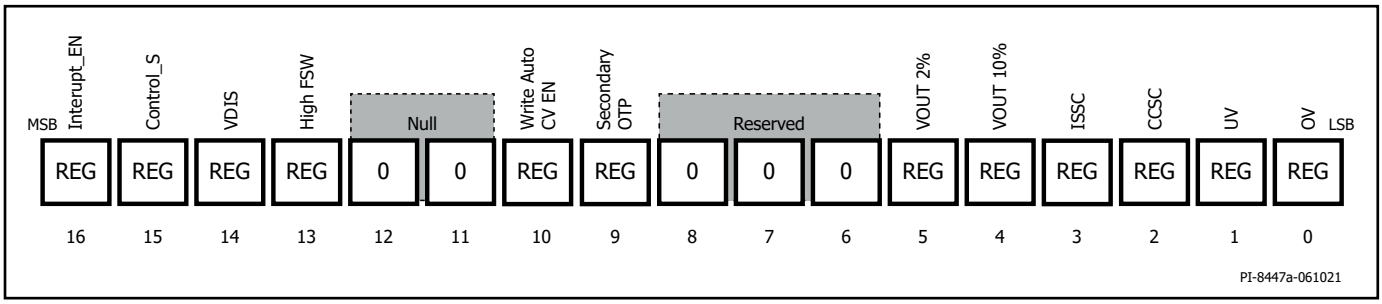


Figure 12. {Reg_Control_s} Telemetry Register (READ 10).

Example: Reading the {Reg_control_s} bit:

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
Read Register:	0x80
PI_Command:	READ10 (0x14), READ10 (0x14) PI_SLAVE_
ADDRESS [r]:	0x31 (8'b0011 0001)

Programming Output Voltage (CV), Output Constant Current (CC), Constant Power Mode (CP), Cable Drop Compensation (CDC) and Constant Voltage Only Mode (CVO)

CV Register (0x10)
The output voltage of the power supply is regulated on the VOUT pin. The valid programming range is from 3 V to 30 V with 10 mV / lsb. The default CV register value is 5 V. Below 5 V and at light load below 50 mA, output monotonicity may not be visible with 10 mV / steps.

Example: to change CV from 5 V to 8 V
Convert 8 V to lsb representation: 8/(10mV/lsb) = 800 Convert to hex format (800 = 0x0320)
With odd parity bits added the hex data is 0x8620)
The bit I²C command for this is shown below:

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	CV Register (0x10)
Low Byte:	0x20 (8'b0010 0000)
High Byte:	0x86 (8'b1000 0110)

This sequence of commands is shown in Figure 10 and Figure 24.

CC Register (0x98)
The constant current regulation register address is 0x18 and with odd parity it is 0x98. The constant current regulation threshold is adjustable from 15% (d'29) CC up to 100% (d'192) of the full scale. The full-scale constant-current threshold is set with the sense resistor between the IS and GND pins. The typical value for the full-scale current voltage drop is 32 mV ($I_{SV(TH)}$). The resolution step size is (0.52%/step):

32 mV/192 = 0.167 mV/step/Rs

Constant Output Power Voltage Threshold VKP (0x1A)
A constant output power characteristic is programmed via the "knee power voltage" in conjunction with the 100% constant current regulation threshold (full-scale current setting). If the full-scale CC is 2.5 A and the knee power voltage is set to 8 V, the constant power is 20 W. If the VKP register were set to 12 V, the resultant constant power characteristic above the VKP threshold would be 30 W.

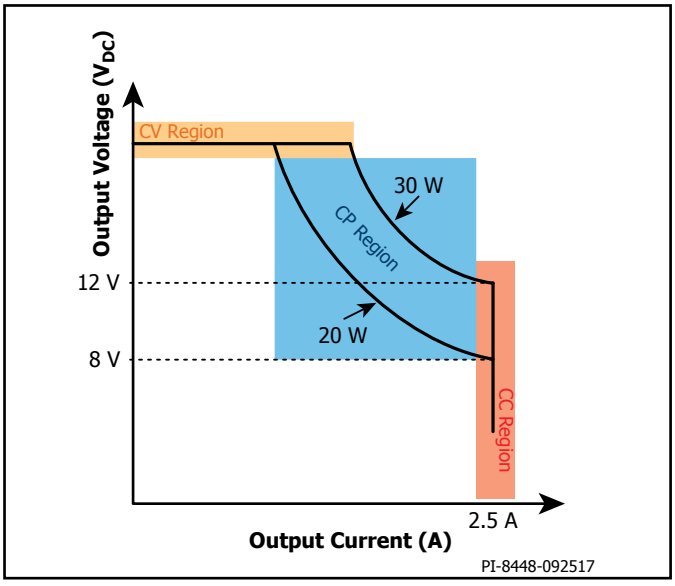


Figure 13. Constant Output Power Profile.

From no-load to heavy loading conditions, InnoSwitch5-Pro will operate in CV then transition into CP then into CC region below the VKP threshold. Setting VKP to maximum value (30 V) results in no Constant Output Power regulation region.

Example: To change VKP from 30 V (d'300) (0xF0 = 0x0170 with odd parity) to 8 V (0x50 = 0x80D0):

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	VKP Register (0x1A)
Low Byte:	0xD0 (8'b1101 0000)
High Byte:	0x80 (8'b1000 0000)

Reducing the constant current regulation threshold does not modify the maximum programmed output power with a given VKP setting. From the example shown above, setting CC regulation to 2 A (full-scale CC is still 2.5 A), with VKP = 8 V, would result in output profile shown below with CP characteristic intercept of 10 V for the same 20 W constant power characteristic.

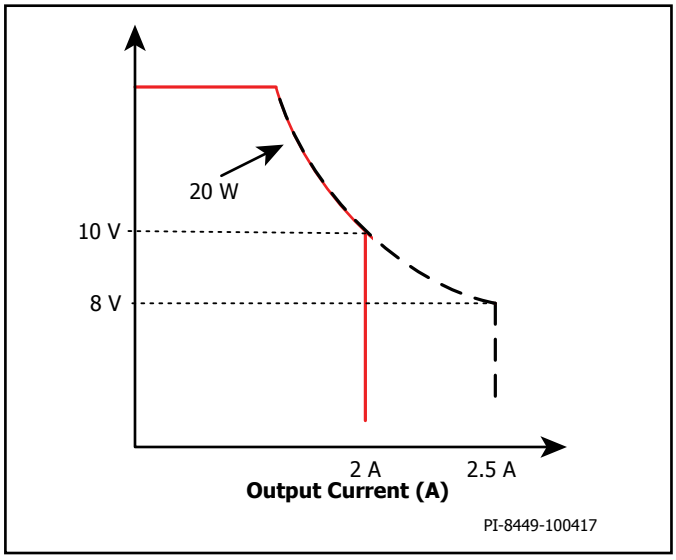


Figure 14. Constant Output Power Profile with Reduced CC Regulation Threshold.

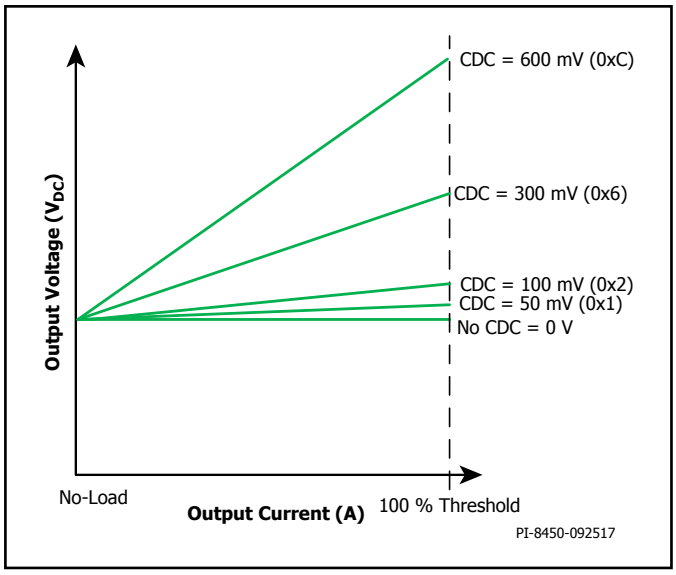


Figure 15. CDC as Function of Load Current.

Cable Drop Compensation (CDC) (0x16)

The amount of cable drop compensation has a controllable range of 0 V to 600 mV in 50 mV/steps. CDC is applied as a function of the current through the sense resistor (resistor between IS and GND pins) used to program the constant current regulation threshold. At no-load there is no CDC and the compensation is increased linearly as load increases and reaches the maximum programmed value at the onset of the 100% constant-current regulation threshold (full-scale voltage across the current sense resistor).

The table below shows the register values to program the desired CDC:

CDC (mV)	Hex Value	Binary
0	0x00	4'b0000
100	0x02	4'b0010
150	0x03	4'b0011
200	0x04	4'b0100
250	0x05	4'b0101
300	0x06	4'b0110
350	0x07	4'b0111
400	0x08	4'b1000
450	0x09	4'b1001
500	0x0A	4'b1010
550	0x0B	4'b1011
600	0x0C	4'b1100

Table 9. Cable Drop Compensation.

If the current sense resistor between IS pin to GND pin is shorted, there will be neither any cable drop compensation nor any constant current regulation.

Example: To change CDC from 0 V to 300 mV (0x06):

PI_SLAVE_ADDRESS [W]:	0x30 (8'b1011 0000)
PI_Command:	CDC Register (0x16)
Byte:	0x06 (4'b0110)

Constant Voltage Only Mode (0x0E)

The InnoSwitch5-Pro can be programmed to operate with constant-voltage only and have no constant current regulation mode. The set output current register (0x98) sets the overload threshold instead of regulating the constant current when the CVO mode is enabled. Once the load current exceeds the programmed current a peak load timer (t_{PLT}) is started. The options for the peak load timer (CVO timer bit [4:3] of Register 0x0E) are 8 ms, 16 ms, 32 ms or 64 ms. If the peak load exceeds the programmed timer, the InnoSwitch5-Pro can be programmed to respond to this fault as disable output, auto-restart, latch-off or no-response through the CVO Register 0x0E bit [2:1]. The default response for peak overload is auto-restart with 8 ms timer.

In case of Disable – Output (DO) response, InnoSwitch5-Pro will open the series bus switch and reset to default configuration when the fault occurs. After reset, InnoSwitch5-Pro might annunciate other faults – example VOUT OV AR depending on the operating condition of the power supply.

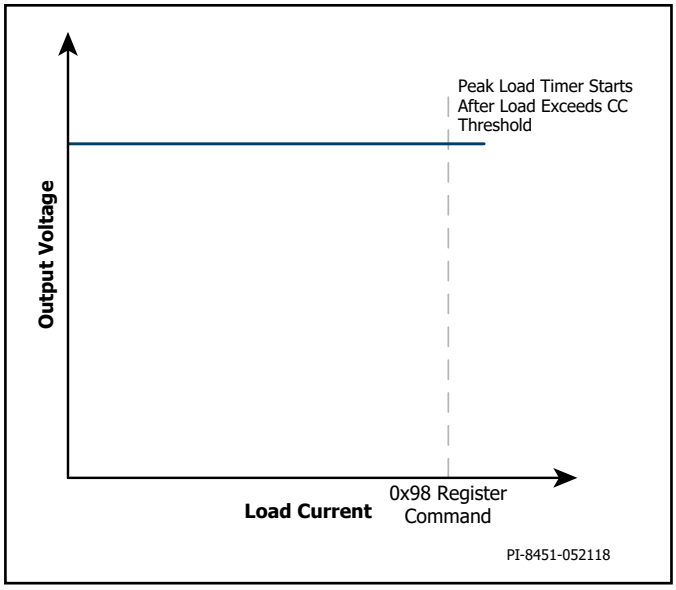


Figure 16. Constant Voltage Only (CVO) Mode.

Example: Enable CVO Mode, set t_{PLT} to 16 ms and fault response to Disable - Output (DO): (0x0F):

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	CVO Register (0x0E)
Byte:	0x0F (8'b0000 1111)

Synchronous Rectifier based Zero Voltage Switching (SR-ZVS)

In Quasi-Resonant (QR) mode of operation of InnoSwitch5-Pro IC, zero voltage switching of the primary switch can be achieved using the secondary SR FET through an I²C command.

With SR-ZVS mode enabled, the secondary controller detects when the power supply enters in discontinuous-mode and turns ON SR FET for the duration programmed in SR-ZVS Register (0x3E, bit [4:0] – SR-ZVS ON-time). During this time magnetizing current is charged in negative direction at the rate determined by the reflected output voltage on the primary. At the end of SR-ZVS ON time, the magnetizing energy will start discharging the drain node capacitance on the primary switch. The duration for this discharge before sending out the secondary cycle request is programmable through SR-ZVS Register (0x3E, bit [7:5] – SR-ZVS Delay time). The minimum delay programmed should allow the SR gate to discharge below the gate threshold voltage before the switching request is sent. If the delay programmed is too short and the SR gate voltage has not discharged sufficiently, secondary will abort the switching request and device will auto-restart to prevent any kind of cross conduction.

Both the SR-ZVS ON-time and SR-ZVS Delay time can be adjusted through I²C commands in steps of ~85 ns depending on the output voltage and load current to achieve highest efficiency at different operating conditions. Refer to Command Register Assignment Table for programmable limits. The timings measured are approximately one to two clock cycle more than the set values in the SR-ZVS Register.

In case of SR-ZVS ON-time, with the minimum programmed value of d'3, the measured value for SRZVS ON-time is ~400 ns whereas for SR-ZVS Delay time, it is ~350 ns.

In order to improve the thermals and reduce switching losses on the SR FET during this ZVS operation, SR FET can be forced to switch when the FW voltage is near its minimum voltage by writing 1'b1 into SR-ZVS register (0x3E, bit [11] – Valley switching).

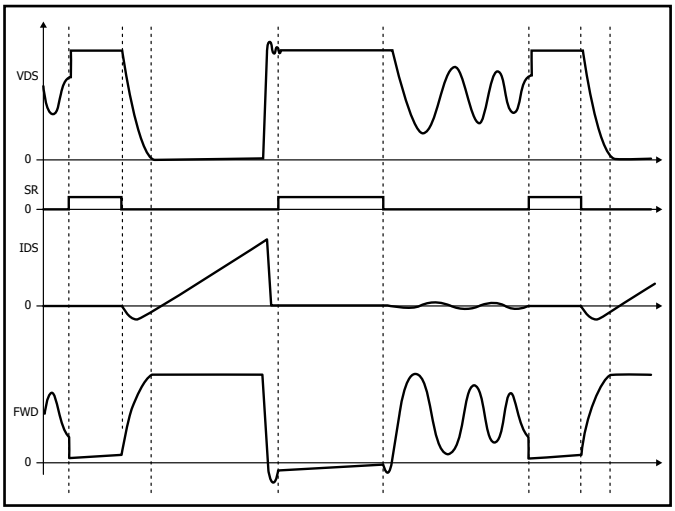


Figure 17. Waveforms for SR-ZVS Mode of Operation.

Example: Enable SR-ZVS mode:

SR-ZVS ON-time = (SRZVS ON count + 1) * 85 ns = (6+1) * 85 ns = ~600ns (bit [4:0] = d'6 or 5'b 00110)

SR-ZVS Delay time = (SRZVS Delay Count + 1) * 85 ns = (3+1) * 85 ns = ~350 ns (bit [7:5] = d'3 or 3'b 011)

SR-ZVS Enable = 1'b1 (bit [10])

Valley Switching Enable = 1'b1 (bit [11])

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	SR-ZVS Register (0x3E)
Low Byte:	0x66 (8'b0110 0110)
High Byte:	0x0C (8'b0000 1100)

During disable of SR-ZVS, valley switching also need to be disabled to have Quasi–Resonant (QR) mode enabled.

Mode of Operation Transition Sequence
While transitioning from Quasi-Resonant (QR) mode of operation to SR-ZVS mode of operation and vice-versa, it is recommended to follow the below sequence.

Quasi-Resonant Mode to SR-ZVS Mode Sequence:

Step 1: Enable SR-ZVS mode without Valley switching enabled.

Example:

*SR-ZVS ON-time = (6+1) * 85 ns = ~600ns (bit [4:0] = d'6)*

*SR-ZVS Delay time = (3+1) * 85 ns = ~350 ns (bit [7:5] = d'3)*

SR-ZVS Enable = 1'b1 (bit [10])

Valley Switching Enable = 1'b0 (bit [11])

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	SR-ZVS Register (0x3E)
Low Byte:	0x66 (8'b0110 0110)
High Byte:	0x04 (8'b0000 0100)

Step 2: Enable Valley switching.

Example:

*SR-ZVS ON-time = (6+1) * 85 ns = ~600ns (bit [4:0] = d'6)*

*SR-ZVS Delay time = (3+1) * 85 ns = ~350 ns (bit [7:5] = d'3)*

SR-ZVS Enable = 1'b1 (bit [10])

Valley Switching Enable = 1'b1 (bit [11])

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	SR-ZVS Register (0x3E)
Low Byte:	0x66 (8'b0110 0110)
High Byte:	0x0C (8'b0000 1100)

SR-ZVS Mode to Quasi-Resonant (QR) Mode Sequence:

Step 1: Disable Valley Switching first.

Example:

*SR-ZVS ON-time = (6+1) * 85 ns = ~600ns (bit [4:0] = d'6)*

*SR-ZVS Delay time = (3+1) * 85 ns = ~350 ns (bit [7:5] = d'3)*

SR-ZVS Enable = 1'b1 (bit [10])

Valley Switching Enable = 1'b0 (bit [11])

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	SR-ZVS Register (0x3E)
Low Byte:	0x66 (8'b0110 0110)
High Byte:	0x04 (8'b0000 0100)

Step 2: Disable SR-ZVS mode with settings provided below.

Example:

SR-ZVS ON-time = bit [4:0] = d'0

SR-ZVS Delay time = bit [7:5] = d'2

SR-ZVS Enable = 1'b0 (bit [10])

Valley Switching Enable = 1'b0 (bit [11])

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	SR-ZVS Register (0x3E)
Low Byte:	0x40 (8'b0100 0000)
High Byte:	0x00 (8'b0000 0000)

With SR-ZVS ON-time of d'0, SR gate drive signal will be observed for minimal ZVS period. The minimum delay programmed should allow the SR gate to discharge below the gate threshold voltage before the switching request is sent.

Programmable Protection Mechanisms

Output Overvoltage and Undervoltage Protection Thresholds/Fault Behavior

Besides the ability of programing the OV/UV thresholds during operation as a function of the set CV, the behavior of the power supply once a fault occurs (a. No-Response which just sets the fault register, b. Latch-off (LO), c. Auto-restart (AR) or d. Disable Output (DO)) and timing for the UV fault detection (8 ms, 16 ms, 32 ms or 64 ms) is programmable as well. In InnoSwitch5-Pro, for UV fault, there is an option to disable the UV timer, in which case the selected timer option will be ignored and the delay is same as the output overvoltage delay fixed at ~80 µs. All faults that are programmed to have no-response will be logged into the telemetry read-back fault register.

In case of Disable – Output (DO) response, InnoSwitch5-Pro will open the series bus switch and reset to default configuration when the fault occurs. After reset, InnoSwitch5-Pro might annunciate other faults – example VOUT OV AR depending on the operating condition of the power supply.

OVA(0x92) : write to this address to specify the overvoltage threshold and fault response to OV fault
UVA(0x94) : write to this address to specify the undervoltage threshold, UV timer and fault response to UV fault

Example: To change the absolute output undervoltage threshold 3 V (d'30), fault response to Disable-Output (DO) and configure fault timer to 64ms: (0xBC9E with odd parity):

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	UVA Register (0x94)
Low Byte:	0x9E (8'b1001 1110)
High Byte:	0xBC (8'b1011 1100)

IS Pin and Output Short-Circuit Fault Protection

The InnoSwitch5-Pro IC can be configured to monitor whether a short-circuit fault occurs across the output current sense resistor or a short-circuit fault across the IS to GND pins.

A fault is annunciated in the event the sensed current through the IS pin does not exceed the programmed current limit threshold (bit [6:4] of ISSC register 0xA2) and switching frequency exceeding the programmed threshold (bit [3:2] of ISSC register 0xA2). The switching frequency can be selected in a range from 30 to 120 kHz. This must be carefully selected to suit the expected operating conditions of the design.

An IS pin short (ISSC) can be programmed to have a response to be a. No-Response, b. Latch-off (LO), c. Auto-restart (AR) or d. Disable Output (DO). In the event the behavior is a No-Response, the Telemetry Read-Back Fault Register is logged.

ISSC (0xA2): write to this address to specify the behavior for an IS-GND short.

Example: To set the behavior of an IS pin short to AR for switching frequency exceeding 30 kHz and current limit threshold of d'48: (0x36):

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	ISSC register (0xA2)
Byte:	0x36 (8'b0011 0110)

The InnoSwitch5-Pro IC sets the CCSC fault register (READ 10 bit 2) once the voltage across the IS pin resistor exceeds more than ~3 times the $I_{SV(TH)}$. The CCSC register can be programmed to have response of a. No-Response, b. Latch-off (LO), or c. Auto-restart (AR). In applications where the output capacitance after the series bus-switch exceeds 100 µF, the response for CCSC should be set to No-Response for proper start-up and may be programmed back to other fault response during normal operation after the series bus-switch is closed.

CCSC (0x20): write to this address to specify the behavior for an output short-circuit.

Example: Set behavior of output short-circuit to No-response:

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	CCSC Register (0x20)
Byte:	0x00 (2'b00)

Setting CCSC register to No-Response and creating a short-circuit condition at output will result in Auto-Restart if switching frequency is $>f_{OVL}$ parameter for longer than t_{AR}.

Series Bus Switch Short-Circuit Fault Protection

Series bus switch short-circuit fault is set in the event when sensed current through IS pin exceeds the programmed threshold (bit [5:4] of VBUSSC register 0xB6) and VBEN is disabled. There is option to program the number of current samples (1, 2, 3 or 4 consecutive samples) exceeding the set threshold before annunciating the fault.

A VBUS switch short (VBUSSC) can be programmed to have a response to be a. No-Response, b. Latch-off (LO) or c. Auto-restart (AR). In the event the behavior is a No-Response, the Telemetry Read-Back Fault Register is logged.

VBUSSC fault once triggered can be cleared with secondary giving up control or by sending the VBEN enable command. Writing into interrupt mask will not clear the fault

Watchdog Timer (0x26)

The Watchdog timer supervises the communication on the I^2C command lines and has an adjustable time-out. The InnoSwitch5-Pro IC will go into a reset state if I^2C commands are not received within the programmable time interval. The watchdog timer does not engage until the master issues the first I^2C command (Read or Write). In the reset state the following occurs:

1. VBUS switch is Disabled (Series switch is open).
2. VOUT pin voltage regulates at the default 5 V threshold.
3. All command registers are cleared.

By writing 0x00 into register 0x26, the Watchdog timer is disabled. Disabling this feature can be useful in initial software debugging or checking functionality of the device on the bench.

Example: To disable the Watchdog timer:

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	Watchdog Timer Register (0x26)
Byte:	0x00 (2'b00)

Opening and Closing the Series VBUS Switch (0x04)

Enabling VBEN (closing the VBUS series switch) speeds up the ADC sampling frequency in order to achieve high control accuracy. Write commands to CV register (0x10) and CC register (0x98) cannot be accepted faster than 80 ms when the VBEN is disabled (Series VBUS switch open).

Write 0x03 (with odd parity this becomes 0x83) into the VBEN register (0x04) to close the series VBUS switch and write 0x00 (with odd parity this becomes 0x80) to this register to open the switch. When the VBUS switch is open (VBEN disabled), the system is reset to the default output voltage set point of 5 V. Disabling the series VBUS switch also resets all the programmable command registers to their default values. The InnoSwitch5-Pro controller is in a state of reset when VBEN is disabled or the VDIS register is enabled.

For both these commands, since the controller is in reset, an ACK or NACK at the end of the command should not be expected.

InnoSwitch5-Pro IC also includes the option of bus switch open and no system reset. Write 0x01 (with odd parity 0x01) into the VBEN register (0x04) to open the switch without system reset. In this case, series bus switch is opened and the output voltage before the switch remains as configured previously in the CV register. All the programmable command registers do not reset to default values, instead retain the previous programmed configuration.

Enabling the VBEN register automatically disables the VDIS register (0x08) described in Active VOUT Pin Bleeder and Output Load Discharge Functions section.

Example: Enabling (Closing) the Series VBUS switch (0x83):

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	VBEN Register (0x04)
Byte:	0x83 (8'b1000 0011)

Prior to sending command to open the series bus switch with system reset (0x00), a command to set the output voltage (CV register 0x10) to 5 V is recommended. In the event of an auto-restart or latch-off, the bus switch is not disabled. In the event of disable-output, the bus switch is disabled and system is reset to default configuration. The VBEN command must be sent to enable the series bus switch (close the switch) prior to increasing the output voltage above 16 V.

Turn-Off the Power Supply (0x8A)

The I²C master has the ability to turn-off the power supply (through an I²C command), which will require AC power cycling to restart the power supply.

Example: Turn-off the power supply:

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	Turn-Off PSU Register (0x8A)
Byte:	0x01 (1'b1)

Fast VI Command

By default, the maximum speed in which CV (0x10) and CC (0x98) commands can be sent to program output voltage/current respectively is 10 ms. However, the speed limit can be removed by setting 0x1 to the Fast VI Command Register (0x8C).

Example: To disable speed limit for V/I commands:

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	Fast VI Speed Register (0x8C)
Byte:	0x01 (1'b1)

Output Load Discharge Functions

The InnoSwitch5-Pro IC can discharge the VBUS output voltage by bringing the VB/D pin to ground. The discharge circuit is a series diode + resistor tied from the VBUS output to the VB/D pin shown in the typical application schematic. The resistor selected should limit the current into VB/D pin within the max current limit specified in the electrical specifications.

Load discharge function can be activated by writing 0x03 (0x83 with odd parity) into VDIS register (0x08). Enabling the VDIS register will automatically disable the VBEN register (0x04) and reset the device to the default state.

The I²C master can use telemetry to monitor the VOUT pin voltage or a fixed timer to help determine when to disable this function.

In circumstances where device reset is not desirable, load discharge function can be activated without reset by writing 0x02 into VDIS register (0x08). This command will enable load discharge without device reset.

Example: Activate the Vout Bleeder:

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	BLEEDER Register (0x86)
Byte:	0x01 (8'b0000 0001)

Example: Discharge the VBUS Output:

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	VDIS Register (0x08)
Byte:	0x83 (8'b1000 0011)

Active VOUT Pin Bleeder with Auto Disable Control for Reducing I²C Traffic

There may be circumstances where the VOUT pin strong bleeder function must be activated to discharge the output voltage from a high to low regulation set point. The InnoSwitch5-Pro IC includes an option of Enable BLEEDER with Auto Disable feature. Writing 0x03 into the BLEEDER register (0x86) will enable the bleeder function with auto disable feature. The bleeder is automatically disabled when the VOUT10PCT or VOUT4PCT register is cleared. This selection is programmable through bit [2] of the BLEEDER command. The VOUT10PCT register is set once the output voltage is above 10% of the target regulation voltage. The VOUT4PCT register is set once the output voltage is above 4% of the target regulation voltage. Weak bleeder should be enabled 0x86=0xDx before exercising the auto bleeder control commands. During output voltage decrement process, it is recommended to have ~1 ms delay between the CV command and enabling the strong bleeder with auto disable feature.

The BLEEDER register must not be enabled for extended period of time to prevent excessive power dissipation in the controller.

The InnoSwitch5-Pro IC automatically disables SR pin when strong bleeder is enabled as the switching is not expected when bleeder is used to reduce the output voltage.

Transient Response

If faster transient response is required in the application the InnoSwitch5-Pro IC includes command registers to reduce the time for low to high output voltage transitions. The command register addresses and recommended settings are shown in the table below:

Command Register Address	Default		Recommended for Speed Up	
	MSB	LSB	MSB	LSB
0x32	0x28	0x1E	0x14	0x0A
0x34	0x18	0xC8	0x1F	0x84

Using values other than the default or recommended settings about could lead to oscillatory behavior.

Constant Voltage Load

The constant current regulation mode in the InnoSwitch5-Pro can be optimized for constant voltage (CV) type load if this is required by the end application. Enabling this command register reduces the output current ripple for CV load only. The command register and setting below should only be used if CV load must be supported.

Command Register		Default		Recommended for CV Lod	
Address	Address with Odd Parity	MSB	LSB	MSB	LSB
0x30	0xB0	0x00	0x1F	0x0A	0x20

DCM-Only

The InnoSwitch5-Pro IC includes a feature to limit the switching cycle requests from secondary to primary such that converter always operates in the Discontinuous Conduction Mode (DCM).

At high line, when a step load occurs, it would normally introduce one or more CCM cycles and raise the peak FWD pin voltage. Enabling the DCM-only feature will limit this peak voltage and thereby reduce the stress on SR FET.

DCM-only feature can be enabled/disabled through I^2C command. Writing 0x04 into DCM-only register (0xBA) will enable this feature.

Example: Enable DCM-only mode:

PI_SLAVE_ADDRESS [W]: 0x30 (8'b0011 0000)
PI_Command: DCM-only Register (0xBA)
Byte: 0x04 (8'b0000 0100)

Telemetry (Read-Back) Registers
Telemetry read registers (READ1 to READ7) show the content of all the command registers in Table 3. Telemetry read register addresses are grouped to allow optimal polling to get the power supply status in single I²C read back command with start and end telemetry addresses of interest.

Fault Registers
All the command registers including set voltage, set current, constant-power knee voltage, control (Series VBUS switch, VOUT pin Bleeder, Load discharge etc.) and all fault status can be read-back using the Telemetry functionality of the InnoSwitch5-Pro through I²C.

The READ10 telemetry registers are instantaneous and are cleared whenever the condition is no longer valid.

The READ15 (0x1E) and READ16 (0x20) Register contains fault register data for auto-restart, latch-off and disable output. This register is only cleared when the BPS pin falls below its undervoltage threshold.

Example: Read the Fault Telemetry Register to determine an auto-restart occurred due to an output undervoltage (UV) Fault:

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
Read Register:	0x80
Telemetry Register:	0x20
PI_SLAVE_ADDRESS [r]:	0x31 (8'b0011 0001)
PI_Slave Response:	Low Byte 8'b0000 0000 (0x00)
	High Byte 8'b0000 0010 (0x02)

Operating Mode Flag (OMF)
The InnoSwitch5-Pro IC reports the mode of operation in telemetry register READ11 (0x16). It reports the InnoSwitch5-Pro IC is operating in CV, CP or CC mode. If interrupt mask is enabled, interrupt is raised whenever operating mode changes between CV, CP and CC modes. The OMF status of the supply should be read when in steady-state operation.

Main Regulation DAC Input
The READ14 telemetry register is the input into the main regulation loop that controls constant voltage, constant current and constant output power regulation. If this register is the same as the Set CV Register (0x10) the converter is operating in constant-voltage mode. If the READ14 is less than the Set CV Register (0x10) the converter is operating in constant-current (CC) or constant-power (CP) mode depending on the value of the Constant Power Knee Voltage Register (0x1A).

The output voltage from the READ14 register is computed as:

$$V_{OUT} = 5\ V + (MSB \times 100\ mV) - (LSB \times 10\ mV).$$

Example: READ14 (0x1C): MSB = 0x00, LSB = 0x0E
LSB is d'14 so the computed $V_{OUT} = 5 - (14 \times 10\ mV) = 4.86\ V$

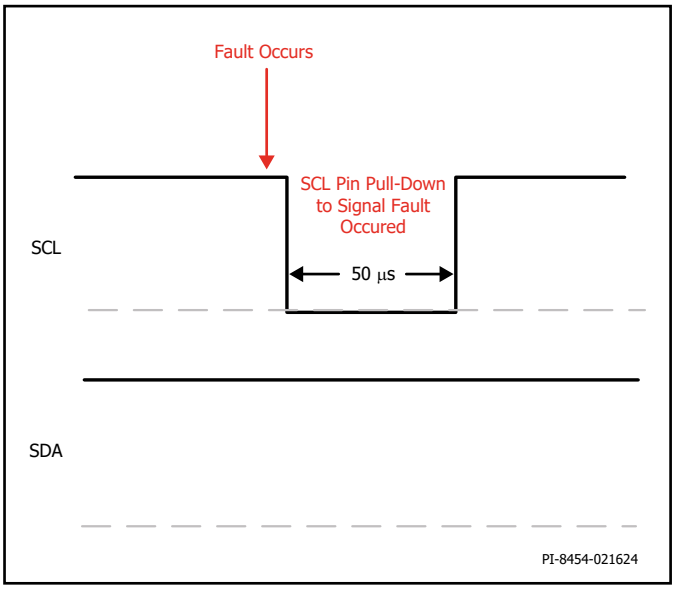


Figure 18. Interrupt Mask During Idle I²C.

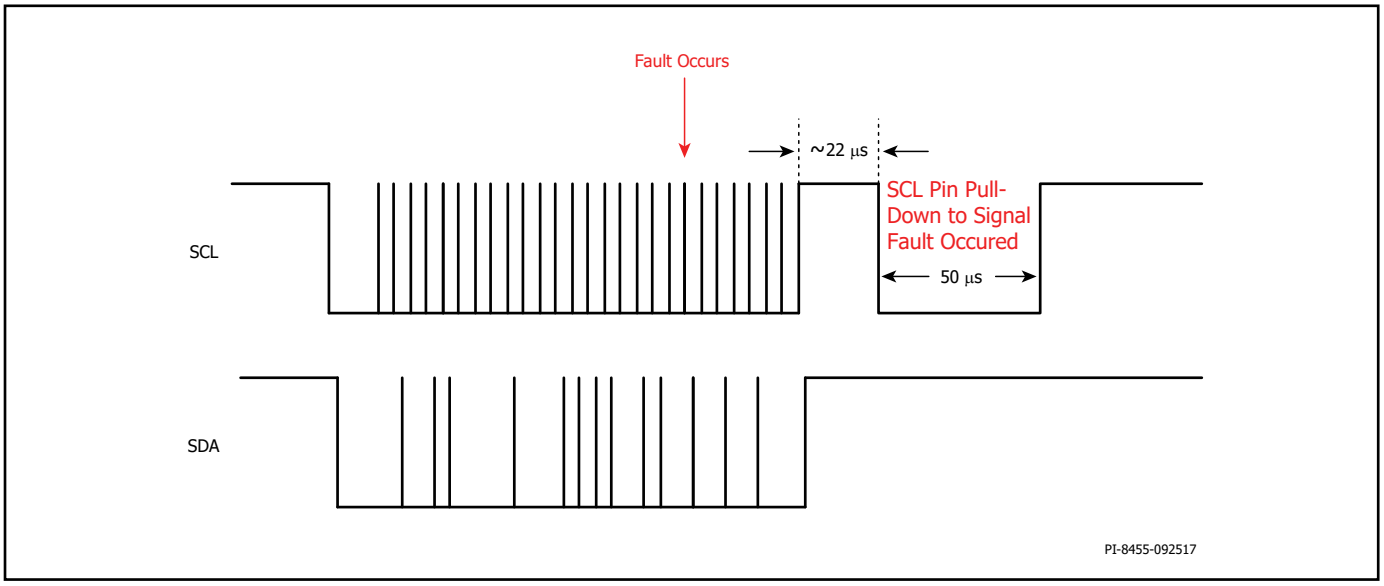


Figure 19. Interrupt Mask During Active I²C Transaction.

Fault Signaling Interrupt Through SCL Pin
In order to improve the fault reporting, an active interrupt reporting scheme is featured on the SCL pin during I²C idle state (when both SDA and SCL pins are pulled high).

When a fault occurs, the SCL pin will behave in one of the following two conditions:

1. When the SCL pin is in idle mode (see Figure 15), the fault interrupt will happen as soon as the fault is detected. The interrupt pulls down the SCL pin for 50 µs then releases it back to HI State.
2. When the SCL pin is busy (active I²C transaction) (see Figure 16), the fault interrupt will wait for the I²C transaction to be completed, wait ~22 µs and then pull down the SCL line for 50 µs (minimum) then releases it back to HI State.

The Interrupt Mask Write Register (0x2C) must be enabled for each of the individual fault conditions. See Figure 19. In order to activate this feature. Once a fault occurs, the Interrupt is reset and the particular faults of interest must be re-enabled to activate the SCL reporting scheme.

The Interrupt Mask read register (0x22) will not be auto cleared when the interrupt triggers and will only reset when the Interrupt Mask write register is re-enabled. The Control Secondary Interrupt bit [6] is an indication that the secondary controller is waiting to handshake with primary. Several system faults could trigger this event such as primary-side thermal shutdown or an input line under or overvoltage condition.

Note 1: Any fault response configured as a No Response and Interrupt Mask enabled will result in an interrupt signal on the SCL pin.

Note 2: Any fault response configured as a Disabled Output and Interrupt Mask enabled results in a system reset when the fault is annunciated and the status of Interrupt signal on the SCL pin is ambivalent. It is recommended not to enable the Interrupt Mask for the faults that are configured to Disable Output response.

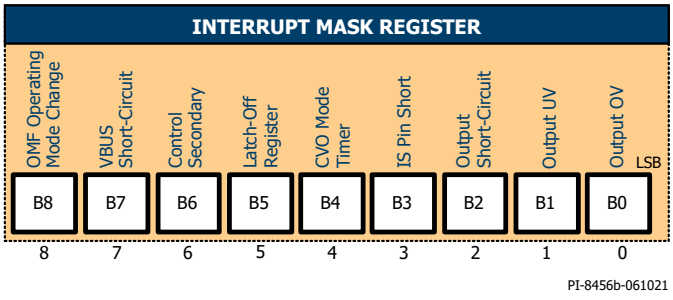


Figure 20. Interrupt Mask Register.

Example: Set the Interrupt Write Register to flag SCL pin fault for output OV, UV or short-circuit only:

PI_SLAVE_ADDRESS [W]:	0x30 (8'b0011 0000)
PI_Command:	INTM Register (0x2C)
Byte:	0x07 (8'b0000 0111)

Output Voltage Measurement
The voltage on the VOUT pin is available on the Telemetry Register READ9 (0x12). The tolerance of this telemetry register is ±3% over the entire regulation range of 3 to 30 V. When the output voltage is below 5 V at loads below ~50 mA, the voltage may fluctuate due to very low switching frequency of the converter but within the specified tolerance. This is normal and expected behavior.

The output voltage report back is in 12-bit format, but the resolution depends on the output voltage range as shown in Table 10. This telemetry register is for indication only, in steady-state operation the VOUT pin is very tightly regulated per the CV Write Register (0x10) discussed in CV Register (0x10) section.

The report back resolution step size depending on output voltage is tabulated below:

Output Voltage Range (V)		Resolution Step Size
3	4	20 mV
4	8	40 mV
8	16	80 mV
16	32	160 mV

Table 10. Output Voltage Report Back Resolution.

Example: If the READ 9 read-back register value is 0xA801 recalling that low byte precedes the high byte, the proper hex to decimal conversion would be from 0x01A8 = 424 in decimal.

The full output voltage range the report back should be multiplied by 10 mV to convert into actual output voltage, which in this example results in an output voltage of 4.24 V.

Read-back of the output voltage set-point READ1 (0x02) as with all the read registers is formatted with low-byte preceding the high-byte.

Output Current Measurement

The load output current is also available on the Telemetry Register.

Telemetry Register READ8 (0x10) contains the instantaneous measured relative output load current data. The load current is available on a relative basis with respect to the full-scale constant current regulation threshold programmed by the sense resistor tied between the IS and GND pin of the InnoSwitch5-Pro.

The ADC full range is 192, which denotes 100% threshold across the current sense resistor.

Example: If a 10 mΩ sense resistor is used and the read-back register is 0x8040.

Removing the odd parity bit from high byte results in 0x40 = 64 in decimal.

Sense current value = N(Decimal) x 0.167/R_{SENSE}
64 x 0.167/10 = 1.068 A. This is the measured output current value:

(0.167 mV = 32 mV/192, where 32 mV = $I_{SV(TH)}$ and 192 is ADC full range).

The READ12 and READ13 are 16 sample rolling averages of the measured output current and output voltage respectively. The value of these average registers is more stable than the instantaneous registers (READ8 and READ9) but take slightly longer to stabilize.

When the series BUS switch is opened these registers are cleared and values are reset to zero until the measurement start to accumulate. The resolution of READ 12 and READ 13 is the same as the READ8 and READ 9 respectively.

The output voltage and current measurement registers are updated every 100 µs.

Input Line Voltage Measurement

The InnoSwitch5-Pro IC reports the primary switch conduction time and the secondary switch (synchronous rectifier) conduction time which could be used in the volt-second balance equation to estimate the line input voltage. Primary switch conduction time referred to as TON is reported in READ21 (0x2A) and Secondary switch (SR) conduction time referred to as TOFF is reported in READ22 (0x2C).

The telemetry is updated only when the Line Sense Enable command is sent by writing 0x01 into command register 0x1C. After the command is sent, the InnoSwitch5-Pro IC updates the TON and TOFF telemetry with 16 sample accumulated value and the Line Sense Reporting Ready flag is set in READ10 register bit [12]. To extract the average TON and TOFF, these values should be divided by 16. To optimize the power consumption, the telemetry of TON and TOFF is updated only when the Line Sense Enable command is sent.

Example: Read the TON and TOFF telemetry:

Line Sense Enable Command
PI_SLAVE_ADDRESS [W]: 0x30 (8'b0011 0000)
PI_Command: Line Sense Register (0x1C)
Byte: 0x01 (8'b0000 0001)

Read Line Sense Reporting Ready Flag
PI_SLAVE_ADDRESS [W]: 0x30 (8'b0011 0000)
Read Register: 0x80
Telemetry Register: 0x14
PI_SLAVE_ADDRESS [r]: 0x31 (8'b0011 0001)
PI_Slave Response: Low Byte 8'b0000 0000 (0x00)
High Byte 8'b0101 0000 (0x50)

Read TON and TOFF telemetry registers
PI_SLAVE_ADDRESS [W]: 0x30 (8'b0011 0000)
Read Register: 0x80
Telemetry Register: 0x2A
PI_SLAVE_ADDRESS [r]: 0x31 (8'b0011 0001)
PI_Slave Response: Low Byte 8'b0010 1110 (0x2E)
High Byte 8'b0000 0110 (0x06)

PI_SLAVE_ADDRESS [W]: 0x30 (8'b0011 0000)
Read Register: 0x80
Telemetry Register: 0x2C
PI_SLAVE_ADDRESS [r]: 0x31 (8'b0011 0001)
PI_Slave Response: Low Byte 8'b1111 0010 (0xF2)
High Byte 8'b0000 0011 (0x03)

Equation to convert TON and TOFF to estimate line input voltage:

$$VIN = \frac{N_P}{N_S} \times (VOUT + V_{DS(SR)}) \times \frac{TOFF}{TON}$$

Example: At 100 V input and 30 V output, using TON, TOFF and average VOUT telemetry reported to estimate the input line voltage

Method 1: Directly using the 16-sample accumulated values (more accurate)

N_P = 25 T; N_S = 5 T

Average VOUT, READ13 (0x1A) = h'0x0B9C or d'2972 (29.72 Volts)
16 sample accumulated TON count, READ21 = h'0x062E or d'1582
16 sample accumulated TOFF count, READ22 = h'0x03F2 or d'1010

$$VIN = \frac{25}{5} \times 30\ V \times \frac{1010}{1518} = 99.8\ V$$

Note: For TON count telemetry value, 4×16 = d'64 needs to be subtracted to account for the delays in the system

Method 2: By converting the reported count values into time.

Convert hex to decimal format:

READ21: 0x062E (hex) to d'1582 (decimal)

*TON_{AVG} = 1582/16 * 85 ns = 8.4 µS*

READ22: 0x03F2 (hex) to d'1010 (decimal)

*$TOFF_{AVG}$ = 1010/16 * 85 ns = 5.36 µS*

Note: TON_{AVG} includes extra delay of 250 ~350 ns which needs to be subtracted to account for the delays in the system.

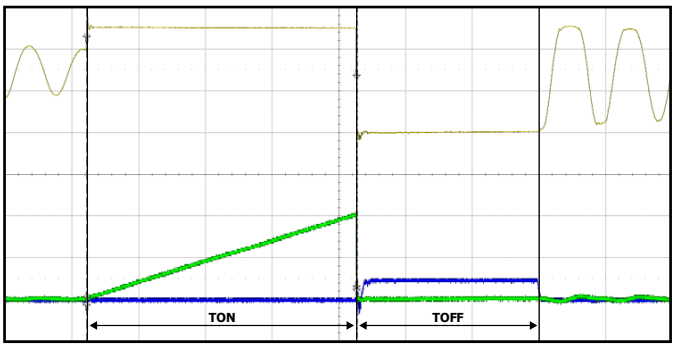


Figure 21. Measurement of TON Time and TOFF Time.

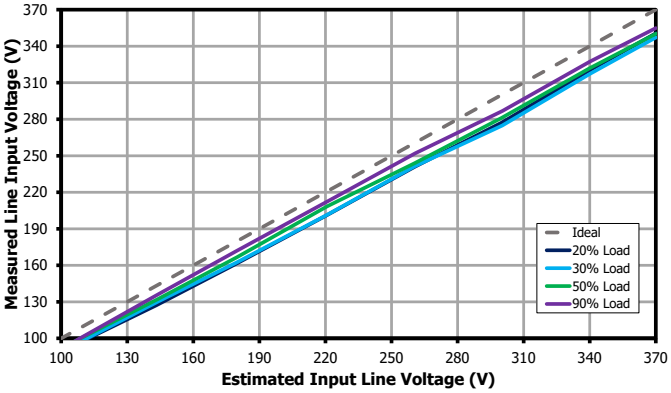


Figure 22. Accuracy of Input Line Voltage Measurement.

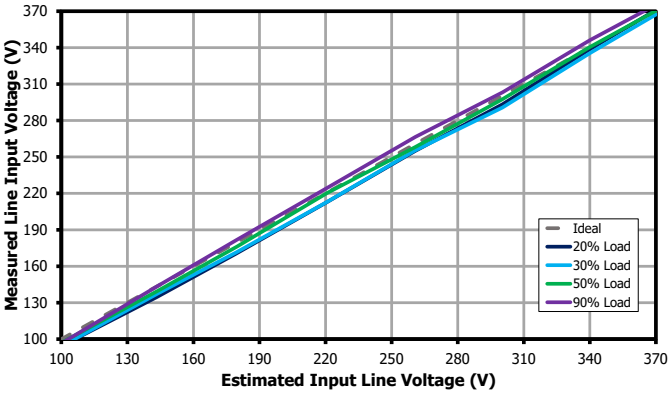


Figure 23. Accuracy of Input Line Voltage Measurement Centered.

The accuracy of the line sense feature requires regular switching pattern with complete SR conduction period. It also depends on how accurately the volt-second balance equation is modeled. At light load, with irregular switching pattern and ON/OFF time approaching minimum conduction time, the accuracy of line sense feature will be compromised. If SR is disabled, this feature cannot be used.

If the SR conduction period is short, then the accuracy will be compromised if the TOFF telemetry is directly used in calculations without compensating for the short SR conduction. For such cases, it is recommended to characterize the design across different operating conditions and include the additional time into TOFF parameter before estimating the line input voltage. This accuracy can be further improved by centering the curves around the ideal line with a correction factor in the firmware.

In the case of SRZVS mode of operation, before exercising the Line Sense Enable command, the SRZVS operation needs to be optimized i.e., the SRZVS ON time and SRZVS delay time need to be set to have optimal ZVS. Excessive SRZVS ON times and delay times lead to inaccuracies in the volt-second balance equation used here for input line voltage estimation. The volt-second balance equation used for QR mode of operation is still valid for SRZVS mode of operation.

Example: At 200 V input and 30 V output, using TON, TOFF and average VOUT telemetry reported to estimate the input line voltage

Method 1: Directly using the 16-sample accumulated value (more accurate)

N_P = 25 T; N_S = 5 T

Average VOUT, READ13 (0x1A) = h'0x0B9A or d'2970 (29.70 Volts)

16 sample accumulated TON count, READ21 = h'0x03A3 or d'931

16 sample accumulated TOFF count, READ22 = h'0x0465 or d'1125

$$VIN = \frac{N_P}{N_S} \times (VOUT + V_{DS(SR)}) \times \frac{TOFF}{TON}$$

$$VIN = \frac{25}{5} \times 30\ V \times \frac{1125}{867} = 194.64\ V$$

Note: For TON count telemetry value, 4 × 16 = d'64 is subtracted to account for the delays in the system.

End of Line Calibration

To enhance the output current tolerance performance, InnoSwitch5-Pro provides End of Line Calibration feature where the variation in the device offset can be independently canceled for each device in the application. InnoSwitch5-Pro provides telemetry of the offset measured during test in READ23 register. This offset can be added or subtracted to the code sent to CC register (0x18) that sets the constant current regulation threshold.

Example: If READ23 telemetry data is 0x0004. The least significant 4 bits are 4'b0100.

End of line calibration telemetry = 4'b0100 (binary) or d'4 (decimal)

Constant Current Regulation Offset bit [2:0] = 3'b100 or d'4 (decimal)

Offset sign bit [3] = 1'b0, implies positive

CC Regulation Code (0x18)
= CC CODE With Zero Offset + End of Line Calibration

If the CC regulation code for 2A is d'64 (calibrated using device with end of line calibration offset = 0), the CC regulation code for this part will be d'64 + d'4 = d'68 to have the same CC performance as the part with '0' offset and tolerance due to part-to-part variation is completely canceled.

Procedure would be to calibrate and derive the CC regulation codes with zero offset part on the application design and then add or subtract the device offset using the end of line calibration telemetry. If the sign bit is positive, add the offset to the CC regulation codes. If the sign bit is negative, subtract the offset from the CC regulation codes.

I²C Connection

uVCC External Power Supply

The uVCC pin provides an accurately regulated 3.6 V supply to an external controller. The maximum load current capability of this supply is 40 mA for 0.5 seconds when the VOUT pin is greater than or equal to 5 V. For steady-state operation, it is expected the current drawn from uVCC is less than 10 mA. The uVCC pin should be decoupled to the GND pin with at least a 2.2 µF ceramic capacitor. When the VOUT pin voltage is less than 3.9 V, the internal LDO will droop and follow VOUT pin voltage. Under these conditions, the uVCC pin voltage is dependent on load current and internal series impedance. At VOUT pin = 3 V and 6 mA load current on R_{uVCC}, the expected output on uVCC will be 3 V – R_{UVCC} (Ω) × 6 mA.

If the VOUT pin voltage falls sufficiently to cause the uVCC pin to go below the $uVCC_{RST}$ threshold, communication through I²C is no longer available.

SCL/SDA Pull-Up Requirements

The SCL and SDA-pins should be pulled-up to the uVCC pin with a resistor. The maximum pull-up resistance is dependent on the capacitance of the SCL/SDA pins and I²C Master. The resultant voltage fall-time to the V_{IL} threshold assuming a total capacitance of 20 pF is tabulated as function of SCL clock frequency in the table below.

The InnoSwitch5-Pro IC can be used with I²C frequency above 535 kHz, however there are specific timing requirements that need to be met as described in the data sheet parameter table and associated notes below the table. Meeting these requirements at frequencies above 535 kHz may require the interface IC to have the ability to produce asymmetrical I²C CLK signals. If such ability is not available in the interface IC (or micro-controller connected to the InnoSwitch5-Pro IC through the I²C bus), it is recommended that I²C frequency of 535 kHz or lower is used.

Max Frequency (kHz)	Max Pull-Up Resistance (kΩ)	t_F (ns)
400	13	300
500	10	240
600	8	200
700	7	178

Table 11. I²C Pull-Up Resistor Values.

I²C Example Waveforms

Setting The Output Voltage To 8 V

Same as Example shown in Figure 10.

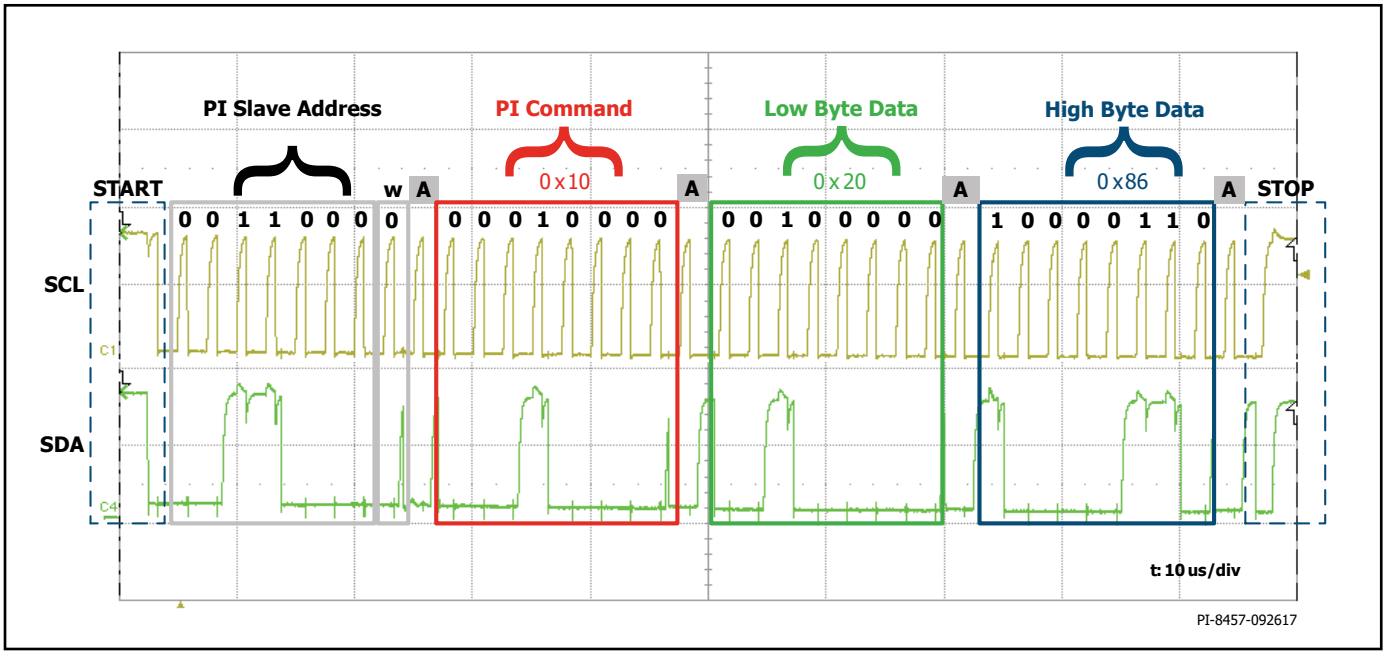


Figure 24. I²C Waveforms for Setting Output Voltage to 8 V.

Reading Telemetry Fault Register After AR Event Caused by Undervoltage

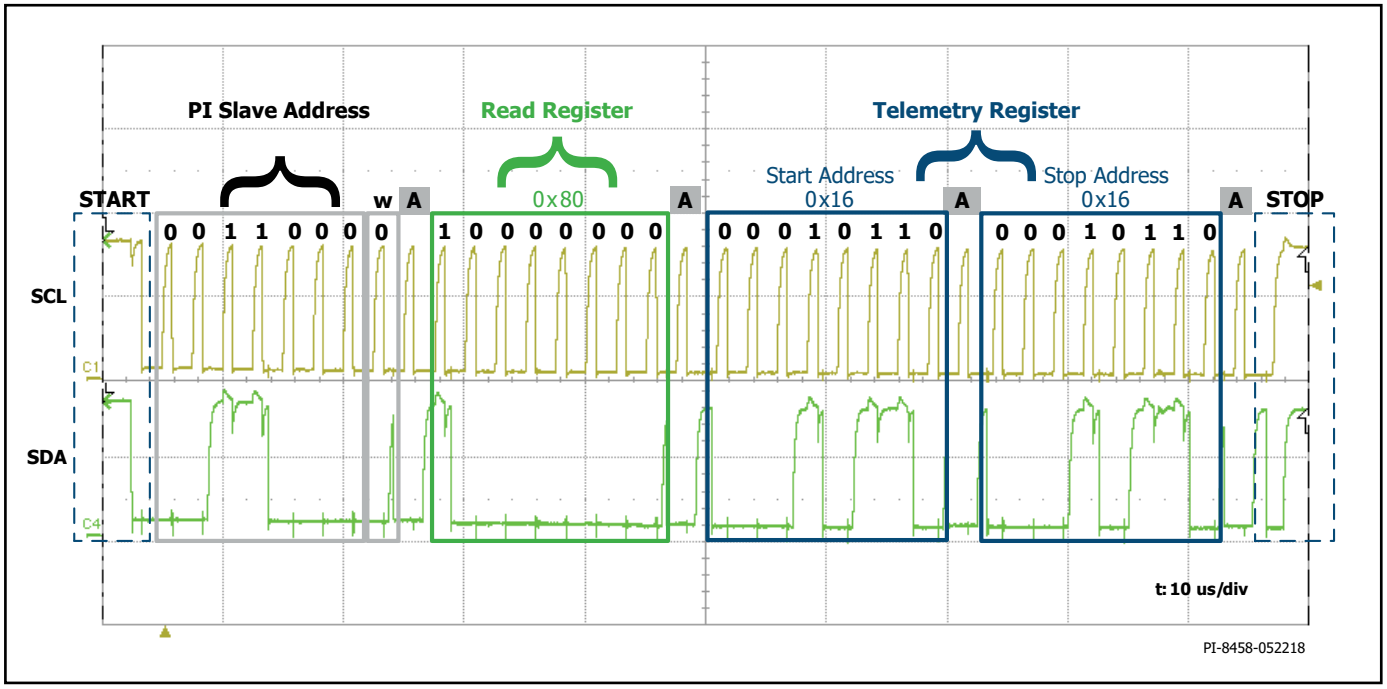


Figure 25. I²C Waveforms for Writing Address of Fault Register READ11 in Read Register (READ0) in Order to Read Back READ11.

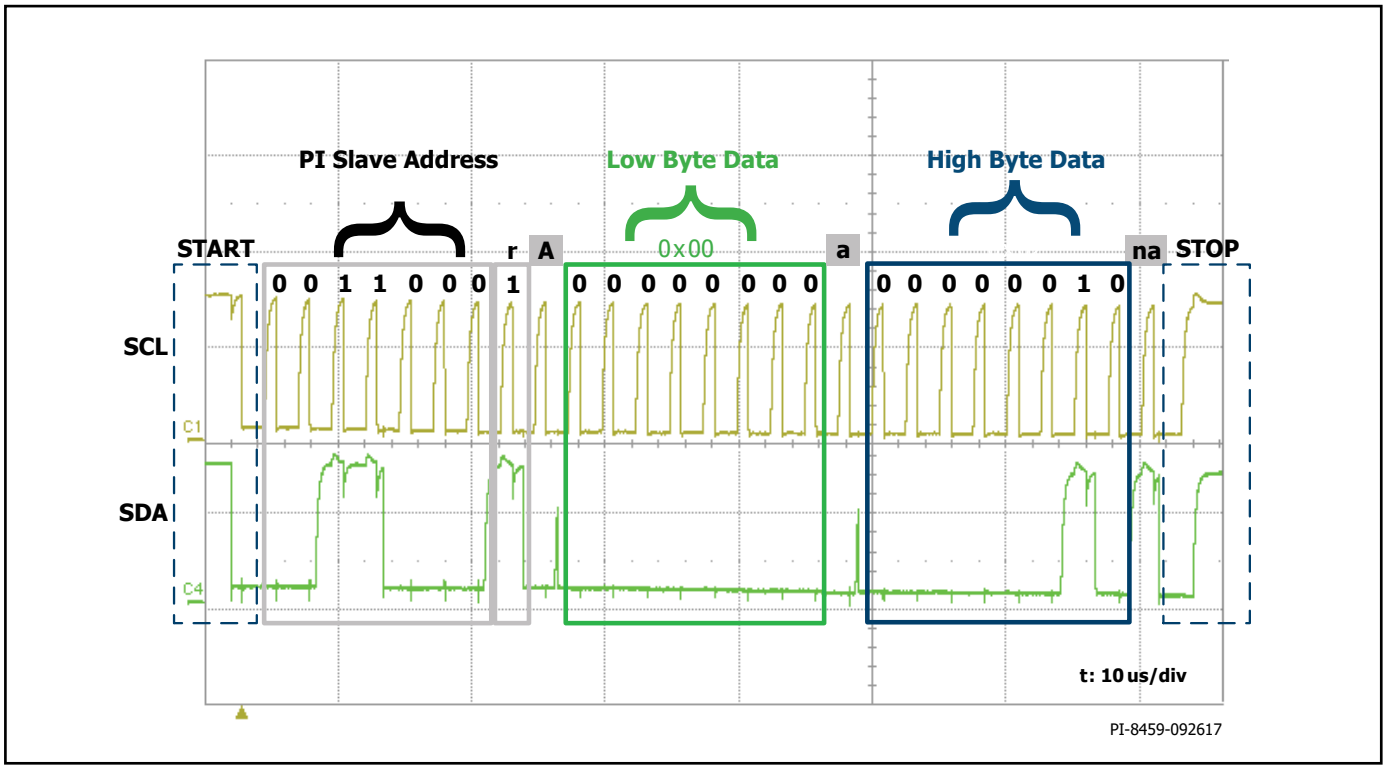
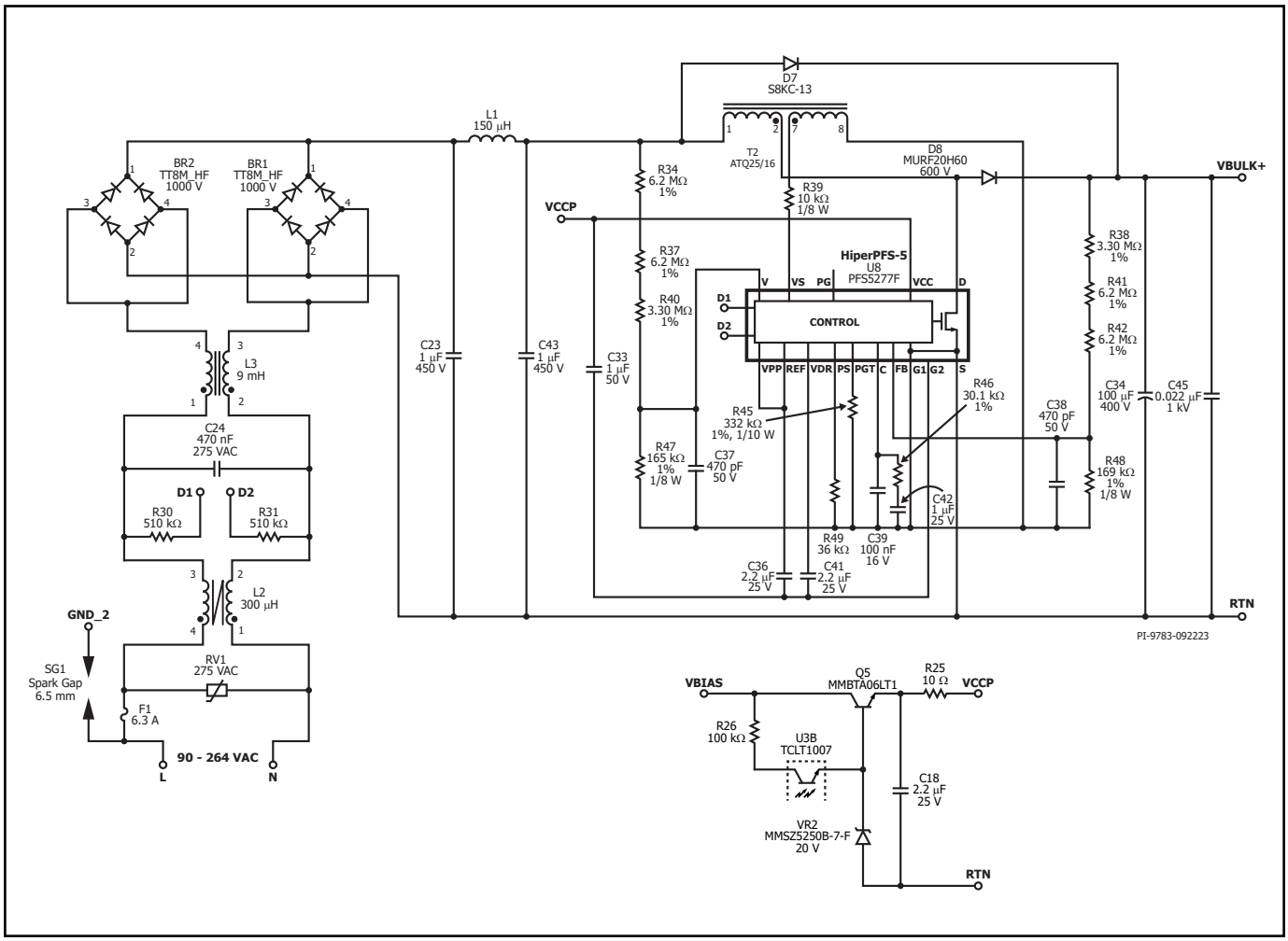
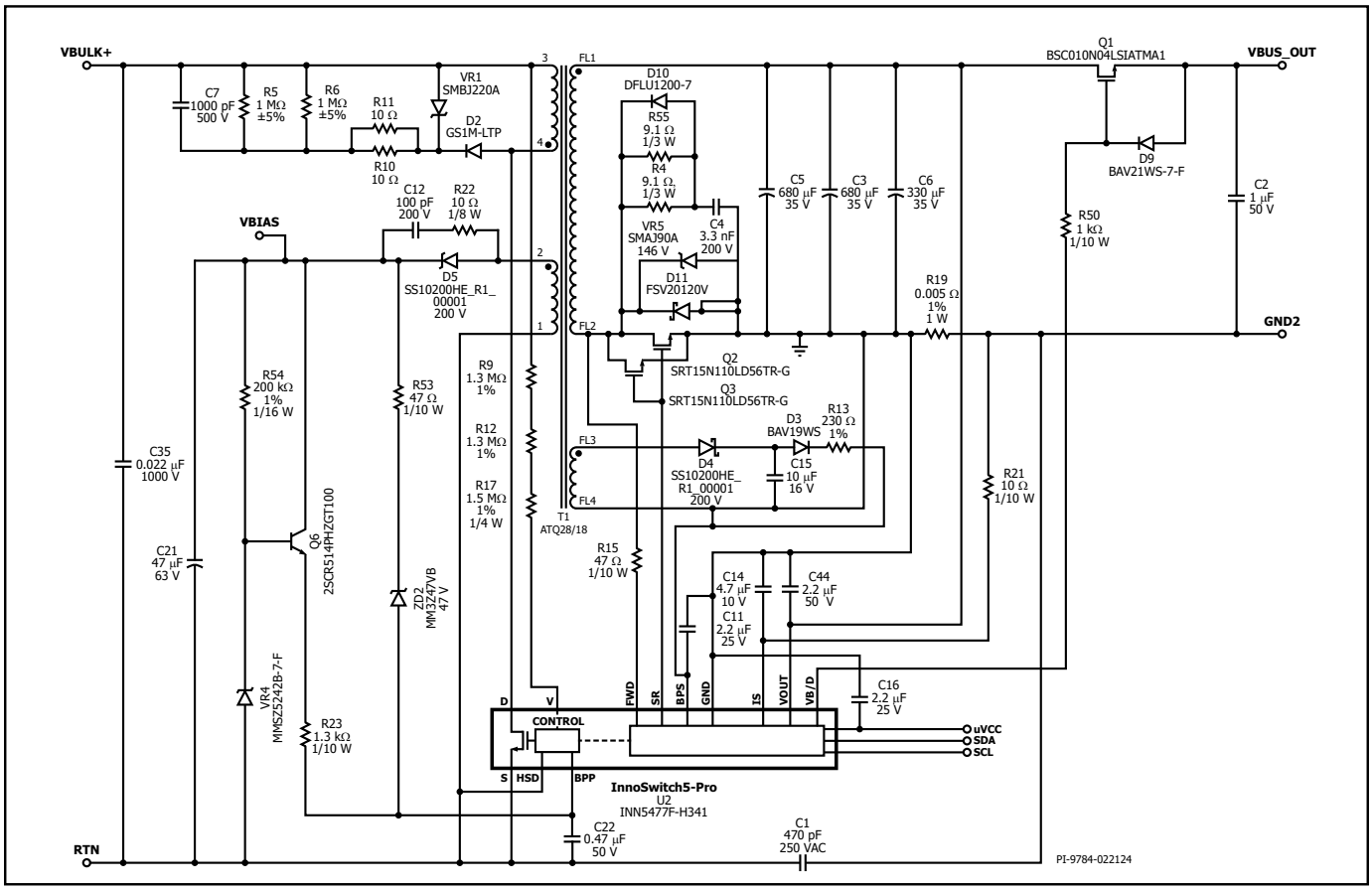


Figure 26. I²C Waveforms for Read Value From READ11 Register.

Applications Example



Flyback Section



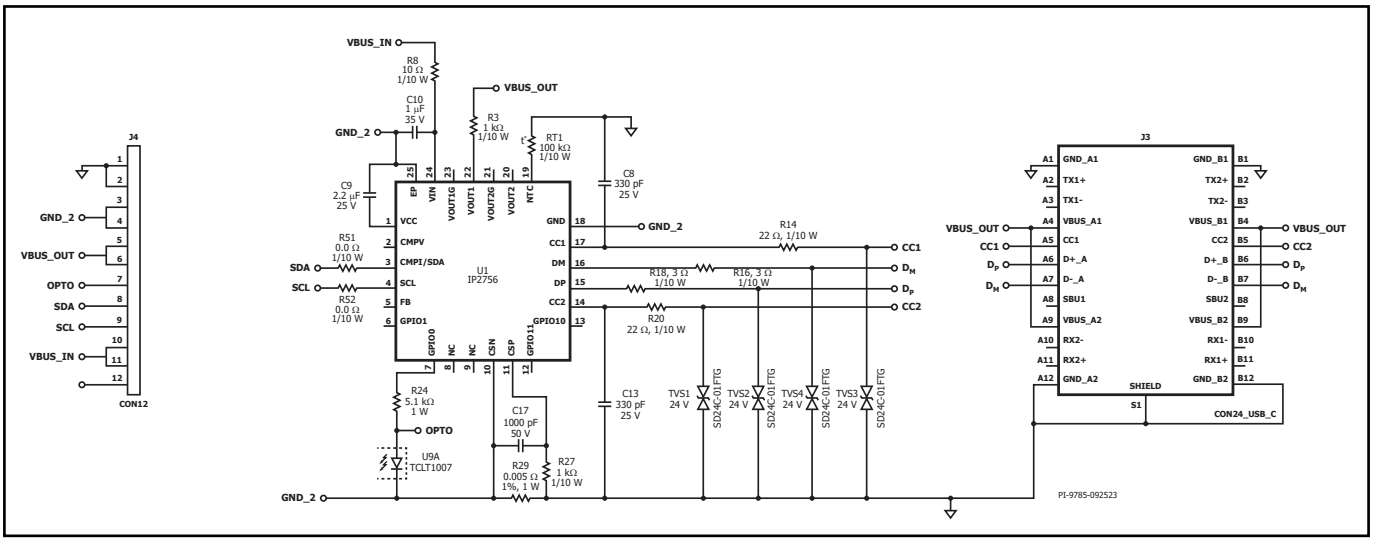


Figure 27. Schematic of 140 W USB PD Power Supply using INN5477F InnoSwitch5-Pro.

Circuit shown in Figure 27 is a USB PD 3.1 Extended Power Range (EPR) power supply using InnoSwitch5-Pro INN5477F flyback switcher IC with a PFC stage using PFS5277F IC and Injoinic IP2756 as USB PD controller. It is designed to deliver a nominal power of 140 W and peak power of 280 W. The USB PD source capabilities supported are 5 V / 5 A, 9 V / 5 A, 15 V / 5 A, 20 V / 5 A, 28 V / 5 A, and 15 V – 28 V / 5 A EPR AVS. Peak power capability is 28 V / 10 A for 1 ms at 5% duty cycle. This USB PD power supply is DOE level 6 and EU CoC v5 compliant.

Input fuse F1 isolates the circuit and provides protection from component failure. Common mode chokes L2, L3 and Y capacitor C1 provide common mode noise filtering, while X capacitor C24, differential choke L1 and capacitors C23, C43 provide differential mode EMI filtering. MOV RV1 is used for surge protection. Bridge rectifiers BR1 and BR2 rectify AC line voltage and provide full wave rectified DC.

One end of the transformer primary is connected to rectified DC bus; other end is connected to the drain terminal of InnoSwitch5-Pro IC. Resistors R9, R12 and R17 provide input voltage sense for under and overvoltage (UV/OV) protection feature. Primary RCD clamp formed by diode D2, capacitor C7, resistors R10, R11, R5, R6 limits the peak drain voltage of INN5477F IC (U2) at the instant of the primary switch turn-off. Energy stored in the leakage inductance of the transformer will be transferred to capacitor C7 and later dissipated primarily across R5 and R6. Resistors R10 and R11 are used to reduce ringing on Drain voltage of U2, when it is turned off and during reverse recovery of diode D2. Due to their damping effect, R10 and R11 help improve EMI performance. TVS diode VR1 is used to limit the peak drain voltage of U2 during abnormal transient events such as ESD or EFT. High-voltage ceramic capacitor C35 is used to decouple the bulk voltage and when placed close to transformer pin connected to positive of bulk capacitor and SOURCE pin of InnoSwitch5-Pro IC, helps reduce the loop area of high frequency switching currents.

The InnoSwitch5-Pro IC operates with either SR zero-voltage switching (SR-ZVS) or quasi-resonant (QR) flyback control-scheme, wherein both methods use variable frequency and variable primary current limit to regulate power delivery to the secondary-side. The power supply can operate in continuous conduction mode (CCM), discontinuous conduction mode (DCM), and critical conduction mode (CRM), providing seamless transition between states. Secondary-side control of both synchronous rectifier gate drive and instant of turn-on of primary-side power switch helps avoid any possibility of cross conduction of the two switches and ensures extremely reliable operation.

In QR mode of operation, SR FET is turned on only once in a switching cycle - during secondary conduction time for both CCM and DCM cycles. For CCM pulses, SR gate drive is turned off just prior to secondary-side commanding a new switching cycle to primary through FluxLink, while for DCM pulses, SR gate drive is turned off when magnitude of voltage drop across SR FET drops below $V_{SR(TH)}$ as defined in this data sheet.

When SR-ZVS mode of operation is enabled, for a CCM pulse, SR FET is turned on at the beginning of secondary conduction time and turned off just before secondary controller commanding a new switching cycle to primary. Therefore, a CCM switching cycle looks exactly alike for QR and SR-ZVS modes. With DCM mode, apart from the usual turn-on and off of SR FET at the beginning and end of secondary conduction time, SR FET is turned on and off for a second time in a switching cycle (referred to as SR-ZVS pulse) just prior to secondary controller requesting for the next primary switch turn-on.

The SR-ZVS pulse ON-time is user programmable through an I^2C command. Since current through SR FET flows from Drain to Source during this interval, some energy from the output is stored in the magnetizing inductance. Once the SR-ZVS pulse ON-time elapses, SR FET is turned off and the secondary controller waits for a duration defined by SR-ZVS delay time, which is user programmable, before sending the request for the next primary switch turn-on. During this SR-ZVS delay time, primary magnetizing inductance resonates with switching node capacitance, facilitating ZVS turn-on of primary switch in the subsequent cycle. Full ZVS can be achieved through proper tuning of SR. In SR-ZVS mode, a TVS clamp is required to limit BV_{DSS} of the primary device in abnormal operation conditions.

Different input and output voltage cases might require different SR-ZVS ON and delay times to achieve ZVS turn-on of primary to achieve maximum efficiency. Unnecessarily large values of SR-ZVS ON-time might lead to excess negative current in the primary, leading to a drop in efficiency. Similarly, extremely large delay times might lead to primary switch voltage resonating back again from its valley, thereby preventing ZVS turn-on of primary switch. It is advisable to tune the SR-ZVS delay time to be closer to half the time period of resonance ring between magnetizing inductance and switch node capacitance to achieve optimal turn-on. To reduce turn-on loss across SR FET, it is recommended to enable FWD valley switching when SR-ZVS mode is enabled. When QR mode is enabled, it is desirable to turn on the primary switch when FWD voltage is at its peak (primary drain voltage at its valley) to reduce turn on loss.

By default, InnoSwitch5-Pro operates in QR mode of operation. SR-ZVS can be enabled or disabled through I^2C commands. On disabling SR-ZVS feature, secondary controller would automatically revert to QR mode of operation. It is important to note that when SR-ZVS feature is enabled, secondary controller would implement the SR-ZVS pulse only for DCM cycles. In case of CCM operation, SR-ZVS pulse would not be generated, and therefore, switching cycle would look exactly like the QR mode.

The InnoSwitch5-Pro IC is self-starting, using its internal high-voltage current source to charge the BPP pin capacitor C22 when input is first applied. During normal operation, primary-side block is powered from an auxiliary winding on transformer T1. Output of auxiliary (or bias) winding is rectified using diode D5 and filtered using capacitor C21. Linear regulator circuit comprises of BJT Q6, R54, R23 and Zener Diode VR4. This circuit ensures that sufficient current is supplied into BPP pin of the InnoSwitch5-Pro IC. By injecting sufficient current into BPP pin, internal current source of U2 is not required to charge C22, thereby reducing no-load power consumption and improving efficiency during normal operation. Current consumption of BPP pin increases with switching frequency. A resistor, if connected in series with VR4 provides positive slope in emitter voltage of BJT Q6 with load, thereby ensuring increasing current supplied into BPP pin as load increases. This improves overall efficiency. The HSD pin is required to be connected to SOURCE pin.

Zener diode ZD2 offers primary sensed output overvoltage protection. In a flyback converter, output of auxiliary winding tracks output voltage of the converter. In case of overvoltage at output of the power supply, auxiliary winding voltage increases and causes breakdown of ZD2. If the current injected into BPP of InnoSwitch5-Pro IC exceeds I_{SD} threshold, InnoSwitch5-Pro controller will latch-off the power supply and prevent any further increase in output voltage. Resistor R53 limits current injected into BPP pin when output overvoltage protection is triggered.

Output regulation is achieved using modulation control where frequency and I_{LIM} of switching cycles are adjusted based on output load. At higher load, secondary controller requests switching cycles more often, leading to higher I_{LIM}, while at lighter load or no-load, switching frequency is reduced leading to lower I_{LIM} values. In a switching cycle, primary switch remains ON until the primary current ramps to the device current limit for the specific operating state.

Secondary-side of the InnoSwitch5-Pro IC has output voltage and current sensing and provides gate drive to a FET for synchronous rectification. Voltage across transformer secondary winding is rectified by secondary-side synchronous rectifier FETs (SR FETs) Q2 and Q3, and filtered by capacitors C3, C5 and C6. C6 (330 µF) is added to support peak power of 280 W. For a power supply with 140 W rated power, C3 and C5 (680 µF each) are generally sufficient. High frequency ringing during switching transients that would otherwise create radiated EMI are reduced by the RCD snubber, resistors R4, R55, capacitor C4, and Diode D10. Diode D10 minimizes dissipation across resistors R4 and R55 when capacitor C4 discharges. This RCD snubber also helps reduce voltage stress on SR FETs. TVS diode VR5 is added to limit the peak drain voltage of Q2 and Q3 for peak power operation.

Gates of Q2 and Q3 are driven by the circuit in secondary-side controller inside U2. SR FET Q2 and Q3 are turned on based on the secondary winding voltage sensed by FWD pin of the IC via resistor R15.

Secondary-side of U2 is self-powered from either the secondary winding forward voltage or output voltage. For designs with the InnoSwitch5-Pro IC, especially with 28 V output cases, use of secondary bias winding circuit is strongly suggested to ensure high system efficiency and that secondary-side die temperature remains within acceptable levels. In this design, secondary bias winding voltage is rectified by diode D4 and filtered by capacitor C15. Resistor R13 limits current flowing into BPS pin. In case of designs with higher output voltages (>24 V), it is suggested to choose a value for R13 such that the secondary bias winding supplies ~7 mA of current into BPS pin at full load condition with max output voltage. Capacitor C11 connected to the BPS pin of InnoSwitch5-Pro IC provides decoupling for the internal circuitry.

IC U2 monitors output current by sensing the voltage drop across resistor R19. Measurement is then filtered by resistor R21 and capacitor C14, and monitored across the IS and SECONDARY GROUND pins. An internal current sense threshold of up to 32 mV configured by the USB PD controller via I²C interface is used to reduce losses. Once the output current threshold is exceeded, the InnoSwitch5-Pro IC responds depending on its configuration to either maintain a fixed output current by using variable frequency and variable primary switch peak current control schemes or to shut down the power supply.

For constant current (CC) operation, when output voltage falls below 5 V, secondary-side controller inside the InnoSwitch5-Pro IC will directly power itself from the secondary winding. During on-time of the primary-side power switch, forward voltage that appears across secondary winding is used to charge the SECONDARY BYPASS pin decoupling capacitor C11 via an internal regulator. This allows output current regulation to be maintained down to the minimum value of UV threshold. Below this level, the unit enters auto-restart until output load is reduced.

When output current is below the CC threshold, the converter operates in constant voltage (CV) mode. Output voltage is monitored by the VOUT pin of the InnoSwitch5-Pro IC. Measured output voltage is compared to an internal voltage threshold that is set via the integrated secondary controller of the InnoSwitch5-Pro IC and USB PD controller IC. Output voltage regulation is achieved by variable frequency and variable primary switch peak current limit control schemes. Capacitor C44 serves as a decoupling capacitor and is suggested to be placed closer to the VOUT pin.

N-channel MOSFET Q1 functions as the bus switch which connects or disconnects output of the flyback converter from USB Type-C receptacle. MOSFET Q1 is controlled by the VB/D pin on InnoSwitch5-Pro IC. Diode D9 is connected across the Source and Gate terminals of Q1 and resistor R50 is connected from the Gate terminal of Q1 to the VB/D pin. These 2 components provide a discharge path for bus voltage when Q1 is turned off. Capacitor C2 is used at the output for ESD protection and output voltage ripple reduction.

In this design, Injoinic IP2756 (U1) is used as the USB Type-C and PD controller. Output of InnoSwitch5-Pro IC powers IP2756 device directly from the flyback output voltage VBUS_IN. USB PD protocol is communicated over either CC1 or CC2 line depending on the orientation of Type-C plug.

The IP2756 IC communicates with the InnoSwitch5-Pro IC through the I²C interface using SCL and SDA lines through which it configures the power supply operating parameters such as set points (output voltage CV, constant current CC, cable drop compensation CDC), protection thresholds and responses (output overvoltage OVA / undervoltage UVA), and gathers telemetry status (output voltage, output current). The complete list of available PI Command and Telemetry registers can be found in this data sheet. Capacitor C16 is used as the decoupling capacitor for uVCC pin. U1 monitors output current by sensing the voltage drop across resistor R29 and is filtered by resistor R27 and capacitor C17.

Capacitors C9 and C10 are used as decoupling capacitors on VCC and VIN pins of U1. Resistors R14, R16, R18, R20, TVS diodes TVS1-TVS4 are used to protect CC1, CC2, DP and DM lines from ESD surge events. Capacitors C8 and C13 are used to protect CC1 and CC2.

Key Application Considerations

Output Power Table

The data sheet output power table (Table 1) represents the maximum practical continuous output power level that can be obtained under the following conditions:

1. The minimum DC input voltage is 90 V or higher for 85 VAC input, 220 V or higher for 230 VAC input or 115 VAC with a voltage doubler. Voltage rating of the input capacitor selected should meet the criteria for AC input designs.
2. Efficiency assumptions depend on power level. Smallest device power level assumes efficiency >88% increasing to >93% for the largest device.
3. Transformer primary inductance tolerance of ±5%.
4. Reflected output voltage (V_{OR}) is set to maintain $K_P \geq 0.7$ at minimum input voltage for universal line and $K_P \geq 1$ for high-line input designs (for thermally constrained environment efficiency should be >94% with larger devices). $K_P \geq 1.2$ is suggested to utilize the full advantage of SR-ZVS at a given operating condition.
5. Maximum conduction losses for adapters and open frame designs are limited to 0.6 W and 0.8 W respectively.
6. Increased current limit is selected for peak and open frame power columns and standard current limit for adapter columns.
7. The part is board mounted with SOURCE pins soldered to a sufficient area of copper and/or a heat sink to keep the SOURCE pin temperature at or below 110 °C.
8. Ambient temperature of 50 °C for open frame designs and 40 °C for sealed adapters.
9. Below a value of 1, K_P is the ratio of ripple to peak primary current. To prevent reduced power delivery, due to premature termination of switching cycles, a transient K_P limit of ≥0.25 is recommended. This prevents the initial current limit (I_{INT}) from being exceeded at switch turn-on.

Primary-Side Sensed Output Overvoltage Protection

Primary-side sensed output overvoltage protection provided by the InnoSwitch5-Pro IC uses internal protection that is triggered when current into PRIMARY BYPASS pin exceeds the threshold current of I_{SD}. Protection response in this case is dependent on the feature code of the device, either latch-off or auto-restart. In addition to serving as an internal filter, the PRIMARY BYPASS filter capacitor

provides noise immunity. For the bypass capacitor to be effective as a high frequency filter, the capacitor should be located as close as possible to the PRIMARY BYPASS and SOURCE pins of the device.

Primary sensed OVP function can be realized by connecting a series combination of Zener diode and resistor from the rectified and filtered bias winding voltage supply to the PRIMARY BYPASS pin. The ratio of rectified and filtered bias winding voltage to winding voltage may be higher or lower than the expected value (between 0.7x to 1.5x the turns ratio). Poor coupling of primary bias winding with secondary winding contributes to lower than expected value, while peak charging of the primary bias winding capacitor leads to higher than expected voltage. The rectified and filtered bias winding voltage is determined by an interplay between the two factors. It is therefore recommended that the rectified bias winding voltage be measured prior to selecting primary bias component values. This measurement should be ideally done at the lowest input voltage and with the highest load at the output. This measured voltage should be used to select the components required to achieve primary sensed OVP. For resistor in the OVP circuit (R53), it is suggested to use 1) 47 Ω OVP resistor and Zener diode in series, or 2) ≥47 Ω OVP resistor, Zener diode, and general purpose blocking diode in series, oriented to allow current into BPP during OVP event, but prevent BPP capacitor discharge through the OVP circuit.

Zener diode and resistor values must be chosen such that the current drawn by BPP at the target OVP level exceeds minimum limit of BPP pin fault shutdown threshold current I_{SD}. The Zener diode must not conduct during normal steady-state and transient conditions. So, the clamping voltage of OVP circuit must be higher than the difference between bias capacitor voltage and BPP voltage during those conditions. It is recommended to use a 500 mW rated Zener diode in the OVP circuit.

Reducing No-Load Consumption

The InnoSwitch-5 Pro IC can start in self-powered mode, drawing energy from the BYPASS pin capacitor charged through an internal current source. To reduce no-load power consumption and to improve overall efficiency at other conditions, use of primary bias winding is suggested to provide supply current to the PRIMARY BYPASS pin, once the InnoSwitch-5 Pro IC has started switching. An auxiliary (bias) winding in the transformer serves this purpose. Bias winding driver supply to the PRIMARY BYPASS pin enables the design of power supplies with low no-load power consumption of less than 30 mW. Resistor R23 shown in Figure 27 should be adjusted to achieve the lowest no-load input power. It is recommended to measure rectified bias winding voltage at max input voltage, 5 V, no-load condition prior to choosing a value for R23.

Secondary-Side Overvoltage Protection

Secondary-side sensed output overvoltage protection is provided by the InnoSwitch5-Pro IC. Users can program the magnitude of over voltage threshold and the type of response through I^2C commands.

Selection of Components

Components for InnoSwitch5-Pro Primary-Side Circuit

BPP Capacitor

A capacitor connected from PRIMARY BYPASS pin of the InnoSwitch5-Pro IC to GND provides decoupling for the primary-side controller, and its value also determines the current limit. A 0.47 μF or 4.7 μF capacitor may be used for Standard and Increased I_{LIM} respectively. Even though electrolytic capacitors can be used; surface mount multi-layer ceramic capacitors are highly preferred for use on double-sided boards as they enable placement of capacitors close to the IC and offer lower ESL. Their small size also makes them ideal for compact power supplies. Capacitors rated for at least 10 V, 0805 or larger sizes with X5R or X7R dielectric are recommended to ensure that minimum capacitance requirement is met. Ceramic capacitor type designations, such as X7R, X5R from different manufacturers or different product families do not have the same voltage coefficients.

It is recommended that capacitor data sheets be reviewed to ensure that the selected capacitor does not have more than 20% drop in capacitance at 5 V. Do not use Y5U or Z5U / 0603 rated MLCC as these types of SMD ceramic capacitors have very poor voltage and temperature coefficient characteristics.

Bias Winding and External Bias Circuit

The internal regulated current source present between DRAIN pin of Primary switch to PRIMARY BYPASS pin of the InnoSwitch5-Pro primary-side controller charges the capacitor connected to PRIMARY BYPASS pin to achieve start-up. A bias winding should be provided on the transformer with a suitable rectifier and filter capacitor to create a bias supply that can be used to supply the required current for BPP. Turns ratio for bias winding should be selected such that 7 V to 8 V minimum is developed across the capacitor at the highest input voltage and 5 V, no-load output condition. If the voltage across bias winding is lower than this, the bias circuit may not be able to inject sufficient current into BPP, resulting in the turn-on of internal source, leading to increased no-load power consumption.

For designs with a single output voltage, a single resistor regulator circuit might be sufficient. However, in USB PD applications, output voltage range can be very wide – such as 5 V to 28 V in EPR designs. Such a wide output voltage variation results in a large change on primary bias winding voltage. Therefore, for wide output range designs, a linear regulator circuit is generally required to regulate current injected into the PRIMARY BYPASS pin of the InnoSwitch5-Pro IC.

Primary bias current from the external circuit during 5 V no-load condition should be set to max of I_{S1} for the InnoSwitch5-Pro IC to achieve lowest power consumption. BPP voltage can be used as an indicator of whether the injected BPP current is sufficient. When the BPP voltage reaches V_{SHUNT} (5.36 V typical), there is enough current externally supplied into BPP. Otherwise, primary controller consumes power from the DRAIN pin using the internal regulated current source, which increases overall power consumption. BPP current required to achieve V_{SHUNT} is directly proportional to the operating switching frequency and can be interpolated using I_{S1} and I_{S2} parameters from the data sheet.

A glass passivated standard recovery rectifier diode with low junction capacitance is recommended to avoid the snappy recovery typically seen with fast or ultrafast diodes that can lead to higher radiated EMI.

An aluminum capacitor of at least 22 μF with a voltage rating 1.2 times greater than the highest voltage developed across the capacitor is recommended. The highest voltage is typically developed across this capacitor when the supply is operated at the highest rated output voltage and load with the lowest input voltage. For designs with 28 V output, a BJT rated for at least 80 V, 500 mW is recommended.

Line UV and OV Protection

Resistors connected from the UNDER/OVER INPUT VOLTAGE pin to the DC bus enable sensing of input voltage for line undervoltage and overvoltage protection. For a typical universal input application, 2 or 3 resistors with 1206 packages each of value 1.2 to 2 MΩ amounting to a total V pin resistance of 3.6 to 4 MΩ is recommended.

The InnoSwitch5-Pro IC features primary sensed line OV protection that can be used to inhibit further switching cycles when current through V pin exceeds UV/OV Pin Line Overvoltage Threshold (I_{OV+}) with a deglitch filter (t_{OV+}). Switching resumes when current through V pin drops below UV/OV Pin Line Overvoltage Recovery Threshold(I_{OV-}). A fast AC reset can be achieved using the modified circuit configuration shown in Figure 28. The voltage across capacitor C_S reduces rapidly after input supply is disconnected, reducing current into the INPUT VOLTAGE MONITOR pin of the InnoSwitch5-Pro IC and resetting the InnoSwitch5-Pro controller. Line UV/OV protection feature can be disabled by shorting V pin to SOURCE pin of the InnoSwitch5-Pro IC.

Primary-Side Clamp

In Figure 27 once primary switch is turned off, leakage energy is transferred to the clamp capacitor C7 through resistors R10 and R11. Later this energy is dissipated as heat across parallel resistors R5 and R6. A glass passivated standard recovery rectifier diode with low junction capacitance is recommended to avoid the snappy recovery typically seen with fast or ultrafast diodes that can lead to higher radiated EMI.

Increasing the value of C7 capacitor helps better clamp the Drain voltage of primary switch. However, it is important to note that this might also lead to a larger loss.

The clamp capacitor voltage rating must be higher than V_{OR}. Since V_{OR} is usually within 135 V to 185 V range for designs with 28 V output, 1206 size capacitors rated for at least 200 V with values in the range of 1.5 nF to 3.3 nF are typically suitable for the primary RCD clamp circuit. In addition to reducing ringing due to reverse recovery of clamp diode, resistors R10 and R11 help improve EMI performance. Since current with a large initial spike flows through resistors R10 and R11 after primary switch turn-off, it is recommended to use resistors with values in the range of a few tens of ohms and 1206 size for the series clamp resistors. Parallel resistors R5 and R6 dissipate energy stored across clamp capacitor as heat. Even though using low value resistors helps clamp the Drain voltage better, that leads to higher losses. Since the energy dissipated in these resistors is proportional to the square of I_{LIM} of the InnoSwitch5-Pro IC, for higher I_{LIM} devices, especially, it suggested to use 2 or more resistors with 1206 package.

For a 28 V output design with universal AC input, a TVS with reverse stand-off voltage of 200 V and with power rating of 3.3 W or 5 W continuous is typically sufficient.

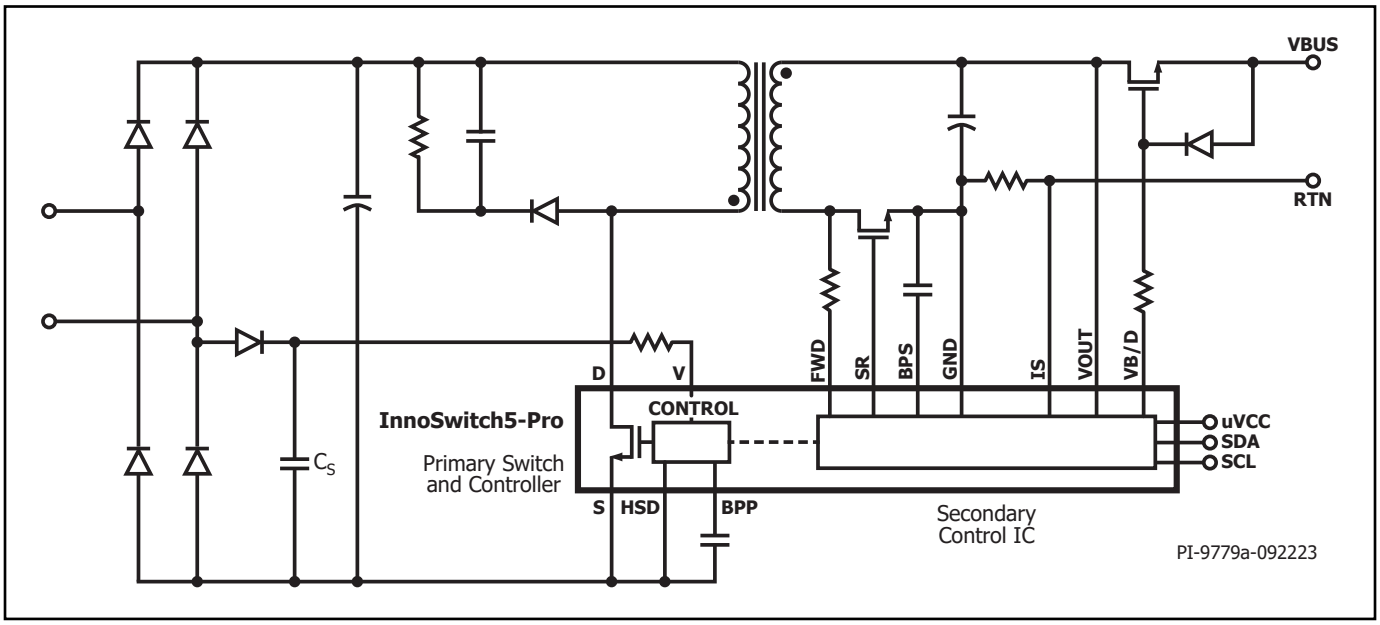


Figure 28. Fast AC Reset Configuration.

Components for InnoSwitch5-Pro Secondary-Side Circuit

SECONDARY BYPASS Pin - Decoupling Capacitor

A 2.2 µF, 10 V / X7R or X5R / 0805 or larger size multi-layer ceramic capacitor should be used for decoupling the SECONDARY BYPASS pin of the InnoSwitch5-Pro IC. Since SECONDARY BYPASS pin voltage needs to be 4.5 V before output voltage reaches regulation voltage level, a significantly higher BPS capacitor value could lead to output voltage overshoot during start-up. Values lower than 1.5 µF may not offer enough capacitance and cause unpredictable operation. The capacitor must be located adjacent to the IC pins. At least 10 V rating is recommended for the BPS capacitor to give enough margin from BPS voltage. 0805 size is necessary to guarantee the actual value in operation since the capacitance of ceramic capacitors drops significantly with applied DC voltage especially with small package SMD such as 0603. 6.3 V / 0603 / X5U or Z5U type of MLCCs are not recommended for this reason. Ceramic capacitor type designations, such as X7R, X5R from different manufacturers or different product families do not have the same voltage coefficients. It is recommended that capacitor data sheets be reviewed to ensure that the selected capacitor will not have more than 20% drop in capacitance at 4.5 V. Capacitors with X5R or X7R dielectrics should be used for the best results.

When output voltage of the power supply is 5 V or higher, the supply current for the secondary-side controller is provided by the OUTPUT VOLTAGE (VOUT) pin of the IC as the voltage at this pin is higher than the SECONDARY BYPASS pin voltage. During start-up and operating conditions where the output voltage of the power supply is below 5 V, the secondary-side controller is supplied by current from an internal current source connected to the FORWARD pin.

If the power supply operates at higher output voltages, deriving secondary bias supply from V_{OUT} will incur significant losses across the internal linear regulator, leading to increased secondary-side die temperature. A bias winding may be provided from the transformer with suitable rectifier and filter to supply the required current to BPS pin at the highest output voltage. This bias supply may not be able to supply the current required at lower output voltages since it scales with the output and should be greater than V_{BPS} (4.5 V). Ratio of number of secondary bias winding turns to secondary winding turns determines the output voltage beyond which the bias winding current starts supplying current into BPS pin. It is suggested that the value of resistor located between BPS capacitor and secondary bias winding filter capacitor be chosen to ensure that at least 7 mA current flows into BPS pin at 28 V, Full load condition.

FORWARD Pin Resistor

A 47 Ω, 5% resistor is recommended to ensure sufficient IC supply current. A lower resistor value should not be used as it can affect device operation such as timing of synchronous rectifier drive. A higher resistance value up to 1 kΩ can be used with an optional parallel fast recovery diode to adjust the synchronous rectifier gate drive duty. The diode anode is connected to the transformer winding while the cathode is connected to the FORWARD pin. Figures 29, 30, 31 and 32 show examples of unacceptable and acceptable FORWARD pin voltage waveforms. V_D is forward voltage drop across the SR.

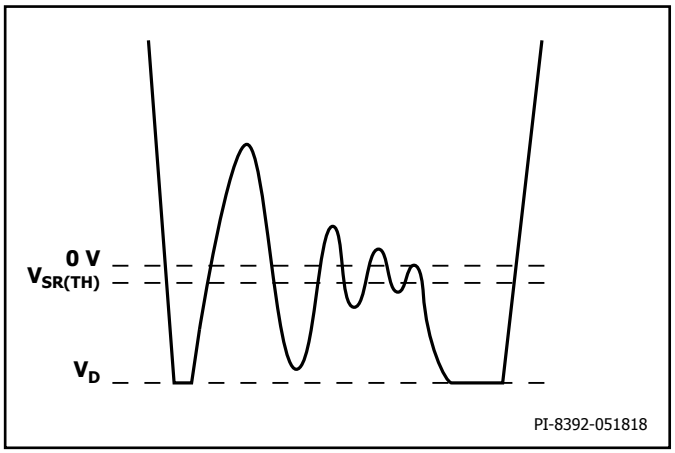


Figure 29. Unacceptable FORWARD Pin Waveform After Handshake with SR Switch Conduction During Flyback Cycle.

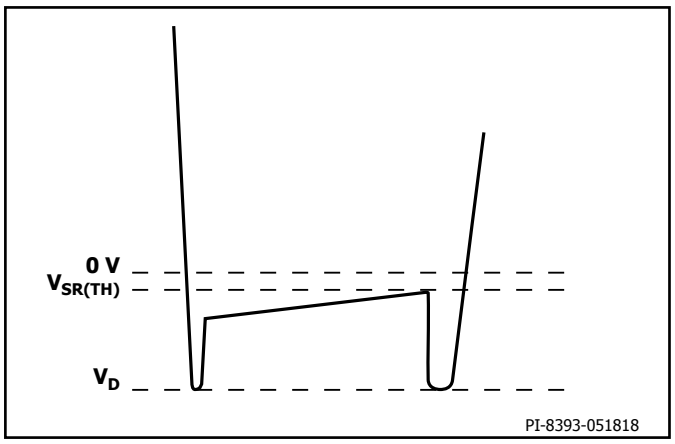


Figure 30. Acceptable FORWARD Pin Waveform After Handshake with SR Switch Conduction During Flyback Cycle.

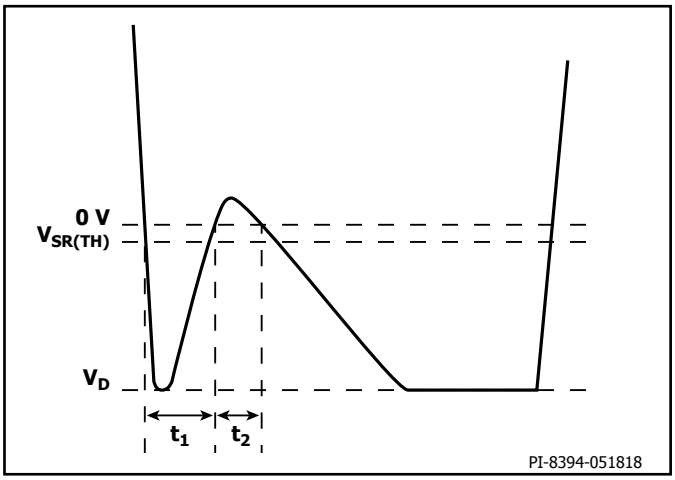


Figure 31. Unacceptable FORWARD Pin Waveform Before Handshake with Body Diode Conduction During Flyback Cycle

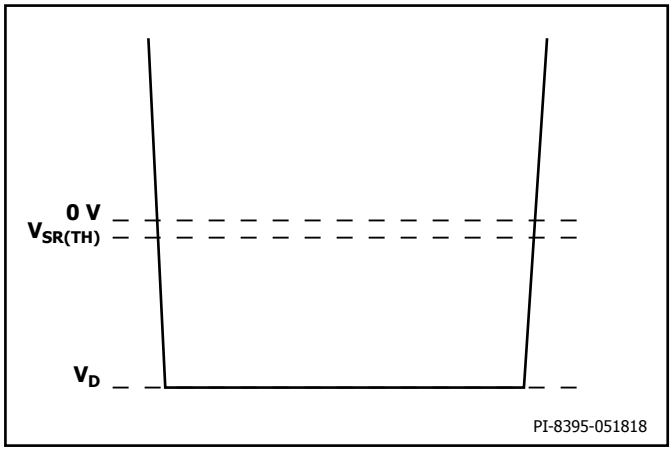


Figure 32. Acceptable FORWARD Pin Waveform Before Handshake with Body Diode Conduction During Flyback Cycle.

Synchronous Rectifier FET

Although a simple diode rectifier works for the output, use of SR FET enables significant improvement in operating efficiency often necessary to meet the European CoC and the U.S. DoE energy efficiency requirements. SR FET gate should be tied directly to the SYNCHRONOUS RECTIFIER DRIVE pin of the InnoSwitch5-Pro IC (no additional resistors should be connected in the gate circuit of the SR FET). Following a secondary controller takeover after primary-secondary handshake during start-up, the secondary-side controller turns on the SR FET once the flyback cycle begins. The SR FET is turned off once the magnitude of V_{DS} of SR FET drops below $V_{SR(TH)}$. Once SR FET is turned off, any remaining portion of the flyback cycle is completed with the current commutating through the body diode of SR FET. It is to be noted that the length of the FWD trace involving SR drain pin – FWD resistor – FWD pin determines the duty ratio of SR FET. In case this trace is longer, SR FET might turn off earlier than expected during flyback cycle, leading to undesirable longer diode conduction and therefore, reduction in efficiency. In other cases, where SR FET conducts for a duration little bit longer than secondary conduction time, leading to a negative secondary current, it is recommended to increase the resistance connected to FWD pin (up to 1 kΩ) until the desired behavior is observed.

The following table provides a recommendation for the SR FET $R_{DS(ON)}$ selection for different designs. For designs rated for 100 W or more, it is recommended to use 2 SR FETs in parallel to reduce effective $R_{DS(ON)}$, thereby improving efficiency and reducing SR FET part temperature for the same secondary RMS current.

Output	FET $R_{DS(ON)}$
20 V / 3 A	7 mΩ
28 V / 3 A and above	3 mΩ or lower

Table 12. Recommended SR FET $R_{DS(ON)}$ for Different Designs.

The SR FET driver uses SECONDARY BYPASS pin for its supply rail, and this voltage is typically 4.5 V. A FET with a high threshold voltage is therefore not suitable; FETs with a threshold voltage of 1.5 V to 2.5 V are ideal although switches with a threshold voltage (absolute maximum) as high as 4 V may be used provided their data sheets specify $R_{DS(ON)}$ across temperature for a gate voltage of 4.5 V.

For designs with InnoSwitch5-Pro IC, a Schottky diode across SR FET is generally not necessary. The rise and fall time of the SR FET gate-source voltage is determined by its Gate-Source capacitance and the drive strength of InnoSwitch5-Pro IC. Therefore, these timings would be longer when two SR FETs connected in parallel are used, instead of just one.

The SR FET drain-source voltage rating should have enough margin compared to the expected worst-case peak inverse voltage (PIV) based on the transformer turns ratio, input and output voltages, and SR FET turn-off voltage spike. 120 V rated FETs are suitable for designs with output voltage 20 V and above.

The interaction between the leakage reactance of the output windings and the SR FET capacitance (C_{OSS}) leads to ringing on the voltage waveform at the instance of voltage reversal at the winding due to the primary switch turn-on. This ringing can be suppressed using an RC or RCD snubber connected across the SR FET. A snubber resistance in the range of 5 Ω to 47 Ω may be used (higher values lead to a noticeable drop in efficiency). The number of resistors used, and their device package must be selected such that they can handle the power loss in snubber circuit. A switching diode can also be paralleled with the snubber resistor to minimize its dissipation. An X7R capacitor of value 220 pF to 3.3 nF is adequate for most designs. For higher I_{LIM} designs, to reduce SR FET voltage stress during start-up, aside from the SR snubber described above, an RCD clamp is recommended across the secondary winding. In this additional clamp circuit, the anode of diode is connected to SR FET DRAIN pin, followed by a parallel RC circuit connected in series to the diode. 1206 size resistors in the range of 5 kΩ to 20 kΩ are recommended along with 1206 size 200 V rated capacitor in the range of 10 nF to 100 nF range.

Output Capacitor

Low ESR aluminum electrolytic capacitors are suitable for use with most high frequency flyback switching power supplies though the use of aluminum-polymer solid capacitors has gained considerable popularity due to their compact size, stable temperature characteristics, extremely low ESR and high RMS ripple current rating. These capacitors enable the design of ultra-compact chargers and adapters.

Typically, 200 µF to 300 µF of aluminum-polymer capacitance per ampere of output current is adequate. The other factor that influences the choice of capacitance is the output ripple. Ensure that capacitors with a voltage rating higher than the highest output voltage plus sufficient margin is used.

Output Overload Protection

The maximum power which can be delivered by the power supply is obtained by the product of the programmed V_{KP} and the full-scale current limit. For output voltage below the programmed V_{KP} threshold, the InnoSwitch5-Pro IC will limit the output current once the programmed current limit is reached. The full-scale current limit is set by the resistor between the IS and GND pins. A lower value of the current limit can be programmed over I²C. For any output voltage above the programmed V_{KP} threshold, InnoSwitch5-Pro IC will provide a constant power characteristic. An increase in load current within the programmed current limit will result in a drop in output voltage such that the product of output voltage and current equals the maximum power set by the product of V_{KP} and the full-scale current limit.

Decoupling Capacitor on uVCC Pin

It is recommended that at least a 2.2 µF, X7R ceramic capacitor be placed between the uVCC and GND pins. In case of 28 V output designs where the external micro-controller is powered from uVCC, an optional linear regulator circuit is suggested from the secondary bias winding to uVCC.

Pull-Up Resistors for SDA and SCL Pins

A 4.7 kΩ pull-up resistor from each of the SDA and SCL pin to the uVCC pin is recommended for communication at a frequency of 400 kHz. The maximum value of the pull-up resistor is dependent on the capacitance presented by the SDA/SCL lines and the I²C master. The resultant voltage rises to the V_{IL} threshold assuming a total capacitance of 20 pF is tabulated as a function of SCL clock frequency in Table 11.

Decoupling Capacitor at VOUT Pin

It is recommended that a X7R rated 1 µF - 2.2 µF ceramic capacitor be placed close to the VOUT pin. It is recommended to tie the ground of BPS, uVCC and VOUT pin decoupling capacitors together and located closer to the IC, while having a Kelvin connection through a thin trace with power GND to ensure good noise immunity.

IS to GND Pin Current Sense Resistor

This sense resistor is chosen such that the required full-scale current produces a 32 mV drop across IS and GND pins. A 1% or lower tolerance resistor is recommended. This sense resistor must have a kelvin connection to the IS pin filter circuit (formed by a 10 Ω resistor and at least 1 µF capacitor) and is preferred to be placed as close as possible to the InnoSwitch5-Pro IC pins for accurate current measurement and CC regulation.

Output Decoupling Capacitor

A ceramic output decoupling capacitor helps improve ESD performance. This capacitor must be placed as close as possible to output terminals or Type-C connector of the power supply.

Bus Switch

A low $R_{DS(ON)}$ N-channel FET bus switch is recommended to reduce the impact of high load currents on efficiency. The FET need not be a logic level FET. VB/D pin can supply typically 7 V above V_{OUT} so it can sufficiently enhance FETs with gate threshold of 4 V. The FET drain-source voltage rating must have sufficient margin from the maximum output voltage of the power supply. For designs with 28 V output, it is recommended to use FETs rated for at least 40 V.

Bus Discharge

The resistor value for bus discharge is chosen as per the discharge time requirements to bring down the output voltage at the Type-C connector to 0 V (i.e., when the bus switch needs to be opened), also considering the VB/D pin internal current discharge limit $I_{B/D(DS)}$ of 50 mA. 1 kΩ resistor is recommended for 28 V designs to meet the USB PD discharge time specification and also provide sufficient margin from $I_{B/D(DS)}$. A general-purpose diode in series is recommended across the bus switch SOURCE to GATE pins for unidirectional current flow.

External Controller
An external controller is needed to send the I^2C commands to the InnoSwitch5-Pro IC over the SDA and SCL lines. For standalone applications, the external controller can get its supply from the uVCC pin of the InnoSwitch5-Pro IC. It should be able to sustain operation for a supply voltage as low as 2.8 V.

Recommendations for Circuit Board Layout

See Figure 33 and 34 for a recommended circuit board layout for an InnoSwitch5-Pro based power supply.

Single-Point Grounding
Use a single-point ground connection from the input filter capacitor to the area of copper connected to the SOURCE pins.

Bypass Capacitors
PRIMARY BYPASS and SECONDARY BYPASS pin capacitor must be located directly adjacent to the PRIMARY BYPASS-SOURCE and SECONDARY BYPASS-SECONDARY GROUND pins respectively and connections to these capacitors should be routed with short traces.

Primary Loop Area
The area of primary loop that connects input filter capacitor, transformer primary and IC should be kept as small as possible.

IS to GND pin Capacitor
A 1 μF or higher ceramic capacitor is recommended to be used between the IS and GND pins of the InnoSwitch5-Pro IC for accurate constant current regulation.

Primary Clamp Circuit
To reduce leakage related voltage stress on Drain of primary switch and EMI, minimize the loop involving clamp components to transformer and Innoswitch5-Pro IC.

Thermal Considerations
SOURCE pin is internally connected to the IC lead frame and provides the main path to remove heat from the device. Therefore, the SOURCE pin should be connected to a copper area underneath the IC to act not only as a single point ground, but also as a heat sink. As this area is connected to the quiet source node, it can be maximized for good heat sinking without compromising EMI performance. Similarly, for the output SR switch, maximize the PCB area connected to the pins on the package through which heat is dissipated from the SR switch.

Sufficient copper area should be provided on the board to keep IC temperature safely below absolute maximum limits. It is recommended that the copper area provided for copper plane on which the SOURCE pin of the IC is soldered is sufficiently large to keep the IC temperature below 110 °C when operating the power supply at full rated load and at the lowest rated input AC supply voltage.

Y Capacitor
The Y capacitor should be placed directly between the primary input filter capacitor positive terminal and the output positive or return terminal of the transformer secondary. This routes high amplitude common-mode surge currents away from the IC. Note - if an input pi-filter (C, L, C) is used as an EMI filter, then the inductor in the filter should be placed between the negative terminals of the input filter capacitors.

Output SR FET
For best performance, area of the loop connecting secondary winding, output SR FET and output filter capacitor, should be minimized.

IS-GND Pin, Sense Resistor Traces
It is recommended to have traces from the current sense resistor to IS-GND pins be in a star connection at the respective two nodes of current sense resistor to have an accurate CC set-point. IS-GND sense traces should be at the innermost of the solder pads of current sense resistor to avoid measuring any drop across solder pads of the resistor or load traces coming in and out of the sense resistor.

uVCC, SDA and SCL Pins
Traces to SDA and SCL pins should be kept away from any noisy node or trace. If possible, a shield trace should be made in parallel to the SDA and SCL traces.

ESD
Sufficient clearance should be maintained (>8 mm) between the primary-side and secondary-side circuits to enable easy compliance with any ESD / HIPOT requirements. Spark gap is best placed directly between output positive rail and one of the AC inputs. In this configuration, a 6.2 mm spark gap is often sufficient to meet the creepage and clearance requirements of many applicable safety standards. This is less than the primary to secondary spacing because the voltage across spark gap does not exceed the peak of the AC input.

If there is a controller used for USB PD communication then the Ground of the controller should be connected to the GND pin of the InnoSwitch5-Pro IC and not the GND pin of the type C connector, this helps for ESD performance. However, if there is a separate daughter board connected with the controller IC on it and the Ground path becomes long then the Ground of the controller IC can be connected closer to the USB connector GND pins to help in the eye diagram during USB PD compliance tests.

Drain Node
Drain switching node is the dominant noise generator. As such, components connected to drain node should be placed close to the IC and away from sensitive feedback circuits. Clamp circuit components should be located physically away from the PRIMARY BYPASS pin and trace lengths minimized.

Area of the loop comprising of the input rectifier filter capacitor, primary winding and the IC primary-side switch should be kept as small as possible.

Layout Example

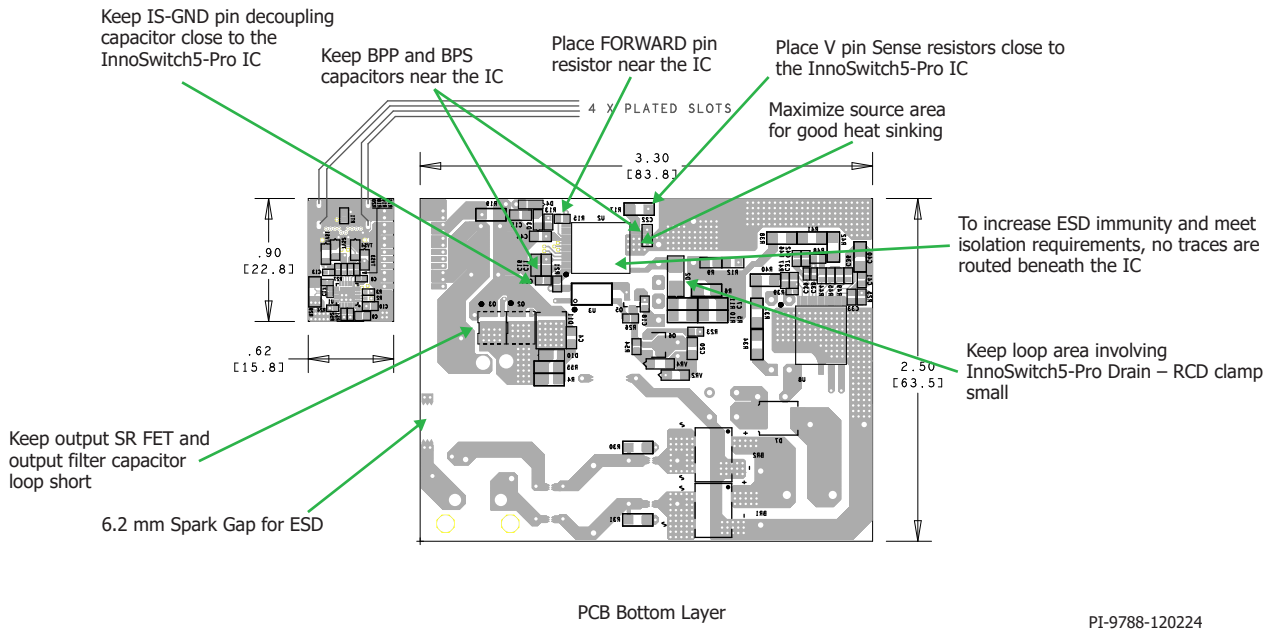


Figure 33. PCB Layout Recommendation – Bottom Layer.

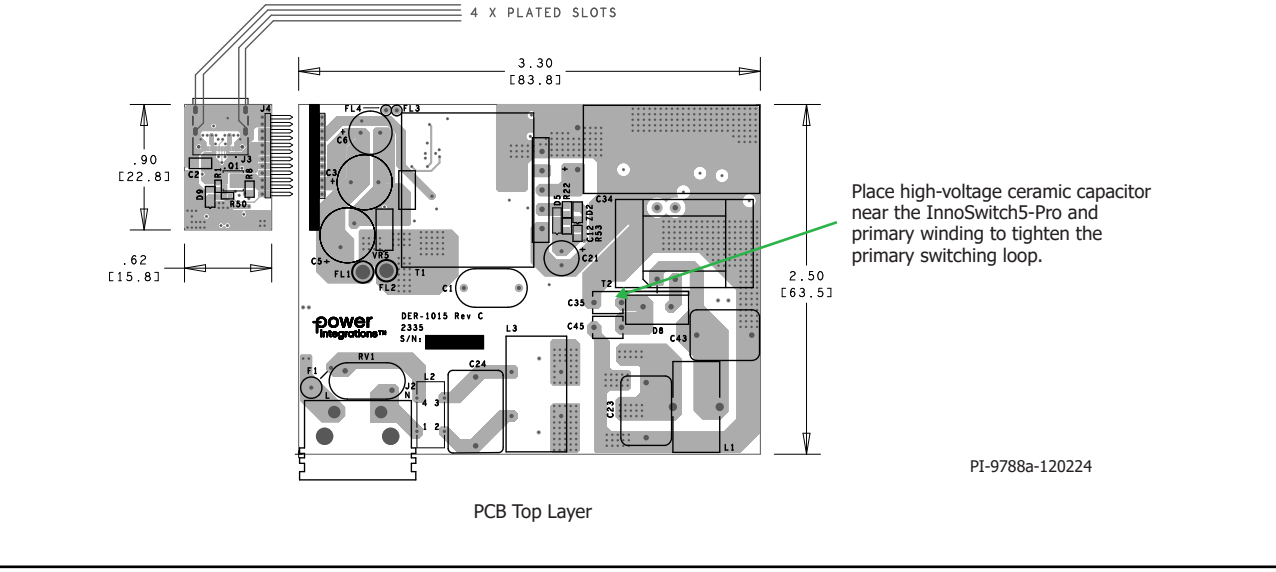


Figure 34. PCB Layout Recommendation – Top Layer.

Recommendations for EMI Reduction

1. Appropriate component placement and small loop areas of the primary and secondary power circuits help minimize radiated and conducted EMI. Care should be taken to achieve a compact loop area.
2. Resistor in series with diode in the primary RCD clamp circuit helps ringing, thereby aiding with EMI.
3. Resistor in series with the primary bias winding helps reduce radiated EMI.
4. Common mode chokes are typically required at the input of the power supply to sufficiently attenuate common mode noise. However, the same performance can be achieved by using shield windings on the transformer. Shield windings can also be used in conjunction with common mode filter inductors at the input to improve conducted and radiated EMI margins.
5. Adjusting SR switch RC snubber component values can help reduce high frequency radiated and conducted EMI.
6. A pi-filter comprising differential inductors and capacitors can be used in the input rectifier circuit to reduce low frequency differential EMI.
7. A 1 µF ceramic capacitor connected at the output of the power supply helps to reduce radiated EMI.

Transformer design must ensure that the power supply delivers rated power at the lowest input voltage. The lowest voltage on the rectified DC bus depends on capacitance of the filter capacitor used. At least 2 µF/W is recommended to always keep DC bus voltage above 70 V, though 3 µF/W provides sufficient margin. Ripple on DC bus should be measured to confirm the design calculations for transformer primary-winding inductance selection. PI Expert Online (https://piexpertonline.power.com/) can be used to easily create designs for InnoSwitch5-Pro.

Switching Frequency (f_{sw})
It is a unique feature in InnoSwitch5-Pro IC that for full load, the designer can set the switching frequency to between 50 kHz to 130 kHz. For a smaller transformer, full load switching frequency could be set to 130 kHz. When setting the full load switching frequency it is important to consider primary inductance and peak current tolerances to ensure that average switching frequency does not exceed minimum threshold of overload detection frequency f_{OVL} to prevent auto-restart.

Table 13 provides a guide for switching frequency selection based on device size. This represents the best compromise between the overall device losses based on the internal high-voltage switch and transformer size.

Device	Recommended Full Load Switching Frequency
INN5375F	90-110 kHz
INN5377F	70-90 kHz
INN5477F	60-80 kHz

Table 13. Recommended Switching Frequency for Different Devices*.

* Higher size devices have lower $R_{DS(ON)}$ and larger I_{LIM}. They are intended for use in higher power applications (>75 W). In accordance with IEC standards, these designs must meet the harmonic current requirements and thus need a power factor correction front end. It is assumed for these designs that the input voltage to the DC-DC section is in the range of 380-400 VDC.

Reflected Output Voltage, V_{OR} (V)
This parameter is the primary winding voltage reflected from the secondary winding (through the transformer turns ratio) during secondary conduction-time. To make full use of ZVS capability and ensure flattest efficiency over line/load, set reflected output voltage (V_{OR}) to maintain K_P = 0.7 at minimum input voltage for universal input and K_P = 1 for high-line-only conditions.

Consider the following for design optimization:
1. Higher V_{OR} allows increased power delivery at V_{MIN}, which minimizes the value of the input capacitor and maximizes power delivery from a given InnoSwitch5-Pro device.
2. Higher V_{OR} reduces the voltage stress on the output diodes and SR switches.
3. Higher V_{OR} increases leakage inductance which reduces power supply efficiency.
4. Higher V_{OR} increases peak and RMS current on the secondary-side which may increase secondary-side copper and diode losses.

There are some exceptions to this. For very high output currents, V_{OR} should be reduced to get the highest efficiency. For output voltages above 15 V, V_{OR} should be higher to maintain an acceptable PIV across the output synchronous rectifier.

Ripple to Peak Current Ratio, KP
K_P below 1 indicates continuous conduction mode, where K_P is the ratio of ripple-current to peak-primary-current (Figure 35).

$$K_P \equiv K_{RP} = I_R / I_P$$

K_P higher than 1, indicates discontinuous conduction mode (Figure 36). In this case, K_P is the ratio of primary switch off-time to the secondary diode conduction-time.

$$K_P \equiv K_{DP} = (1 - D) \times T/ t = V_{OR} \times (1 - D_{MAX}) / ((V_{MIN} - V_{DS}) \times D_{MAX})$$

It is recommended that $K_P \geq 0.7$ at the minimum expected DC bus voltage be used for InnoSwitch5-Pro designs. Since SR-ZVS with the InnoSwitch5-Pro IC ensures ZVS turn-on of primary switch only DCM cycles (i.e. $K_P \geq 1$), it is recommended that designs completely operate in DCM at high-line input. Ensuring this also ensures lower SR FET voltage stress. In case of SR-ZVS operation, $K_P \geq 1.2$, at least at high-line, is suggested to utilize the full advantage of this feature and thereby achieve ZVS turn-on.

For a typical USB PD and rapid charge designs which require a wide output voltage range, K_P will change significantly as the output voltage changes. K_P will be high for high output voltage conditions and will drop as the output voltage is lowered. PIXIs spreadsheet can be used to effectively optimize selection of K_P, inductance of primary winding, transformer turns ratio, and operating frequency while ensuring appropriate design margins.

Core Type
Choice of a suitable core is dependent on the physical limits of the power supply enclosure. It is recommended that only cores with low loss be used to reduce thermal challenges.

Safety Margin, M (mm)
For designs that require safety isolation between primary and secondary that do not use triple insulated wire, width of the safety margin to be used on each side of the bobbin is important. For universal input designs, a total margin of 6.2 mm is typically required – 3.1 mm being used on either side of the winding. For vertical bobbins, margin may not be symmetrical. However, if a total margin of 6.2 mm is required then the physical margin can be placed on only one side of the bobbin. For designs using triple insulated wire it may still be necessary to add a small margin to meet required creepage distances. Many bobbins exist for every core size, each with different

mechanical spacings. Refer to the bobbin data sheet or seek guidance to determine what specific margin is required. As margin reduces, available area for windings, winding area will disproportionately reduce for small core sizes. It is recommended that for compact power supply designs using an InnoSwitch5-Pro IC, triple insulated wire should be used for the secondary windings which then eliminates the need for margins.

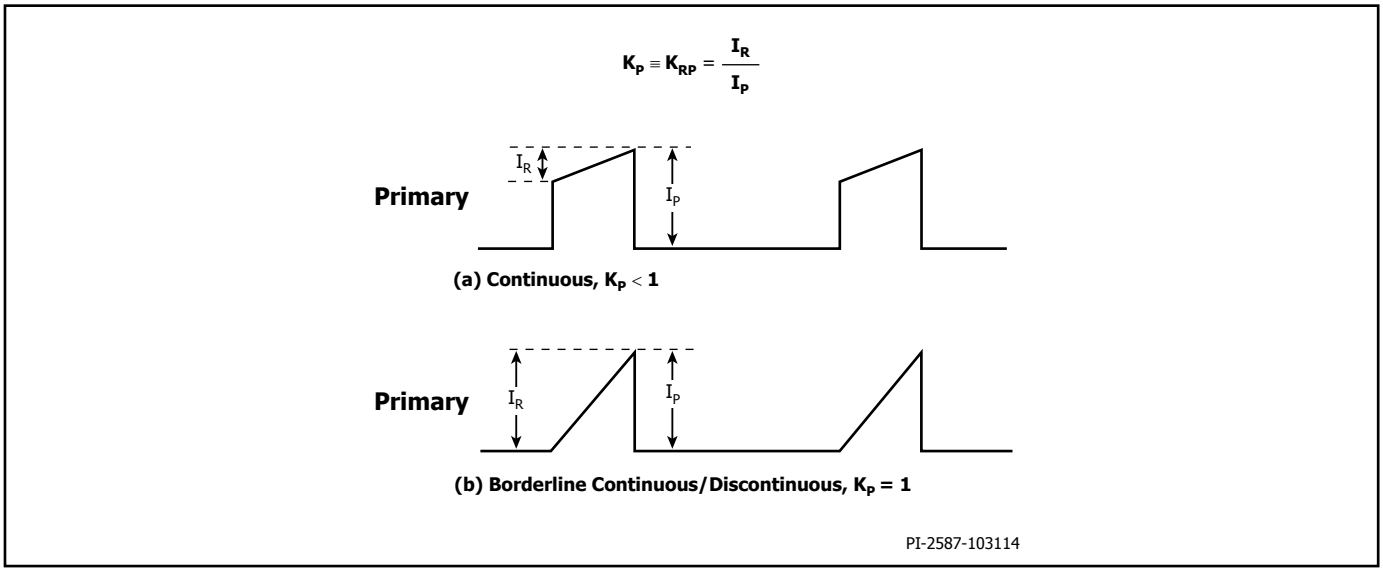


Figure 35. Continuous Conduction Mode Current Waveform $K_P \leq 1$. SR-ZVS Mode will Automatically be Disabled for CCM Cycles.

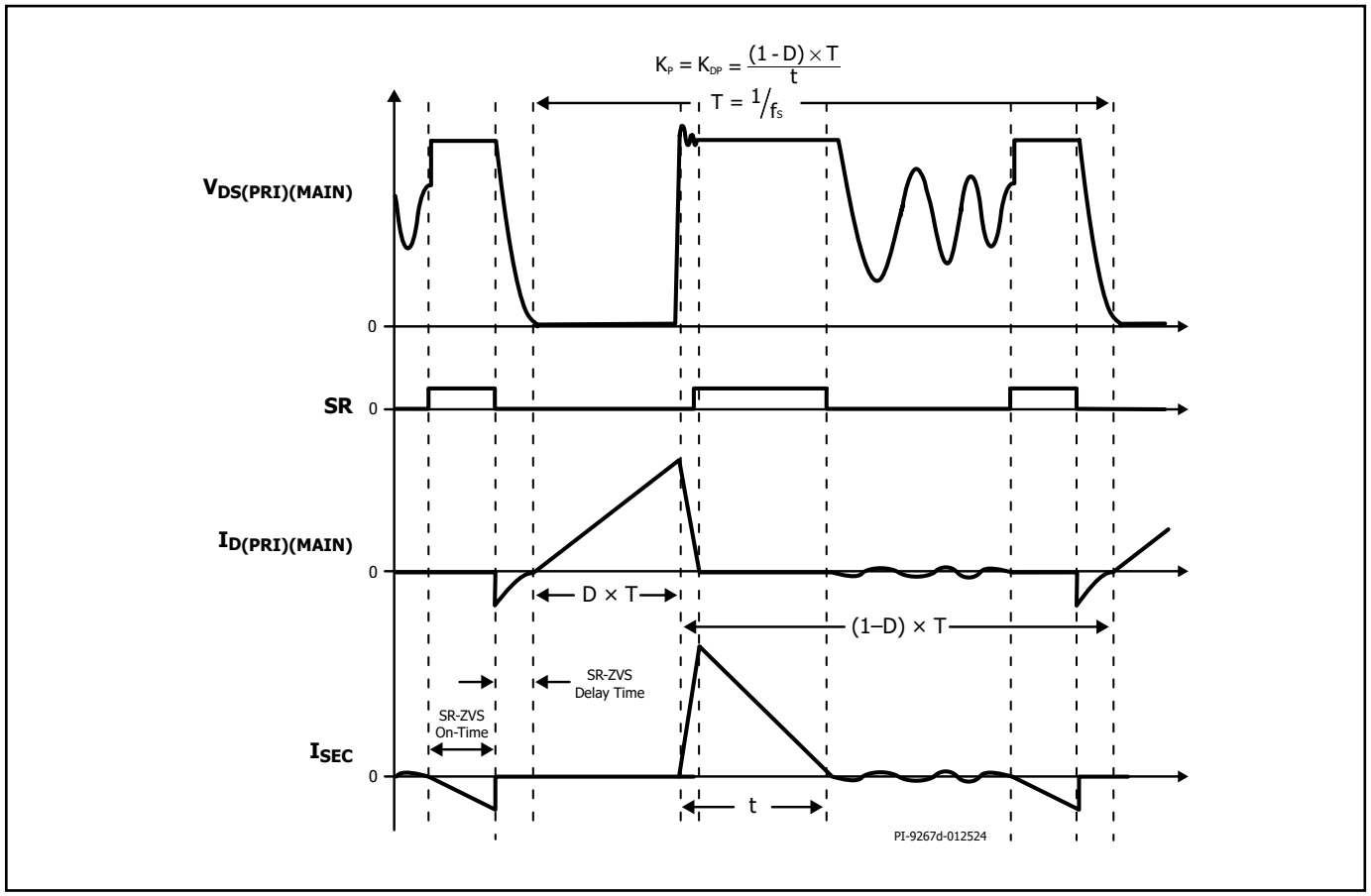


Figure 36. Discontinuous Conduction Mode Current Waveform at High-Line, $K_P > 1$. SR-ZVS On and Delay Times are Included in the Primary Off Duration.

Primary Layers, L
Primary layers should be in the range of 1 ≤ L ≤ 3 and in general should be the lowest number that meets the primary current density limit (CMA). A value of ≥200 Cmils / Amp can be used as a starting point for most designs. Higher values may be required due to thermal constraints. It is recommended to minimize leakage inductance to reduce primary switch voltage stress. Designs with more than 3 layers are possible, but the increased leakage inductance and the physical fit of the windings within the bobbin might be constraining factors that need be carefully considered.

Maximum Operating Flux Density, B_M (gauss)
A maximum value of 3800 gauss at the peak device current limit (at 180 kHz) is recommended to limit the peak flux density during worst-case output transient and output short-circuit conditions. Under these conditions the output voltage is low and little reset of the transformer occurs during the switch off-time. This allows transformer flux density to staircase beyond the normal operating level. A value of 3800 gauss at the peak current limit of the selected device together with the built-in protection features of InnoSwitch5-Pro IC provide sufficient margin to prevent core saturation under start-up or output short circuit conditions.

Transformer Primary Inductance, (LP)
Once the lowest operating input voltage, switching frequency at full load, and required V_{OR} are determined, the transformers primary inductance can be calculated. The PIXIs design spreadsheet can be used to assist in designing the transformer.

Quick Design Checklist

As with any power supply, the operation of all InnoSwitch5-Pro designs should be verified on the bench to make sure that component limits are not exceeded under worst-case conditions.

As a minimum, the following tests are strongly recommended:
1. Maximum Drain Voltage – Verify that V_{DS} of InnoSwitch5-Pro IC and SR FET do not exceed 90% of breakdown voltages at the highest input voltage and peak (overload) output power in normal operation and during start-up.
2. Maximum Drain Current – At maximum ambient temperature, maximum input voltage and peak output (overload) power. Review drain current waveforms for any signs of transformer saturation or excessive leading-edge current spikes at start-up. Repeat tests under steady-state conditions and verify that the leading edge current spike is below $I_{LIMIT(MIN)}$ at the end of $t_{LEB(MIN)}$. Under all conditions, the maximum drain current for the primary switch should be below the specified absolute maximum ratings.
3. Thermal Check – At specified maximum output power, minimum input voltage and maximum ambient temperature, verify that temperature specification limits for InnoSwitch5-Pro IC, transformer, output SR FET, and output capacitors are not exceeded. Enough thermal margin should be allowed for part-to-part variation of the $R_{DS(ON)}$ of the InnoSwitch5-Pro IC.
4. Under low-line, maximum power, a maximum InnoSwitch5-Pro SOURCE pin temperature of 110 °C is recommended to allow for these variation.

Design Considerations When Using PowiGaN Devices

For a flyback converter configuration, typical voltage waveform at the DRAIN pin of the IC is shown in Figure 37.

V_{OR} is the reflected output voltage across the primary winding when the secondary is conducting. V_{BUS} is the DC voltage connected to one end of the transformer primary winding. The peak drain voltage of the primary switch is the total of V_{BUS} and V_{OR}. V_{OR} and the clamp voltage V_{CLM} should be selected such that the peak drain voltage is lower than 650 V for all normal operating conditions. This provides sufficient margin to ensure that occasional increase in voltage during line transients such as line surges will maintain the peak drain voltage well below 750 V under abnormal transient operating conditions. This ensures excellent long-term reliability and design margin.

To make full use of ZVS capability and ensure flattest efficiency over line/load, set reflected output voltage (V_{OR}) to maintain K_P = 0.7 at minimum input voltage for universal input and K_P ≥ 1 for high-line-only conditions.

Consider the following for design optimization:
1. Higher V_{OR} allows increased power delivery at V_{MIN}, which minimizes the value of the input capacitor and maximizes power delivery from a given PowiGaN device.
2. Higher V_{OR} reduces the voltage stress on the output diodes and SR FETs.

Higher V_{OR} increases peak and RMS current on the secondary-side which may increase secondary-side copper and diode losses.

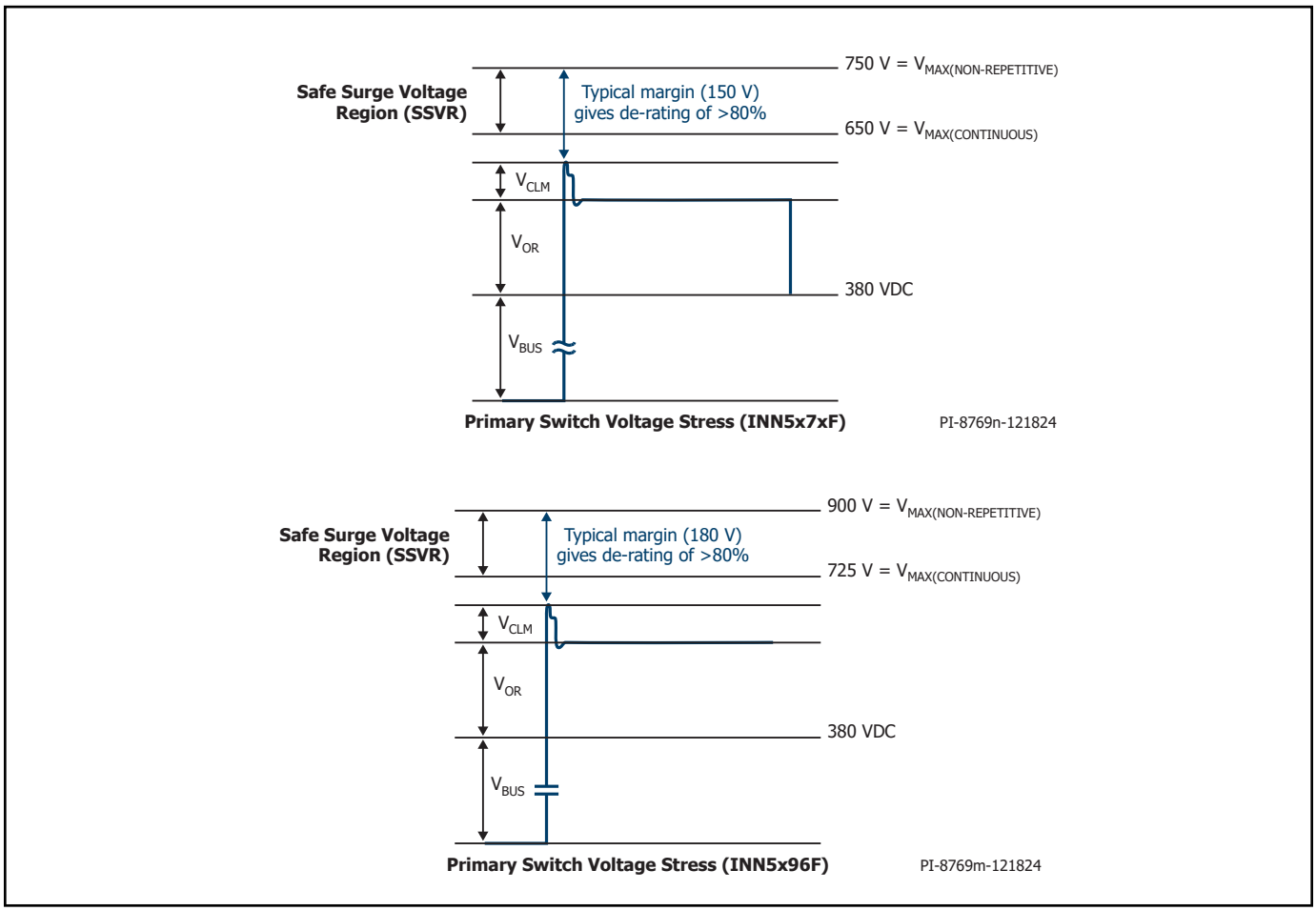


Figure 37. Peak Drain Voltage for 264 VAC Input Voltage.

There are some exceptions to this. For very high output currents the V_{OR} should be reduced to get the highest efficiency. For output voltages above 15 V, V_{OR} should be maintained higher to maintain an acceptable PIV across the output synchronous rectifier. V_{OR} choice will affect operating efficiency and should be selected carefully.

Table 14 shows the typical range of V_{OR} for optimal performance:

Output Voltage	Optimal Range for V_{OR}
5 V	45-70
12 V	80-120
15 V	100-135
20 V	120-160
28 V	135-180

Table 14. Recommended V_{OR} for Optimal Performance.

Absolute Maximum Ratings[1,2]

DRAIN Pin Voltage[6]: PowiGaN device INN537xF..... -0.3 V to 750 V
PowiGaN device INN547xF..... -0.3 V to 750 V
PowiGaN device INN5x96F..... -0.3 V to 900 V[9]
DRAIN Pin Peak Current: PowiGaN device INN5x75F..... 14 A[7]
PowiGaN device INN5x76F..... 19 A[7]
PowiGaN device INN5x77F..... 26 A[7]
PowiGaN device INN5396F ..... 19 A[7]
PowiGaN device INN5496F ..... 19 A[7]
BPP/BPS Pin Voltage ..... -0.3 to 6 V
BPP/BPS Pin Current ..... 100 mA
SCL, SDA, uVCC Pin Voltage ..... -0.3 to 6 V
uVCC Pin Current[5] ..... 12 mA
FWD Pin Voltage ..... -1.5 V to 150 V
SR Pin Voltage ..... -0.3 V to 6 V
V Pin Voltage ..... -0.3 V to 650 V
VOUT Pin Voltage ..... -0.3 V to 34 V
VB/D Pin Current ..... 50 mA
VB/D Pin Voltage ..... -0.3 V to 40 V
IS Pin Voltage ..... -0.3 V to 0.3 V[8]
Storage Temperature ..... -65 to 150 °C
Operating Junction Temperature[3] ..... -40 to 150 °C
Ambient Temperature ..... -40 to 105 °C
Lead Temperature[4] ..... 260 °C

Notes:
1. All voltages referenced to SOURCE and Secondary GROUND, T_A = 25 °C.
2. Maximum ratings specified may be applied one at a time without causing permanent damage to the product. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect product reliability.
3. Normally limited by internal circuitry.
4. 1/16" from case for 5 seconds.
5. Only at 5 V output, the uVCC pin can supply 40 mA maximum current for 0.5 seconds.
6. PowiGaN devices: INN5x7xF
   Maximum drain voltage (non-repetitive pulse); for derating calculation ..... 0.3 V to 750 V.
   Maximum continuous drain voltage ..... 0.3 V to 650 V.
7. Please refer to Figure 42 for maximum allowable voltage and current combinations.
8. Absolute maximum voltage for less that 500 µs is 3 V.
9. PowiGaN devices: INN5x96F
   Maximum continuous drain voltage ..... -0.3 to 725 V.
   Maximum drain voltage (non repetitive pulse) ..... -0.3 to 900 V.

Thermal Resistance

Thermal Resistance: INN5x75F
(θ_{JA}) ..... 70 °C/W[2], 64 °C/W[3]
(θ_{JC}) ..... 21 °C/W[1]
INN5x77F
(θ_{JA}) ..... 55 °C/W[2], 51 °C/W[3]
(θ_{JC}) ..... 16 °C/W[1]
INN5x96F
(θ_{JA}) ..... 71 °C/W[2], 66 °C/W[3]
(θ_{JC}) ..... 25 °C/W[1]

Notes:
1. The case temperature is measured on the top of the package.
2. Soldered to 0.36 sq. inch (232 mm2), 2 oz. (610 g/m2) copper clad.
3. Soldered to 1.0 sq. inch (645 mm2), 2 oz. (610 g/m2) copper clad.

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Functions							
Start-Up Switching Frequency	f_{SW}	T_J = 25 °C			25	27	kHz
Jitter Modulation Frequency	f_M	T_J = 25 °C, f_{SW} = 100 kHz			1.25		kHz
Maximum On-Time	$t_{ON(MAX)}$	T_J = 25 °C			16.5		µs
BPP Supply Current	I_{S1}	V_{BPP} = V_{BPP} + 0.1 V (Switch not Switching) T_J = 25 °C			300	460	µA
	I_{S2}	V_{BPP} = V_{BPP} + 0.1 V (Switch Switching at 180 kHz) T_J = 25 °C	INN5375F		3.2	3.7	mA
			INN5376F		4.29	5.15	
			INN5377F		4.3	5.16	
			INN5396F		4.38	5.27	
			INN5475F		2.96	3.55	
			INN5476F		4.2	5.04	
			INN5477F		4.29	5.15	
			INN5496F		4.36	5.25	
BPP Pin Charge Current	I_{CH1}	V_{BP} = 0 V, T_J = 25 °C			-1.35		mA
	I_{CH2}	V_{BP} = 4 V, T_J = 25 °C			-4.65		
BPP Pin Voltage	V_{BPP}	T_J = 25 °C		4.8	5.00	5.16	V
BPP Pin Voltage Hysteresis	$V_{BPP(H)}$	T_J = 25 °C			0.5		V
BPP Shunt Voltage	V_{SHUNT}	I_{BPP} = 2 mA T_J = 25 °C		5.16	5.36	5.7	V
UV/OV Pin Brown-In Threshold	I_{UV+}	T_J = 25 °C		23.1	25.2	27.5	µA
UV/OV Pin Brown-Out Threshold	I_{UV-}	T_J = 25 °C		20.5	23	25	µA
Brown-Out Delay Time	t_{UV-}	T_J = 25 °C			35		ms
UV/OV Pin Line Overvoltage Threshold	I_{OV+}	T_J = 25 °C		106	115	118	µA
UV/OV Pin Line Overvoltage Hysteresis	$I_{OV(H)}$	T_J = 25 °C			8		µA
UV/OV Pin Line Overvoltage Recovery Threshold	I_{OV-}	T_J = 25 °C		100	107		µA
Line Fault Protection							
VOLTAGE Pin Line Overvoltage Deglitch Filter	t_{OV+}	T_J = 25 °C See Note B			3		µs

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Circuit Protection							
Standard Current Limit (BPP) Capacitor = 0.47 µF	I_{LIMIT} (Switching at 100 kHz)	di/dt = 500 mA/µs T_J = 25 °C	INN5375F	2139	2300	2461	mA
		di/dt = 660 mA/µs T_J = 25 °C	INN5376F	2697	2900	3103	
		di/dt = 770 mA/µs T_J = 25 °C	INN5377F	3162	3400	3638	
		di/dt = 660 mA/µs T_J = 25 °C	INN5396F	2705	2900	3105	
		di/dt = 1300 mA/µs T_J = 25 °C	INN5475F	3534	3800	4066	
		di/dt = 1600 mA/µs T_J = 25 °C	INN5476F	3906	4200	4494	
		di/dt = 1700 mA/µs T_J = 25 °C	INN5477F	4278	4600	4922	
		di/dt = 1600 mA/µs T_J = 25 °C	INN5496F	3920	4200	4495	
Increased Current Limit (BPP) Capacitor = 4.7 µF	$I_{LIMIT+1}$ (Switching at 100 kHz)	di/dt = 500 mA/µs T_J = 25 °C	INN5375F	2374	2580	2786	mA
		di/dt = 660 mA/µs T_J = 25 °C	INN5376F	2990	3250	3510	
		di/dt = 770 mA/µs T_J = 25 °C	INN5377F	3505	3810	4115	
		di/dt = 660 mA/µs T_J = 25 °C	INN5396F	3005	3250	3510	
		di/dt = 1300 mA/µs T_J = 25 °C	INN5475F	3919	4260	4601	
		di/dt = 1600 mA/µs T_J = 25 °C	INN5476F	4324	4700	5076	
		di/dt = 1700 mA/µs T_J = 25 °C	INN5477F	4738	5150	5562	
		di/dt = 1600 mA/µs T_J = 25 °C	INN5496F	4350	4.7	5077	
Overload Detection Frequency	f_{OVL}	T_J = 25 °C		148	155	161	kHz
BYPASS Pin Latching Shutdown Threshold Current	I_{SD}	T_J = 25 °C		6.0	7.5		mA
Auto-Restart On-Time	t_{AR}	T_J = 25 °C			82		ms
Auto-Restart Trigger Skip Time	$t_{AR(SK)}$	T_J = 25 °C See Note A			1.3		sec
Auto-Restart Off-Time	$t_{AR(OFF)}$	T_J = 25 °C			2.00		sec
Short Auto-Restart Off-Time	$t_{AR(OFF)SH}$	T_J = 25 °C			0.20		sec

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Output							
ON-State Resistance	$R_{DS(ON)}$	INN5375F $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.29	0.39	Ω
			T_J = 100 °C		0.41	0.54	
		INN5376F $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.18	0.28	
			T_J = 100 °C		0.27	0.37	
		INN5377F $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.145	0.21	
			T_J = 100 °C		0.23	0.29	
		INN5396F $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.21	0.33	
			T_J = 100 °C		0.32	0.44	
		INN5475F $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.29	0.39	
			T_J = 100 °C		0.41	0.54	
		INN5476F $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.18	0.28	
			T_J = 100 °C		0.27	0.37	
		INN5477F $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.145	0.21	
			T_J = 100 °C		0.23	0.29	
		INN5496F $I_D = I_{LIMIT+1}$	T_J = 25 °C		0.21	0.33	
			T_J = 100 °C		0.32	0.44	
OFF-State Drain Leakage Current	I_{DSS1}	$V_{BPP} = V_{BPP}$ + 0.1 V V_{DS} = 80% Peak Drain Voltage T_J = 125 °C				200	µA
	I_{DSS2}	$V_{BPP} = V_{BPP}$ + 0.1 V V_{DS} = 325 V T_J = 25 °C			15		µA
Drain Supply Voltage		See Note B		30			V
Thermal Shutdown	T_{SD}	See Note A		135	142	150	°C
Thermal Shutdown Hysteresis	$T_{SD(H)}$	See Note A			70		°C

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
Secondary						
Maximum Secondary Frequency	f_{SREQ}	T_J = 25 °C	164	180		kHz
Minimum Off-time	$t_{OFF(MIN)}$	C_{LOAD} = 5 nF with SR enabled		1.9	2.2	µs
Start-Up VOUT Pin Regulation Voltage	$VOUT_{REG}$	T_J = 25 °C	4.85	5	5.15	V
Output Voltage Programming Range	$V_{OUT(R)}$	Default = 5 V	3.00		30	V
	TOL_{VOUT}	Tolerance T_J = 25 °C	-3		+3	%
Output Voltage Step Size	ΔV_{OUT}	T_J = 25 °C		10		mW
Report-Back Output Voltage Tolerance	$V_{OUT(T)}$	T_J = 25 °C	-3		+3	%
Normalized Output Current	I_{OUT}	0.6 - 1.0 T_J = 25 °C, See Note C	-5		+5	%
		0.2 T_J = 25 °C, See Note C	-15		+15	
Normalized Output Current Step Size	ΔI_{OUT}	T_J = 25 °		0.52		%
Maximum V/I Update Rate	t_{VI}	See Note B		10		ms
Minimum Time Delay Between I²C Commands	t_{DELAY}	See Note B	150			µs
Internal Current Limit Voltage Threshold	$I_{SV(TH)}$	T_J = 25 °C Across External IS to GND Pin Resistor See Note F		32		mV
Cable Drop Compensation (CDC) Programming Range	φ_{CD}	T_J = 25 °C Default = 0 V	0		600	mV
CDC Tolerance	$TOL\varphi_{CD}$	CDC ≥ 100 mV T_J = 25 °C	-35		+35	mV
CDC Programming Step Size	$\Delta\varphi_{CD}$	T_J = 25 °C		50		mV
Output Overvoltage Programming Range	V_{OVA}	Default = 6.2 V	3.3		40	V
Output Overvoltage Tolerance	TOL_{OVA}	T_J = 25 °C	-3		+3	%
Output Overvoltage Programming Step Size	ΔV_{OVA}			100		mV
Output Undervoltage Programming Range	V_{UVA}	Default = 3.6 V	2.7		40	V
Output Undervoltage Tolerance	TOL_{UVA}	T_J = 25 °C	-3		+3	%

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Secondary (cont.)							
Output Undervoltage Programming Step Size	ΔV_{UVA}				100		mV
Output Undervoltage Timer Programming Options	t_{UVL}	T_J = 25 °C See Notes B, E	Programming Option 1		8		ms
			Programming Option 2		16		
			Programming Option 3		32		
			Default Programming Option 4		64		
Constant Output Power Onset Threshold Programming Range	V_{KP}	Default = 30 V		5.3		30	V
Constant Output Power Tolerance	$TOLP_{OUT}$	At 85% of Full Scale Current		-10		+10	%
Constant Output Power Onset Threshold Programming Step Size	ΔV_{KP}				100		mV
Constant Voltage Mode Timer Programming Options	t_{CVO}	T_J = 25 °C See Notes B, E	Programming Option 1		8		ms
			Programming Option 2		16		
			Programming Option 3		32		
			Programming Option 4		64		
Watchdog Timer	t_{WDT}	Default Programming Option 1 See Note B			0.5		sec
		Programming Option 2, See Note B			1		
		Programming Option 3, See Note B			2		
VB/D Drive Voltage	$V_{VB/D}$	With Respect to VOUT Pin		4	7		V
VB/D Pin Internal Current Discharge	$I_{B/D(DS)}$			50			mA
Secondary Over-Temperature Hysteresis	$T_{SEC(HYS)}$	Programming Option 1 See Note B			40		°C
		Programming Option 2 See Note B			60		
VOUT Pin Bleeder Current	IVO_{BLD}	VOUT = 5 V			270		mA
uVCC Supply Voltage	uVCC	V_{OUT} = 5 V, 10 mA < I_{UVCC} ≤ 40 mA, T_J = 25 °C, See Note 5 in Absolute Maximum Ratings Table		3.42	3.6	3.78	V
		V_{OUT} ≥ 3.9 V I_{uVCC} ≤ 10 mA T_J = 25 °C		3.42	3.6	3.78	

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
Secondary (cont.)						
uVCC Pin Output Resistance	R_{uVCC}	T_J = 25 °C			20	Ω
uVCC Reset Voltage Threshold	$uVCC_{RST}$	See Note A		2.5	2.65	V
BPS Pin Voltage	V_{BPS}		4.3	4.5		V
BPS Pin Current	I_{SNL}	T_J = 25 °C VBUS Switch Open		0.7	0.980	mA
		T_J = 25 °C VBUS Switch Closed		1	1.550	
BPS Pin Current	I_{S3}	F_{SW} = 180 kHz T_J = 25°C	7	8.2	9.5	mA
BPS Pin Undervoltage Threshold	$V_{BPS(UVLO)TH}$			3.8	4.0	V
BPS Pin Undervoltage Hysteresis	$V_{BPS(UVLO)H}$			0.7		V
FORWARD Pin Breakdown Voltage	BV_{FWD}		150			V
Synchronous Rectifier @ T_J = 25 °C						
SR Pin Drive Voltage	V_{SR}			4.5		V
SR Pin Voltage Threshold	$V_{SR(TH)}$			-3		mV
Rise Time	$t_{R(SR)}$	T_J = 25 °C C_{LOAD} = 2nF See Note B 10-90%		50		ns
Fall Time	$t_{F(SR)}$	T_J = 25 °C C_{LOAD} = 2nF See Note B 90-10%		30		ns
Output Pull-Up Resistance	R_{PU}	T_J = 25 °C V_{BPS} + 0.1 V I_{SR} = 30 mA		8.9	11.5	
Output Pull-Down Resistance	R_{PD}	T_J = 25 °C V_{BPS} + 0.2 V I_{SR} = 30 mA		4.7	5	

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
I²C Bus Specifications (SDA and SCL Pins) *See Note B						
SCL Clock Frequency	f_{SCL}	See Note G	50	400	535	kHz
Low-level Input Voltage	V_{IL}		-0.5		0.3 × uVCC	V
High-level Input Voltage	V_{IH}		0.7 × uVCC		uVCC + 0.5 V	V
Hysteresis of Schmitt Trigger Inputs	V_{HYS}		0.05 × uVCC			V
Low-Level Output Voltage (Open Drain or Collector)	V_{OL}	uVCC >2.8 V 3 mA Sink Current	0		0.4	V
Low-level Output Current	I_{OL}		3			mA
Output Fall-Time from $V_{IH(MIN)}$ to $V_{IL(MAX)}$	t_{OF}	Bus Capacitance from 10 pF to 400 pF	-		250	ns
SDA/SCL Input Current	I_I	(0.1 × uVCC) < (V_{SCL}/V_{SDA}) < (0.9 × uVCC)	-1		1	µA
SDA/SCL Capacitance	C_I		-		10	pF
Pulse Width of Spike Suppressed by Input Filter	t_{SP}		50			ns
High Period for SCL Clock	t_{HIGH}	f_{SCL} = 400 kHz	0.6			µs
Low Period for SCL Clock	t_{LOW}	f_{SCL} = 400 kHz	1.3			µs
Serial Data Set-up Time	$t_{SU:DAT}$		100			ns
Serial Data Hold time	$t_{HD:DAT}$		0			sec
Valid Data Time	$t_{VD:DAT}$	SCL Low to SDA Output Valid			0.9	µs
Valid Data Time for ACK	$t_{VD:ACK}$	ACK from SCL Low to SDA Low			0.9	µs
I²C Bus Free Time Between Start and Stop	t_{BUF}		1.3			µs
I²C Fall Time (Both SCL and SDA)	t_{fCL}				300	ns
I²C Rise Time (Both SCL and SDA)	t_{rCL}				300	ns
I²C Start or Repeated Start Condition Set-up Time	$t_{SU:STA}$		0.6			µs
I²C Start or Repeated Start Condition Hold Time	$t_{HD:STA}$		0.6			µs

Parameter	Symbol	Conditions SOURCE = 0 V T_J = -40 °C to 125 °C (Unless Otherwise Specified)	Min	Typ	Max	Units
I²C Bus Specifications (SDA and SCL Pins) *See Note B						
I²C Stop Condition Set-up Time	$t_{SU:STO}$		0.6			µs
Capacitive Load	C_B				400	pF
Noise Margin at the Low Level	V_{NL}		0.1 × uVCC			V
Noise Margin at the High Level	V_{NH}		0.1 × uVCC			V
SCL Pin Interrupt Timer	$t_{INT(SCL)}$	T_J = 25 °C		50		µs

A. This parameter is derived from characterization.
B. This parameter is guaranteed by design.
C. Use 1% tolerance resistor.
D. To ensure correct current limit it is recommended that nominal 0.47 µF / 4.7 µF capacitors are used. In addition, the BPP capacitor value tolerance should be equal or better than indicated below across the ambient temperature range of the target application. The minimum and maximum capacitor values are guaranteed by characterization.

Nominal BPP Pin Capacitor Value	BPP Capacitor Value Tolerance	
	Minimum	Maximum
0.47 µF	-60%	+100%
4.7 µF	-50%	N/A

Recommended to use at least 10 V / 0805 / X7R SMD MLCC.

E. Settling delay in averaging register will increase total observed time under light and no-load conditions.
F. This parameter should be used only for calculation of typical value of current sense resistor. The value programmed in CC register (0x98) regulates the output current. The tolerance is specified in the Normalized Output Current parameter (I_{OUT}).
G. Guarantee minimum low period for SCL clock of 930 ns while operating at any SCL clock frequency. This may require using asymmetrical SCL clock (reduced duty cycle) at higher frequencies.

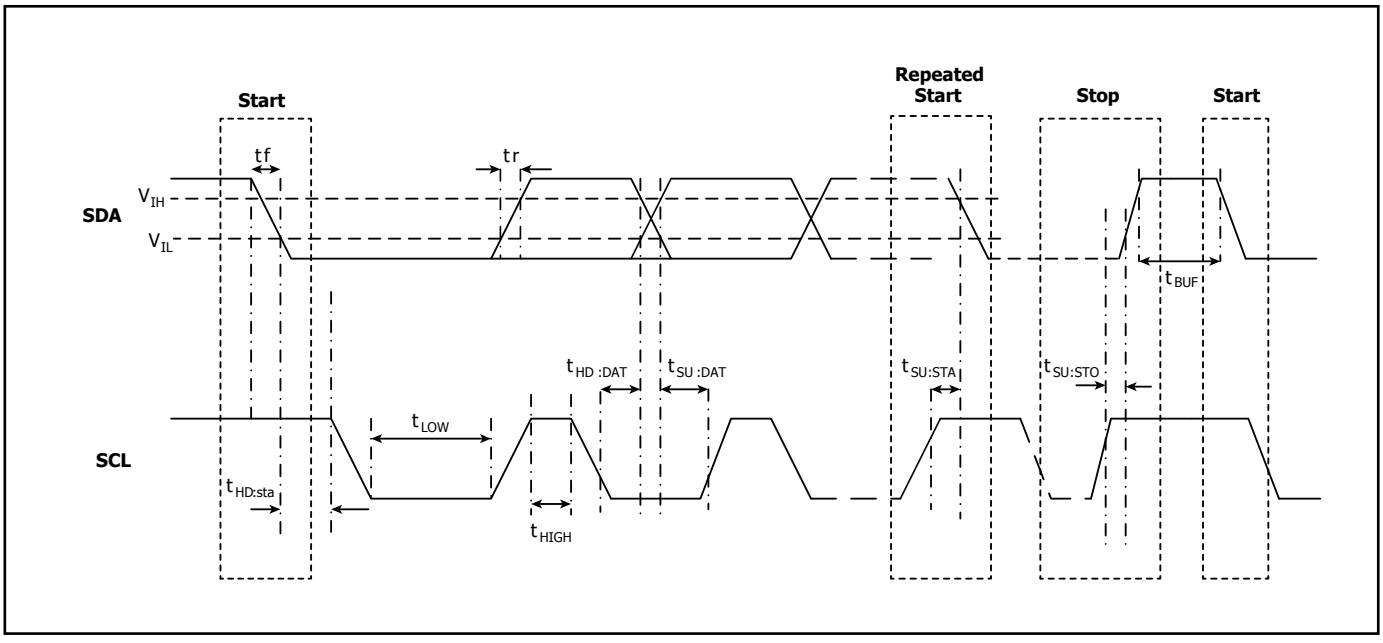


Figure 38. I²C Timing Diagram.

Typical Performance Curves

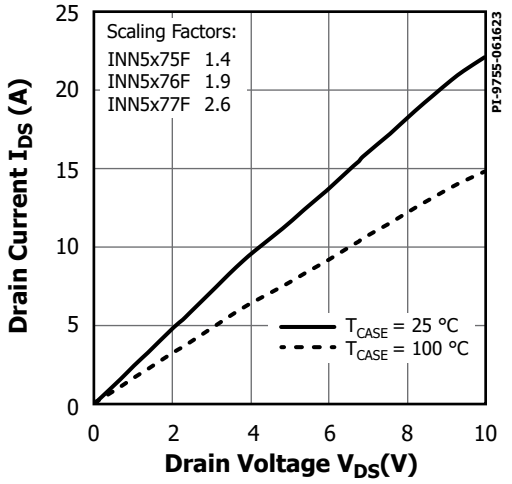


Figure 39. Output Characteristics.

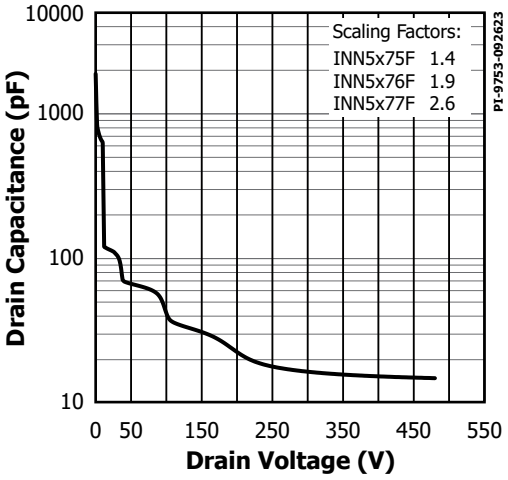


Figure 40. C_{OSS} vs. Drain Voltage.

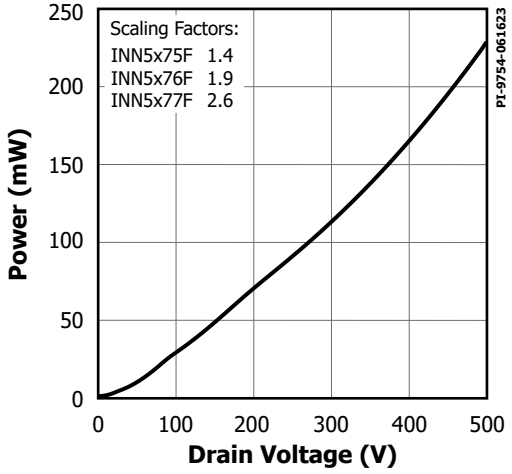


Figure 41. Drain Capacitance Power.

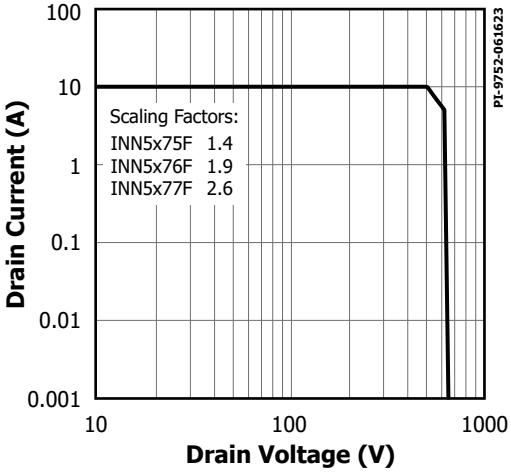


Figure 42. Maximum Allowable Drain Current vs. Drain Voltage .

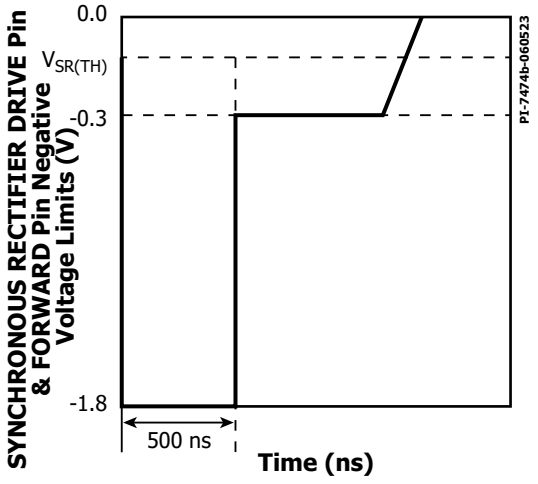


Figure 43. SYNCHRONOUS RECTIFIER DRIVE Pin Negative Voltage.

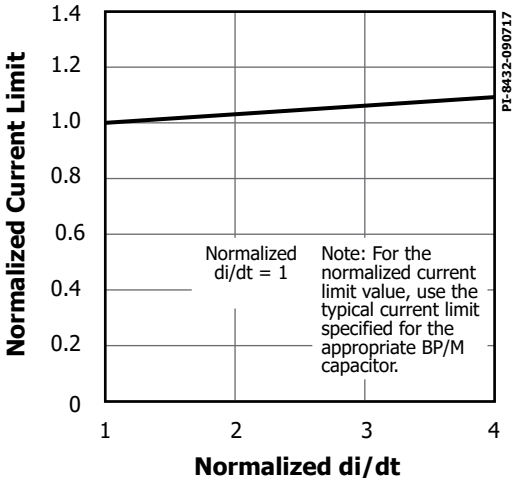


Figure 44. Standard Current Limit vs. di/dt.

Typical Performance Curves

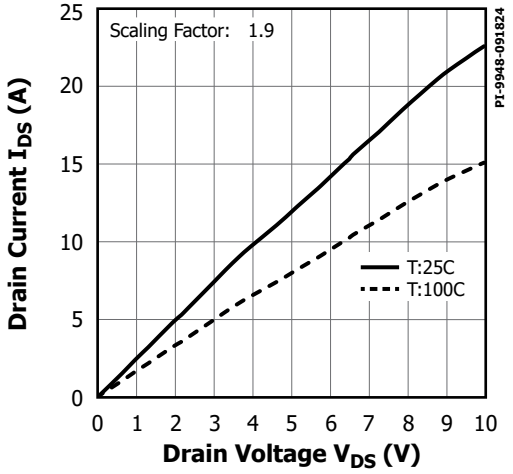


Figure 45. Output Characteristics (for INN5x96F only).

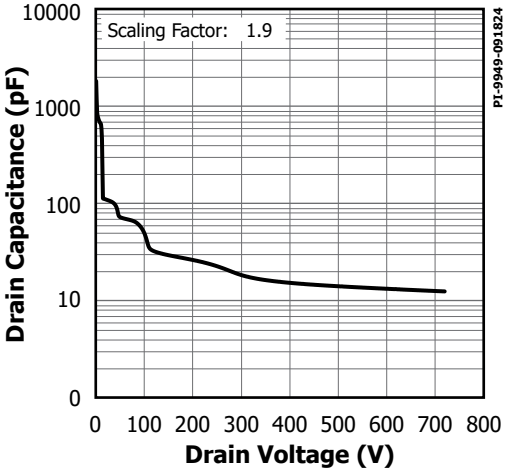


Figure 46. C_{OSS} vs. Drain Voltage (for INN5x96F only).

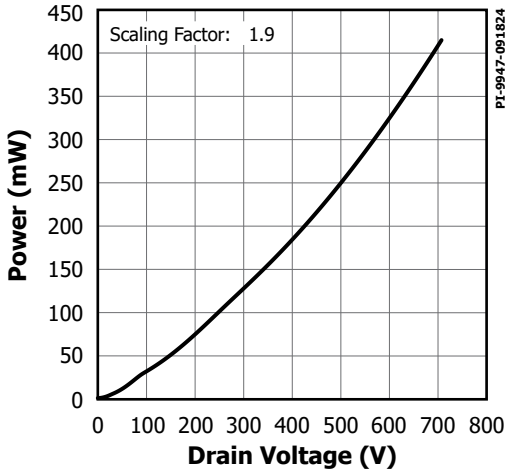


Figure 47. Drain Capacitance Power (for INN5x96F only).

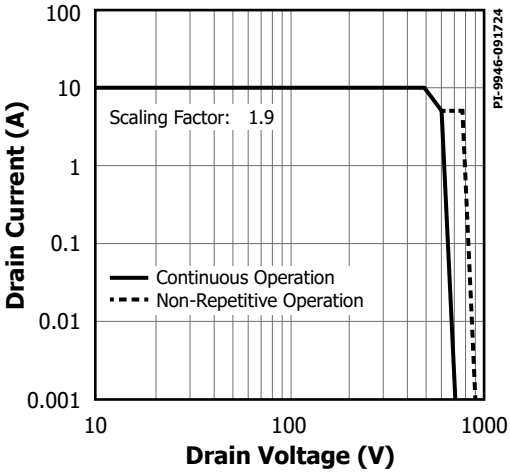
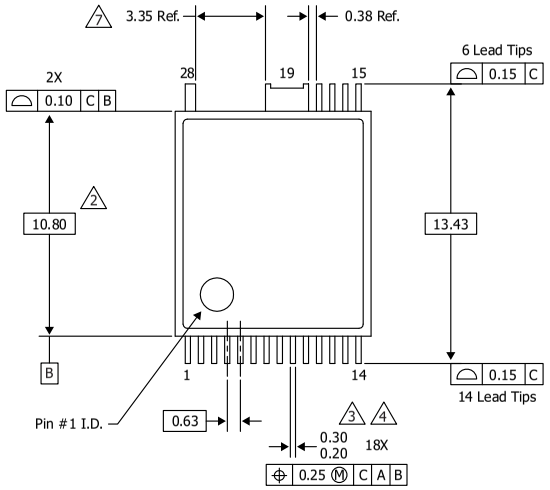
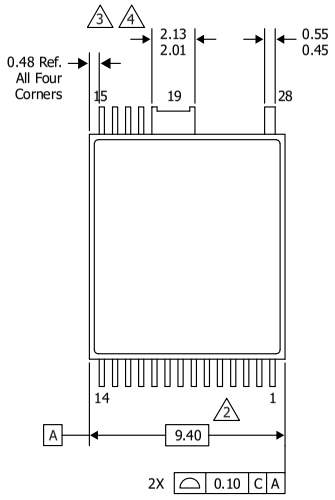


Figure 48. Maximum Allowable Drain Current vs. Drain Voltage (for INN5x96F only).

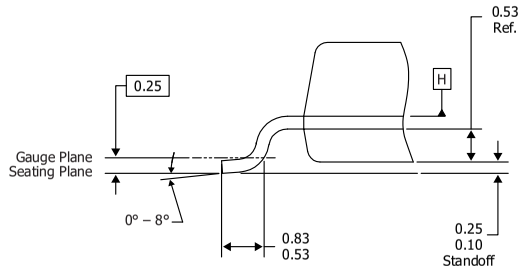
InSOP-T28D



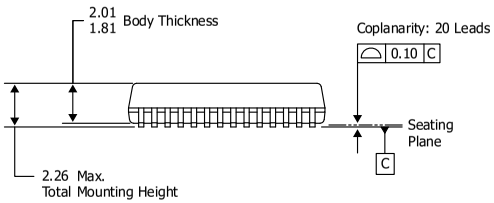
TOP VIEW



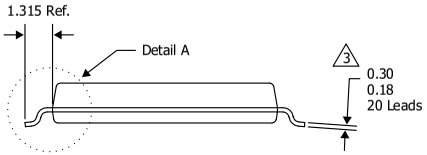
BOTTOM VIEW



DETAIL A



SIDE VIEW



END VIEW

NOTES:

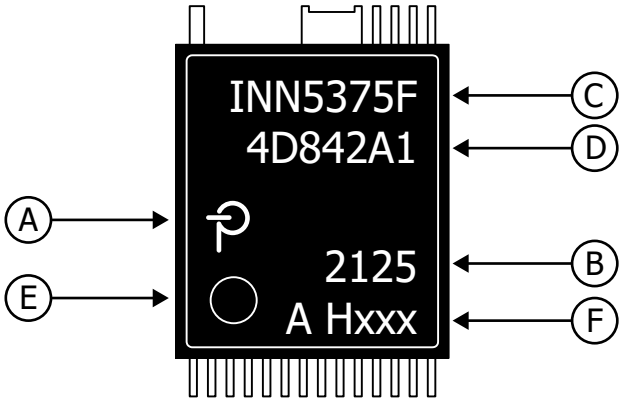
1. Dimensioning and Tolerancing per ASME Y14.5M – 1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.18 per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include inter-lead flash or protrusions.
5. Controlling dimensions in millimeters.
6. Datums A & B to be determined at Datum H.
7. This dimension is the nominal dimension between leadtips, not including plating, and not including metal protrusions. Metal-to-Metal distance (Creepage) is 3.20 mm minimum.

PI-9406-041923
POD-inSOP-T28D Rev B

POD-inSOP-T28D_B_032623

PACKAGE MARKING

InSOP-T28D



A. Power Integrations Registered Trademark
B. Assembly Date Code (last two digits of year (YY) followed by 2-digit work week (WW)
C. Product Identification (Part #/Package Type)
D. Lot Identification Code
E. Pin 1 Indicator
F. Test Lot Information and Feature Code

PI-9756-062023

Safety Certification Specifications (Safety approval pending)

Parameter	Conditions	Rating	Units
Ratings for UL1577			
Primary-Side Current Rating	Current from pin (16-19) to pin 24	1.5	A
Primary-Side Power Rating	T_{AMB} = 25 °C (Device mounted in socket resulting in T_{CASE} = 120 °C)	1.35	W
Secondary-Side Power Rating	T_{AMB} = 25 °C (Device mounted in socket)	0.125	W
Package Characteristics			
Clearance		11.4	mm (min)
Creepage		11.4	mm (min)
Distance Through Insulation (DTI)		0.4	mm (min)
Transient Isolation Voltage		6	kV (min)
Comparative Tracking Index (CTI)		>600	V

Feature Code Table

Summary Features	H901
I_{LIM} Selectable	Yes
Over-Temperature Protection	Hysteretic
Line OV/UV	Enabled
Line UV Timer (35 ms or 400 ms)	35 ms

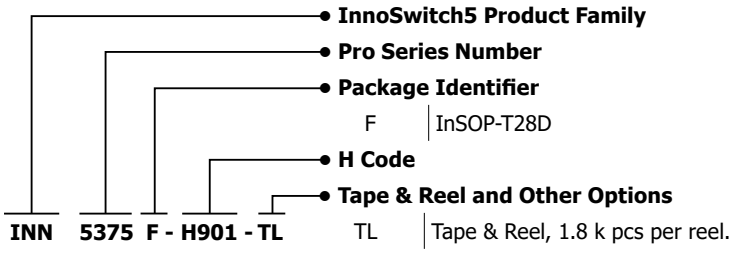
MSL Table

Part Number	MSL Rating
INN5x7xF	3
INN5x9xF	3

ESD and Latch-Up Table

Test	Conditions	Results
Latch-up at 125 °C	**JESD78D**	> ±100 mA or > 1.5 × V_{MAX} on all pins
Charge Device Model ESD	**ANSI/ESDA/JEDEC JS-002-2014**	> ±1 kV on all pins

Part Ordering Information



Revision	Notes	Date
C	Production release.	01/24
D	Updated limits and added Performance Curves for INN5396F and INN5496F parameters, updated Figure 37.	12/24

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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