Evaluation board circuit diagram and implementation <MN63Y1208>

Ver 1.3

2013/10/10

Semiconductor Business Group
Industrial Devices Company
Panasonic Corporation

List of pin placement / pins of the NFC tag

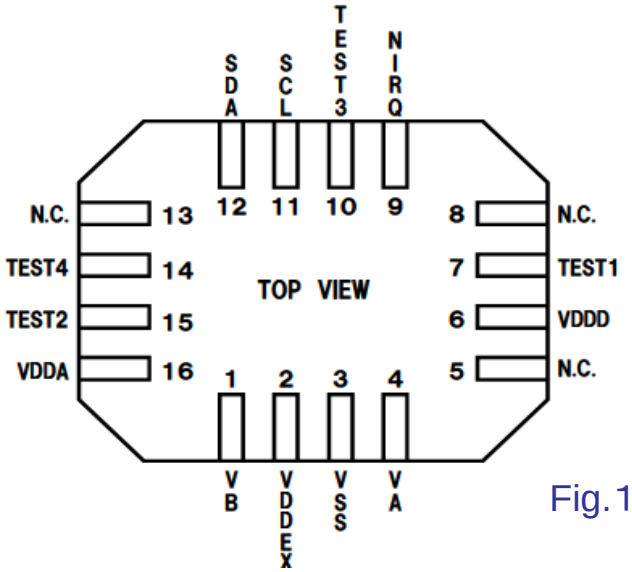


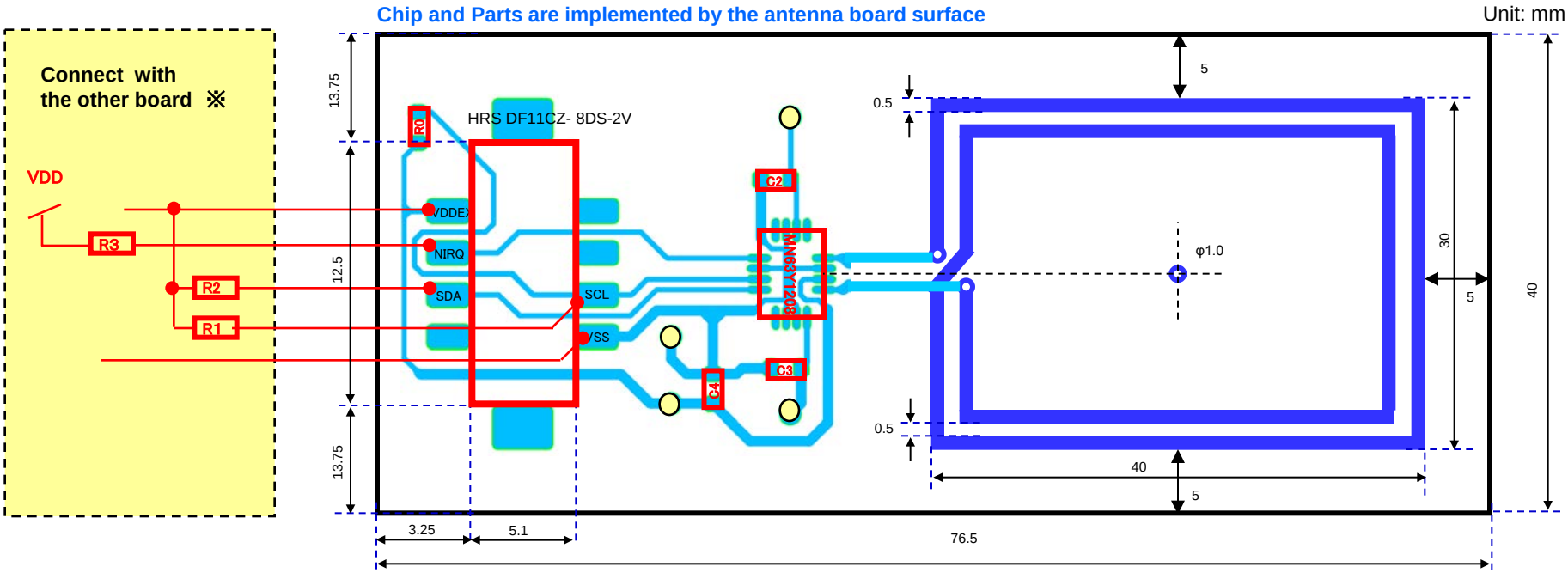
Fig.1 List of pin placement

Tab.1 Pins of the NFC tag

PIN Number	Terminal name	Input/output	Input and output type	function
1	VB	I/O	—	Coil terminal
2	VDDEX	—	Power	Power supply for contact (Input 1.7V ～ 3.6V)
3	VSS	—	GND	Ground
4	VA	I/O	—	Coil terminal
5	N.C.	—	—	Unconnected pin
6	VDDD	—	Power	Digital internal power supply (Connect capacitance between VSS)
7	TEST1	input	—	Test control (Normally connected to VSS)
8	N.C.	—	—	Unconnected pin
9	NIRQ	output	Open Drain	Interrupt request output
10	TEST3	input	—	Test control (Normally connected to VSS)
11	SCL	input	—	HOST I/F (I2C 100kHz)
12	SDA	I/O	Open Drain	HOST I/F (I2C 100kHz)
13	N.C.	—	—	Unconnected pin
14	TEST4	input	—	Test control (Normally connected to VSS)
15	TEST2	input	—	Test control (Normally connected to VSS)
16	VDDA	—	Power	Analog internal power supply (Connect capacitance between VSS)

Figure of pattern of the evaluation board

2013/10/10

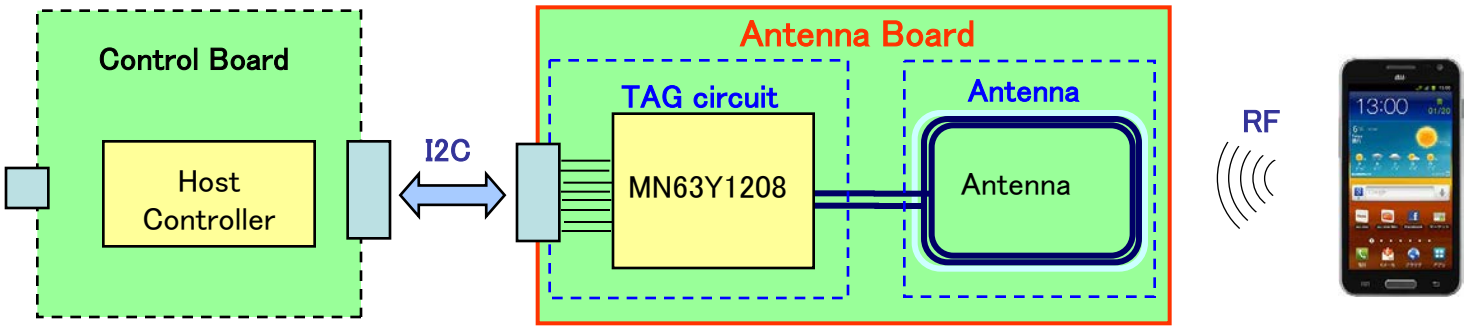


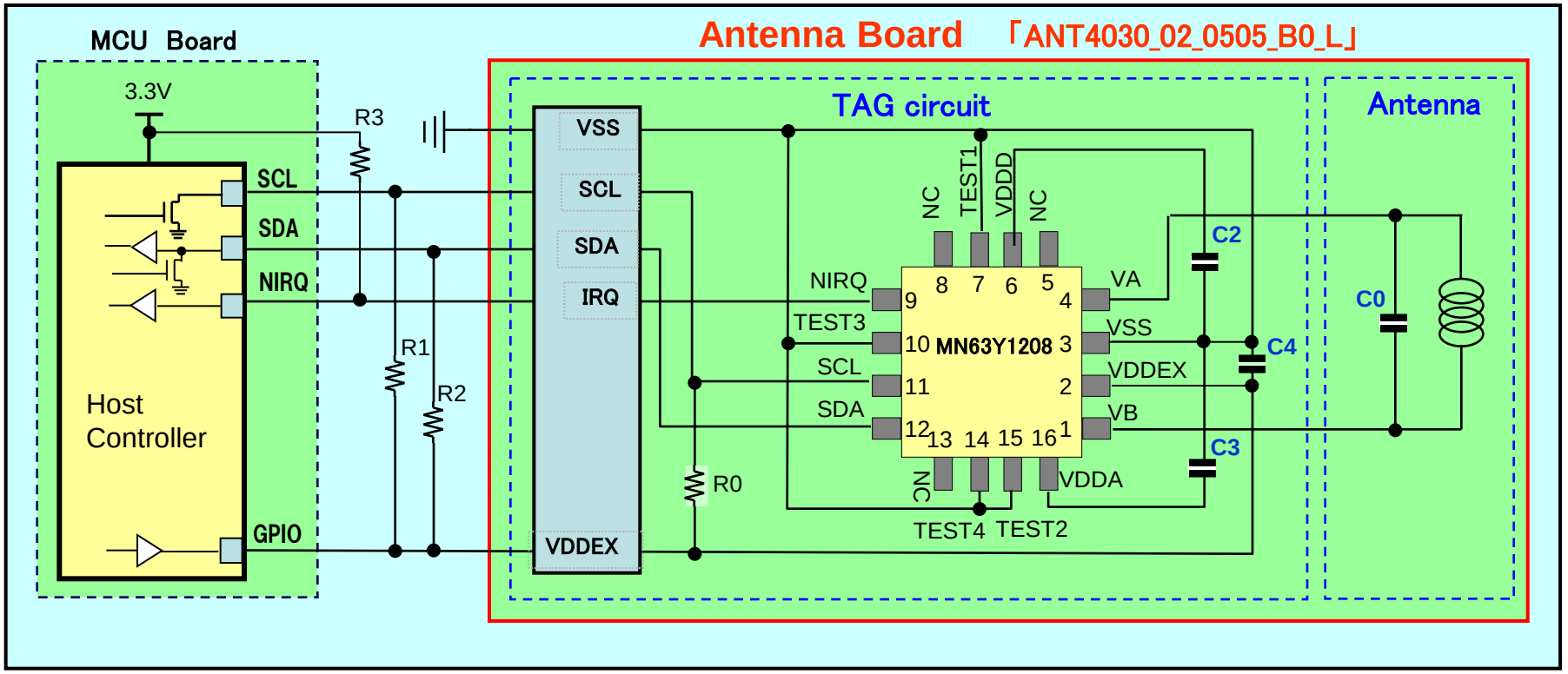
※ Substrate size may differ from the substrate which exists to a visitor.
※ I connect pulling up resistance (R,R2,R3) to the microcomputer board of our offer.

External part	Recommendation Value	Detailed explanation
R1,R2	3.3kΩ	It is pulling up resistance for I2C signal lines.Please decide the resistance level in consideration of transmission rate, wiring capacity, current ability. In our NFC tag board "ANT4030_02_0505_B0_L ," it is not implemented.
R3	3.3kΩ	It is pulling up resistance for interrupt signal lines. Please decide the resistance level in consideration of wiring capacity, current ability. In our NFC tag board "ANT4030_02_0505_B0_L ," it is not implemented.
C2、C3、C4	0.1μF	It is a fixed value at the capacity between the power supply for operation stabilization of the tag LSI. C2 is connected to VDDD, and C3 is connected to VDDA and C4 is connected to VDDEX
R0	100kΩ	It is pulling up resistance to prevent an uncertainty state of SCL causing the malfunction. When NFC tag LSI has the terms of use that R1 is not connected to, I am necessary.

Connection example with the MCU board

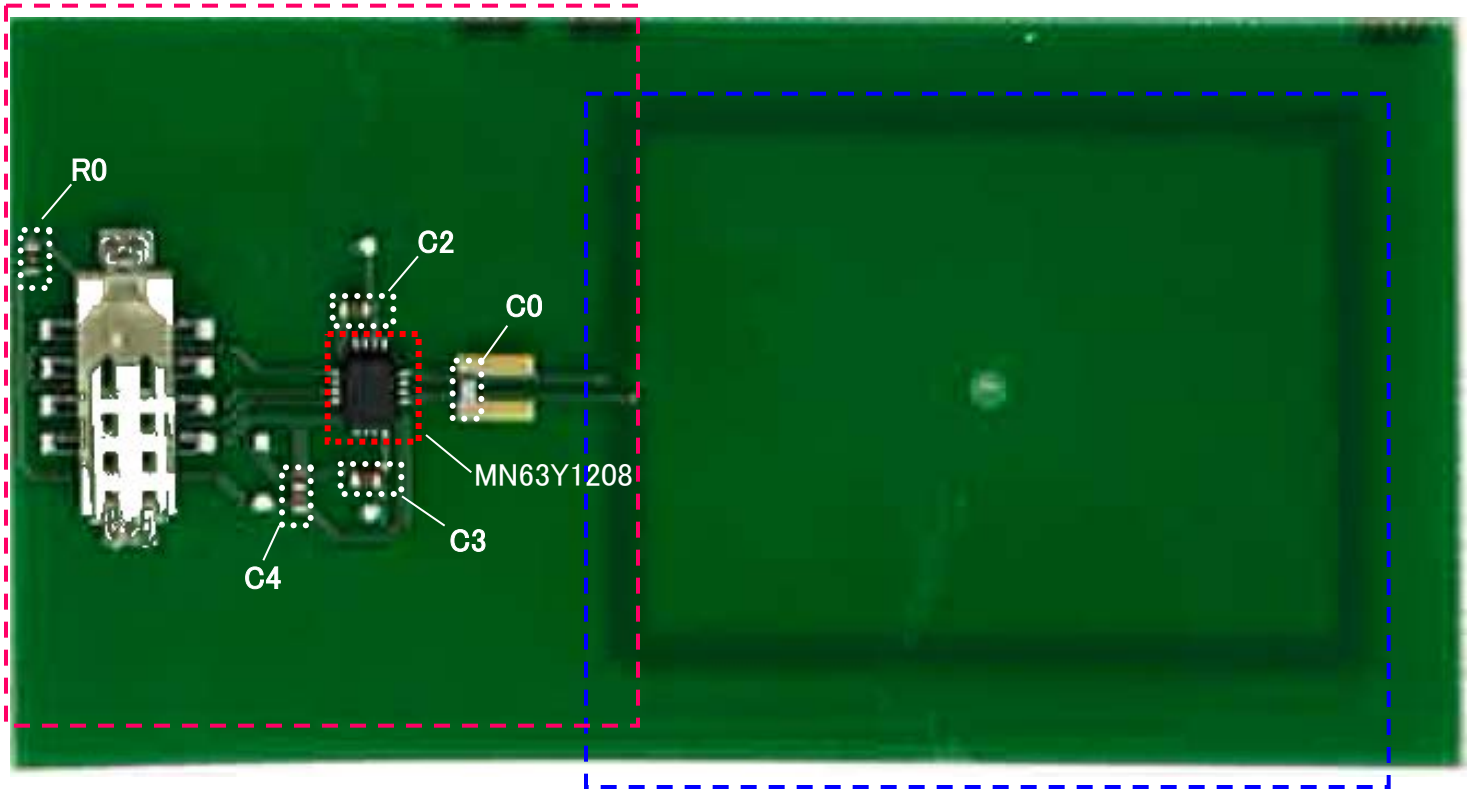
NFC tag system constitution





Implementation of the evaluation board

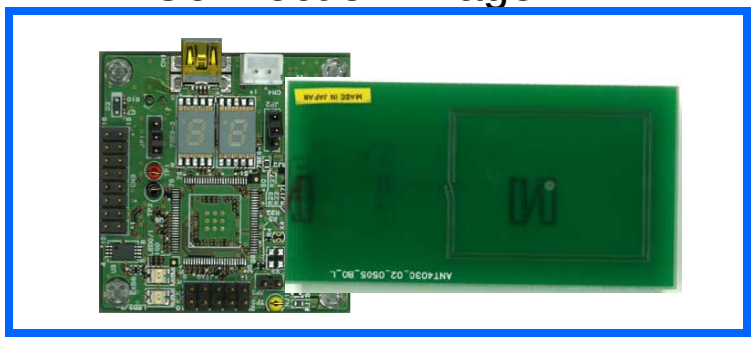
Chip and Parts are implemented by the board surface



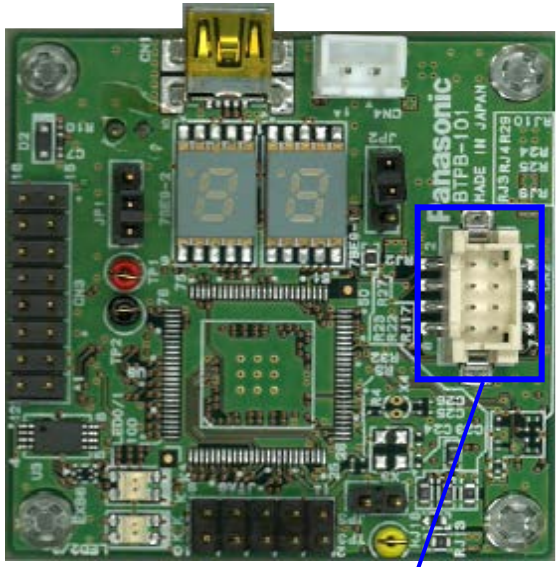
Antenna is implemented by the board back side

Connector specifications

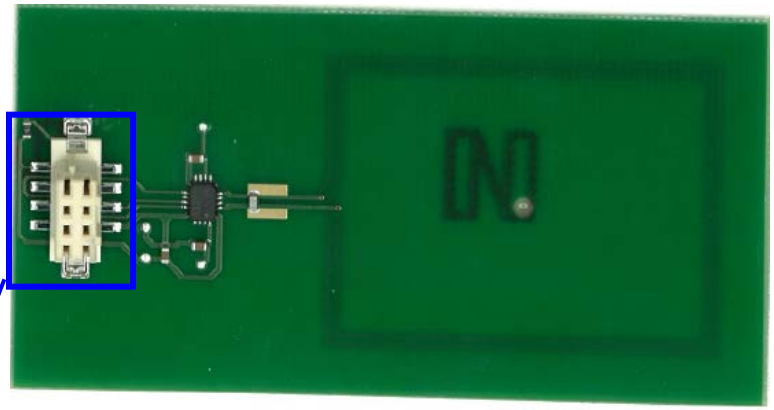
Connection image



Micon Board [BTPB101-B]



Antenna Board [ANT4030_02_0505_B0_L]



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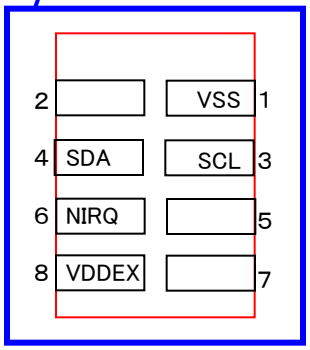
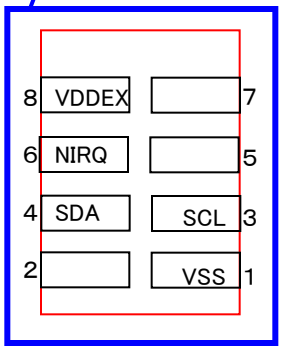
(Hirose Electric)





HRS DF11CZ- 8DS-2V
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