MOSFET - Power, N-Channel, PowerTrench® Power Clip, Symmetric Dual 30 V NTTFD2D8N03P1E

FET	$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
Q1	30 V	2.5 mΩ @ 10 V	80 A
		3.0 mΩ @ 4.5 V	
Q2	30 V	2.5 mΩ @ 10 V	80 A
		3.0 mΩ @ 4.5 V	

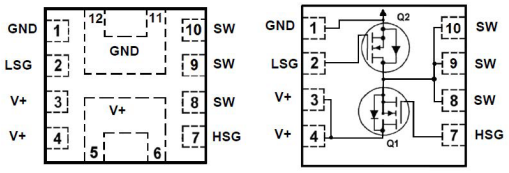
Features

- Small Footprint (3.3mm x 3.3mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- These Devices are Pb−Free and are RoHS Compliant

Typical Applications

- DC−DC Converters
- System Voltage Rails

ELECTRICAL CONNECTION

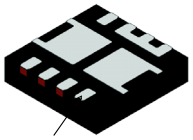


MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Q1	Q2	Unit
Drain−to−Source Voltage			V_{DSS}	30	30	V
Gate−to−Source Voltage			V_{GS}	+16 −12	+16 −12	V
Continuous Drain Current $R_{\theta JC}$ (Note 3)	Steady State	T_C = 25°C	I_D	80	80	A
		T_C = 85°C		58	58	
Power Dissipation $R_{\theta JC}$ (Note 3)	Steady State	T_A = 25°C	P_D	26	26	W
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 3)	Steady State	T_A = 25°C	I_D	21.1	21.1	A
		T_A = 85°C		15.2	15.2	
Power Dissipation $R_{\theta JA}$ (Notes 1, 3)	Steady State	T_A = 25°C	P_D	1.79	1.79	W
Continuous Drain Current $R_{\theta JA}$ (Notes 2, 3)	Steady State	T_A = 25°C	I_D	16.1	16.1	A
		T_A = 85°C		11.6	11.6	
Power Dissipation $R_{\theta JA}$ (Notes 2, 3)	Steady State	T_A = 25°C	P_D	1.04	1.04	W
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	327	356	A
Single Pulse Drain−to−Source Avalanche Energy Q1: I_L = 33.3 A_{pk}, L = 0.1 mH (Note 4) Q2: I_L = 34.3 A_{pk}, L = 0.1 mH (Note 4)			E_{AS}	55.4	58.8	mJ
Operating Junction and Storage Temperature			T_J, T_{stg}	−55 to + 150		°C
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface−mounted on FR4 board using a 1 in^2 pad size, 2 oz. Cu pad.
2. Surface−mounted on FR4 board using minimum pad size, 2 oz. Cu pad.
3. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted. Actual continuous current will be limited by thermal & electro−mechanical application board design. $R_{\theta JC}$ is determined by the user's board design.
4. Q1 100% UIS tested at L = 0.1 mH, IAS = 21.1 A.
   Q2 100% UIS tested at L = 0.1 mH, IAS = 21.1 A.
5. This device is Class 1B ESD HBM Rating.



WQFN12
3.3X3.3, 0.65P
CASE 510CJ

MARKING DIAGRAM

3ESN = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

ORDERING INFORMATION

Device	Package	Shipping†
NTTFD2D8N03P1E	WQFN12 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Q1 Max	Q2 Max	Unit
Junction−to−Case − Steady State (Notes 1, 3)	$R_{\theta JC}$	4.8	4.8	°C/W
Junction−to−Ambient − Steady State (Notes 1, 3)	$R_{\theta JA}$	70	70	
Junction−to−Ambient − Steady State (Notes 2, 3)	$R_{\theta JA}$	120	120	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	FET	Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1 mA	Q1	30			V
		V_{GS} = 0 V, I_D = 1 mA	Q2	30			
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = 1 mA, ref to 25°C	Q1		17.9		mV/°C
		I_D = 1 mA, ref to 25°C	Q2		17.2		
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 24 V, T_J = 25°C	Q1			1.0	μA
			Q2			1.0	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = +16 V / −12 V	Q1			±100	nA
		V_{DS} = 0 V, V_{GS} = +16 V / −12 V	Q2			±100	
ON CHARACTERISTICS (Note 6)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 400 μA	Q1	1.2		2.2	V
		V_{GS} = V_{DS}, I_D = 400 μA	Q2	1.2		2.2	
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	I_D = 400 μA, ref to 25°C	Q1		−4.3		mV/°C
		I_D = 400 μA, ref to 25°C	Q2		−4.5		
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 18 A	Q1		2.0	2.5	mΩ
		V_{GS} = 4.5 V, I_D = 16 A			2.6	3.0	
		V_{GS} = 10 V, I_D = 18 A	Q2		1.8	2.5	
		V_{GS} = 4.5 V, I_D = 16 A			2.4	3.0	
Forward Transconductance	g_{FS}	V_{DS} = 5 V, I_D = 18 A	Q1		129		S
		V_{DS} = 5 V, I_D = 18 A	Q2		141		
Gate−Resistance	R_G	T_A = 25°C	Q1		0.68		Ω
			Q2		0.75		
CHARGES, CAPACITANCES & GATE RESISTANCE							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, V_{DS} = 15 V, f = 1 MHz	Q1		1500		pF
			Q2		1521		
Output Capacitance	C_{OSS}		Q1		483		pF
			Q2		498		
Reverse Transfer Capacitance	C_{RSS}		Q1		29		pF
			Q2		22		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
7. Switching characteristics are independent of operating junction temperatures.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		FET	Min	Typ	Max	Unit
CHARGES, CAPACITANCES & GATE RESISTANCE								
Total Gate Charge	$Q_{G(TOT)}$	Q1: V_{GS} = 4.5 V, V_{DS} = 15 V; I_D = 18 A Q2: V_{GS} = 4.5 V, V_{DS} = 15 V; I_D = 18 A		Q1		9.5		nC
				Q2		9.3		
Gate−to−Drain Charge	Q_{GD}			Q1		2.0		nC
				Q2		1.6		
Gate−to−Source Charge	Q_{GS}			Q1		3.7		nC
				Q2		3.7		
Total Gate Charge	$Q_{G(TOT)}$	Q1: V_{GS} = 10 V, V_{DS} = 15 V; I_D = 18 A		Q1		20.8		nC
		Q2: V_{GS} = 10 V, V_{DS} = 15 V; I_D = 18 A		Q2		20.5		
SWITCHING CHARACTERISTICS, VGS = 4.5 V (Note 7)								
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 4.5 V Q1: I_D = 18 A, V_{DD} = 15 V, R_G = 6 Ω Q2: I_D = 18 A, V_{DD} = 15 V, R_G = 6 Ω		Q1		13		ns
				Q2		13.3		
Rise Time	t_r			Q1		5.5		ns
				Q2		5.8		
Turn−Off Delay Time	$t_{d(OFF)}$			Q1		18.9		ns
				Q2		19		
Fall Time	t_f			Q1		5.5		ns
				Q2		5.5		
SWITCHING CHARACTERISTICS, VGS = 10 V (Note 7)								
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 10 V Q1: I_D = 18 A, V_{DD} = 15 V, R_G = 6 Ω Q2: I_D = 18 A, V_{DD} = 15 V, R_G = 6 Ω		Q1		8.4		ns
				Q2		8.7		
Rise Time	t_r			Q1		2		ns
				Q2		2		
Turn−Off Delay Time	$t_{d(OFF)}$			Q1		26.3		ns
				Q2		26.3		
Fall Time	t_f			Q1		3.8		ns
				Q2		3.6		
DRAIN−SOURCE DIODE CHARACTERISTICS								
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 18 A	T_J = 25°C	Q1		0.8	1.2	V
			T_J = 125°C			0.67		
		V_{GS} = 0 V, I_S = 18 A	T_J = 25°C	Q2		0.8	1.2	
			T_J = 125°C			0.66		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, V_{DD} = 15 V Q1: I_S = 18 A, dI_S/dt = 100 A/μs Q2: I_S = 18 A, dI_S/dt = 100 A/μs		Q1		30		ns
				Q2		29		
Reverse Recovery Charge	Q_{RR}			Q1		13		nC
				Q2		12.5		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
7. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS – Q1

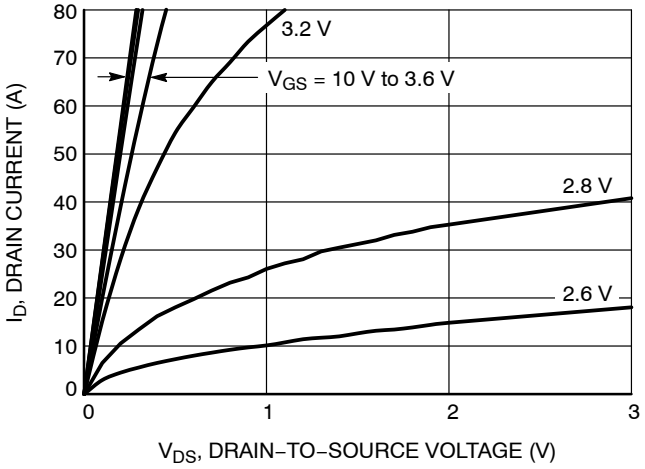


Figure 1. On−Region Characteristics

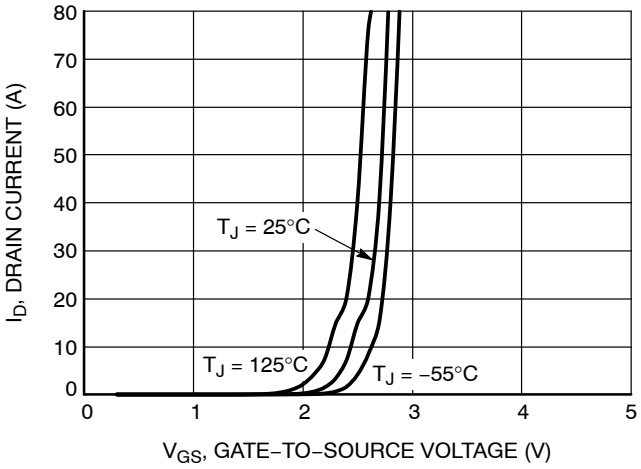


Figure 2. Transfer Characteristics

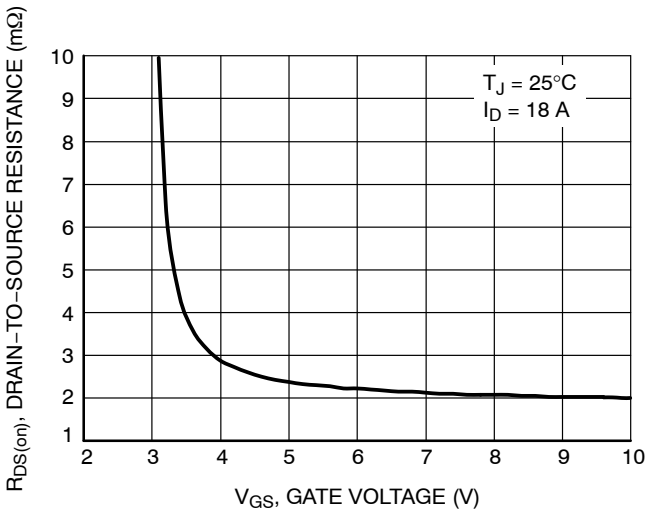


Figure 3. On−Resistance vs. Gate−to−Source Voltage

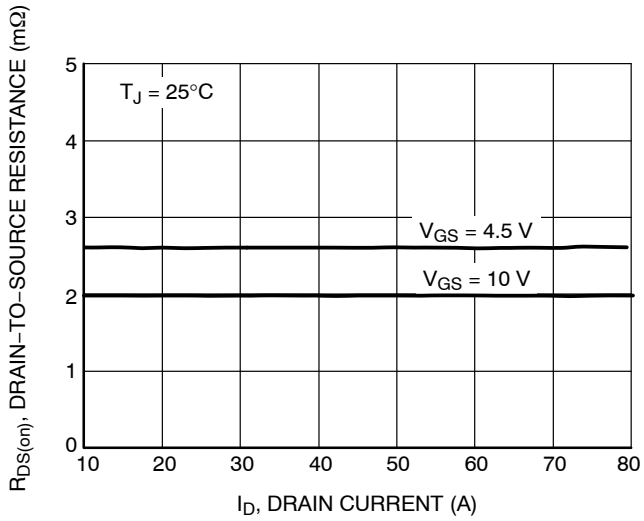


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

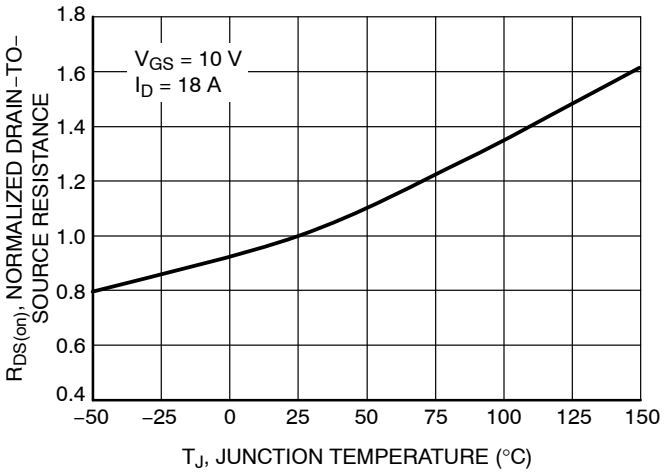


Figure 5. On−Resistance Variation with Temperature

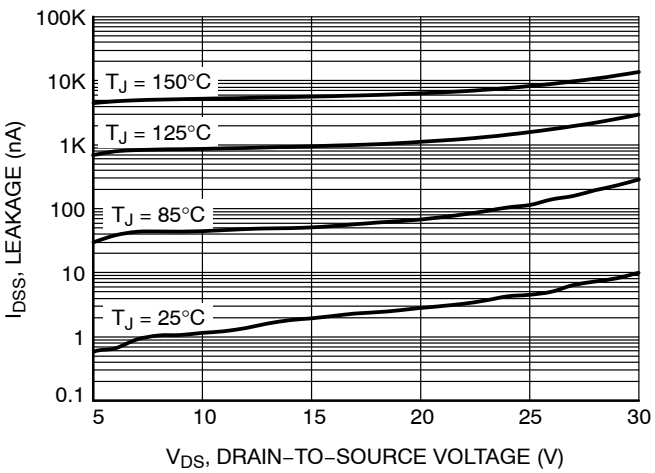


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS – Q1

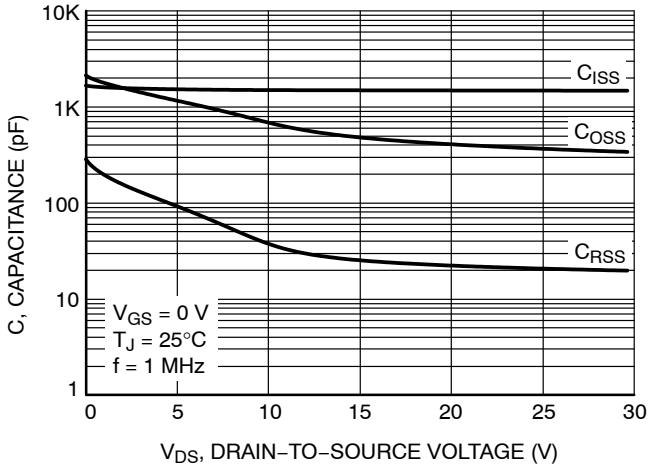


Figure 7. Capacitance Variation

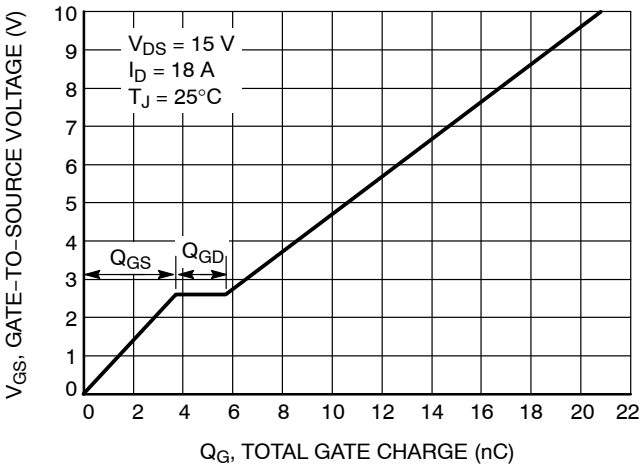


Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

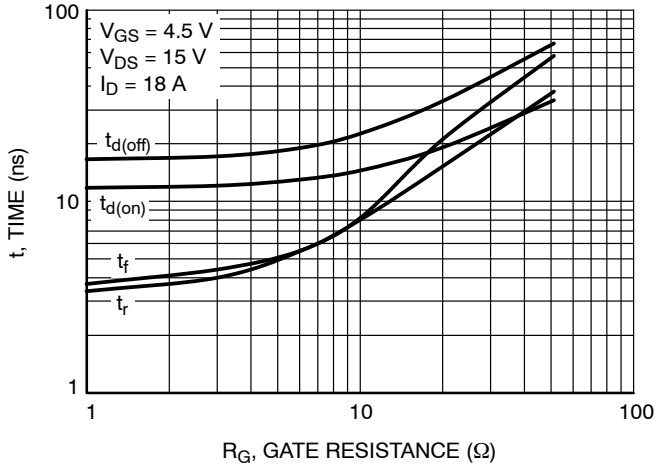


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

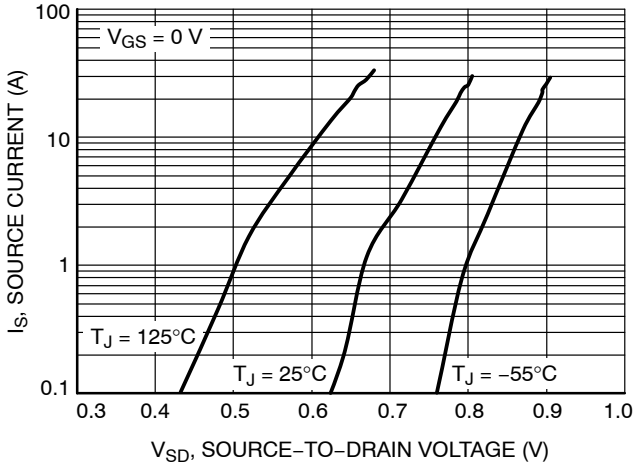


Figure 10. Diode Forward Voltage vs. Current

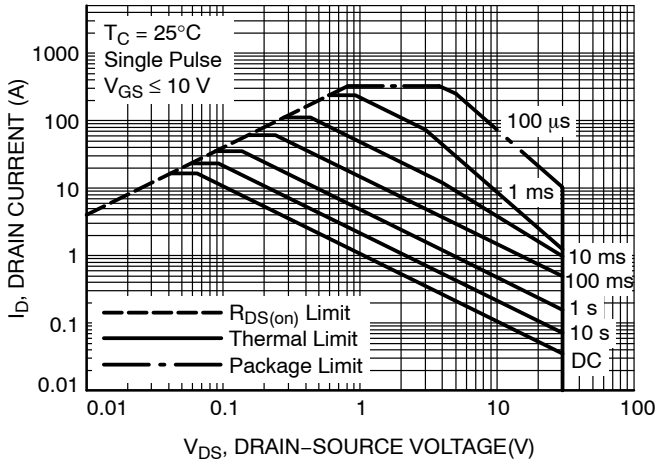


Figure 11. Safe Operating Area

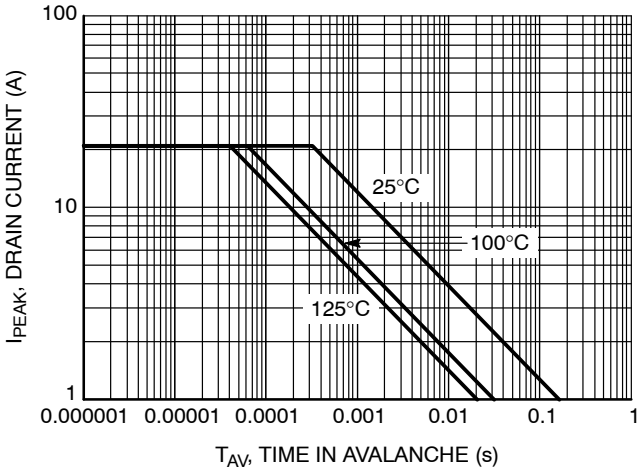


Figure 12. I_{PEAK} vs. Time in Avalanche

TYPICAL CHARACTERISTICS – Q1

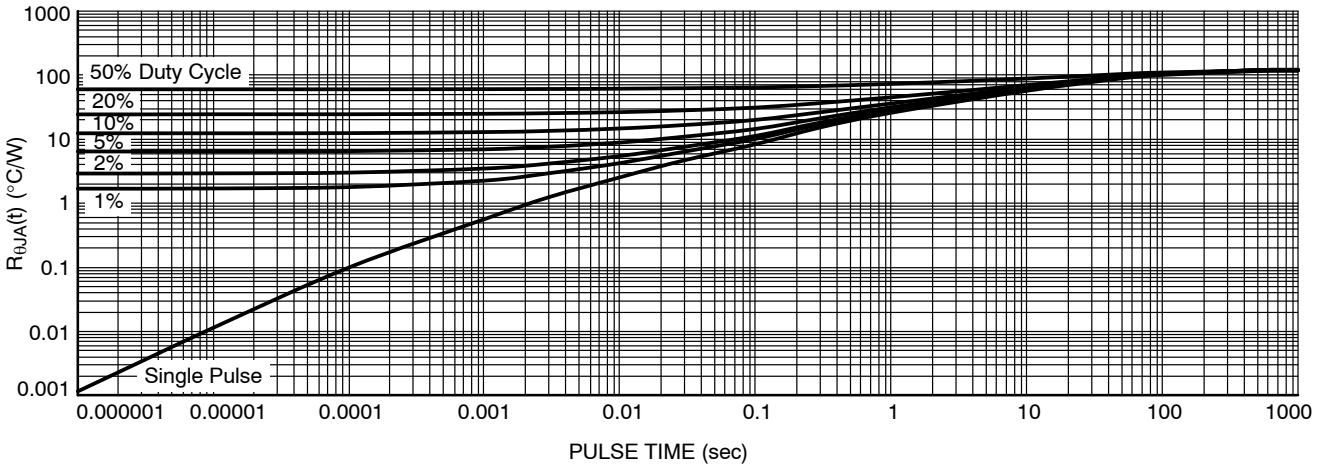


Figure 13. Thermal Characteristics

TYPICAL CHARACTERISTICS – Q2

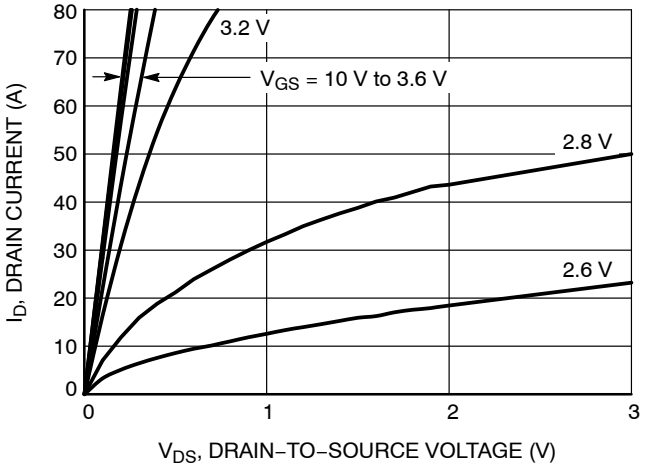


Figure 14. On−Region Characteristics

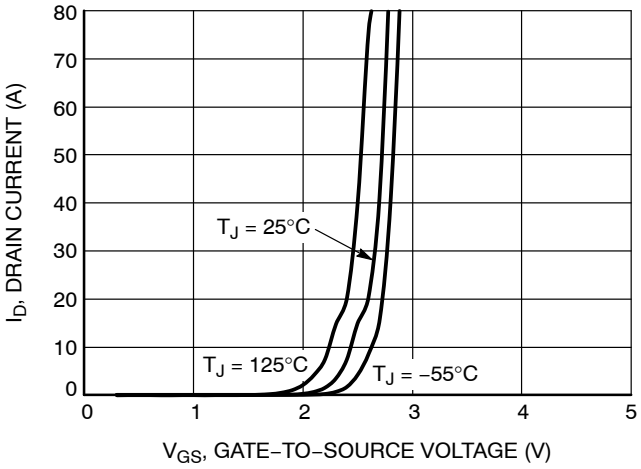


Figure 15. Transfer Characteristics

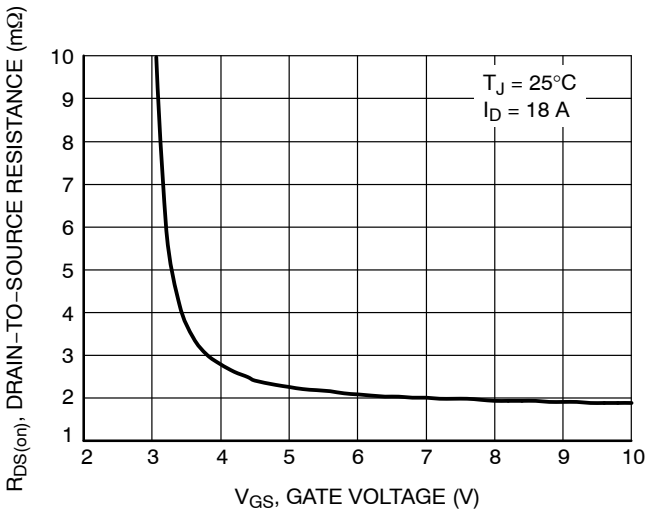


Figure 16. On−Resistance vs. Gate−to−Source Voltage

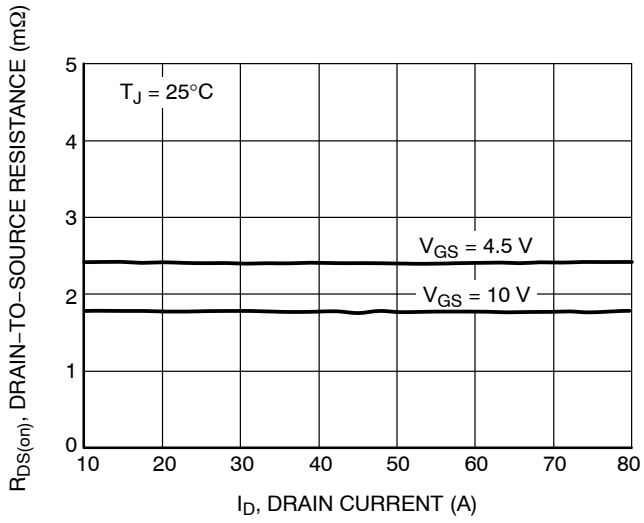


Figure 17. On−Resistance vs. Drain Current and Gate Voltage

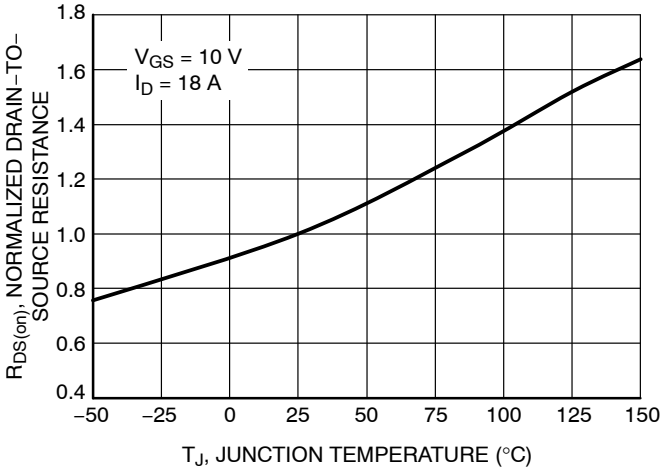


Figure 18. On−Resistance Variation with Temperature

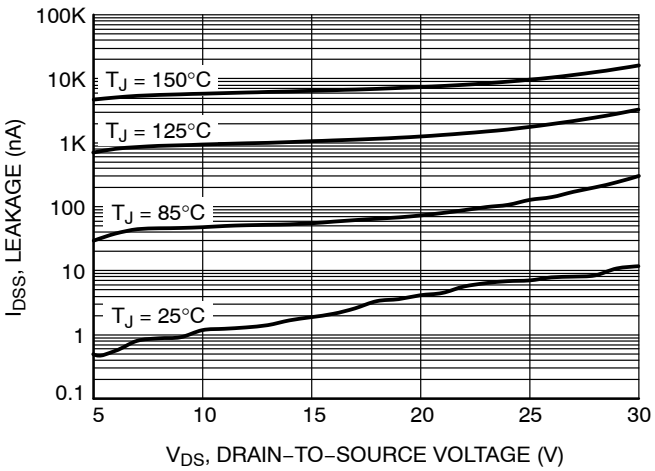


Figure 19. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS – Q2

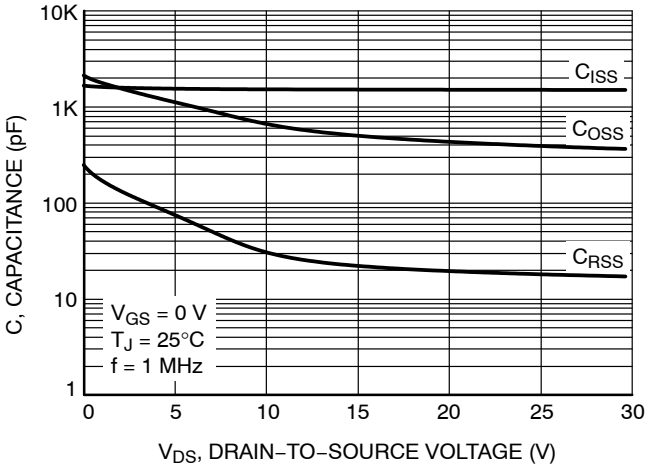


Figure 20. Capacitance Variation

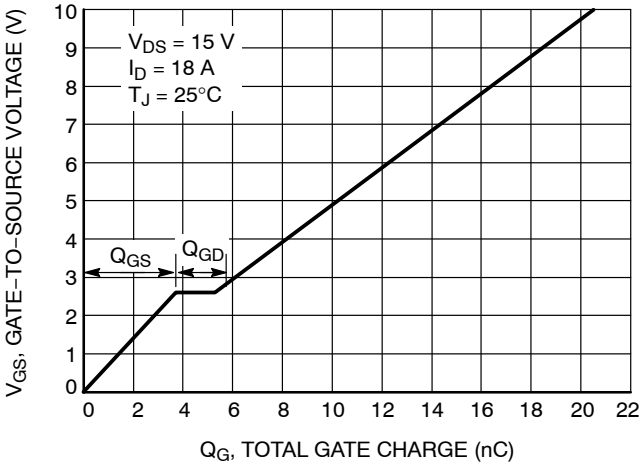


Figure 21. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

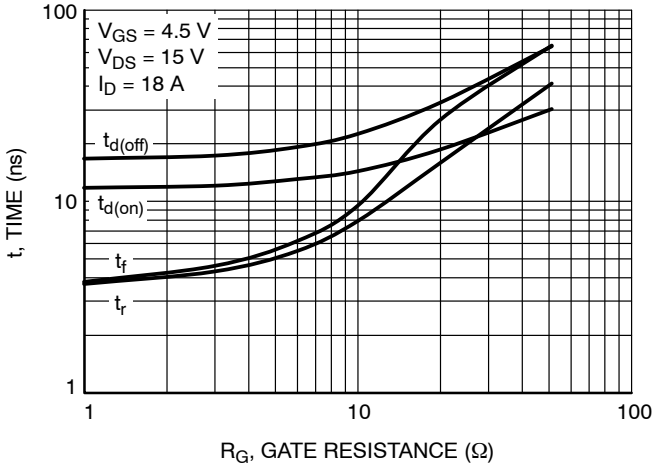


Figure 22. Resistive Switching Time Variation vs. Gate Resistance

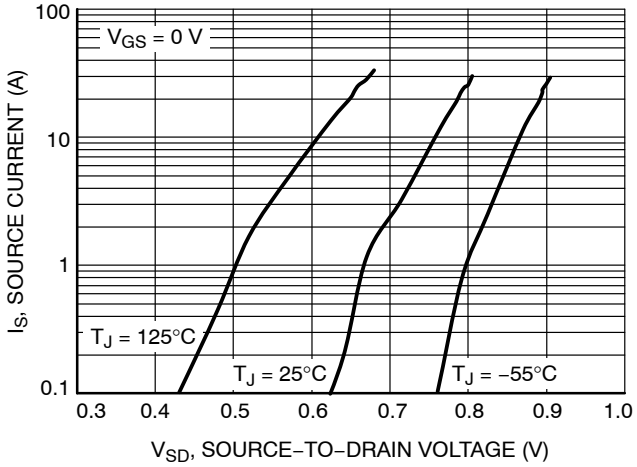


Figure 23. Diode Forward Voltage vs. Current

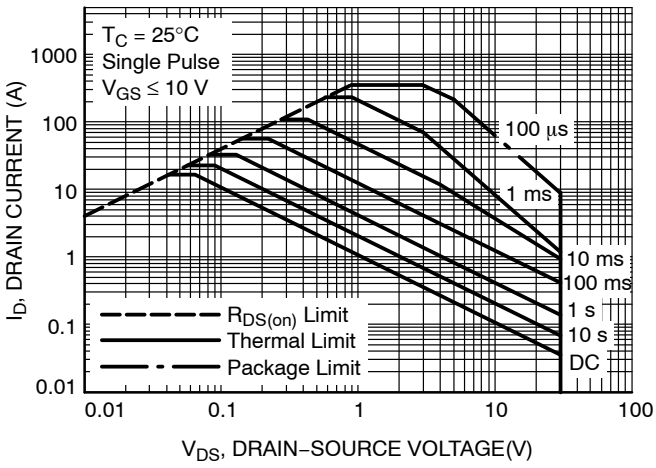


Figure 24. Safe Operating Area

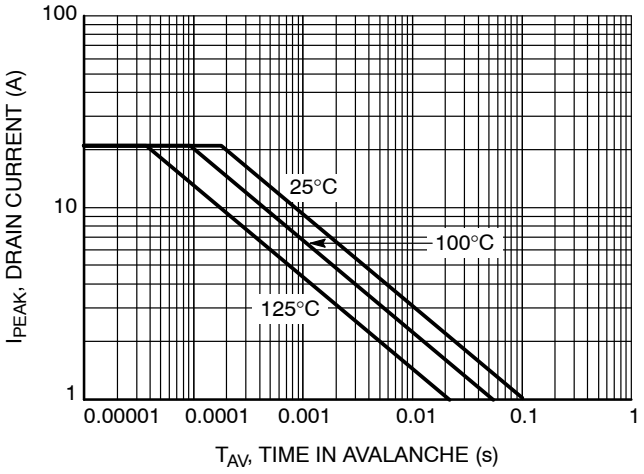


Figure 25. I_{PEAK} vs. Time in Avalanche

TYPICAL CHARACTERISTICS – Q2

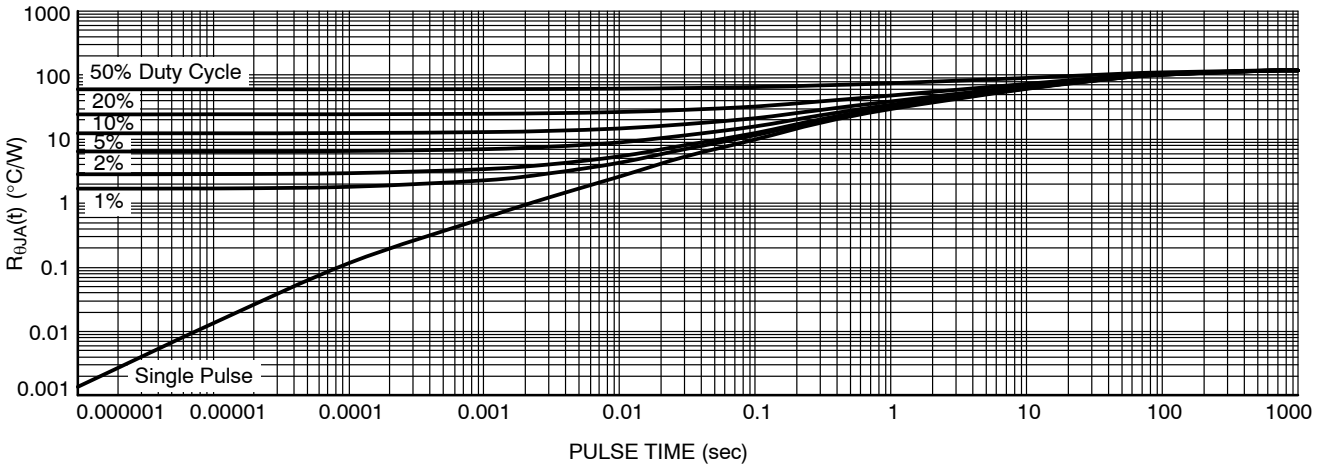
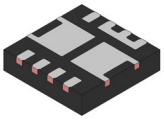
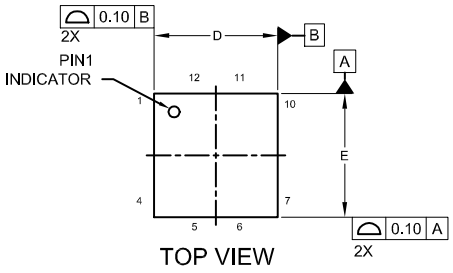


Figure 26. Thermal Characteristics

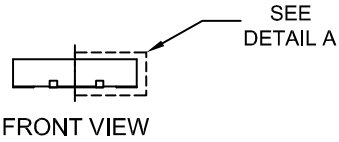


WQFN12 3.3X3.3, 0.65P
CASE 510CJ
ISSUE A

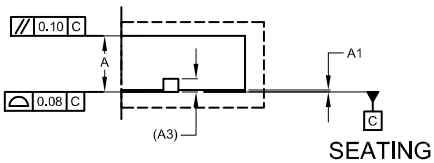
DATE 08 AUG 2022



TOP VIEW

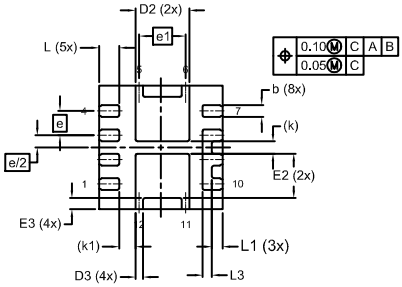


FRONT VIEW



DETAIL 'A'
SCALE 2:1

SEATING
PLANE

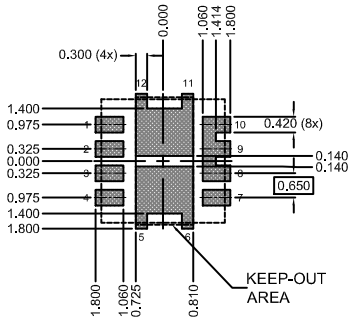


BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
5. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

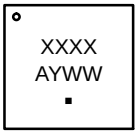
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	--	0.05
A3	0.20 REF		
b	0.27	0.32	0.37
D	3.20	3.30	3.40
D2	1.34	1.44	1.54
D3	0.10	0.20	0.30
E	3.20	3.30	3.40
E2	1.09	1.19	1.29
E3	0.20	0.30	0.40
e	0.65 BSC		
e/2	0.325 BSC		
e1	1.24 BSC		
k	0.33 REF		
k1	0.43 REF		
L	0.44	0.54	0.64
L1	0.19	0.29	0.39
L3	0.15	0.25	0.35



LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**WQFN12 3.3X3.3, 0.65P**		**PAGE 1 OF 1**

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