Programmable Shunt Regulator

LM431SA, LM431SB, LM431SC

SOT−89
CASE 528AH

1. Ref
2. Anode
3. Cathode

3

SOT−23FL
CASE 318AB

1. Cathode
2. Ref
3. Anode

3

SOT−23
CASE 318BM

M32
1. Ref
2. Cathode
3. Anode

M3
1. Cathode
2. Ref
3. Anode

Description

The LM431SA / LM431SB / LM431SC are three−terminal the output adjustable regulators with thermal stability over operating temperature range. The output voltage can be set any value between V_{REF} (approximately 2.5 V) and 36 V with two external resistors. These devices have a typical dynamic output impedance of 0.2 Ω. Active output circuit provides a sharp turn−on characteristic, making these devices excellent replacement for zener diodes in many applications.

Features

- Programmable Output Voltage to 36 V
- Low Dynamic Output Impedance: 0.2 Ω (Typical)
- Sink Current Capability: 1.0 to 100 mA
- Equivalent Full−Range Temperature Coefficient of 50 ppm/°C (Typical)
- Temperature Compensated for Operation Over Full Rated Operating Temperature Range
- Low Output Noise Voltage
- Fast Turn−on Response
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

ORDERING INFORMATION

Product Number	Output Voltage Tolerance	Operating Temperature	Top Mark(1)	Package	Shipping†
LM431SACMFX	2%	−25 to +85°C	43A □	SOT−23FL 3L	Tape and Reel
LM431SACM3X			43L ◎	SOT−23 3L	
LM431SACM32X			43G ◎	SOT−23 3L	
LM431SBCMFX	1%		43B □	SOT−23FL 3L	
LM431SBCM3X			43M ◎	SOT−23 3L	
LM431SBCM32X			43H ◎	SOT−23 3L	
LM431SCCMLX	0.5%		43C	SOT−89 3L	
LM431SCCMFX			43C □	SOT−23FL 3L	
LM431SCCM3X			43N ◎	SOT−23 3L	
LM431SCCM32X			43J ◎	SOT−23 3L	
LM431SAIMFX	2%	−40 to +85°C	43AI	SOT−23FL 3L	
LM431SBIMFX	1%		43BI	SOT−23FL 3L	
LM431SCIMFX	0.5%		43CI	SOT−23FL 3L	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.
1. SOT−23 and SOT−23FL have basically four−character marking except LM431SAIMFX. (3 letters for device code + 1 letter for date code) SOT−23FL date code is composed of 1 digit numeric or alphabetic week code adding bar−type year code.

BLOCK DIAGRAM

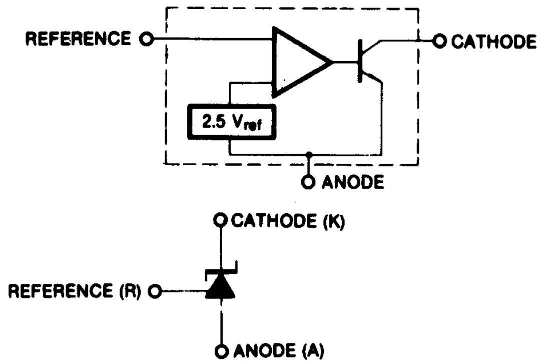


Figure 1. Block Diagram

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter		Value	Unit
V_{KA}	Cathode Voltage		37	V
I_{KA}	Cathode current Range (Continuous)		−100 to +150	mA
I_{REF}	Reference Input Current Range		−0.05 to +10.00	mA
$R_{\theta JA}$	Thermal Resistance Junction−Air (2, 3)	ML Suffix Package (SOT−89)	220	°C/W
		MF Suffix Package (SOT−23FL)	350	
		M32, M3 Suffix Package (SOT−23)	400	
P_D	Power Dissipation (4, 5)	ML Suffix Package (SOT−89)	560	mW
		MF Suffix Package (SOT−23FL)	350	
		M32, M3 Suffix Package (SOT−23)	310	
T_J	Junction Temperature		150	°C
T_{OPR}	Operating Temperature Range	All products except LM431SAIMFX	−25 to +85	°C
		LM431SAIMFX, SBIMFX, SCIMFX	−40 to +85	
T_{STG}	Storage Temperature Range		−65 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Thermal resistance test board
   Size: 1.6 mm x 76.2 mm x 114.3 mm (1S0P) JEDEC Standard: JESD51−3, JESD51−7.
3. Assume no ambient airflow.
4. T_{JMAX} = 150°C; ratings apply to ambient temperature at 25°C.
5. Power dissipation calculation: $P_D = (T_J - T_A) / R_{\theta JA}$.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V_{KA}	Cathode Voltage	V_{REF}	36	V
I_{KA}	Cathode Current	1	100	mA

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 6, Values are at T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions		LM431SA			LM431SB			LM431SC			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{REF}	Reference Input Voltage	$V_{KA} = V_{REF}$, I_{KA} = 10 mA		2.450	2.500	2.550	2.470	2.495	2.520	2.482	2.495	2.508	V
$\Delta V_{REF} / \Delta T$	Deviation of Reference Input Voltage Over– Temperature	$V_{KA} = V_{REF}$, I_{KA} = 10 mA $T_{MIN} \leq T_A \leq T_{MAX}$	SOT−89 SOT−23FL		4.5	17.0		4.5	17.0		4.5	17.0	mV
			SOT−23		6.6	24		6.6	24		6.6	24	mV
$\Delta V_{REF} / \Delta V_{KA}$	Ratio of Change in Reference Input Voltage to the Change in Cathode Voltage	I_{KA} =10 mA	ΔV_{KA} = 10 V−V_{REF}		−1.0	−2.7		−1.0	−2.7		−1.0	−2.7	mV/V
			ΔV_{KA} = 36 V − 10 V		−0.5	−2.0		−0.5	−2.0		−0.5	−2.0	
I_{REF}	Reference Input Current	I_{KA} = 10 mA, R_1 = 10 KΩ, $R_2 = \infty$			1.5	4.0		1.5	4.0		1.5	4.0	µA
$\Delta I_{REF} / \Delta T$	Deviation of Reference Input Current Over Full Temperature Range	I_{KA} = 10 mA, R_1 = 10 KΩ, $R_2 = \infty$, T_A = Full Range	SOT−89 SOT−23FL		0.4	1.2		0.4	1.2		0.4	1.2	µA
			SOT−23		0.8	2.0		0.8	2.0		0.8	2.0	µA
$I_{KA(MIN)}$	Minimum Cathode Current for Regulation	$V_{KA} = V_{REF}$			0.45	1.00		0.45	1.00		0.45	1.00	mA
$I_{KA(OFF)}$	Off −Stage Cathode Current	V_{KA} = 36 V, V_{REF} = 0			0.05	1.00		0.05	1.00		0.05	1.00	µA
Z_{KA}	Dynamic Impedance	$V_{KA} = V_{REF}$, I_{KA} = 1 to 100 mA, f ≥ 1.0 kHz			0.15	0.50		0.15	0.50		0.15	0.50	Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

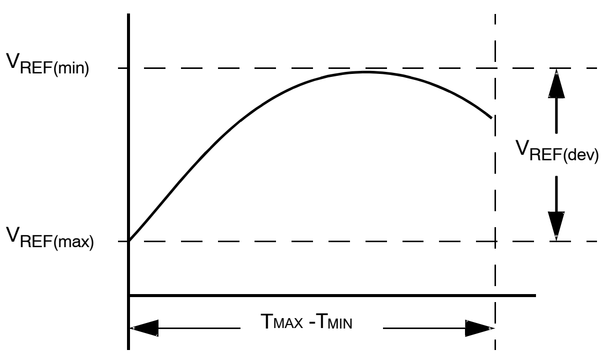
6. LM431SAI, LM431SBI, LM431SCI: − $T_{A(min)}$ = −40°C, $T_{A(max)}$ = +85°C
   All other pins: − $T_{A(min)}$ = −25°C, $T_{A(max)}$ = +85°C

ELECTRICAL CHARACTERISTICS (Continued) (Notes 7 and 8, Values are at T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	LM431SAI Min.	LM431SAI Typ.	LM431SAI Max.	LM431SBI Min.	LM431SBI Typ.	LM431SBI Max.	LM431SCI Min.	LM431SCI Typ.	LM431SCI Max.	Unit
V_{REF}	Reference Input Voltage	$V_{KA} = V_{REF}$, I_{KA} = 10 mA	2.450	2.500	2.550	2.470	2.495	2.520	2.482	2.495	2.508	V
$V_{REF(dev)}$	Deviation of Reference Input Voltage Over−Temperature	$V_{KA} = V_{REF}$, I_{KA} = 10 mA, $T_{MIN} \le T_A \le T_{MAX}$		5	20		5	20		5	20	mV
$\Delta V_{REF} / \Delta V_{KA}$	Ratio of Change in Reference Input Voltage to Change in Cathode Voltage	I_{KA} = 10 mA, ΔV_{KA} = 10 V−V_{REF}		−1.0	−2.7		−1.0	−2.7		−1.0	−2.7	mV/V
		I_{KA} = 10 mA, ΔV_{KA} = 36 V − 10 V		−0.5	−2.0		−0.5	−2.0		−0.5	−2.0	
I_{REF}	Reference Input Current	I_{KA} = 10 mA, R_1 =10 KΩ, $R_2 = \infty$		1.5	4.0		1.5	4.0		1.5	4.0	μA
$I_{REF(dev)}$	Deviation of Reference Input Current Over Full Temperature Range	I_{KA} = 10 mA, R_1 = 10 KΩ, $R_2 = \infty$, $T_{MIN} \le T_A \le T_{MAX}$		0.8	2.0		0.8	2.0		0.8	2.0	μA
$I_{KA(MIN)}$	Minimum Cathode Current for Regulation	$V_{KA} = V_{REF}$		0.45	1.00		0.45	1.00		0.45	1.00	mA
$I_{KA(OFF)}$	Off −Stage Cathode Current	V_{KA} = 36 V, V_{REF} = 0		0.05	1.00		0.05	1.00		0.05	1.00	μA
ZKA	Dynamic Impedance	$V_{KA} = V_{REF}$, I_{KA} = 1 to 100 mA, f ≥ 1.0 kHz		0.15	0.50		0.15	0.50		0.15	0.50	Ω

7. LM431SAI, LM431SBI, LM431SCI: − $T_{A(min)}$ = −40°C, $T_{A(max)}$ = +85°C
   All other pins: − $T_{A(min)}$ = −25°C, $T_{A(max)}$ = +85°C
8. The deviation parameters $V_{REF(dev)}$ and $I_{REF(dev)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The average full−range temperature coefficient of the reference input voltage, αV_{REF}, is defined as:

$$|\alpha V_{REF}|\left(\frac{ppm}{°C}\right) = \frac{\left(\frac{V_{REF(dev)}}{V_{REF(at\ 25°C)}}\right) \cdot 10^6}{T_{MAX} - T_{MIN}}$$



where $T_{MAX} - T_{MIN}$ is the rated operating free−air temperature range of the device.

αV_{REF} can be positive or negative, depending on whether minimum V_{REF} or maximum V_{REF}, respectively, occurs at the lower temperature.

Example:

$V_{REF(dev)}$ = 4.5 mV, V_{REF} = 2500 mV at 25°C,

$T_{MAX} - T_{MIN}$ = 125°C for LM431SAI.

$$|\alpha V_{REF}| = \frac{\left(\frac{4.5\ mV}{2500\ mV}\right) \cdot 10^6}{125°C} = 14.4\ ppm/°C$$

Because minimum V_{REF} occurs at the lower temperature, the coefficient is positive.

TEST CIRCUITS

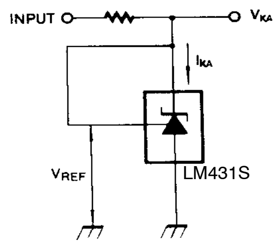


Figure 2. Test Circuit for $V_{KA} = V_{REF}$

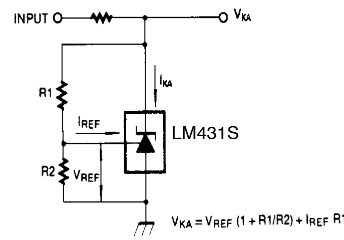


Figure 3. Test Circuit for $V_{KA} \geq V_{REF}$

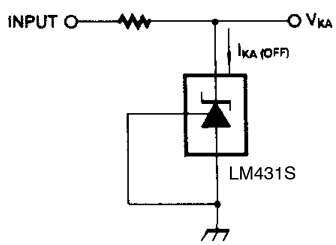


Figure 4. Test Circuit for $I_{KA(OFF)}$

TYPICAL APPLICATIONS

$$V_O = \left(1 + \frac{R_1}{R_2}\right) V_{ref}$$

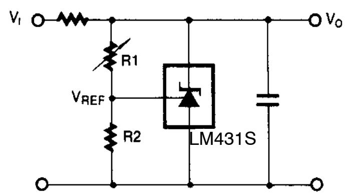


Figure 5. Shunt Regulator

$$V_O = \left(1 + \frac{R_1}{R_2}\right) V_{ref}$$

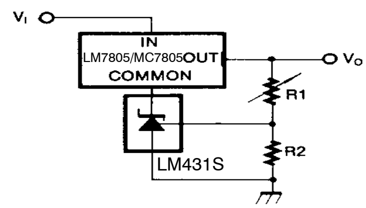


Figure 6. Output Control for Three−Terminal Fixed Regulator

$$V_O = \left(1 + \frac{R_1}{R_2}\right) V_{ref}$$

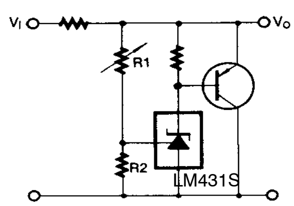
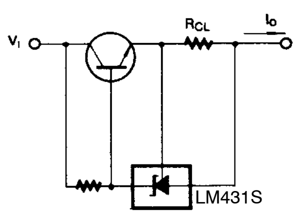
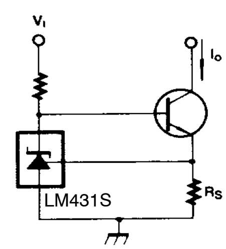


Figure 7. High Current Shunt Regulator



$$I_O = \frac{V_{REF}}{R_{CL}}$$

Figure 8. Current Limit or Current Source



$$I_O = \frac{V_{REF}}{R_S}$$

Figure 9. Constant−Current Sink

TYPICAL PERFORMANCE CHARACTERISTICS

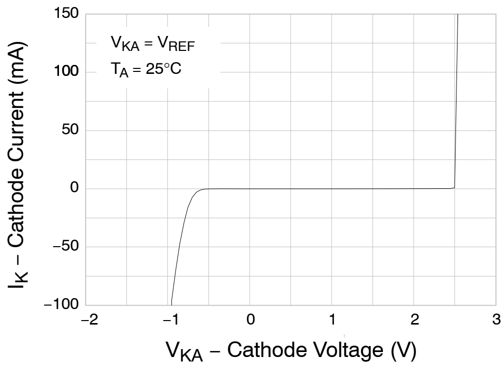


Figure 10. Cathode Current vs. Cathode Voltage

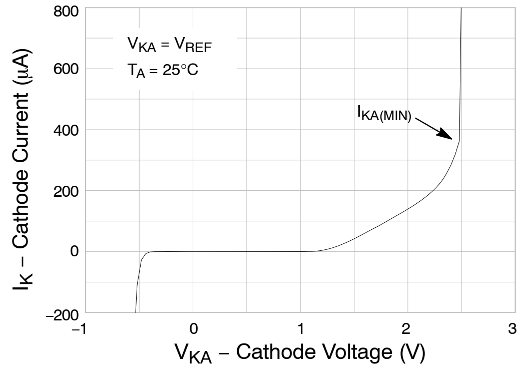


Figure 11. Cathode Current vs. Cathode Voltage

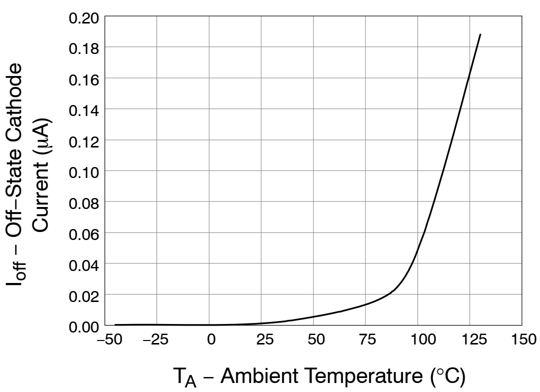


Figure 12. OFF−State Cathode Current vs. Ambient Temperature

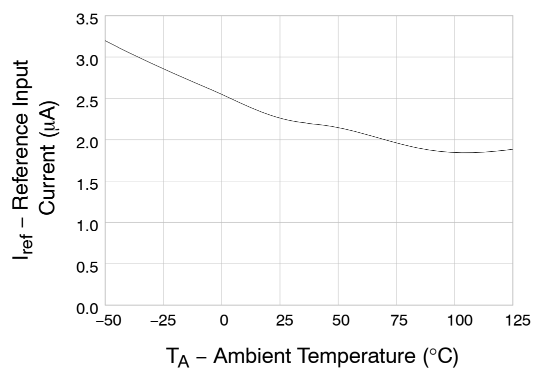


Figure 13. Reference Input Current vs. Ambient Temperature

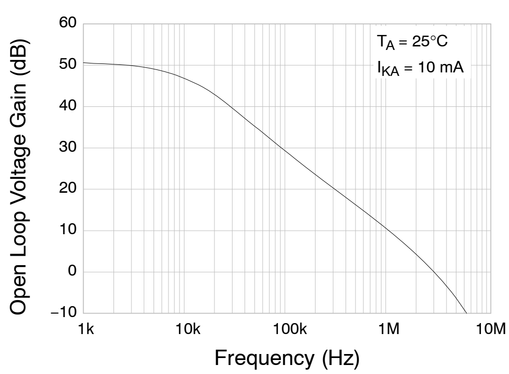


Figure 14. Frequency vs. Small Signal Voltage Amplification

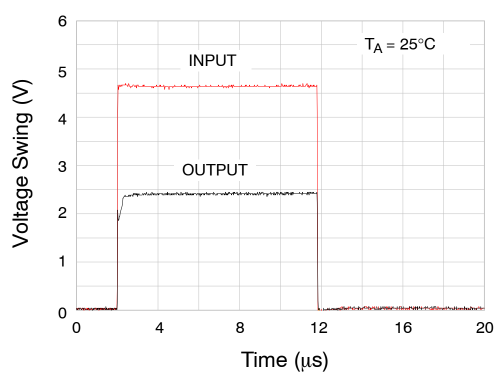


Figure 15. Pulse Response

TYPICAL PERFORMANCE CHARACTERISTICS

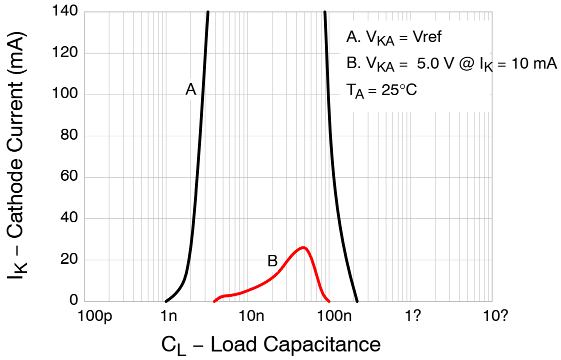


Figure 16. Stability Boundary Conditions

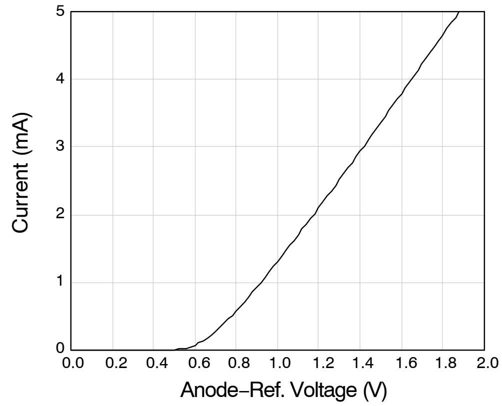


Figure 17. Anode−Reference Diode Curve

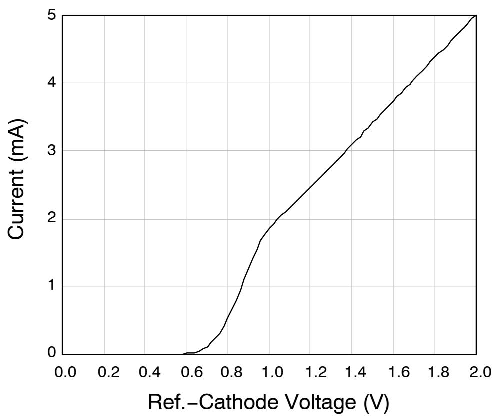


Figure 18. Reference−Cathode Diode Curve

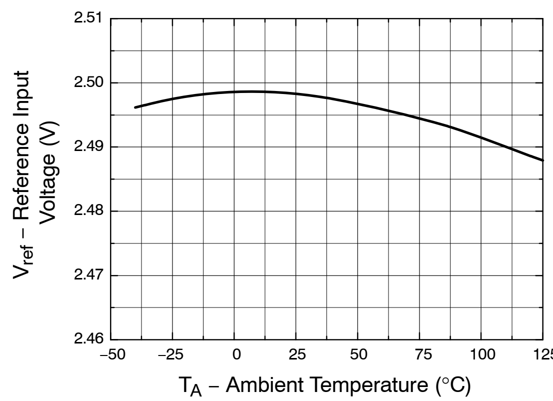
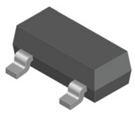
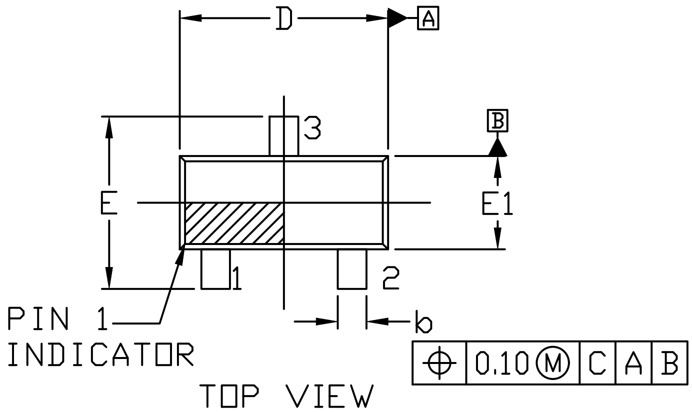


Figure 19. Reference Input Voltage vs. Ambient Temperature



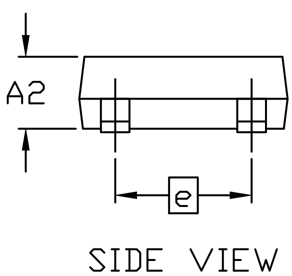
SOT23−3L
CASE 318AB
ISSUE A

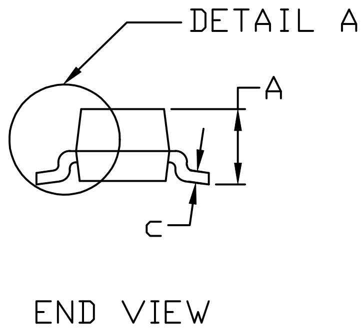
DATE 14 DEC 2021

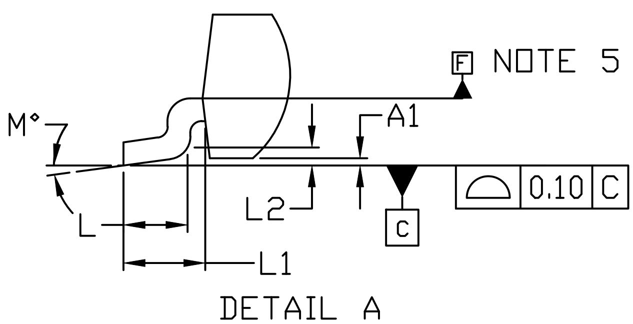


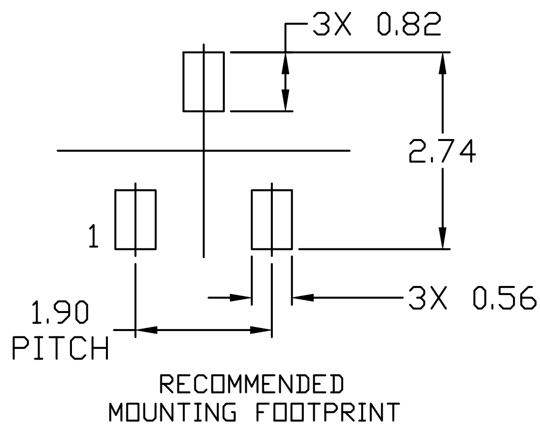
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.127 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM F.
5. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
7. LEAD THICKNESS (c) AND LEAD WIDTH (b) INCLUDE PLATING THICKNESS.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	---	---	1.15
A1	0.00	---	0.10
A2	0.90	1.00	1.10
b	0.30	---	0.50
c	0.127 REF		
D	2.80	2.90	3.00
E	2.25	2.40	2.55
E1	1.20	1.30	1.40
e	1.90 BSC		
L	0.30	---	---
L1	0.55 REF		
L2	0.25 REF		
M	0°	---	8°



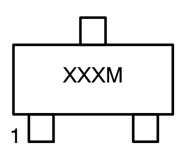






* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

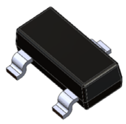
GENERIC
MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code

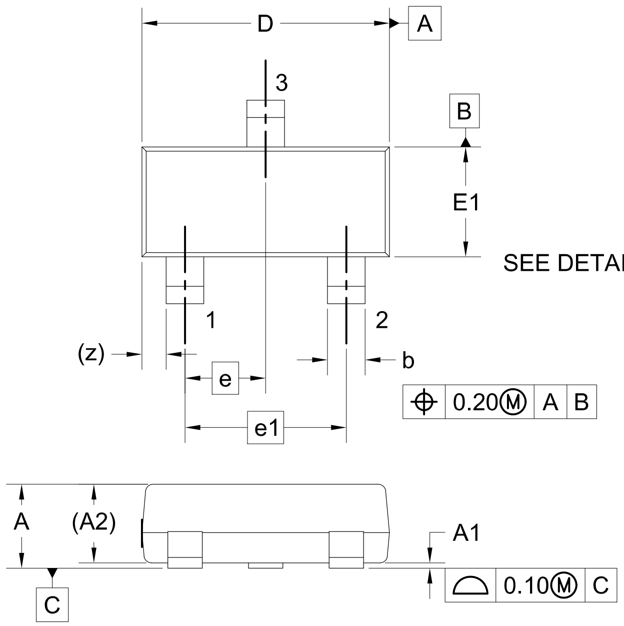
*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

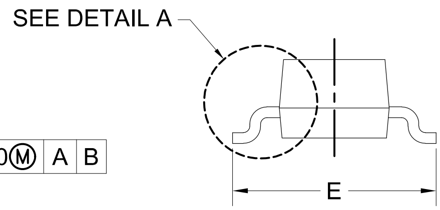
DOCUMENT NUMBER:	**98AON27911H**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**SOT23−3L**	**PAGE 1 OF 1**



SOT−23
CASE 318BM
ISSUE A

DATE 01 SEP 2021

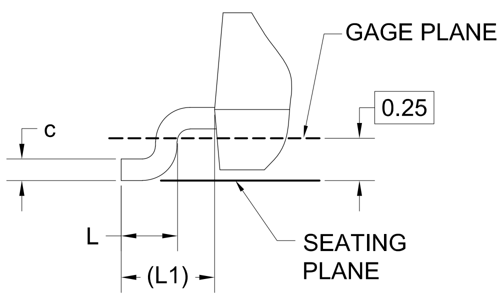




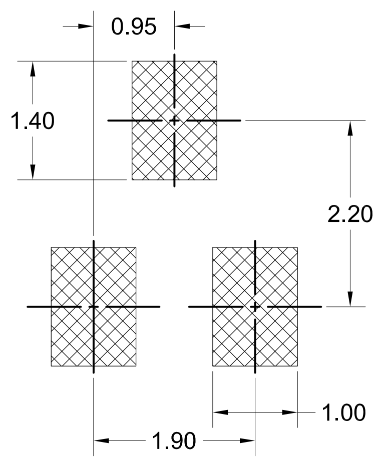
NOTES: UNLESS OTHERWISE SPECIFIED

A) REFERENCE JEDEC REGISTRATION TO-236, VARIATION AB, ISSUE H.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS ARE INCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 2009.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.20
A1	0.00	0.05	0.10
A2	0.93 REF		
b	0.37	0.44	0.60
c	0.08	0.15	0.23
D	2.72	2.92	3.12
E	2.10	2.40	2.70
E1	1.15	1.30	1.50
e	0.95 BSC		
e1	1.90 BSC		
L	0.20	---	---
L1	0.55 REF		
z	0.29 REF		



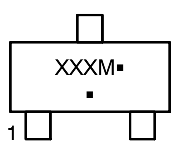
DETAIL A
SCALE: 2X



LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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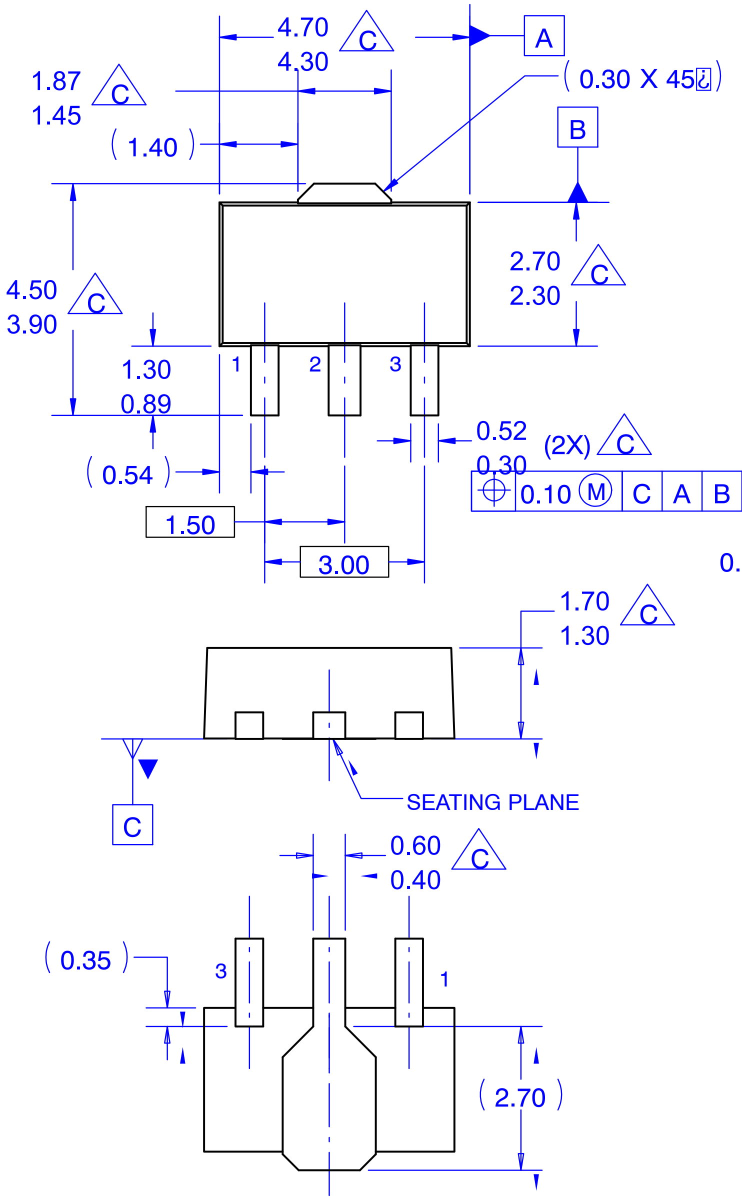
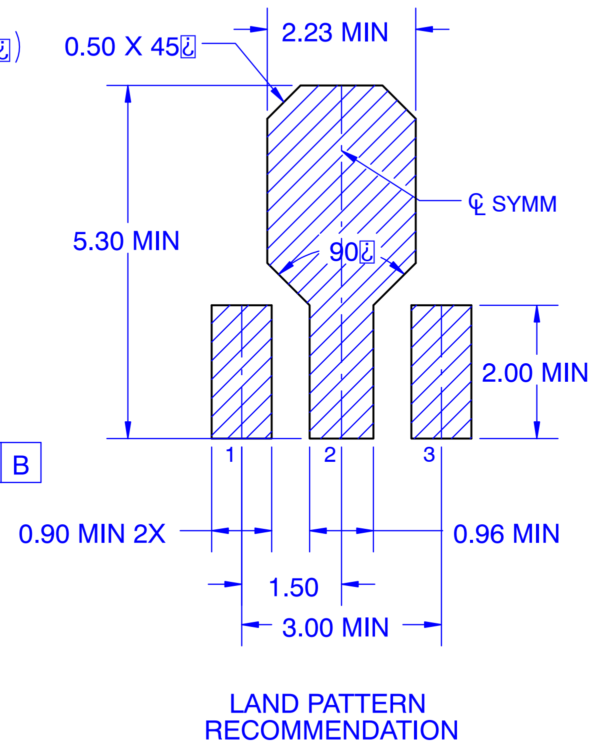
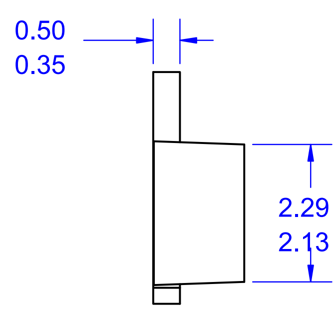
DESCRIPTION:	**SOT−23**	**PAGE 1 OF 1**

SOT−89 3 LEAD
CASE 528AH
ISSUE O

DATE 31 AUG 2016







NOTES: UNLESS OTHERWISE SPECIFIED.
A. REFERENCE TO JEDEC TO-243 VARIATION AA.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DOES NOT COMPLY JEDEC STANDARD VALUE.
D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSION.
E. DIMENSION AND TOLERANCE AS PER ASME Y14.5−1994.

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