FDU5N60NZTU

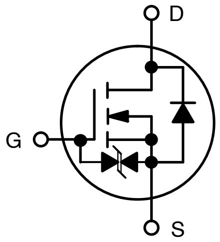
N-Channel UniFET II MOSFET

600 V, 4 A, 2 Ω

ON Semiconductor®

www.onsemi.com

UniFET II MOSFET is ON Semiconductor's high voltage MOSFET family based on advanced planar stripe and DMOS technology. This advanced MOSFET family has the smallest on−state resistance among the planar MOSFET, and also provides superior switching performance and higher avalanche energy strength. In addition, internal gate−source ESD diode allows UniFET II MOSFET to withstand over 2 kV HBM surge stress. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.

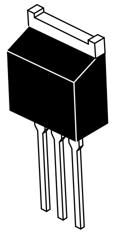


Features

- $R_{DS(on)}$ = 1.65 Ω (Typ.) @ V_{GS} = 10 V, I_D = 2 A
- Low Gate Charge (Typ. 10 nC)
- Low C_{rss} (Typ. 5 pF)
- 100% Avalanche Tested
- Improved dv/dt Capability
- ESD Improved Capability
- These Devices are Pb−Free and are RoHS Compliant

Applications

- LCD / LED TV
- Lighting
- Charger / Adapter



IPAK3
CASE 369AR

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 2 of this data sheet.

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Parameter		Value	Unit
V_{DSS}	Drain−to−Source Voltage		600	V
V_{GSS}	Gate−to−Source Voltage		±25	V
I_D	Drain Current	Continuous (T_C = 25°C)	4	A
		Continuous (T_C = 100°C)	2.4	
I_{DM}	Drain Current	Pulsed (Note 1)	16	A
E_{AS}	Single Pulse Avalanche Energy (Note 2)		216	mJ
I_{AR}	Avalanche Current (Note 1)		4	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		8.3	mJ
dv/dt	Peak Diode Recovery (Note 3)		10	V/ns
P_D	Power Dissipation	T_C = 25°C	83	W
		Derate Above 25°C	0.7	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		−55 to +150	°C
T_L	Maximum Lead Temperature for Soldering Purposes (1/8″ from case for 5 seconds)		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. I_{AS} = 4 A, V_{DD} = 50 V, L = 27 mH, R_G = 25 Ω, starting T_J = 25°C.
3. $I_{SD} \leq 4$ A, di/dt ≤ 200 A/μs, $V_{DD} \leq BV_{DSS}$, Starting T_J = 25°C.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction−to−Case, Max.	1.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient, Max.	90	

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDU5N60NZTU	FDU5N60NZ	IPAK	Tube	N/A	N/A	75 units

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain−to−Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V, T_J = 25°C	600	–	–	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	–	0.6	–	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 600 V, V_{GS} = 0 V	–	–	50	μA
		V_{DS} = 480 V, T_C = 125°C	–	–	100	
I_{GSS}	Gate−to−Body Leakage Current	V_{GS} = ±25 V, V_{DS} = 0 V	–	–	±10	μA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	3.0	–	5.0	V
$R_{DS(on)}$	Static Drain−to−Source On Resistance	V_{GS} = 10 V, I_D = 2 A	–	1.65	2.00	Ω
g_{FS}	Forward Transconductance	V_{DS} = 20 V, I_D = 2 A	–	5	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	–	450	600	pF
C_{oss}	Output Capacitance		–	50	65	
C_{rss}	Reverse Transfer Capacitance		–	5	7.5	
$Q_{g(tot)}$	Total Gate Charge at 10 V	V_{DS} = 400 V, I_D = 4 A, V_{GS} = 10 V (Note 4)	–	10	13	nC
Q_{gs}	Gate−to−Source Gate Charge		–	2.5	–	
Q_{gd}	Gate−to−Drain “Miller” Charge		–	4	–	
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 250 V, I_D = 4 A, V_{GS} = 10 V, R_G = 25 Ω (Note 4)	–	15	40	ns
t_r	Turn−On Rise Time		–	20	50	
$t_{d(off)}$	Turn−Off Delay Time		–	35	80	
t_f	Turn−Off Fall Time		–	20	50	
DRAIN−SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuous Drain to Source Diode Forward Current		–	–	4	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		–	–	16	
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 4 A	–	–	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 4 A, dI_F/dt = 100 A/μs	–	230	–	ns
Q_{rr}	Reverse Recovery Charge		–	0.9	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of Operating Temperature Typical Characteristics.

TYPICAL CHARACTERISTICS

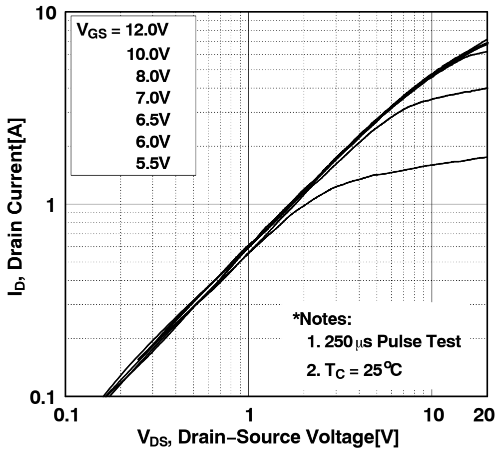


Figure 1. On−Region Characteristics

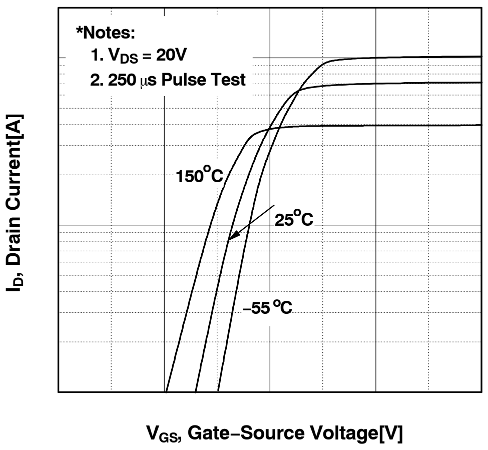


Figure 2. Transfer Characteristics

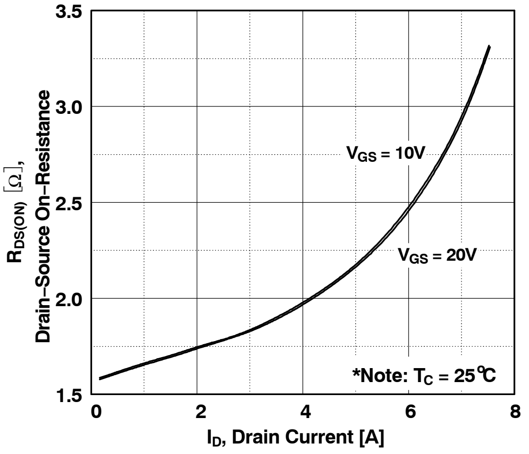


Figure 3. On−Resistance Variation vs. Drain Current and Gate Voltage

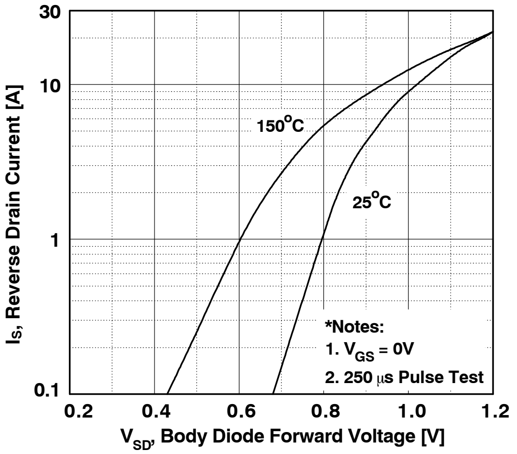


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

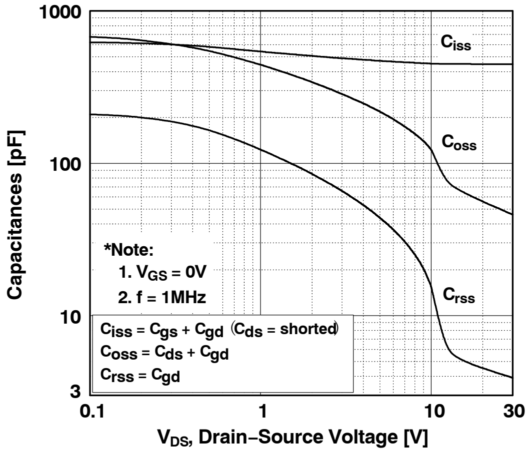


Figure 5. Capacitance Characteristics

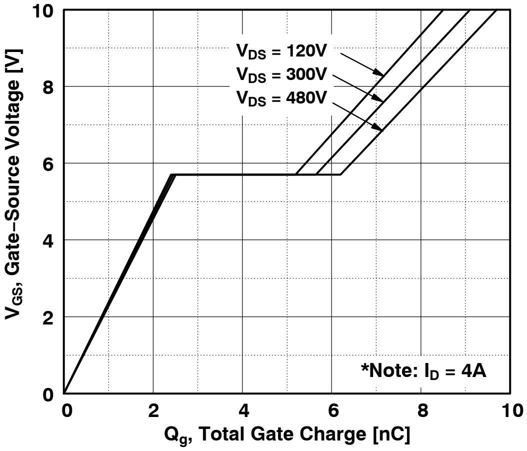


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS

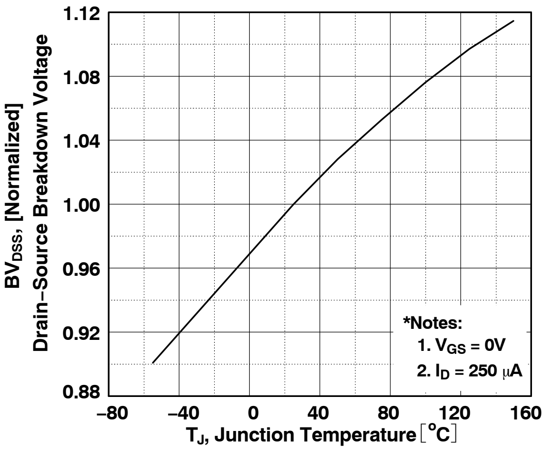


Figure 7. Breakdown Voltage Variation vs. Temperature

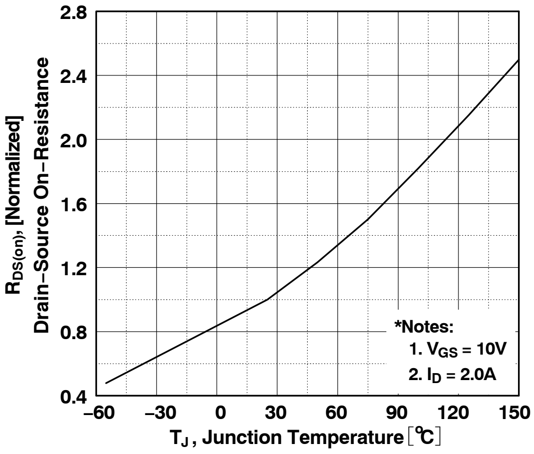


Figure 8. On−Resistance Variation vs. Temperature

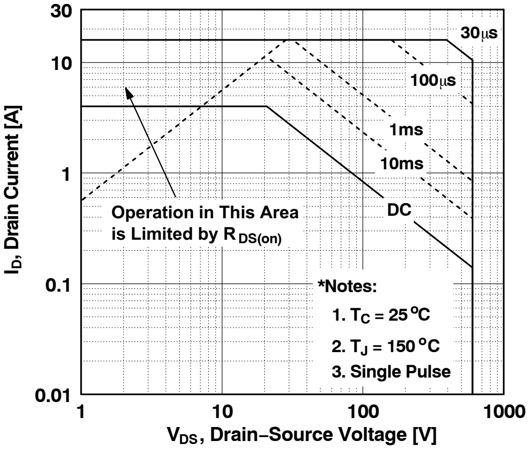


Figure 9. Maximum Safe Operating Area

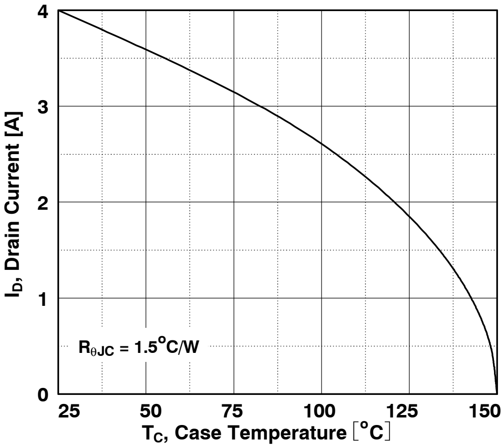


Figure 10. Maximum Drain Current vs. Case Temperature

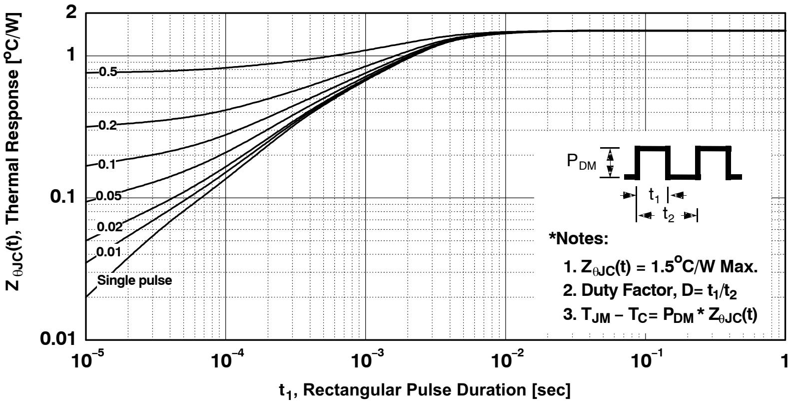


Figure 11. Transient Thermal Response Curve

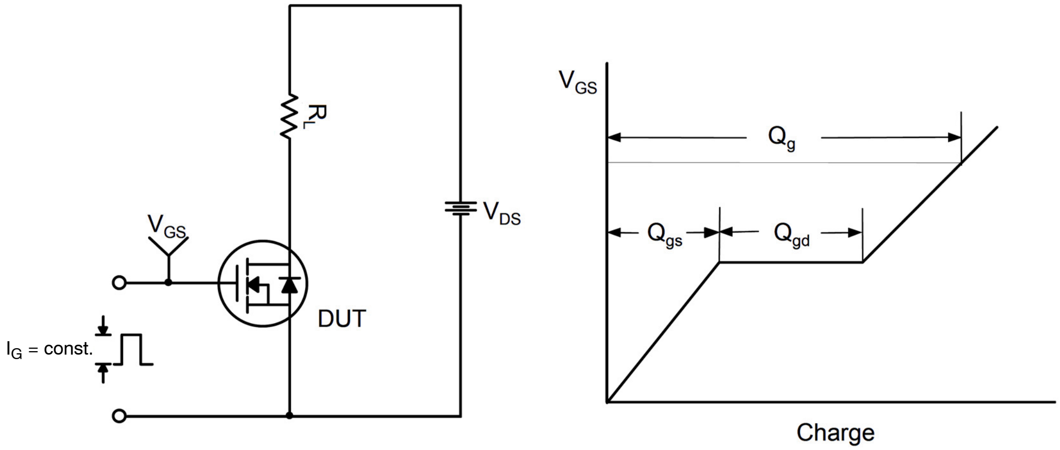


Figure 12. Gate Charge Test Circuit & Waveform

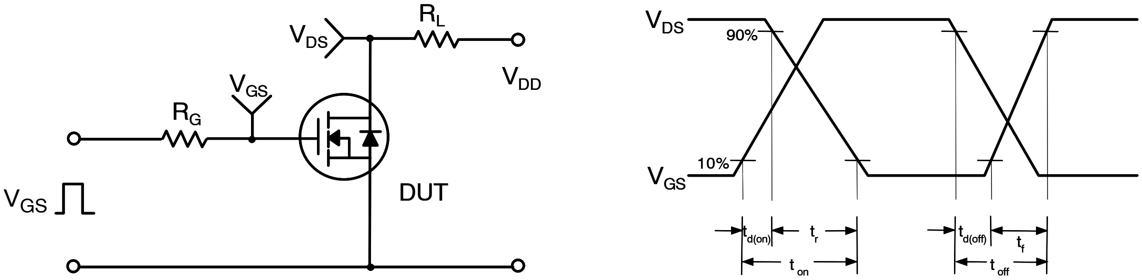


Figure 13. Resistive Switching Test Circuit & Waveforms

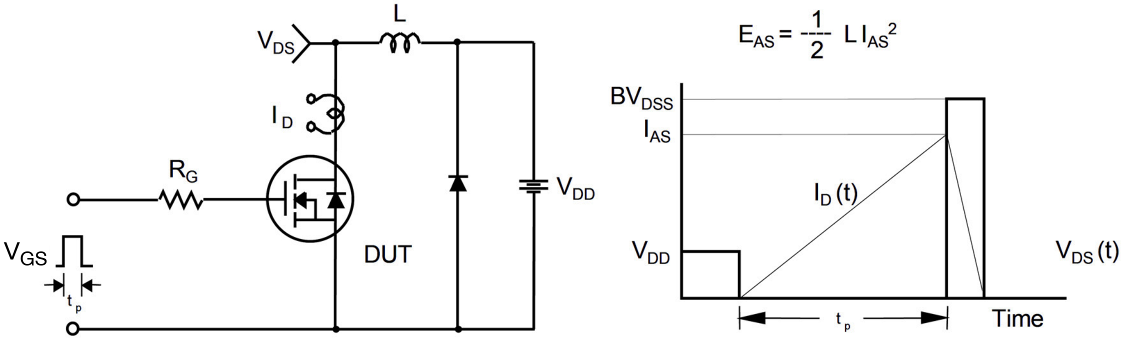


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

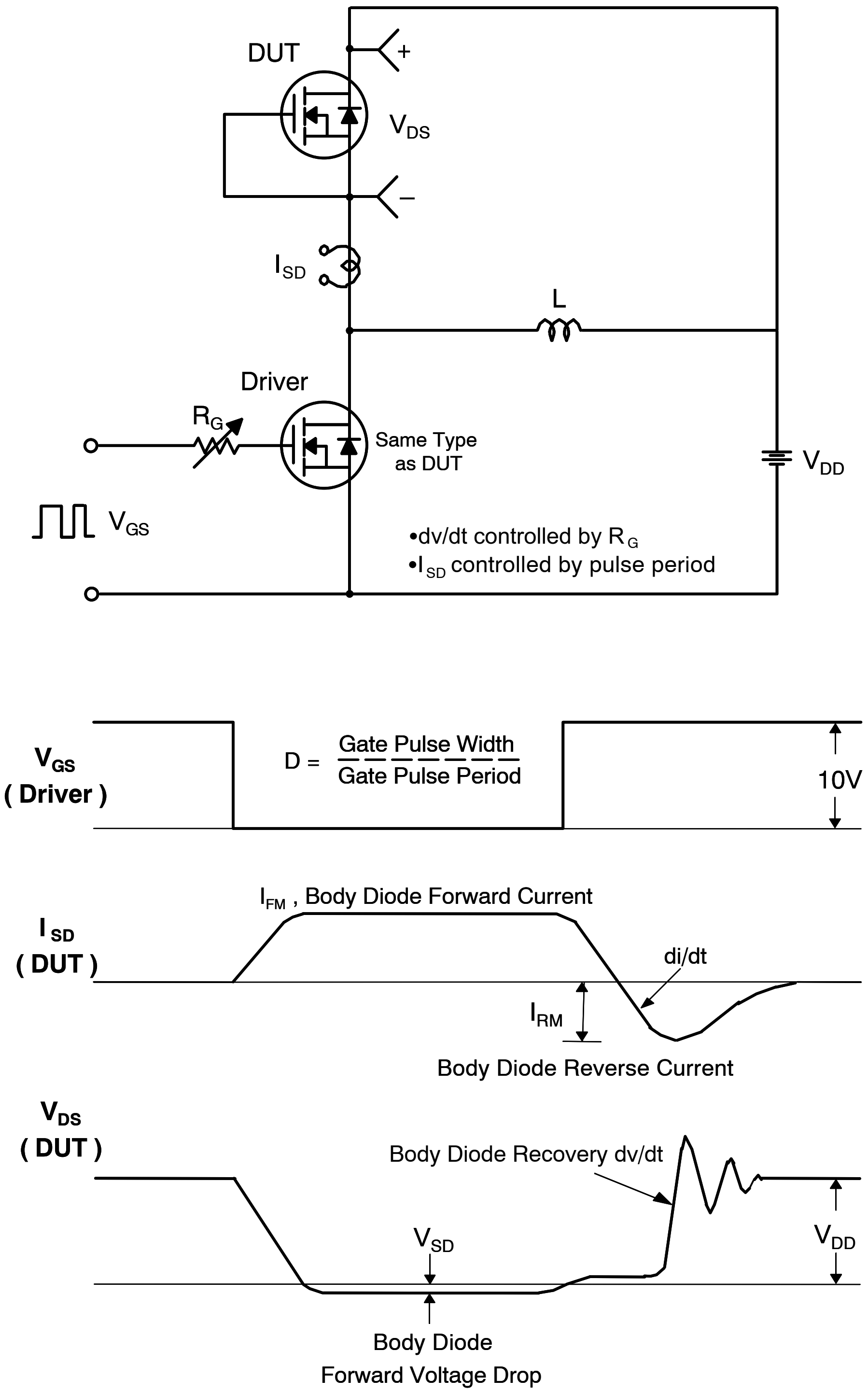
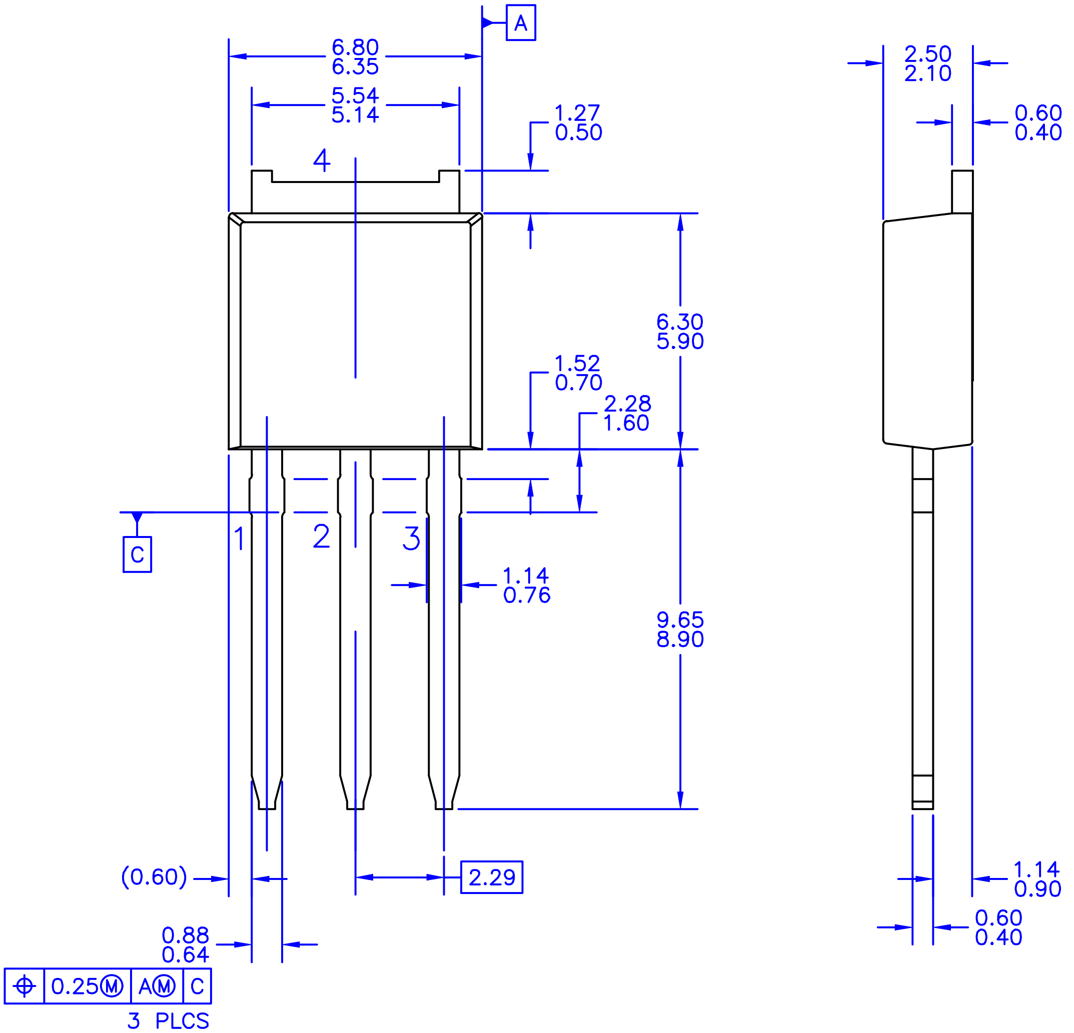
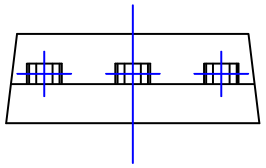


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

PACKAGE DIMENSIONS

DPAK3 (IPAK)
CASE 369AR
ISSUE O





NOTES: UNLESS OTHERWISE SPECIFIED

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C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M−1994.

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