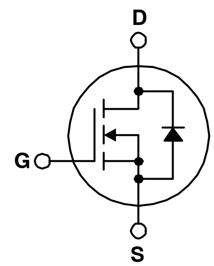
DATA SHEET
www.onsemi.com

MOSFET – N-Channel, SUPERFET® II

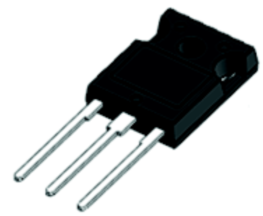
800 V, 46 A, 85 mΩ

FCH085N80

V_{DS}	$R_{DS(ON)}$ MAX	I_D MAX
800 V	85 mΩ @ 10 V	46 A



N-CHANNEL MOSFET



TO−247−3LD
CASE 340CH

Description

SuperFET II MOSFET is **onsemi**'s brand−new high voltage super−junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on−resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET II MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications.

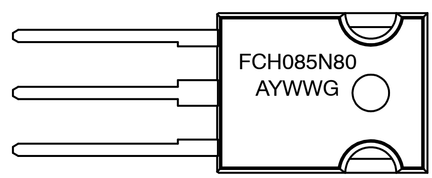
Features

- Typ. $R_{DS(on)}$ = 67 mΩ
- 850 V @ T_J = 150°C
- Ultra Low Gate Charge (Typ. Q_g = 196 nC)
- Low E_{OSS} (Typ. 18 µJ @ 400 V)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)}$ = 568 pF)
- 100% Avalanche Tested
- These Devices are Pb−Free and are RoHS Compliant

Applications

- AC−DC Power Supply
- LED Lighting

MARKING DIAGRAM



FCH085N80	= Specific Device Code
A	= Assembly Location
Y	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

August, 2024 − Rev. 4
Publication Order Number:
FCH085N80/D

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Parameter		Value	Unit
V_{DSS}	Drain to Source Voltage		800	V
V_{GSS}	Gate to Source Voltage	– DC	±20	V
		– AC (f > 1 Hz)	±30	
I_D	Drain Current:	– Continuous (T_C = 25°C)	46	A
		– Continuous (T_C = 100°C)	29	
I_{DM}	Drain Current:	– Pulsed (Note 1)	138	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		1701	mJ
I_{AS}	Avalanche Current (Note 2)		9.2	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		4.4	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt (Note 3)		20	
P_D	Power Dissipation	(T_C = 25°C)	446	W
		Derate Above 25°C	3.5	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		–55 to + 150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8″ from Case for 5 seconds		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse–width limited by maximum junction temperature.
2. I_{AS} = 9.2 A, V_{DD} = 50 V, R_G = 25 Ω, starting T_J = 25 °C.
3. $I_{SD} \leq$ 46 A, di/dt ≤ 200 A/μs, $V_{DD} \leq BV_{DSS}$, starting T_J = 25 °C.

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Packing Method	Reel Size	Tape Width	Quantity
FCH085N80–F155	FCH085N80	TO–247 G03	Tube	N/A	N/A	30 Units

THERMAL CHARACTERISTICS

Symbol	Parameter	FCH085N80–F155	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.28	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	40.0	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 1 mA, T_J = 25°C	800	–	–	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 1 mA, Referenced to 25°C	–	0.8	–	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 800 V, V_{GS} = 0 V	–	–	25	μA
		V_{DS} = 640 V, V_{GS} = 0 V, T_C = 125 °C	–	–	250	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	–	–	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 4.6 mA	2.5	–	4.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 23 A	–	67	85	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 20 V, I_D = 23 A	–	55	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 100 V, V_{GS} = 0 V, f = 1 MHz	–	8140	10825	pF
C_{oss}	Output Capacitance		–	255	340	pF
C_{rss}	Reverse Transfer Capacitance		–	10	–	pF
C_{oss}	Output Capacitance	V_{DS} = 480 V, V_{GS} = 0 V, f = 1 MHz	–	1000	–	pF
$C_{oss(eff.)}$	Effective Output Capacitance	V_{DS} = 0 V to 480 V, V_{GS} = 0 V	–	728	–	pF
$Q_{g(tot)}$	Total Gate Charge at 10 V	V_{DS} = 640 V, I_D = 46 A, V_{GS} = 10 V (Note 4)	–	196	255	nC
Q_{gs}	Gate to Source Gate Charge		–	40	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	72	–	nC
ESR	Equivalent Series Resistance	f = 1 MHz	–	0.8	–	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 400 V, I_D = 46 A, V_{GS} = 10 V, R_g = 4.7 Ω (Note 4)	–	45	100	ns
t_r	Turn–On Rise Time		–	55	120	ns
$t_{d(off)}$	Turn-Off Delay Time		–	160	330	ns
t_f	Turn–Off Fall Time		–	35	80	ns
DRAIN-SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuous Source to Drain Diode Forward Current		–	–	46	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		–	–	138	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 46 A	–	–	1.2	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 46 A, di_F/dt = 100 A/μs	–	800	–	ns
Q_{rr}	Reverse Recovery Charge		–	32	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

TYPICAL CHARACTERISTICS

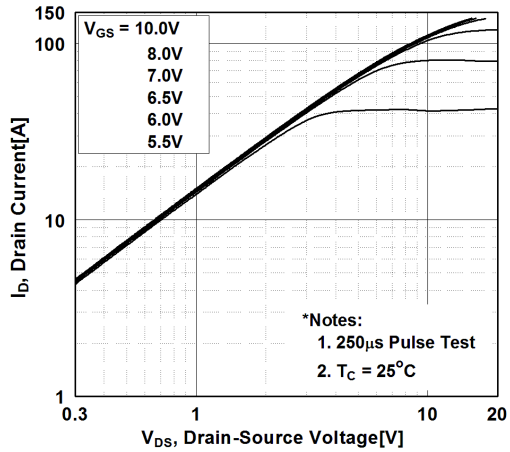


Figure 1. On−Region Characteristics

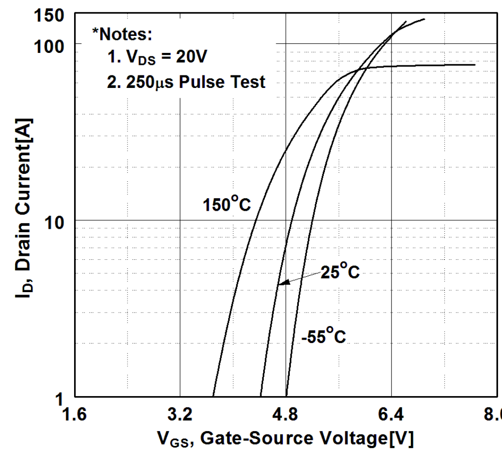


Figure 2. Transfer Characteristics

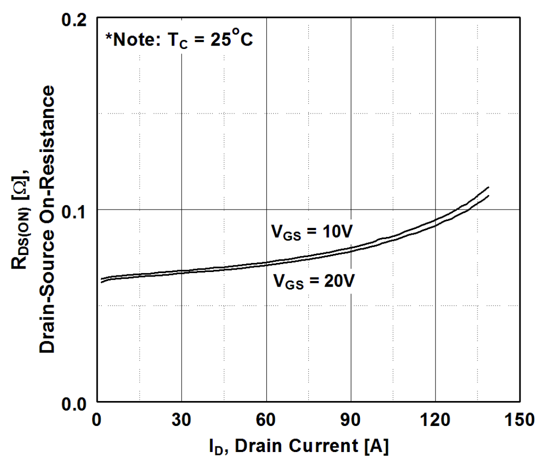


Figure 3. On−Resistance Variation vs. Drain Current and Gate Voltage

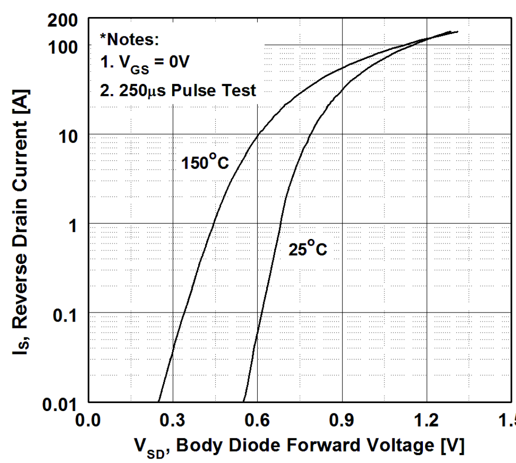


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

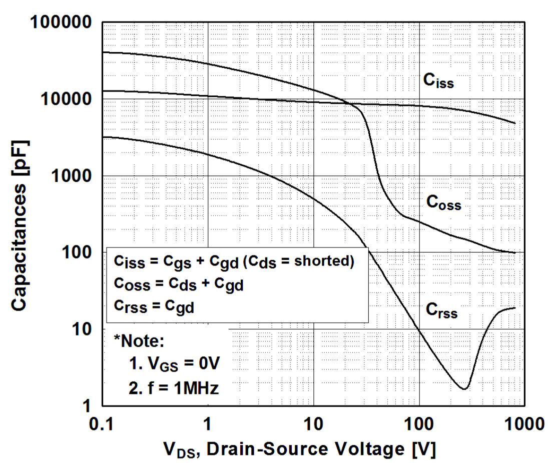


Figure 5. Capacitance Characteristics

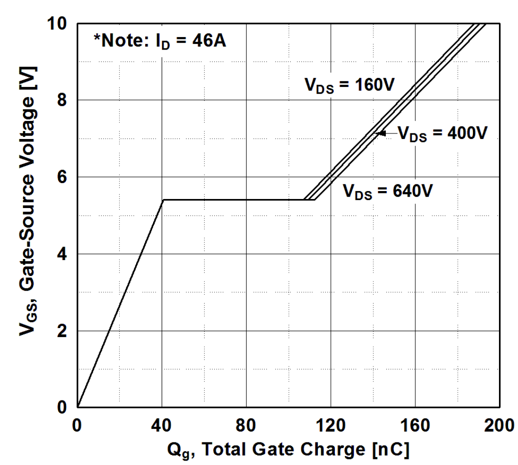


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS

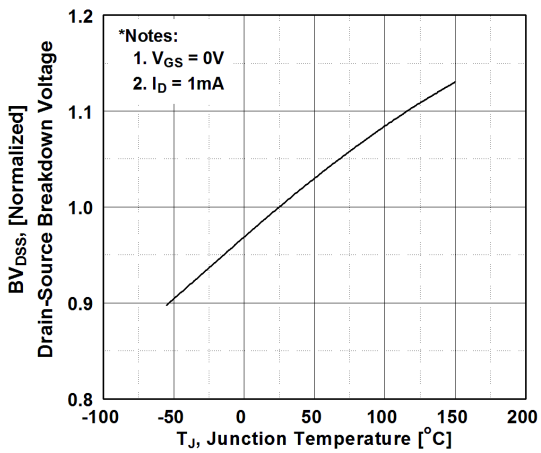


Figure 7. Breakdown Voltage Variation vs. Temperature

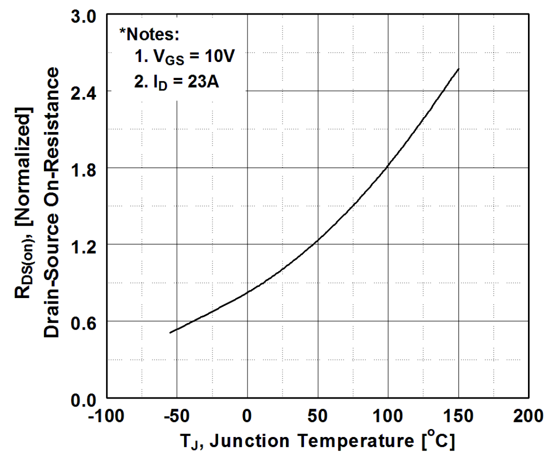


Figure 8. On−Resistance Variation vs. Temperature

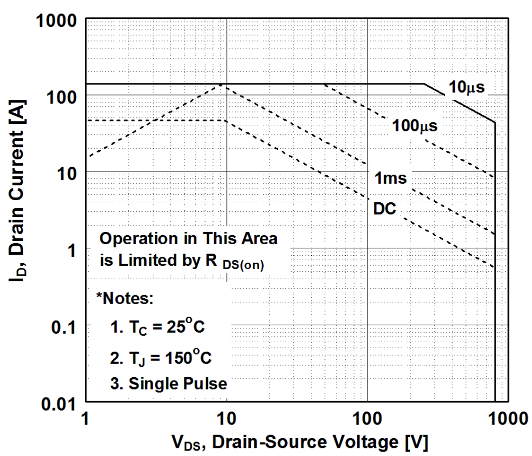


Figure 9. Maximum Safe Operating Area

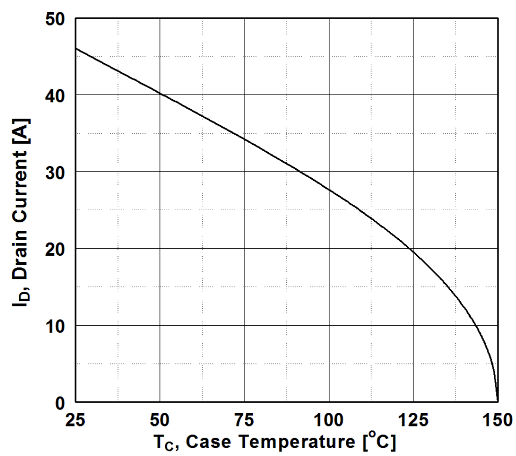


Figure 10. Maximum Drain Current vs. Case Temperature

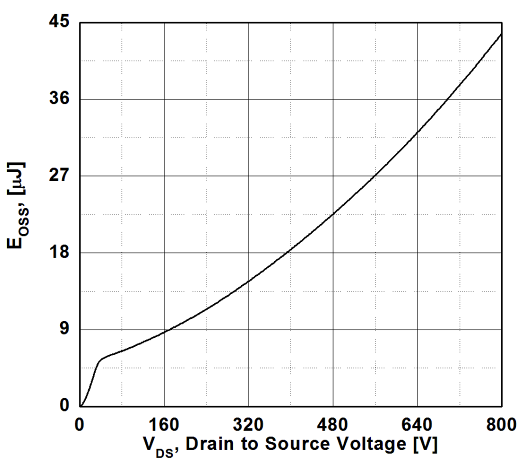


Figure 11. Eoss vs. Drain to Source Voltage

TYPICAL CHARACTERISTICS

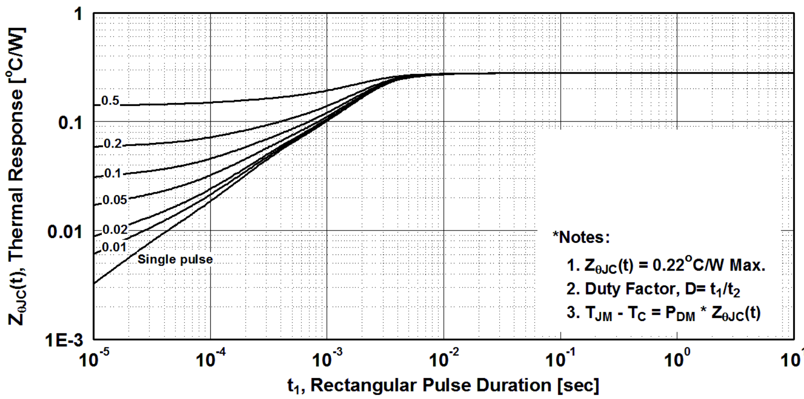


Figure 12. Transient Thermal Response Curve

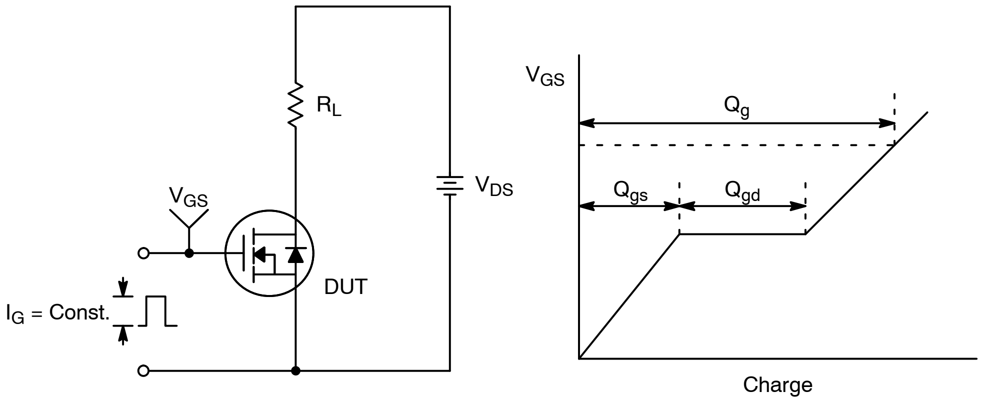


Figure 13. Gate Charge Test Circuit & Waveform

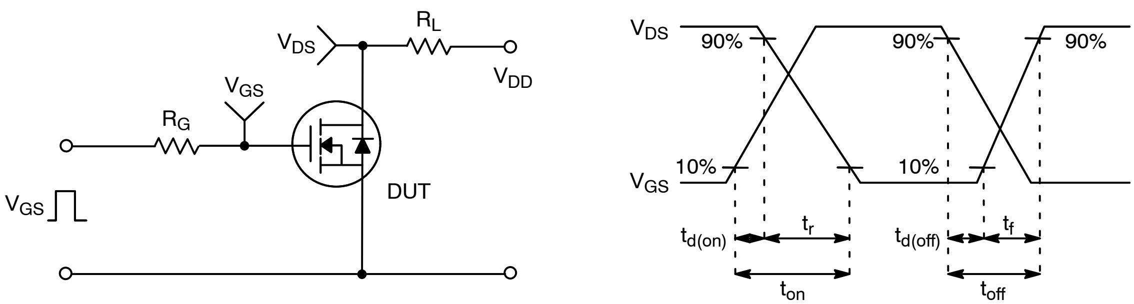


Figure 14. Resistive Switching Test Circuit & Waveforms

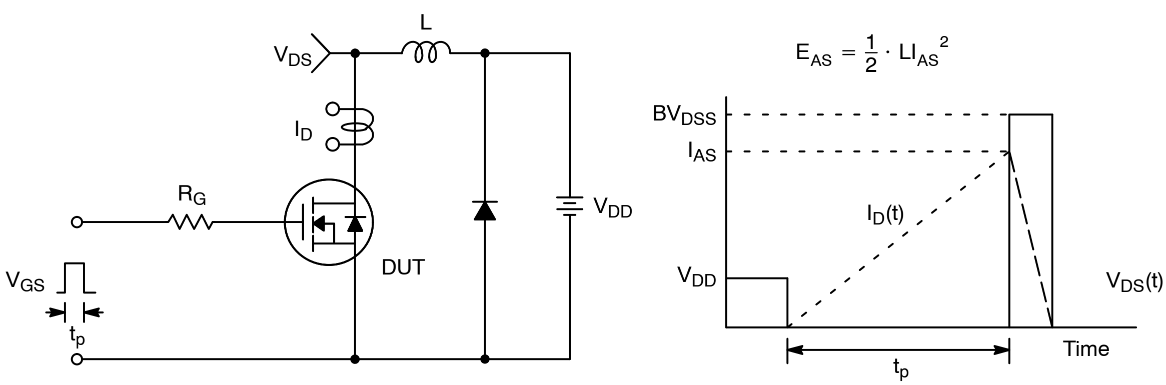


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

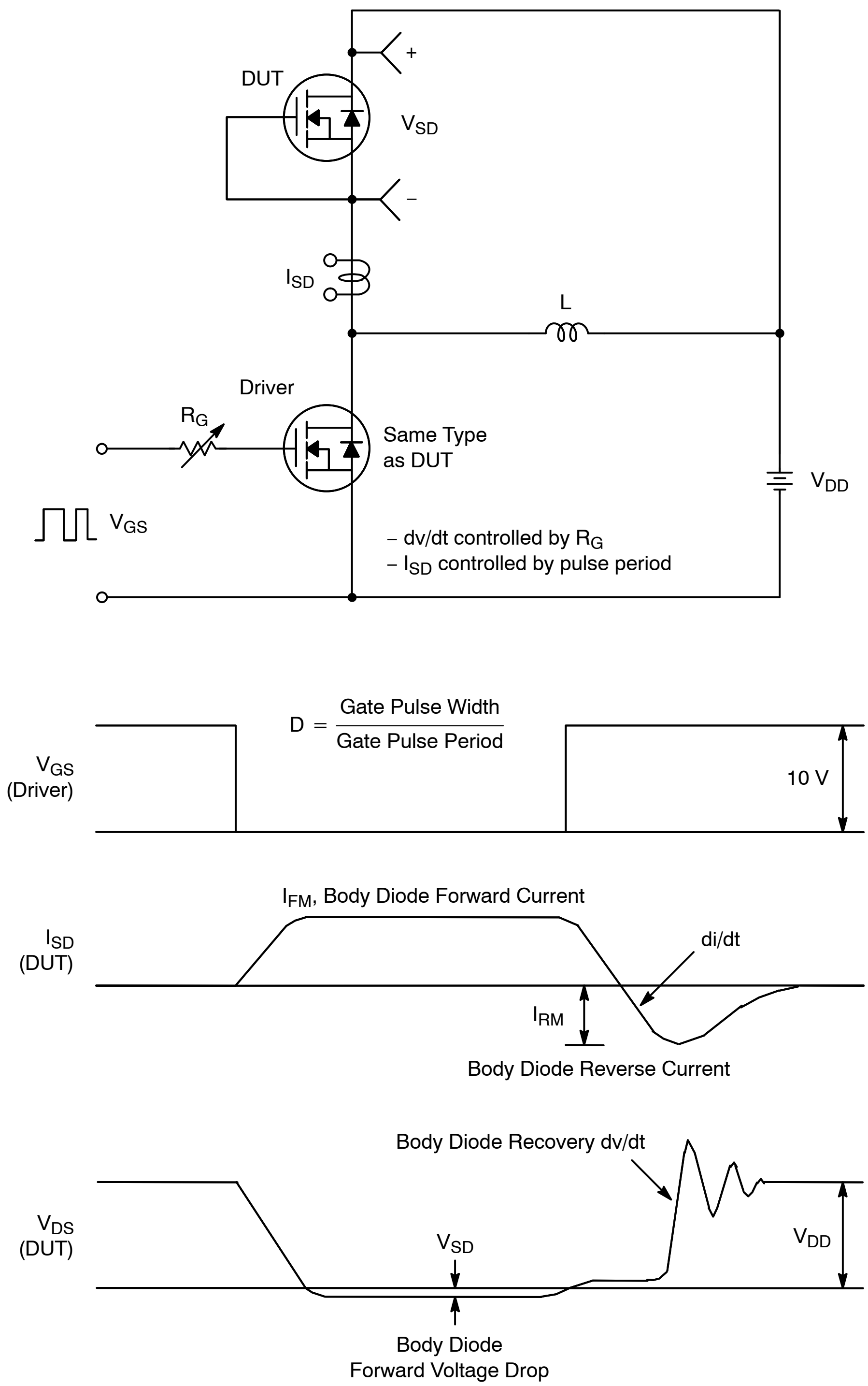
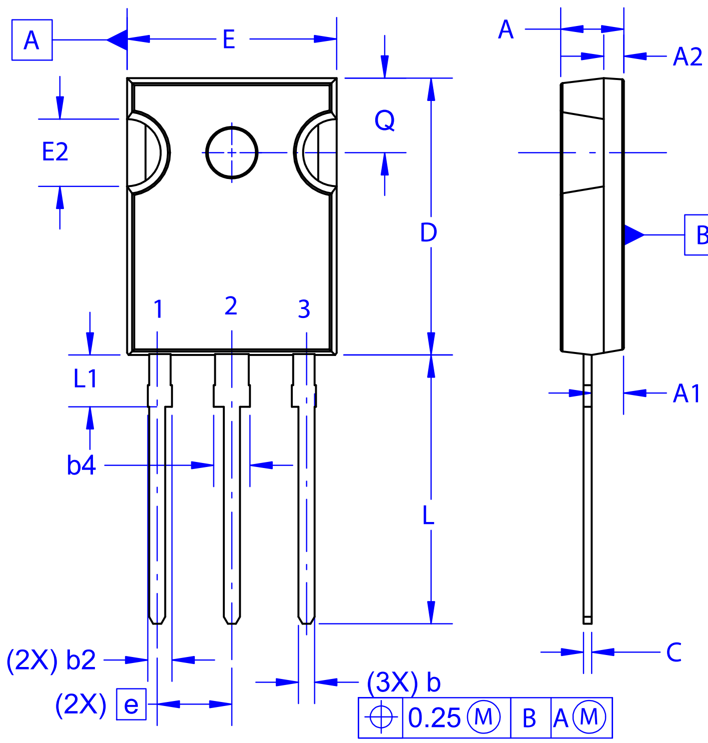
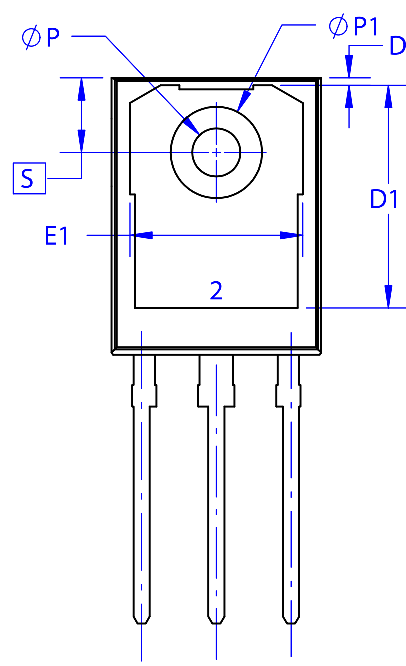


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

TO−247−3LD
CASE 340CH
ISSUE A

DATE 09 OCT 2019



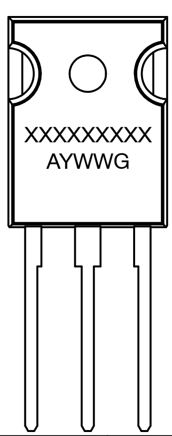


NOTES: UNLESS OTHERWISE SPECIFIED.

A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DRAWING CONFORMS TO ASME Y14.5 - 2009.
D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.58	4.70	4.82
A1	2.29	2.475	2.66
A2	1.40	1.50	1.60
D	20.32	20.57	20.82
E	15.37	15.62	15.87
E2	4.96	5.08	5.20
e	~	5.56	~
L	19.75	20.00	20.25
L1	3.69	3.81	3.93
ØP	3.51	3.58	3.65
Q	5.34	5.46	5.58
S	5.34	5.46	5.58
b	1.17	1.26	1.35
b2	1.53	1.65	1.77
b4	2.42	2.54	2.66
c	0.51	0.61	0.71
D1	13.08	~	~
D2	0.51	0.93	1.35
E1	12.81	~	~
ØP1	6.61	6.73	6.85

GENERIC
MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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