AR0143AT

1/4-Inch 1.3 Mp Digital Image Sensor

ON Semiconductor®

www.onsemi.com

General Description

ON Semiconductor's AR0143AT is a 1/4−inch CMOS digital image sensor with a 1344Hx968V active−pixel array. It captures images in either linear, high dynamic range, or LFM modes, with a rolling−shutter readout. The LFM mode eliminates high frequency LED flicker in the image allowing Traffic Sign Reading (TSR) algorithms to operate in all lighting conditions. It includes sophisticated camera functions such as in−pixel binning, windowing and both video and single frame modes. It is designed for both low light and high dynamic range scene performance, with sensor fault detection features that can enable ASIL B compliance for the camera system. It is programmable through a simple two−wire serial interface. The AR0143AT produces extraordinarily clear, sharp digital pictures, and its ability to capture both continuous video and single frames makes it the perfect choice for a wide range of applications, including automotive ADAS, automotive scene viewing, and 720p HDR video.

Features

- Key Technologies:
  - Automotive grade Backside Illuminated Pixel
  - LED Flicker Mitigation mode
  - Sensor Fault Detection for ASIL−B Compliance
  - Up to 4−exposure HDR at 1344x968 and 30 fps
- Latest 3.0 μm Back Side Illuminated (BSI) pixel with ON Semiconductor DR−Pix™ technology
- Data interfaces: up to 4−lane MIPI CSI−2, Parallel, or up to 4−lane high speed pixel interface (HiSPi) serial interface (SLVS and HiVCM)
- Advanced HDR with flexible exposure ratio control
- LED Flicker Mitigation (LFM) mode
- Selectable automatic or user controlled black level control
- Frame to frame switching among up to 4 contexts to enable multi−function systems
- Spread−spectrum input clock support
- Multi−Camera synchronization support
- AEC−Q100 Grade 2 Qualified

Applications

- Automotive ADAS
- High dynamic range imaging
- Mirror Replacement
- ADAS + Viewing Fusion

Table 1. KEY PARAMETERS

Parameter	Value
Optical format	1/4 inch
Maximum resolution	1344 x 968 (1.3 Mp)
Shutter type	Electronic Rolling Shutter (ERS)
Pixel size	3 μm
Pixel output interfaces	12−bit parallel MIPI CSI−2 Up to 4−lane HiSPi with SLVS and HiVCM
Output formats	12−bit Uncompressed Linear 20−bit Uncompressed HDR 10−bit Companded Linear 16−bit, 14−bit, or 12−bit Companded HDR
Control interface	2−wire, Serial Control 100 kHz/400 kHz/1 MHz
Input clock range	6−50 MHz in PLL mode
Default Frame Rate	30 fps (Note 1)
Output pixel clock maximum	78 MHz
Responsivity	28.7 Ke−/lux−s (Note 2)
SNRmax	36.5 dB (LCG), 34.7 dB (HCG)
Max Dynamic Range	>140 dB, 4−exposure (Note 3)
Packaging options	9 mm x 9 mm iBGA
Operating temp. range	−40°C to 110°C Ambient −40°C to 125°C Junction
Supply voltage	I/O 1.8 V or 2.8 V Digital 1.2 V Analog 2.8 V HiSPi 0.4 V or 1.8 V
Power consumption	<330 mW typical (1344x968, 3exp HDR, 30 fps)

1. Maximum frame rates will depend on various sensor settings including resolution, output format, and output pixel clock.
2. D65, 670 IRCF
3. Assumes off−chip HDR linearization

Table 2. ORDERING INFORMATION

Part Number	Product Description
AR0143ATSC00XUEA0-DPBR	1.3 MP, 1/4”, 0deg 9x9 iBGA, Dry pack with PF
AR0143ATSC00XUEA0-DRBR	1.3 MP, 1/4”, 0deg 9x9 iBGA, Dry pack without PF
AR0143ATSC00XUEA0-TPBR	1.3 MP, 1/4”, 0deg 9x9 iBGA, Tape & reel with PF
AR0143ATSC00XUEA0-TRBR	1.3 MP, 1/4”, 0deg 9x9 iBGA, Tape & reel without PF
AR0143ATSC00XUEAH3-GEVB	1.3 MP, 1/4”, 0deg 9x9 iBGA, Parallel/MIPI, HB
MARS1−AR0143ATS−GEVB	1.3 MP, 1/4”, 0deg 9x9 iBGA, MARS Parallel
MARS1−AR0143ATSCS−GEVB	1.3 MP, 1/4”, 0deg 9x9 iBGA, MARS MIPI

NOTE: Contact the ON Semiconductor sales or marketing representative to discuss your specific requirements.

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GENERAL DESCRIPTION

The ON Semiconductor AR0143AT can be operated in its default mode or programmed for frame size, exposure, gain, and other parameters. The default mode output is a 720p−resolution image at 30 frames per second (fps) in HDR mode through the parallel or serial output ports. In linear mode, it outputs 12−bit uncompressed or 10−bit compressed raw data, using either the parallel or serial output ports. In high dynamic range (HDR) mode, it outputs 12, 14, or 16−bit compressed data, or 20−bit linearized data using either the parallel or serial output ports. The device may be operated in video (master) mode or in single frame trigger mode. The LFM mode is used to minimize the impact of LED flicker for applications where there is dynamic LED lighting, such as TSR, and is output in linear mode.

FRAME_VALID and LINE_VALID signals are output on dedicated pins, along with a synchronized pixel clock in parallel mode.

The AR0143AT has additional ASIL features, including but not limited to: two on-board independent temperature sensor, start−up tests, memory BIST, analog and digital CRC, and test patterns. Optional register information and histogram statistic information can be embedded in the first and last 2 lines of the image frame.

The sensor is designed to operate in a wide junction temperature range (−40°C to + 125°C).

FUNCTIONAL OVERVIEW

The AR0143AT is a 1/4 inch progressive-scan sensor that generates a stream of pixel data at a constant frame rate. It uses an on−chip, phase-locked loop (PLL) that can be option− ally enabled to generate all internal clocks from a single master input clock running between 6 and 50 MHz. The maximum output pixel rate is 600 Mb/s in serial modes, and 78 Mp/s in parallel modes, corresponding to a clock rate of 78 MHz. Figure 1 shows a block diagram of the sensor.

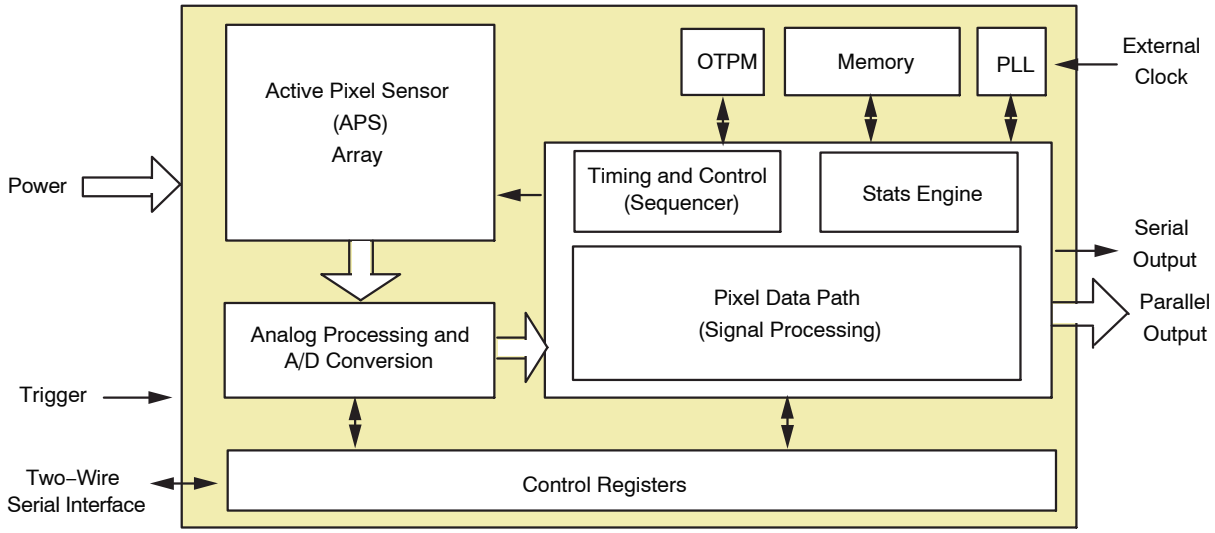


Figure 1. Block Diagram

User interaction with the sensor is through the two−wire serial bus, which communicates with the array control, analog signal chain, and digital signal chain. The core of the sensor is a 1.3 Mp BSI Active−Pixel Sensor array. The timing and control circuitry sequences through the rows of the array, resetting and then reading each row in turn. In the time interval between resetting a row and reading that row, the pixels in the row inte− grate incident light. The exposure is controlled by varying the time interval between reset and readout. Once a row has been read, the data from the columns is sequenced through an analog signal chain (providing offset correction and gain), and then through an analog−to−digital converter (ADC). The output from the ADC is a 13−bit value for each pixel in the array. The ADC output passes through a digital processing signal chain (which provides further data path corrections and applies digital gain). The sensor also offers a high dynamic range mode of operation where multiple images are combined on−chip to produce a single image at 20−bit per pixel value. A compressing mode is further offered to allow this 20−bit pixel value to be transmitted to the host system as a 12− or 14− or 16−bit value with close to zero loss in image quality.

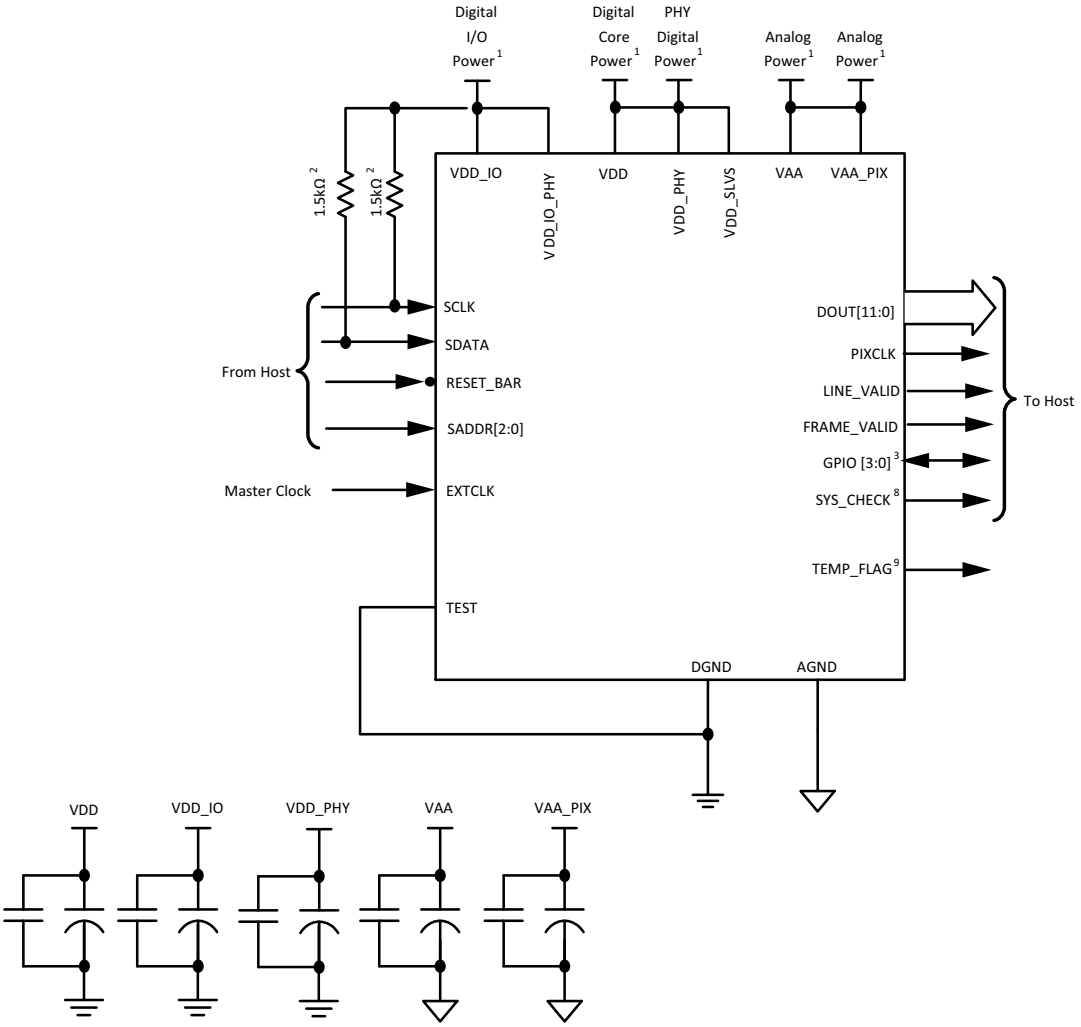


Figure 2. Typical Configuration, Parallel

1. All power supplies must be adequately decoupled.
2. ON Semiconductor recommends a resistor value of 1.5 kΩ, but a greater value may be used for slower two−wire speed.
3. GPIO[2:0] can be left unconnected if not used. GPIO3 should be tied to DGND if not used.
4. The serial output data interface pads can be left unconnected when the parallel output interface is used. The serial output data supply pads should remain connected and powered appropriately.
5. ON Semiconductor recommends that 0.1 μF and 10 μF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on lay− out and design considerations. Refer to the AR0143AT demo headboard schematics for circuit recommendations.
6. ON Semiconductor recommends that analog power planes are placed in a manner such that coupling with the digital power planes is minimized.
7. I/O signals voltage must be configured to match VDD_IO voltage to minimize any leakage currents.
8. Leave unconnected if not used.
9. Open drain. Leave unconnected if not used.

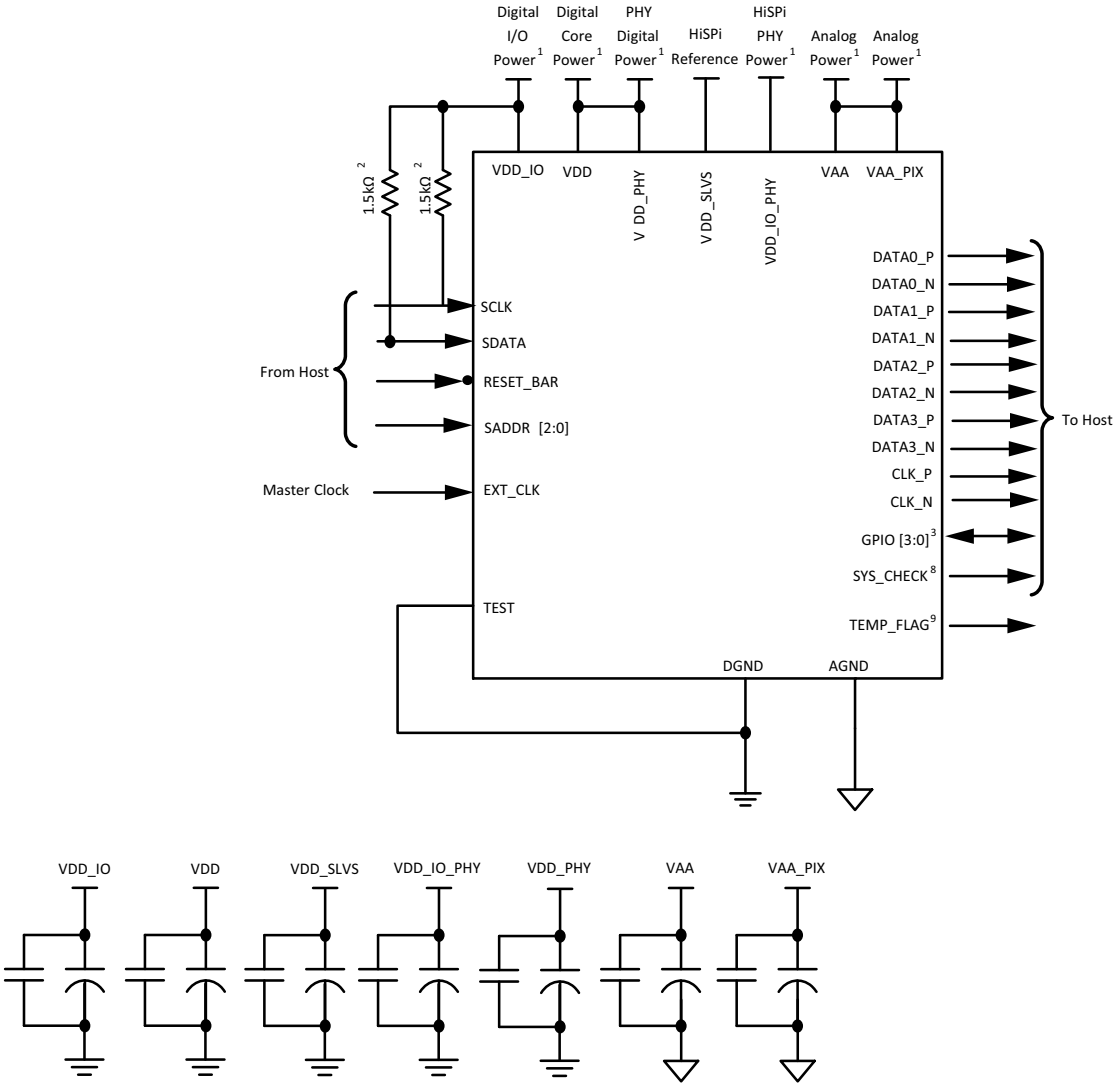


Figure 3. Typical Configuration, 4−Lane HiSPi

1. All power supplies must be adequately decoupled.
2. ON Semiconductor recommends a resistor value of 1.5 kΩ, but a greater value may be used for slower two−wire speed.
3. GPIO[2:0] can be left unconnected if not used. GPIO3 should be tied to DGND if not used.
4. The parallel interface output pads can be left unconnected when the serial output interface is used.
5. ON Semiconductor recommends that 0.1 μF and 10 μF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on lay− out and design considerations. Refer to the AR0143AT demo headboard schematics for circuit recommendations.
6. ON Semiconductor recommends that analog power planes are placed in a manner such that coupling with the digital power planes is minimized.
7. I/O signals voltage must be configured to match VDD_IO voltage to minimize any leakage currents.
8. Leave unconnected if not used.
9. Open drain. Leave unconnected if not used.

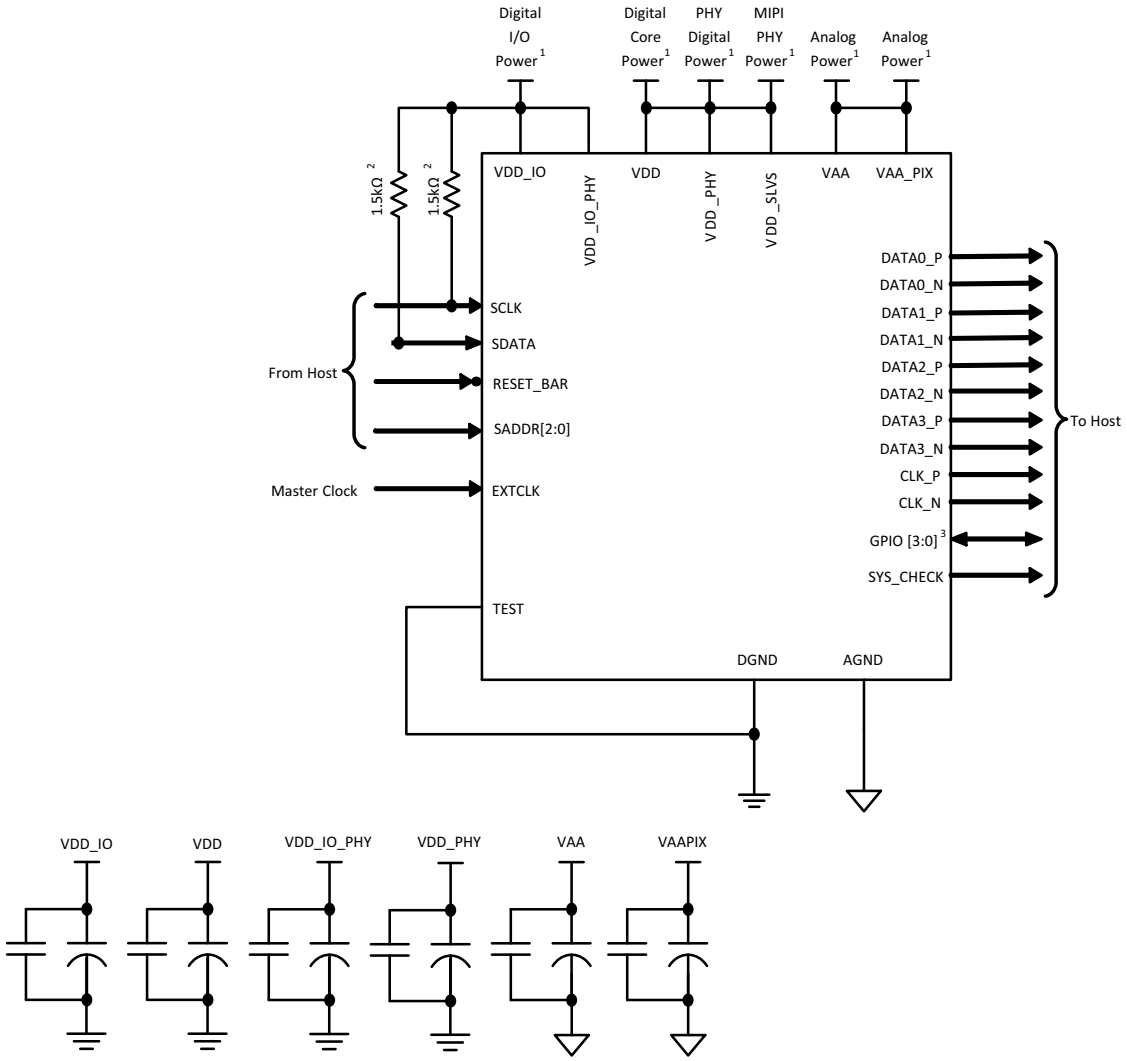


Figure 4. Typical Configuration, 4−Lane MIPI

1. All power supplies must be adequately decoupled.
2. ON Semiconductor recommends a resistor value of 1.5 kΩ, but a greater value may be used for slower two−wire speed.
3. GPIO[2:0] can be left unconnected if not used. GPIO3 should be tied to DGND if not used.
4. The parallel interface output pads can be left unconnected if the serial output interface is used.
5. ON Semiconductor recommends that 0.1 μF and 10 μF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on lay− out and design considerations. Refer to the AR0143AT demo headboard schematics for circuit recommendations.
6. ON Semiconductor recommends that analog power planes are placed in a manner such that coupling with the digital power planes is minimized.
7. I/O signals voltage must be configured to match VDD_10 voltage to minimize any leakage currents.

PIXEL DATA FORMAT

Pixel Array Structure

While the sensor's format is 1344x968, additional active columns and active rows are included for use when horizontal or vertical mirrored readout is enabled, to allow readout to start on the same pixel. The pixel adjustment is always performed for mono− chrome or color versions. The active area is surrounded with optically transparent dummy pixels to improve image uniformity within the active area. Not all dummy pixels or barrier pixels can be read out.

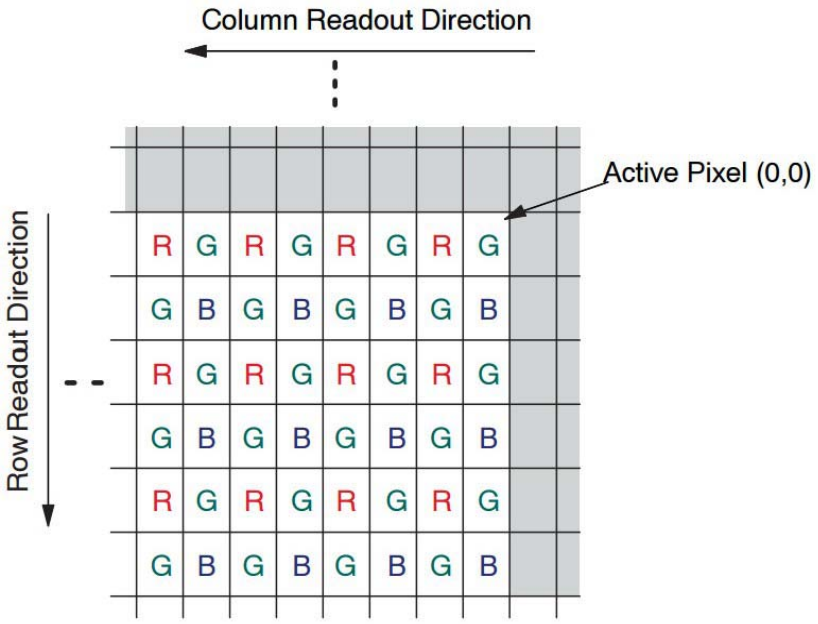


Figure 5. Pixel Color Pattern Detail (Top Right Corner)

Default Readout Order

By convention, the sensor core pixel array is shown with pixel (0,0) in the top right corner (see Figure 5). This reflects the actual layout of the array on the die. Also, the first readable pixel location of the sensor in default condition is that of physical pixel address (256, 6). This first readable pixel location corresponds to the register X_ADDR_START_ (R0x3004)=0x0000 and the register Y_ADDR_START_ (R0x3002)=0x0000.

When the sensor is imaging, the active surface of the sensor faces the scene as shown in Figure 6. When the image is read out of the sensor, it is read one row at a time, with the rows and columns sequenced as shown in Figure 6.

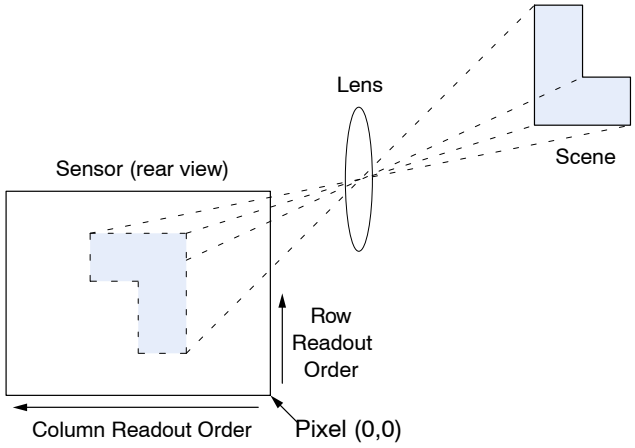


Figure 6. Imaging a Scene

OPERATING MODES AND FEATURES

For a complete description, recommendations, and usage guidelines for product features, refer to the AR0143AT Developer Guide.

3.0 μm Dual Conversion Gain Pixel

To improve the low light performance and keep the high dynamic range, a large (3.0 μm) dual conversion gain pixel is implemented for better image optimization. With a dual conversion gain pixel, the conversion gain of the pixel may be dynamically changed to better adapt the pixel response based on dynamic range of the scene. This gain can be switched manually or automatically by an external auto exposure control module.

Dual conversion gain can also be controlled independently for each exposure in HDR mode, allowing a mixture of high conversion gain (HCG) and low conversion gain (LCG) across multiple exposures.

Resolution

The active array supports a maximum of 1344 x 968 pixels to support 720p resolution. Utilizing a 3.0 μm pixel will result in an optical format of 1/4−inch.

Frame Rate

At full resolution, the AR0143AT is capable of running up to 50 fps in parallel, MIPI, and HiSPi modes, depending on the number of exposures. The AR0143AT has a maximum frame rate of 30 fps at full resolution in 4−exposure HDR, and 50 fps at full resolution in 3−exposure HDR, 2−exposure HDR, and linear modes.

High Dynamic Range

The AR0143AT can operate in an HDR mode to acquire video data using ON Semiconductor's multi−exposure technology. This allows the sensor to handle >140 dB of dynamic range in 4−exposure mode (assuming off−chip HDR linearization). The sensor also features a linear or standard dynamic range (SDR) mode where a single image is captured. In HDR mode, the sensor sequentially captures up to four exposures by maintaining separate read and reset pointers that are interleaved within the rolling shutter readout. The intermediate pixel values are stored in line buffers while waiting for all the exposure values to be present. As soon as all exposure values are available, they are combined to create a linearized 20−bit value for each pixel's response. This 20−bit value may be output directly or optionally companded to 16, 14 or 12-bits before output.

The exposure ratios may be set to 2x, 4x, 8x, 16x, or 32x, or can be individually controlled per exposure to allow a wide range of flexible exposure ratios. The individual exposure ratio control for T1, T2, T3, and T4 is limited by the number of line buffers allocated to each exposure.

Options to output each individual exposures only, or pixel interleaved data are also available. Individual exposures may be read out in a line interleaved mode as described in the Line Interleaved Mode section.

Motion Compensation and Linearization

In typical multi−exposure HDR systems, motion artifacts can be created when objects move during the integration time of the exposures used to construct the image. When this happens, edge artifacts can potentially be visible and might look like a tearing or ghosting effect. To correct for this issue, the AR0143AT incorporates both motion compensation and improved digital lateral overflow (DLO2) algorithm, but with the addition of individual color knee points as well as an additional knee point for the fourth exposure.

LED Flicker Mitigation (LFM)

LED sign flicker causes traffic signs to be incorrectly read in bright daylight conditions as the LEDs may be illuminated when the sensor is not integrating. The AR0143AT includes a new mode, LFM, for reading these signs. In LFM mode, the effective sensitivity of the pixel can be controlled and reduced, enabling exposure times to be extended. On AR0143AT variants with color CFAs, color will be maintained in the sensor output to aid in sign discrimination.

Multi−camera Synchronization

AR0143AT supports multi−camera synchronization Slave modes. The Slave modes support synchronization of multiple cameras within 8 pixel clocks from the beginning of FRAME_VALID/LINE_VALID from sensors without reducing the maximum frame rate. This feature saves the line memory buffer at the host system to combine a multiple of video input streams from the sensors.

Slave Mode

The slave mode feature of the AR0143AT supports triggering the start of a frame readout from an input signal that is supplied from an external ASIC. The slave mode signal allows for precise control of frame rate and register change updates.

Context Switching and Register Updates

The user has the option of using the highly configurable context memory, or a simplified implementation in which only a subset of registers is available for switching. The AR0143AT supports a highly configurable context switching RAM of size 256 x 16. Within this Context Memory, changes to registers within the chip may be stored. The register set for each context must be the same, but the number of contexts and registers per context are limited only by the size of the context memory.

Alternatively, the user may switch between two predefined register sets A and B by writing to a context switch change bit. When the context switch is configured to context A the sensor will reference the context A registers. If the context switch is changed from A to B during the readout of frame n, the sensor will then reference the context B coarse_integration_time registers in frame n+1 and all other context B registers at the beginning of reading frame

n+2. The sensor will show the same behavior when changing from context B to context A.

Embedded Data and Statistics

The AR0143AT has the capability to output image data and statistics within the frame timing. There are two types of information embedded within the frame readout.

Embedded data can be enabled on two rows before the active image pixels are displayed, and shows the current settings for the part.

Embedded statistics can be enabled on the two rows after the active image pixels are displayed, and include frame identifiers and histogram information for that image. This can be used by off−chip auto−exposure blocks to make decisions about exposure adjustment.

Histograms for up to two independent regions of interest (ROIs) can be tracked per frame, with programmable registers determining their size and location. Two compression methods are available for the histogram data, with one being a new logarithmic compression scheme that enables more detailed data for dark portions of the image. Note that histogram information can be output for only one pixel plane at a time.

In addition to histograms, the output image frame can be split into a virtual grid of up to 16 ROIs that can each provide the average pixel value for that region. Each of these averages can be included with the statistics embedded in the output image, allowing a simple exposure metric for each region to be generated.

Black Level Control/Correction

Black level correction can optionally be automatically controlled by the AR0143AT; the default setting is for automatic black level calibration to be enabled. The automatic black level correction measures the average value of pixels from a set of optically black pixel rows in the image sensor. The pixels are averaged as if they were light sensitive and passed through the appropriate gain. This line average is then digitally low−pass filtered over many frames to remove temporal noise and random instabilities associated with this measurement. The optically black lines may be read out, bypassing the datapath, for off−chip analysis. The automatic black level correction can be disabled and the black level set manually via register settings. Manual black level settings are frame synchronized to the next start of frame.

Row and Column Correction

Row and column noise correction is applied automatically by the image sensor on a frame by frame basis. Re−triggering of correction circuits due to settings or temperature changes are not necessary. The digital gain can be applied before HDR linearization for white balancing, and after HDR linearization for increasing scene brightness.

Defective Pixel Tracking

Defective Pixel Tracking is intended to tag defective pixels by tagging them by assigning them a ‘0’ value. The defect pixel tracking feature supports up to 200 defects. The locations of defective pixels are stored in a table on chip during the manufacturing process; this table is accessible through the two−wire serial interface. There is no provision for later augmenting the defect table entries. The defect pixels identified during manufacture can be read from on−chip ROM via the 2−wire control interface. In order for the defective pixel tracking feature to function properly, NOISE_PEDESTAL (R0x30FE) must be set to 0.

Analog/Digital Gains

A programmable analog gain of 0.125x to 8x applied simultaneously to all color channels is featured along with two digital gain stages. The two digital gain stages can be programmed both on a per color channel basis and as a global gain. The first digital gain stage is recommended for AWB function, and is programmable from 1x to 16x. The second digital gain stage is recommended as a global gain function, and is programmable from 1x to 3.99x.

Skipping/Binning Modes

The AR0143AT supports subsampling. Subsampling allows the sensor to read out a smaller set of active pixels by either skipping, binning, or summing pixels within the readout window. Horizontal binning is achieved in the digital readout. The sensor samples the combined two adjacent pixels within the same color plane. Vertical row binning is applied in the pixel readout. Row binning can be configured as two rows within the same color plane. Pixel skipping can be configured up to two in both the x−direction and y−direction. Skipping pixels in the x−direction will not reduce the row time. Skipping pixels in the y−direction will reduce the number of rows from the sensor effectively reducing the frame time. Skipping will introduce image artifacts from aliasing. The AR0143AT supports row wise vertical binning. Row wise vertical summing is not supported.

ASIL / ISO26262 Support Features

The AR0143AT incorporates many features assisting the achievement of ASIL−B system compliance by a system that integrates it. Please refer to the AR0143AT Safety Manual for more information.

SYSTEM INTERFACES

This section describes the AR0143AT interfaces. Note that all output port options may not be available on all packaging options.

HiSPi Pixel Output Port

The AR0143AT provides a 4−lane HiSPi pixel output port with support for SLVS and HiVCM modes. Supported configurations are described in Table 3. Additional information is provided in the ON Semiconductor HiSPi Protocol and Physical Layer documents.

Table 3. HiSPi PROTOCOL SUPPORT

Lanes	Width	Data type	Protocols	Max. Mbps/lane	Notes
1, 2, or 4	20-bit	Bayer/RAW	SP-packetized SP-streaming Streaming−S	750 Mbps	HDR output mode (uncompressed)
1, 2, or 4	16-bit	Bayer/RAW	SP-packetized SP-streaming Streaming−S	750 Mbps	HDR output mode (compressed)
1, 2, or 4	14-bit	Bayer/RAW	SP-packetized SP-streaming Streaming−S	750 Mbps	HDR output mode (compressed)
1, 2, or 4	12-bit	Bayer/RAW	SP-packetized SP-streaming Streaming−S	750 Mbps	HDR output mode (compressed) SDR (linear) mode (uncompressed)

MIPI CSI−2 Pixel Output Port

The AR0143AT provides a 4−lane MIPI CSI-2 pixel output port. The AR0143AT is compliant to the following MIPI standards:

- MIPI Alliance Standard for CSI−2 version 1.0
- MIPI Alliance Standard for D−PHY version 1.1

The data protocol support is per Table 4. Please contact ON Semiconductor for additional information.

Table 4. MIPI PROTOCOL SUPPORT

Lanes	Width	Data Type	Max. Mbps/lane	Notes
1, 2, or 4	20−bit	Bayer/RAW	600 Mbps	HDR output mode (uncompressed)
1, 2, or 4	16-bit	Bayer/RAW	600 Mbps	HDR output mode (compressed)
1, 2, or 4	14-bit	Bayer/RAW	600 Mbps	HDR output mode (compressed)
1, 2, or 4	12-bit	Bayer/RAW	600 Mbps	HDR output mode (compressed) SDR (linear) mode (uncompressed)
1, 2, or 4	10-bit	Bayer/RAW	600 Mbps	SDR (linear) mode (compressed)

Parallel Pixel Output Port

The AR0143AT provides a 12−bit data pixel output port with frame and line valid signals. HDR data is companded to 12−bit, and 12−bit SDR (non-HDR) data may be output via this port.

Note that the parallel port cannot be used to output combinations of individual T1/T2/ T3/T4 exposures on a per frame basis.

Line Interleaved Output

The AR0143AT will have the capability to output the T1, T2, T3, and T4 exposures separately, in a line interleaved format. The purpose of this is to enable off chip HDR linear combination and processing.

Embedded data and statistics are also supported in line interleaved mode. See the AR0143AT Developer Guide for more information.

Two−Wire Sensor Control Interface

The two−wire serial interface bus enables read/write access to control and status registers within the AR0143AT. The interface protocol uses a master/slave model in which a master controls one or more slave devices. The sensor acts as a slave device. The master generates a clock (SCLK) that is an input to the sensor and is used to synchronize transfers. Data is transferred between the master and the slave on a bidirectional signal (SDATA). SDATA is pulled up to VDD_IO off−chip by a 1.5 kΩ resistor. Either the slave or master device can drive SDATA LOW—the interface protocol determines which device is allowed to drive SDATA at any given time.

The protocols described in the two−wire serial interface specification allow the slave device to drive SCLK LOW; the AR0143AT uses SCLK as an input only and therefore never drives it LOW.

Protocol

Data transfers on the two−wire serial interface bus are performed by a sequence of low−level protocol elements:

8. A (repeated) start condition
9. A slave address/data direction byte
10. An (a no) acknowledge bit
11. A message byte
12. A stop condition

The bus is idle when both SCLK and SDATA are HIGH. Control of the bus is initiated with a start condition, and the bus is released with a stop condition. Only the master can generate the start and stop conditions.

Start Condition

A start condition is defined as a HIGH−to−LOW transition on SDATA while SCLK is HIGH. At the end of a transfer, the master can generate a start condition without previously generating a stop condition; this is known as a "repeated start" or "restart" condition.

Stop Condition

A stop condition is defined as a LOW−to−HIGH transition on SDATA while SCLK is HIGH.

Data Transfer

Data is transferred serially, 8 bits at a time, with the MSB transmitted first. Each byte of data is followed by an acknowledge bit or a no−acknowledge bit. This data transfer mechanism is used for the slave address/data direction byte and for message bytes.

One data bit is transferred during each SCLK clock period. SDATA can change when SCLK is LOW and must be stable while SCLK is HIGH.

Slave Address/Data Direction Byte

Bits [7:1] of this byte represent the device slave address and bit [0] indicates the data transfer direction. A "0" in bit [0] indicates a WRITE, and a "1" indicates a READ. The default slave addresses used by the AR0143AT are 0x20(write address) and 0x21 (read address) in accordance with the specification. An additional 7 alternate slave address can be selected by enabling and asserting the SADDR [2:0] inputs.

Message Byte

Message bytes are used for sending register addresses and register write data to the slave device and for retrieving register read data.

Acknowledge Bit

Each 8−bit data transfer is followed by an acknowledge bit or a no−acknowledge bit in the SCLK clock period following the data transfer. The transmitter (which is the master when writing, or the slave when reading) releases SDATA. The receiver indicates an acknowledge bit by driving SDATA LOW. As for data transfers, SDATA can change when SCLK is LOW and must be stable while SCLK is HIGH.

No Acknowledge Bit

The no−acknowledge bit is generated when the receiver does not drive SDATA LOW during the SCLK clock period following a data transfer. A no−acknowledge bit is used to terminate a read sequence.

Typical Sequence

A typical READ or WRITE sequence begins by the master generating a start condition on the bus. After the start condition, the master sends the 8−bit slave address/data direction byte. The last bit indicates whether the request is for a read or a write, where a "0" indicates a write and a "1" indicates a read. If the address matches the address of the slave device, the slave device acknowledges receipt of the address by generating an acknowledge bit on the bus.

If the request was a WRITE, the master then transfers the 16−bit register address to which the WRITE should take place. This transfer takes place as two 8−bit sequences and the slave sends an acknowledge bit after each sequence to indicate that the byte has been received. The master then transfers the data as an 8−bit sequence; the slave sends an acknowledge bit at the end of the sequence. The master stops writing by generating a (re)start or stop condition.

If the request was a READ, the master sends the 8−bit write slave address/data direction byte and 16−bit register address, the same way as with a WRITE request. The master then generates a (re)start condition and the 8−bit read slave address/data direction byte, and clocks out the register data, eight bits at a time. The master generates an acknowledge bit after each 8−bit transfer. The slave's internal register address is automatically incremented after every 8 bits are transferred. The data transfer is stopped when the master sends a no−acknowledge bit.

Single READ from Random Location

This sequence (Figure 7) starts with a dummy WRITE to the 16−bit address that is to be used for the READ. The master terminates the WRITE by generating a restart condition. The master then sends the 8−bit read slave address/data direction byte and clocks out one byte of register data. The master terminates the READ by generating a no−acknowledge bit followed by a stop condition. Figure 7 shows how the internal register address maintained by the AR0143AT is loaded and incremented as the sequence proceeds.

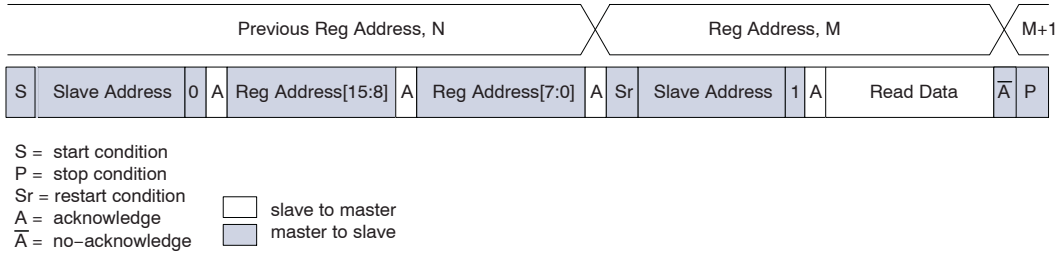


Figure 7. Single READ from Random Location

Single READ from Current Location

This sequence (Figure 8) performs a read using the current value of the AR0143AT internal register address. The master terminates the READ by generating a no−acknowledge bit followed by a stop condition. The figure shows two independent READ sequences.

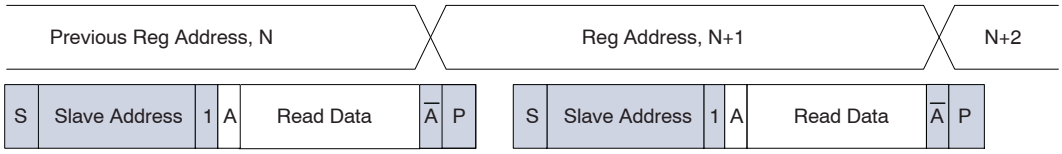


Figure 8. Single READ from Current Location

Sequential READ, Start from Random Location

This sequence (Figure 9) starts in the same way as the single READ from random location (Figure 7). Instead of generating a no−acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte READs until “L” bytes have been read.

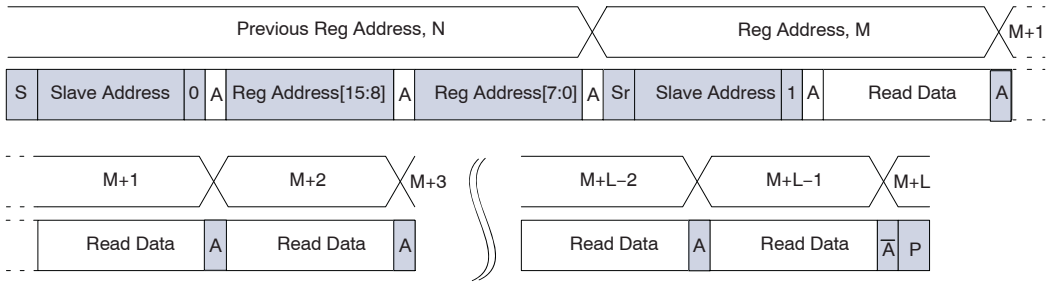


Figure 9. Sequential READ, Start from Random Location

Sequential READ, Start from Current Location

This sequence (Figure 10) starts in the same way as the single READ from current location (Figure 8). Instead of generating a no−acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte READs until “L” bytes have been read.

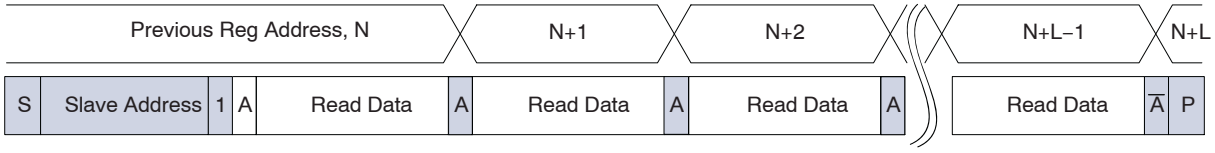


Figure 10. Sequential READ, Start from Current Location

Single WRITE to Random Location

This sequence (Figure 11) begins with the master generating a start condition. The slave address/data direction byte signals a WRITE and is followed by the HIGH then LOW bytes of the register address that is to be written. The master follows this with the byte of write data. The WRITE is terminated by the master generating a stop condition.

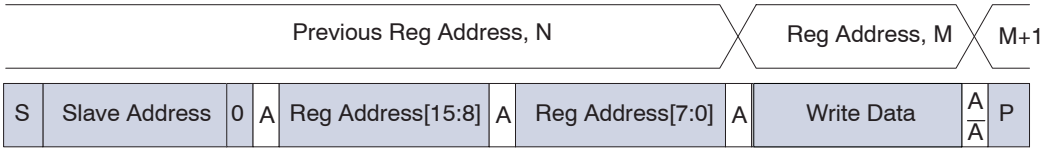


Figure 11. Single WRITE to Random Location

Sequential WRITE, Start at Random Location

This sequence (Figure 12) starts in the same way as the single WRITE to random location (Figure 11). Instead of generating a no−acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte WRITEs until “L” bytes have been written. The WRITE is terminated by the master generating a stop condition.

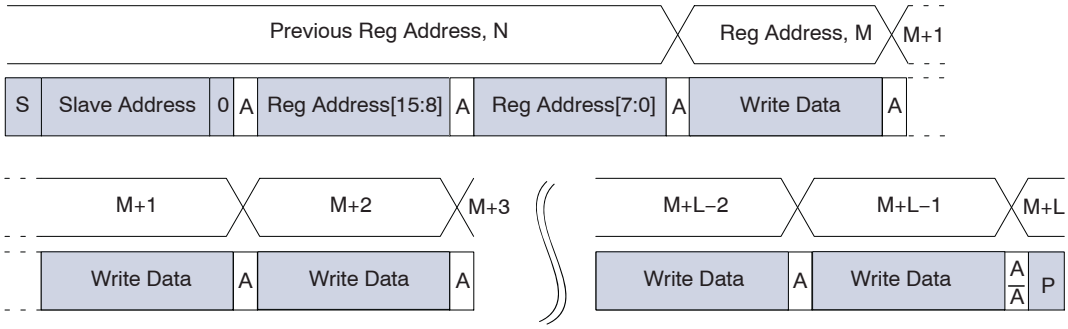


Figure 12. Sequential WRITE, Start at Random Location

Two−Wire Serial Register Interface

The electrical characteristics of the two−wire serial register interface (S_{CLK}, S_{DATA}) are shown in Figure 13 and Table 5.

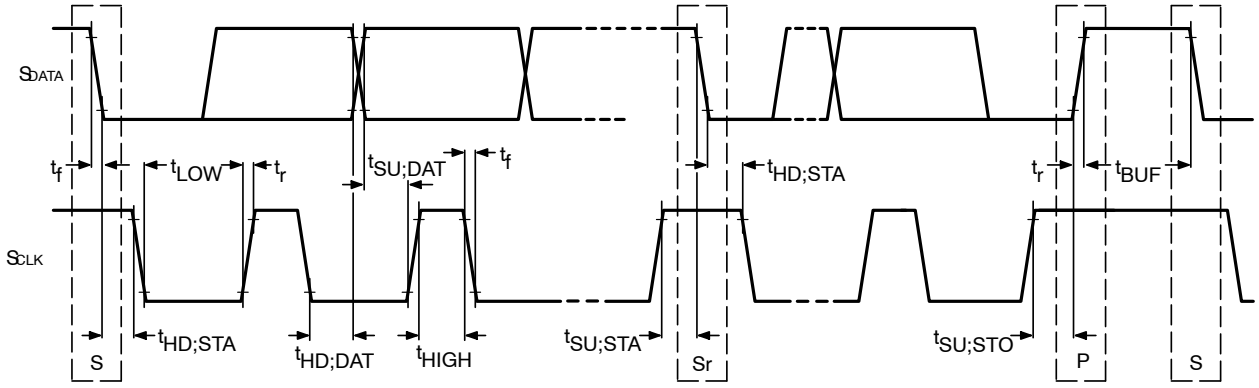


Figure 13. Two−Wire Serial Bus Timing Parameters

NOTE: Read sequence: For an 8−bit READ, read waveforms start after WRITE command and register address are issued.

Table 5. TWO−WIRE SERIAL BUS CHARACTERISTICS

fEXTCLK = 27 MHz; VDD = 1.2 V; VDD_IO = 2.8 V; VAA = 2.8 V; VAA_PIX = 2.8 V; T_A = 25°C

Parameter	Symbol	Standard Mode		Fast Mode		Fast Mode Plus		Unit
		Min	Max	Min	Max	Min	Max	
SCLK Clock Frequency	fSCL	0	100	0	400	0	1000	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	tHD;STA	4.0	–	0.6	–	0.26	–	µs
LOW period of the SCLK clock	tLOW	4.7	–	1.2	–	0.5	–	µs
HIGH period of the SCLK clock	tHIGH	4.0	–	0.6	–	0.26	–	µs
Set−up time for a repeated START condition	tSU;STA	4.7	–	0.6	–	0.26	–	µs
Data hold time	tHD;DAT	2 (Note 4)	3.45 (Note 5)	0 (Note 6)	0.9 (Note 5)	0 (Note 6)	–	µs
Data set-up time	tSU;DAT	250	–	100 (Note 6)	–	50 (Note 6)	–	ns
Rise time of both SDATA and SCLK signals	tr	–	1000	20 + 0.1Cb (Note 7)	300	20 + 0.1Cb (Note 7)	120	ns
Fall time of both SDATA and SCLK signals	tf	–	300	20 + 0.1Cb (Note 7)	300	20 + 0.1Cb (Note 7)	120	ns
Set−up time for STOP condition	tSU;STO	4.0	–	0.6	–	0.26	–	µs
Bus free time between a STOP and START condition	tBUF	4.7	–	1.3	–	0.5	–	µs
Capacitive load for each bus line	Cb	–	400	–	400	–	500	pF
Serial interface input pin capacitance	CIN_SI	–	3.3	–	3.3	–	3.3	pF
SDATA max load capacitance	CLOAD_SD	–	30	–	30	–	30	pF
SDATA pull−up resistor	RSD	1.5	4.7	1.5	4.7	1.5	4.7	kΩ

1. This table is based on I²C standard (v2.1 January 2000). Philips Semiconductor.
2. Two−wire control is I²C−compatible.
3. All values referred to V_{IHmin} = 0.9 VDD_IO and V_{ILmax} = 0.1 VDD_IO levels. Sensor EXCLK = 27 MHz.
4. A device must internally provide a hold time of at least 300 ns for the SDATA signal to bridge the undefined region of the falling edge of SCLK.
5. The maximum tHD;DAT has only to be met if the device does not stretch the LOW period (tLOW) of the SCLK signal.
6. A Fast−mode I²C−bus device can be used in a Standard−mode I²C−bus system, but the requirement tSU;DAT 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCLK signal. If such a device does stretch the LOW period of the SCLK signal, it must output the next data bit to the SDATA line tr max + tSU;DAT = 1000 + 250 = 1250 ns (according to the Standard−mode I²C−bus specification) before the SCLK line is released.
7. Cb = total capacitance of one bus line in pF.

I/O Timing

By default, the AR0143AT launches pixel data, FV, and LV with the falling edge of PIXCLK. The expectation is that the user captures DOUT[11:0], FV, and LV using the rising edge of PIXCLK.

See Figure 14 below and Tables 6–7 on pages 17–18 for I/O timing (AC) characteristics.

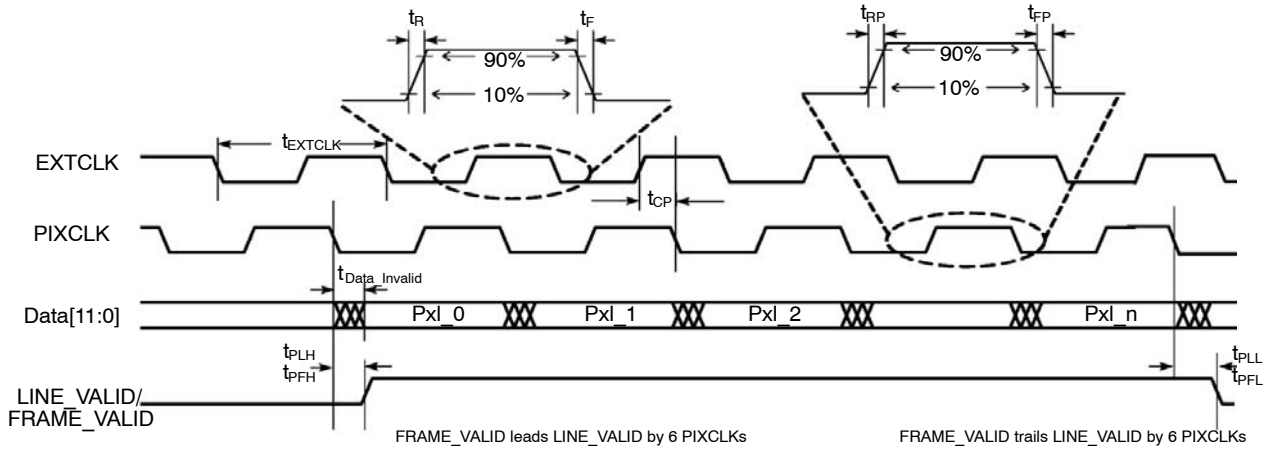


Figure 14. I/O Timing Diagram

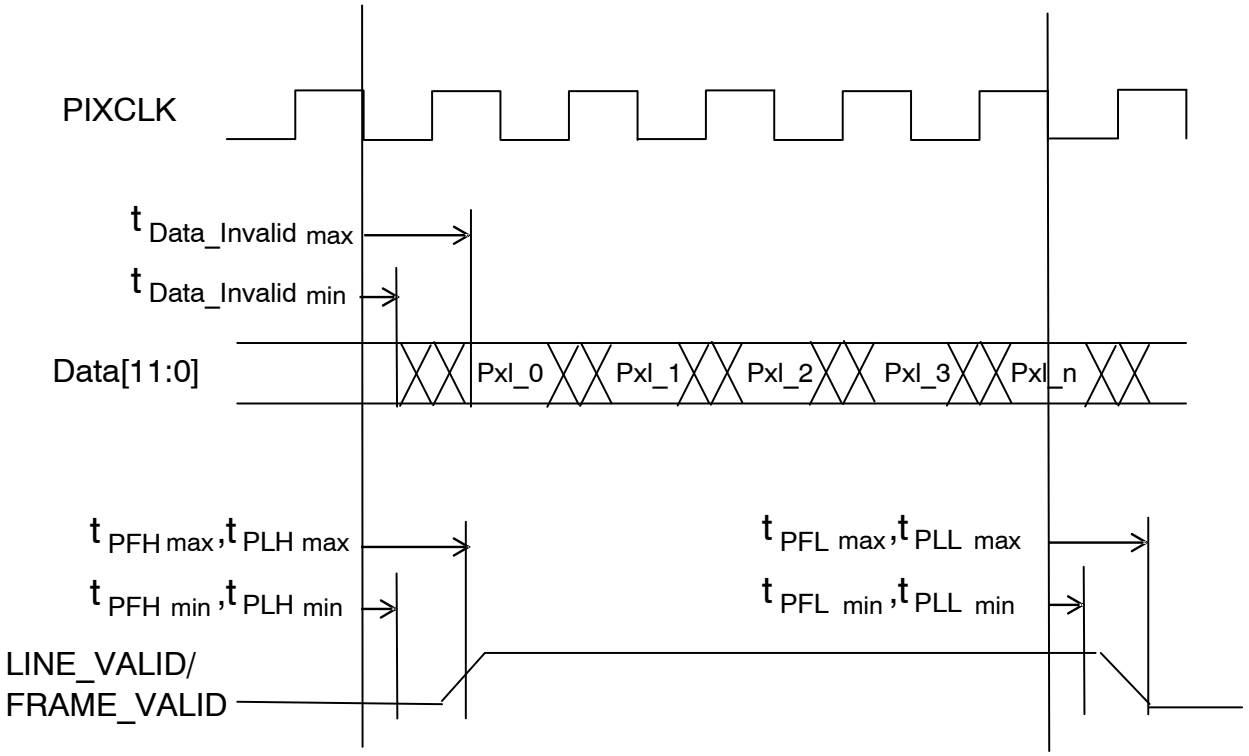


Figure 15. Parallel Port Timing Diagram
(figure not drawn to scale)

Table 6. I/O TIMING CHARACTERISTICS (1.8V VDD_IO) (Note 8)

Symbol	Definition	Condition	Min	Typ	Max	Unit
$f_{EXTCLK1}$	Input clock frequency	PLL Enabled	6 (Note 9)	–	50	MHz
$t_{EXTCLK1}$	Input clock period	PLL Enabled	20	–	166	ns
t_R	Input clock rise time		0.2	–	3	ns
t_F	Input clock fall time		0.2	–	3	ns
t_{JITTER}	Input clock jitter		–	400	–	ps
t_{RP}	Pixclk rise time		0.2	–	3	ns
t_{FP}	Pixclk fall time		0.2	–	3	ns
	Clock duty cycle	PLL Enabled	40	50	60	%
$t_{PIX\ JITTER}$	Jitter on PIXCLK		–	1	–	ns
t_{CP}	EXTCLK to PIXCLK propagation delay	Nominal voltages, PLL Disabled, PIXCLK slew rate = 4 EXTCLK t_R and t_F = 3 ns	7	–	19	ns
f_{PIXCLK}	PIXCLK frequency	Default, Nominal Voltages	6	–	78	MHz
$t_{Data\_Invalid}$	PIXCLK to data not valid	PIXCLK slew rate = 7 Data slew rate = 7	2	–	10.3	ns
t_{PFH}	PIXCLK to FV HIGH	PIXCLK slew rate = 7 Data slew rate = 7	2	–	10.3	ns
t_{PLH}	PIXCLK to LV HIGH	PIXCLK slew rate = 7 Data slew rate = 7	2	–	10.3	ns
t_{PFL}	PIXCLK to FV LOW	PIXCLK slew rate = 7 Data slew rate = 7	2	–	10.3	ns
t_{PLL}	PIXCLK to LV LOW	PIXCLK slew rate = 7 Data slew rate = 7	2	–	10.3	ns
C_{LOAD}	Output load capacitance		–	<20	–	pF
C_{IN}	Input pin capacitance		–	2.5	–	pF

8. I/O timing characteristics are measured under the following conditions:
   a. Minimum and maximum values are taken at 105°C, 1.7 V and −40°C, 1.95 V. All values are taken at the 50% transition point. The loading used is 20 pF.
   b. Jitter from PIXCLK is already taken into account in the data for all of the output parameters.
9. When using a 1 MHz two−wire interface clock, the minimum clock frequency is 16 MHz.

Table 7. I/O TIMING CHARACTERISTICS (2.8V VDD_IO) (Note 10)

Symbol	Definition	Condition	Min	Typ	Max	Unit
$f_{EXTCLK1}$	Input clock frequency	PLL Enabled	6 (Note 11)	–	50	MHz
$t_{EXTCLK1}$	Input clock period	PLL Enabled	20	–	166	ns
t_R	Input clock rise time		0.2	–	3	ns
t_F	Input clock fall time		0.2	–	3	ns
t_{JITTER}	Input clock jitter		–	400	–	ps
t_{RP}	Pixclk rise time		0.2	–	3	ns
t_{FP}	Pixclk fall time		0.2	–	3	ns
	Clock duty cycle	PLL Enabled	40	50	60	%
$t_{PIX\ JITTER}$	Jitter on PIXCLK		–	1	–	ns
t_{CP}	EXTCLK to PIXCLK propagation delay	Nominal voltages, PLL Disabled, PIXCLK slew rate = 4 EXTCLK t_R and t_F = 3 ns	7	–	19	ns
f_{PIXCLK}	PIXCLK frequency	Default, Nominal Voltages	6	–	78	MHz

Table 7. I/O TIMING CHARACTERISTICS (2.8V VDD_IO) (Note 10)

Symbol	Definition	Condition	Min	Typ	Max	Unit
$t_{Data\_Invalid}$	PIXCLK to data not valid	PIXCLK slew rate = 7 Data slew rate = 7	2	–	10.3	ns
t_{PFH}	PIXCLK to FV HIGH	PIXCLK slew rate = 7 Data slew rate = 7	2	–	10.3	ns
t_{PLH}	PIXCLK to LV HIGH	PIXCLK slew rate = 7 Data slew rate = 7	2	–	10.3	ns
t_{PFL}	PIXCLK to FV LOW	PIXCLK slew rate = 7 Data slew rate = 7	2	–	10.3	ns
t_{PLL}	PIXCLK to LV LOW	PIXCLK slew rate = 7 Data slew rate = 7	2	–	10.3	ns
C_{LOAD}	Output load capacitance		–	<20	–	pF
C_{IN}	Input pin capacitance		–	2.5	–	pF

10. I/O timing characteristics are measured under the following conditions:
    a. Minimum and maximum values are taken at 105°C, 2.5 V and −40°C, 3.1 V. All values are taken at the 50% transition point. The loading used is 20 pF.
    b. Jitter from PIXCLK is already taken into account in the data for all of the output parameters.
11. When using a 1 MHz two−wire interface clock, the minimum clock frequency is 16 MHz.

Table 8. I/O Rise Slew Rate (2.8V VDDIO)

Conditions: VDD_IO=2.8V, PAR_HIDRV_EN (R0x306E[8]) = 0

Parallel Slew Rate (R0x306E[15:13])	Conditions	Min	Typ	Max	Units
7	Default	1.55	2.65	4.12	V/ns
6	Default	1.39	2.37	3.71	V/ns
5	Default	1.24	2.12	3.3	V/ns
4	Default	1.09	1.85	2.89	V/ns
3	Default	0.93	1.59	2.47	V/ns
2	Default	0.78	1.32	2.06	V/ns
1	Default	0.62	1.06	1.65	V/ns
0	Default	0.47	0.8	1.24	V/ns

Note: 20pF loads at nominal voltages.

Table 9. I/O Fall Slew Rate (2.8V VDDIO)

Conditions: VDD_IO=2.8V, PAR_HIDRV_EN (R0x306E[8]) = 0

Parallel Slew Rate (R0x306E[15:13])	Conditions	Min	Typ	Max	Units
7	Default	1.29	1.86	2.37	V/ns
6	Default	1.19	1.76	2.26	V/ns
5	Default	1.09	1.64	2.13	V/ns
4	Default	0.99	1.5	1.98	V/ns
3	Default	0.87	1.35	1.81	V/ns
2	Default	0.75	1.17	1.6	V/ns
1	Default	0.61	0.98	1.36	V/ns
0	Default	0.47	0.76	1.08	V/ns

Note: 20pF loads at nominal voltages.

Table 10. I/O Rise Slew Rate (1.8V VDDIO)

Conditions: VDD_IO=1.8V, PAR_HIDRV_EN (R0x306E[8]) = 0

Parallel Slew Rate (R0x306E[15:13])	Conditions	Min	Typ	Max	Units
7	Default	0.54	0.87	1.54	V/ns
6	Default	0.49	0.79	1.38	V/ns
5	Default	0.44	0.7	1.23	V/ns
4	Default	0.38	0.62	1.08	V/ns
3	Default	0.33	0.53	0.93	V/ns
2	Default	0.3	0.44	0.77	V/ns
1	Default	0.22	0.36	0.62	V/ns
0	Default	0.17	0.27	0.47	V/ns

Note: 20pF loads at nominal voltages.

Table 11. I/O Fall Slew Rate (1.8V VDDIO)

Conditions: VDD_IO=1.8V, PAR_HIDRV_EN (R0x306E[8]) = 0

Parallel Slew Rate (R0x306E[15:13])	Conditions	Min	Typ	Max	Units
7	Default	0.57	0.88	1.25	V/ns
6	Default	0.52	0.81	1.18	V/ns
5	Default	0.47	0.74	1.09	V/ns
4	Default	0.42	0.66	0.99	V/ns
3	Default	0.37	0.58	0.89	V/ns
2	Default	0.31	0.49	0.77	V/ns
1	Default	0.25	0.4	0.63	V/ns
0	Default	0.19	0.31	0.49	V/ns

Note: 20pF loads at nominal voltages.

Table 12. I/O Rise Slew Rate (1.8V VDDIO)

Conditions: VDD_IO=1.8V, PAR_HIDRV_EN (R0x306E[8]) = 1

Parallel Slew Rate (R0x306E[15:13])	Conditions	Min	Typ	Max	Units
7	Default	1.05	1.71	3.01	V/ns
6	Default	0.96	1.55	2.73	V/ns
5	Default	0.86	1.39	2.44	V/ns
4	Default	0.76	1.22	2.15	V/ns
3	Default	0.65	1.05	1.85	V/ns
2	Default	0.54	0.88	1.54	V/ns
1	Default	0.44	0.71	1.23	V/ns
0	Default	0.33	0.54	0.93	V/ns

Note: 20pF loads at nominal voltages.

Table 13. I/O Fall Slew Rate (1.8V VDDIO)

Conditions: VDD_IO=1.8V, PAR_HIDRV_EN (R0x306E[8]) = 1

Parallel Slew Rate (R0x306E[15:13])	Conditions	Min	Typ	Max	Units
7	Default	0.9	1.27	1.66	V/ns
6	Default	0.84	1.21	1.6	V/ns
5	Default	0.78	1.13	1.52	V/ns
4	Default	0.7	1.04	1.43	V/ns
3	Default	0.62	0.93	1.32	V/ns
2	Default	0.52	0.81	1.18	V/ns
1	Default	0.42	0.66	0.99	V/ns
0	Default	0.31	0.5	0.77	V/ns

Note: 20pF loads at nominal voltages.

DC ELECTRICAL SPECIFICATIONS

Table 14. ELECTRICAL SPECIFICATIONS

Symbol	Definition	Condition	Min	Nominal	Max	Unit
VDD	Core digital voltage		1.14	1.2	1.26	V
VDD_IO	I/O digital voltage		1.7/2.6	1.8/2.8	1.9/3.0	V
VAA	Analog voltage		2.6	2.8	3.0	V
VAA_PIX	Pixel supply voltage		2.6	2.8	3.0	V
VDD_PHY	PHY supply voltage		1.14	1.2	1.26	V
VDD_IO_PHY	Serial PHY supply voltage		1.7/2.6	1.8/2.8	1.9/3.0	V
VDD_SLVS	Serial supply voltage (SLVS)		0.3	0.4	0.6	V
VDD_SLVS	HiSPi supply voltage (HiVCM)		1.14	1.2	1.26	V
V_{IH}	Input HIGH voltage		0.7xVDDIO	–	VDDIO+0.3	V
V_{IL}	Input LOW voltage		−0.3	–	0.3xVDDIO	V
I_{IN}	Input leakage current	No pull−up resistor: VIN = VDD_IO or DGND	–	–	20	μA
V_{OH}	Output HIGH voltage		0.7xVDDIO	–	–	V
V_{OL}	Output LOW voltage		–	–	0.3xVDDIO	V
I_{OH}	Output HIGH current	At specified VDDIO=1.8V; Vpadd=VDDIO−4	20	–	45	mA
I_{OL}	Output LOW current	At specified VDDIO=1.8V; Vpadd=VDDIO−4	20	–	45	mA

1. VAA_PIX must always be equal to VAA.
2. Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 15. ABSOLUTE MAXIMUM RATINGS

Symbol	Definition	Min	Max	Unit
VDD_MAX	Core Digital Voltage	−0.3	1.6	V
VDD_IO_MAX	I/O Digital Voltage	−0.3	3.6	V
VAA_MAX	Analog voltage	−0.3	3.6	V
VAA_PIX_MAX	Pixel supply voltage	−0.3	3.6	V
VDD_PHY_MAX	PHY supply voltage	−0.3	1.6	V
VDD_IO_PHY_MAX	Serial PHY supply voltage	−0.3	3.6	V
VDD_SLVS	Serial supply voltage	−0.3	1.6	V
T_{STG}	Storage temperature	−40	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. To keep dark current and shot noise artifacts from impacting image quality, keep operating temperature at a minimum.

Table 16. OPERATING CURRENT CONSUMPTION IN PARALLEL 12−BIT 3−EXPOSURE HDR

Current Type	Condition	Symbol	Voltage	Min	Typ	Max	Unit
Analog Operating Current	Streaming Full Res	I_{AA}	2.8	−	50	70	mA
Digital Operating Current	Streaming Full Res	I_{DD}	1.2	−	125	200	mA
PHY Supply Current	Streaming Full Res	I_{DD_PHY}	1.2	−	3	10	mA
Pixel Supply Current	Streaming Full Res	I_{AA_PIX}	2.8	−	10	13	mA
SLVS Supply Current	Streaming Full Res	I_{DD_SLVS}	1.2	−	0	0	mA

NOTE: Operating currents measured under the following conditions:
a. VAA and VAA_PIX are tied together
b. VDD_IO_PHY and VDD_IO are dependent on system design and environment, therefore not listed.
c. PLL enabled and PIXCLK set to 78MHz
d. 3−exposure 12−bit Parallel mode at 30fps
e. Ta=55°C

Table 17. OPERATING CURRENT CONSUMPTION IN MIPI 4−LANE 12−BIT 3−EXPOSURE HDR

Current Type	Condition	Symbol	Voltage	Min	Typ	Max	Unit
Analog Operating Current	Streaming Full Res	I_{AA}	2.8	−	50	70	mA
Digital Operating Current	Streaming Full Res	I_{DD}	1.2	−	125	200	mA
PHY Supply Current	Streaming Full Res	I_{DD_PHY}	1.2	−	7	20	mA
Pixel Supply Current	Streaming Full Res	I_{AA_PIX}	2.8	−	10	15	mA
SLVS Supply Current	Streaming Full Res	I_{DD_SLVS}	1.2	−	5	15	mA

NOTE: Operating currents measured under the following conditions:
a. VAA and VAA_PIX are tied together
b. VDD_IO_PHY and VDD_IO are dependent on system design and environment, therefore not listed.
c. PLL enabled and PIXCLK set to 78 MHz
d. 3−exposure 12−bit MIPI mode at 60 fps
e. T_A = 55°C

Table 18. STANDBY CURRENT CONSUMPTION

Definition	Condition	Symbol	Min	Typ	Max	Units
Hard standby (clock off) (Note 1)	Analog, 2.8V (Note 2)		−−	45	100	μA
	Digital, 1.2V (Note 3)		−−	10	100	mA
Hard standby (clock on) (Note 1)	Analog, 2.8V (Note 2)		−−	45	100	μA
	Digital, 1.2V (Note 3)		−−	10	100	mA
Soft standby (clock off)	Analog, 2.8V (Note 2)		−−	801	950	μA
	Digital, 1.2V (Note 3)		−−	10	100	mA
Soft standby (clock on)	Analog, 2.8V (Note 2)		−−	1151	1350	μA
	Digital, 1.2V (Note 3)		−−	10	100	mA

1. Hard standby is set when RESET_BAR = 0.
2. Analog = VAA + VAA_PIX.
3. Digital = VDD + VDD_PHY + VDD_SLVS.
4. T_A = 55°C

MIPI Electrical Specifications

The ON Semiconductor AR0143AT sensor supports up to four lanes of MIPI data. The AR0143AT is compliant to the following MIPI standards:

- MIPI Alliance Standard for CSI−2 version 1.0
- MIPI Alliance Standard for D−PHY version 1.1

Table 19. MIPI High−Speed Transmitter AC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
	Data bit rate	−−	−−	600	Mbps
Data Lane Trise	20−80% rise time	100	−−	500	ps
Data Lane Tfall	20−80% fall time	100	−−	500	ps
Clock Lane Trise	20−80% fall time	150	−−	500	ps
Clock Lane Tfall	20−80% fall time	150	−−	500	ps

HiSPi Electrical Specifications

The ON Semiconductor AR0143AT sensor supports both SLVS and HiVCM HiSPi modes. Please refer to the High−Speed Serial Pixel (HiSPi) Interface Physical Layer Specification v2.00.00 for electrical definitions, specifications, and timing information. The VDD_SLVS supply in this datasheet corresponds to VDD_TX in the HiSPi Physical Layer Specification. Similarly, VDD is equivalent to VDD_HiSPi as referenced in the specification. The DLL as implemented on AR0143AT is limited in the number of available delay steps and differs from the HiSPi specification as described in this section.

Table 20. CHANNEL SKEW

Measurement Conditions: VDD_HiSPi = 1.8 V;VDD_HiSPi_TX = 0.4 V; Data Rate = 480 Mbps; DLL set to 0

Data Lane Skew in Reference to Clock	tCHSKEW1PHY	−150	ps

Power Up

For controlled power up, RESET_BAR pin must be asserted (low) before supplies can be sequenced up. Once all supplies are valid, RESET_BAR is de−asserted (high), the part will begin boot−up on EXTCLK.

Typical Power Up Sequence:

1. Set RESET_BAR low. The EXTCLK may be applied at any time in the sequence.
2. Power on supplies in the prescribed order: VAA, followed by VDDIO, followed by VDD. Alternatively, supplies can be powered up in any order as long as the following two conditions hold true: (1) VAA achieves 2.35 V prior to VDDIO achieving 1.46 V, and (2) VDDIO achieves 1.46 V prior to VDD achieving 0.91 V.
3. After 1.0 ms, set RESET_BAR high.
4. Wait 160000 EXTCLKs for a full OTPM loading.
5. Set STREAMING bit.
6. Wait 1.0 ms for PLL lock.
7. AR0143 enters streaming mode.

VAA and VDDIO power supplies, if brought up in a non−allowed manner, can create a leakage path from two serial diodes connected between these two supplies where up to 70 mA of leakage current occurs. No known reliability concerns exist as long as the following power supply sequence is followed:

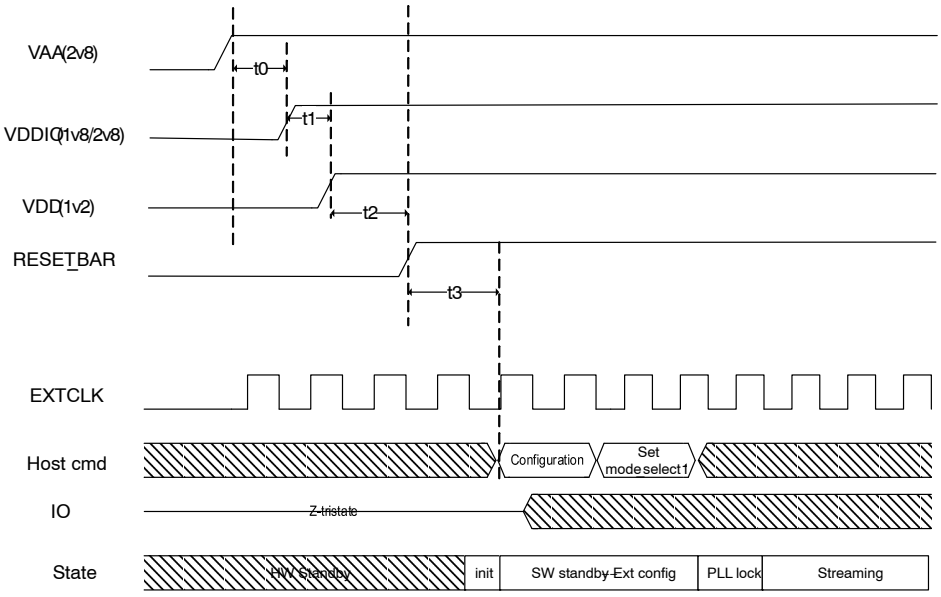


Figure 16. Power Up Sequence

Table 21. POWER UP SEQUENCE

Definition	Symbol	Min	Max	Units
Vaa 2V8 rising trigger voltage (Note 12) to VDDIO rising trigger voltage (Note 13)	t0	0		μs
VDDIO rising trigger voltage[2] to VDD rising trigger voltage (Note 14)	t1	0		μs
DVDD rising trigger voltage[3] to RESET_N	t2	1.0		ms
Minimum number of EXTCLK cycles prior to the first CCI transaction	t3	160000		cycles
PLL lock time	PLL lock		1.0	ms

12. VAA rising trigger voltage is 2.35 V.
13. For both VDDIO=2.8 V and VDDIO=1.8 V, VDDIO rising trigger voltage is 1.46 V.
14. VDD rising trigger voltage is 0.91 V.

Power Down

For controlled power down, streaming must be first disabled. The RESET_BAR pin must be asserted (low) before any external supplies are removed. The supplies should then be powered down in the reverse of power−up sequence order. If VDDIO is not powered down (e.g. “HOLD” I/O state), then VAA should not be powered down.

Typical Power Down Sequence:

1. De−assert STREAMING bit.
2. Wait till the end of the current frame (or end−of−line if so configured).
3. Configure I/O for “hold” if desired. “Hold” state requires maintaining VDDIO and VAA.
4. The EXTCLK can be stopped at this time; or can continue running (not shown to scale).
5. Set RESET_BAR low. (Hard Standby, low−leakage state)
6. Wait t4 power−down delay.
7. Power off supplies in the prescribed order (reverse of power−up sequence order): VDD, followed by VDDIO, followed by VAA. For “hold” I/O state, do not power off VDDIO and VAA supplies. Alternatively, supplies can be powered down in any order as long as the following two conditions hold true: (1) VDD achieves 0.6 V prior to VDDIO achieving 1.11 V, and (2) VDDIO achieves 1.11 V prior to VAA achieving 1.65 V.

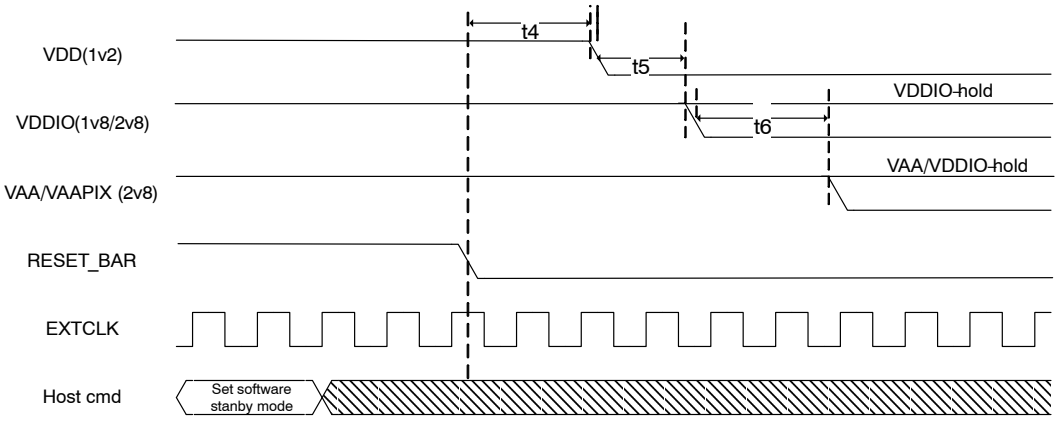


Figure 17. Power Down Sequence

Constraint	Label	Min Value	Units
RESET_N to VDD removal	t4	0	μS
VDD falling trigger voltage (Note 15) to VDDIO removal	t5	0	μS
VDDIO falling trigger voltage (Note 16) to VAA/VAAPIX removal	t6	0	μS

15. VDD falling trigger voltage is 0.6 V.
16. For both VDDIO=2.8 V and VDDIO=1.8 V, VDDIO falling trigger voltage is 1.11 V.

Table 22. AR0143AT PIN LIST

PIN Name	iBGA Pin	Type	Descriptions	Comments
EXTCLK	H2	Input	Master input clock. PLL input clock.	Connect to clock source. Min and Max frequency depends upon output port and clocking method.
RESET_BAR	H8	Input	Asynchronous active−low reset.	Connect to host.
SCLK	C5	Input	CCI clock for access to control and status registers.	Connect to host.
SDATA	D7	Input/Output	CCI data for reads from and writes to control and status registers.	Connect to host.
SADDR0	C7	Input	CCI interface device address select bit 0.	Selects CCI address. 000b sets the address to 0x20/0x21. 001b sets the address to 0x30/0x31. Connect to VDD_IO or DGND accordingly.
SADDR1	C6	Input	CCI interface device address select bit 1.	
SADDR2	D8	Input	CCI interface device address select bit 2.	
PIXCLK	H5	Output	Parallel data output pixel clock. Used to qualify the LINE_VALID, FRAME_VALID and DOUT11 to DOUT0 outputs.	Connect to host/receiver or can be left floating if not used. Use DOUT[11:0] for 12−bit parallel configuration.
FRAME_VALID	H7	Output	Parallel data output FRAME_VALID output. Qualified by PIXCLK.	
LINE_VALID	G7	Output	Parallel data output LINE_VALID output. Qualified by PIXCLK.	
DOUT11	G6	Output	Parallel data output pixel data bit 11. Qualified by PIXCLK.	Connect to host/receiver or can be left floating if not used. Use DOUT[11:0] for 12−bit parallel configuration.
DOUT10	F6	Output	Parallel data output pixel data bit 10. Qualified by PIXCLK.	
DOUT9	G5	Output	Parallel data output pixel data bit 9. Qualified by PIXCLK.	
DOUT8	F5	Output	Parallel data output pixel data bit 8. Qualified by PIXCLK.	
DOUT7	E5	Output	Parallel data output pixel data bit 7. Qualified by PIXCLK.	
DOUT6	D5	Output	Parallel data output pixel data bit 6. Qualified by PIXCLK.	
DOUT5	H4	Output	Parallel data output pixel data bit 5. Qualified by PIXCLK.	
DOUT4	G4	Output	Parallel data output pixel data bit 4. Qualified by PIXCLK.	
DOUT3	F4	Output	Parallel data output pixel data bit 3. Qualified by PIXCLK.	
DOUT2	E4	Output	Parallel data output pixel data bit 2. Qualified by PIXCLK.	
DOUT1	D4	Output	Parallel data output pixel data bit 1. Qualified by PIXCLK.	
DOUT0	H3	Output	Parallel data output pixel data bit 0. Qualified by PIXCLK.	

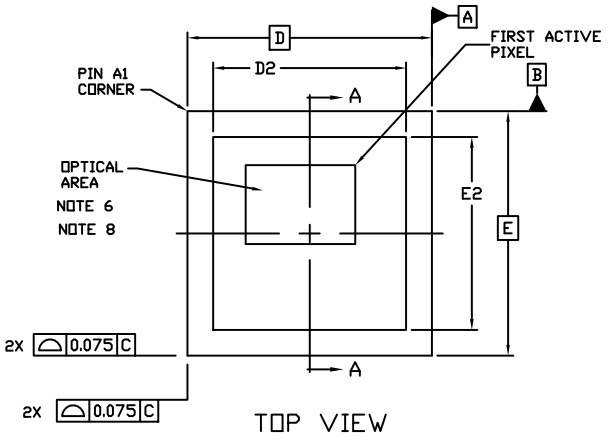
Table 22. AR0143AT PIN LIST

PIN Name	iBGA Pin	Type	Descriptions	Comments
CLK_P	E1	Output	Differential Mipi/HiSpi serial clock.	Connect to host/receiver or can be left floating if not used. Use DATA0 for 1 lane configuration or DATA0 and DATA1 for 2 lane configuration.
CLK_N	E2	Output	Differential Mipi/HiSpi serial clock.	
DATA3_P	C1	Output	Differential Mipi/HiSpi serial data lane 3.	
DATA3_N	C2	Output	Differential Mipi/HiSpi serial data lane 3.	
DATA2_P	D1	Output	Differential Mipi/HiSpi serial data lane 2.	
DATA2_N	D2	Output	Differential Mipi/HiSpi serial data lane 2.	
DATA1_P	F1	Output	Differential Mipi/HiSpi serial data lane 1.	
DATA1_N	F2	Output	Differential Mipi/HiSpi serial data lane 1.	
DATA0_P	G1	Output	Differential Mipi/HiSpi serial data lane 0.	
DATA0_N	G2	Output	Differential Mipi/HiSpi serial data lane 0.	
TEST	D6	Input	Enable manufacturing test modes.	Tie to DGND.
ATEST1	B7	Input/Output	Analog manufacturing test access	Leave unconnected.
ATEST2	B6	Input/Output	Analog manufacturing test access	
ATEST3	B5	Input/Output	Analog manufacturing test access	
ATEST4	B4	Input/Output	Analog manufacturing test access	
GPIO0	F7	Input/Output	GPIO Pin 0	GPIO[2:0] can be left unconnected if not used. GPIO3 should be tied to DGND if not used.
GPIO1	E8	Input/Output	GPIO Pin 1	
GPIO2	E7	Input/Output	GPIO Pin 2	
GPIO3	E6	Input/Output	GPIO Pin 3	
SYS_CHECK	G8	Output	Combined OR of error flags	Leave unconnected if not used.
TEMP_FLAG	H6	Output	Temperature monitoring flag	Open−drain. Leave unconnected if not used.
DGND	J1, B3, E3, G3, A4, C4, J5, A7, C8, F8, A9, J9	Power	Digital ground.	
VDD	B1, J2, J4, A5, J7, F9, H9	Power	Core Digital power.	
VDD_PHY	D3	Power	PHY Digital power.	Connect to VDD
VDD_IO	H1, B2, J3, A6, J6, J8, E9, G9	Power	Digital I/O power.	
AGND	A3, B8	Power	Analog ground.	
VAA	A2, A8, C9	Power	Analog power.	
VAA_PIX	B9	Power	Analog pixel array power.	Connect to VAA
VDD_IO_PHY	C3	Power	Power to MIPI and HiSPi PHYs.	Use 1.8 V nominal for HiSPi HiVCM or Sub−LVDS. Use 1.8 V or 2.8 V nominal for MIPI or HiSPi SLVS. Tie to VDD_IO when Parallel interface is used.
VDD_SLVS	F3	Power	Reference voltage for HiSPi serial interface.	Set according to desired HiSPi output common mode voltage. Use 0.4 V nominal for HiSPi SLVS, otherwise use 1.2 V nominal. Tie to VDD when MIPI is being used
VPP	D9	Power	High voltage supply for programming OTPM.	Leave unconnected.

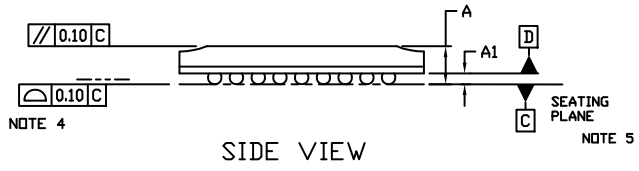
PACKAGE DIMENSIONS

IBGA80 9x9
CASE 503BM
ISSUE C

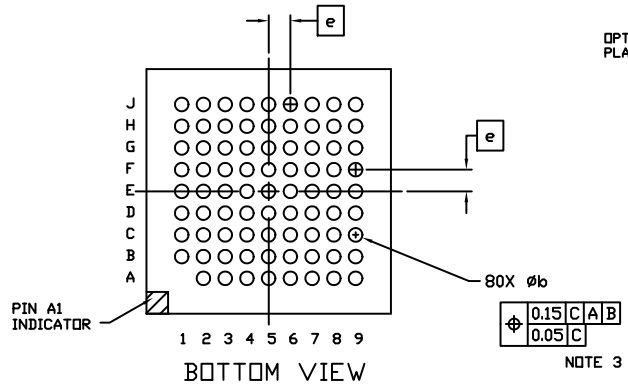
DATE 25 JUN 2018



TOP VIEW



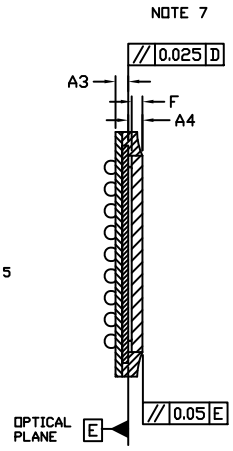
SIDE VIEW



BOTTOM VIEW

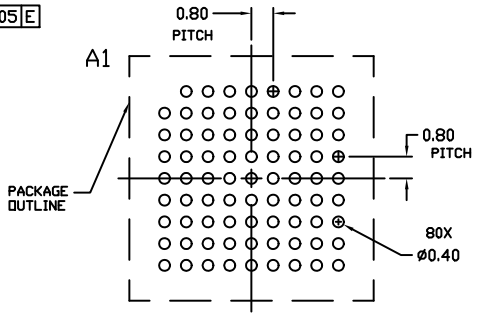
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM C.
4. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. MAXIMUM ROTATION OF THE OPTICAL AREA RELATIVE TO D AND E WILL BE 1°. OPTICAL AREA IS DEFINED BY THE ACTIVE PIXEL ARRAY. REFER TO THE DEVICE DATASHEET FOR TOTAL ARRAY AND FIRST PIXEL DEFINITIONS.
7. PARALLELISM APPLIES ONLY TO THE OPTICAL AREA.
8. OPTICAL CENTER OFFSET WITH RESPECT TO THE PACKAGE CENTER IS X=−337.94 MICRONS, Y=1062.58 MICRONS ±75 MICRONS.



SECTION A-A

DIM	MILLIMETERS MIN.	MAX.
A	---	1.55
A1	0.35	0.45
A3	0.425	0.525
A4	0.475	0.575
b	0.45	0.55
D	9.00 BSC	
D2	7.00	7.20
E	9.00 BSC	
E2	7.00	7.20
e	0.80 BSC	
F	0.38	0.42



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