P1817A/B

Low-Power Mobile VGA EMI Reduction IC

Features

- FCC approved method of EMI attenuation.
- Generates a low EMI spread spectrum clock of the input frequency.
- Optimized for frequency range from:
  P1817A – 20 to 32MHz
  P1817B – 10 to 20MHz
- Internal loop filter minimizes external components and board space.
- Two selectable spread ranges.
- Low inherent cycle-to-cycle jitter.
- 3.3V or 5V operating voltage range.
- TTL or CMOS compatible inputs and outputs.
- Ultra-low power CMOS design.
  3.17mA @ 3.3V, 10MHz | 6.20mA @ 5.0V, 10MHz
  4.28mA @ 3.3V, 14MHz | 7.50mA @ 5.0V, 14MHz
  5.50mA @ 3.3V, 20MHz | 9.50mA @ 5.0V, 20MHz
- Supports notebook VGA and other LCD timing controller applications.
- SSON / SBM pin for Spread Spectrum On/Off and Standby Mode controls.
- Available in 8-pin SOIC package.

Product Description

The P1817 is a versatile spread spectrum frequency modulator designed specifically for input clock frequencies. The P1817 reduces electromagnetic interference (EMI) at the clock source, allowing system wide reduction of EMI of downstream clock and data dependent signals. The P1817 allows significant system cost savings by reducing the number of circuit board layers, ferrite beads, shielding and other passive components that are traditionally required to pass EMI regulations.

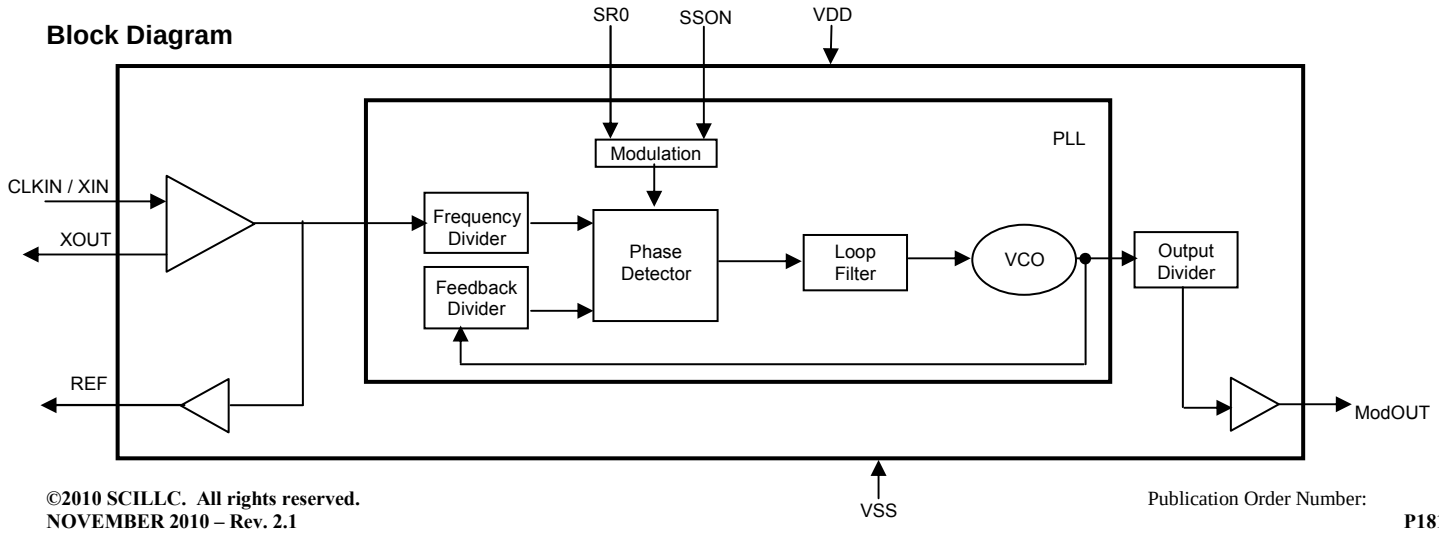
The P1817 modulates the output of a single PLL in order to “spread” the bandwidth of a synthesized clock, and more importantly, decreases the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal’s bandwidth is called ‘spread spectrum clock generation.’

The P1817 uses the most efficient and optimized modulation profile approved by the FCC and is implemented in a proprietary all digital method.

Applications

The P1817 is targeted towards notebook LCD displays, and other displays using an LVDS interface, PC peripheral devices, and embedded systems.

Block Diagram



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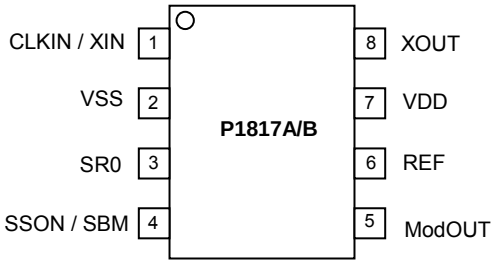
Publication Order Number:
P1817/D

Pin Configuration



Pin Description

Pin#	Pin Name	Type	Description
1	CLKIN / XIN	I	Crystal connection or external reference frequency input. This pin has dual functions. It can be connected either to an external crystal or an external reference clock. To put the part into standby mode, disable the input clock signal to this pin and pull SSON/SBM (pin4) low. Refer to *Standby Mode Selection* Table.
2	VSS	P	Ground Connection. Connect to system ground.
3	SR0	I	Digital logic input used to select Spreading Range. Refer to *Spread Spectrum Selection* Table. This pin has an internal pull-up resistor.
4	SSON / SBM	I	Spread Spectrum On/Off and standby mode control. Refer to *Standby Mode Selection* Table.
5	ModOUT	O	Spread spectrum clock output or Reference output. Refer to *Standby Mode Selection* Table.
6	REF	O	Reference Output.
7	VDD	P	Connect to +3.3V or 5.0V.
8	XOUT	O	Connect to crystal. No connect if externally generated clock signal is used.

Standby Mode Selection

CLKIN	SSON / SBM	Spread Spectrum	ModOUT	PLL	Mode
Disabled	0	N/A	Disabled	Disabled	Standby
Disabled	1	N/A	Disabled	Free Running	Free Running
Enabled	0	OFF	Reference	Disabled	Buffer out
Enabled	1	ON	Normal	Normal	Normal

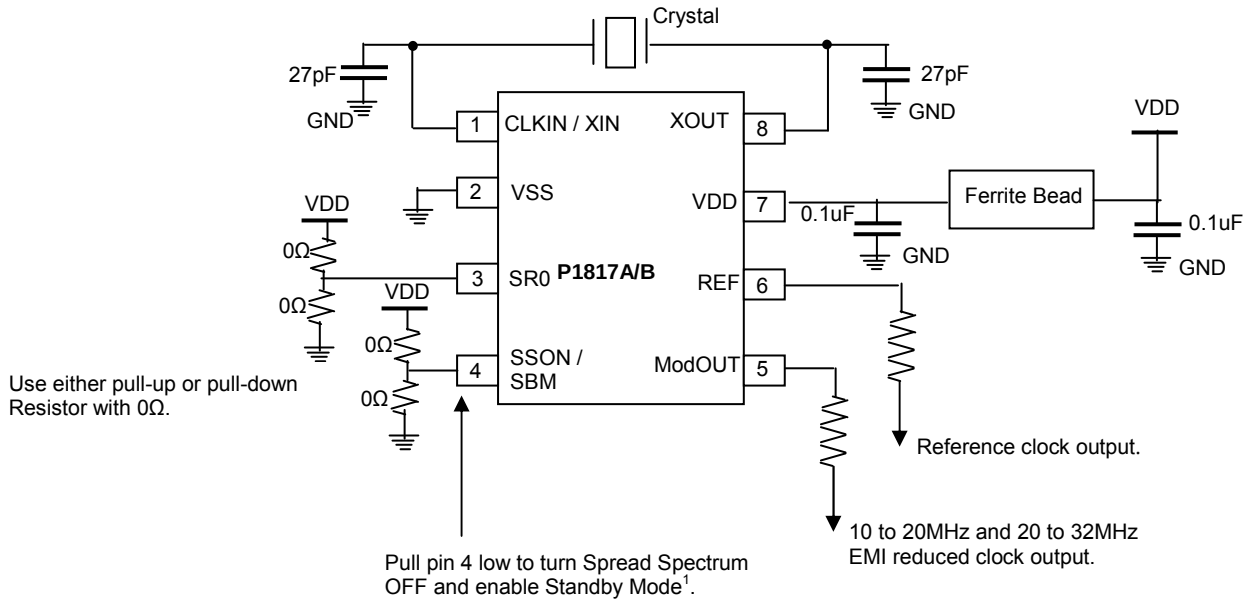
Spread Range Selection, VDD = 5V

CLKIN Frequency	SR0	Spreading Range	Modulation Rate
10MHz	1	±1.50%	(CLKIN/10)*20.83KHz
	0	±1.90%	
14.318MHz	1	±1.36%	
	0	±1.64%	
15MHz	1	±1.30%	
	0	±1.50%	
20MHz	1	±0.95%	
	0	±1.125%	

Spread Range Selection, VDD = 3.3V

CLKIN Frequency	SR0	Spreading Range	Modulation Rate
10MHz	1	±1.50%	(CLKIN/10)*20.83KHz
	0	±1.65%	
14.318MHz	1	±1.40%	
	0	±1.70%	
15MHz	1	±1.37%	
	0	±1.63%	
20MHz	1	±1.10%	
	0	±1.28%	

Schematic for Notebook VGA Application



[1] To set the P1817 to standby mode, disable the input clock (pin 1, CLKIN) and pull pin 4 SSON / SBM low.

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
VDD, V_{IN}	Voltage on any pin with respect to GND	-0.5 to +7.0	V
T_{STG}	Storage temperature	-65 to +125	℃
T_s	Max. Soldering Temperature (10 sec)	260	℃
T_J	Junction Temperature	150	℃
T_{DV}	Static Discharge Voltage (As per JEDEC STD22- A114-B)	2	KV

Note: These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Operating Conditions

Parameter	Description	Min	Max	Unit
VDD	Supply Voltage	2.7	5.5	V
T_A	Operating Temperature (Ambient Temperature)	-40	+85	℃
C_L	Load Capacitance		15	pF
C_{IN}	Input Capacitance		7	pF

DC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Unit
V_{IL}	Input low voltage		GND-0.3		0.8	V
V_{IH}	Input high voltage		2.0		VDD+0.3	V
I_{IL}	Input low current (pull-up resistors on inputs SR0, and SSON / SBM)				-35	µA
I_{IH}	Input high current (pull-down resistors on inputs SR0, and SSON / SBM)				35	µA
I_{XOL}	X_{OUT} output low current	@ 0.4V, VDD = 3.3V		3		mA
		@ 0.4V, VDD = 5.0V		20		
I_{XOH}	X_{OUT} output high current	@ 2.5V, VDD = 3.3V		3		mA
		@ 4.5V, VDD = 5.0V		20		
V_{OL}	Output low voltage	VDD = 3.3V, I_{OL} = 20mA			0.4	V
		VDD = 5.0V, I_{OL} = 20mA				
V_{OH}	Output high voltage	VDD = 3.3V, I_{OH} = 20mA	2.5			V
		VDD = 5.0V, I_{OH} = 20mA	4.5			
I_{CC}	Dynamic supply current standby mode	Normal Mode	f_{IN-min}	f_{IN-typ}	f_{IN-max}	mA
		3.3Vand 10pF loading	3.2		7.0	
		5.0Vand 10pF loading	6.2		13.6	
I_{DD}	Static supply current standby mode			0.6		mA
VDD	Operating voltage		2.7	3.3	5.5	V
t_{ON}	Power up time (first locked clock cycle after power up)			0.18		mS
Z_{OUT}	Clock output impedance			50		Ω

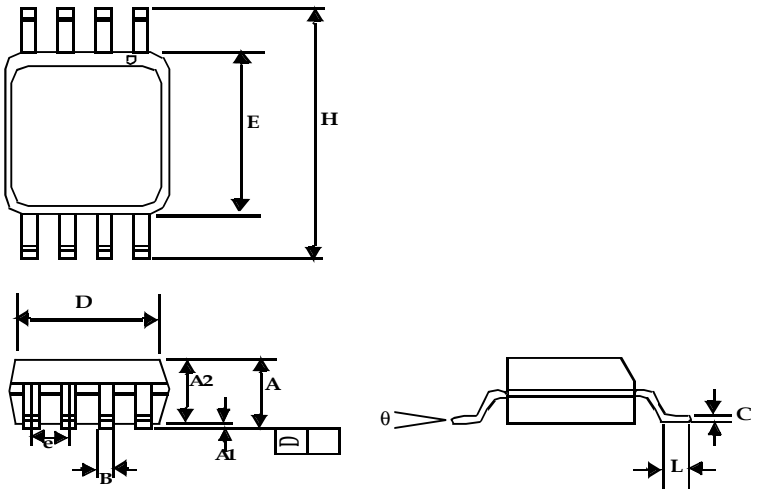
AC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Unit
f_{IN}	Input frequency (See device type P1817A or 1817B)		10		32	MHz
f_{OUT}	Output frequency (See device type P1817A or 1817B)		10		32	MHz
t_{LH}[1]	Output rise time	Measured at 0.8V to 2.0V	0.7	0.9	1.1	nS
		Measured at 1.2V to 3.75V		0.75		
t_{HL}[1]	Output fall time	Measured at 0.8V to 2.0V	0.6	0.8	1.0	nS
		Measured at 1.2V to 3.75V		0.75		
t_{JC}	Jitter (cycle-to-cycle)				360	pS
t_D	Output duty cycle		45	50	55	%

Note: 1. t_{LH} and t_{HL} are measured into a capacitive load of 15pF.

Package Information

8-lead (150-mil) SOIC Package



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A1	0.004	0.010	0.10	0.25
A	0.053	0.069	1.35	1.75
A2	0.049	0.059	1.25	1.50
B	0.012	0.020	0.31	0.51
C	0.007	0.010	0.18	0.25
D	0.193 BSC		4.90 BSC	
E	0.154 BSC		3.91 BSC	
e	0.050 BSC		1.27 BSC	
H	0.236 BSC		6.00 BSC	
L	0.016	0.050	0.41	1.27
θ	0°	8°	0°	8°

Ordering Code

Part Number	Marking	Package Type	Temperature
P1817AF-08SR	ABA	8-Pin SOIC, Tape & Reel, Pb free	0℃ to 70℃
P1817BF-08SR	ABC	8-Pin SOIC, Tape & Reel, Pb free	0℃ to 70℃

A “microdot” placed at the end of last row of marking or just below the last row toward the center of package indicates Pb-free

PUBLICATION ORDERING INFORMATION

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