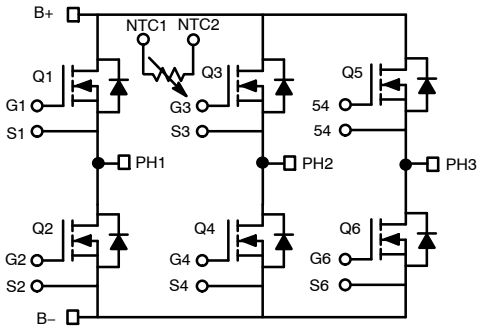
SiC Power MOSFET Module

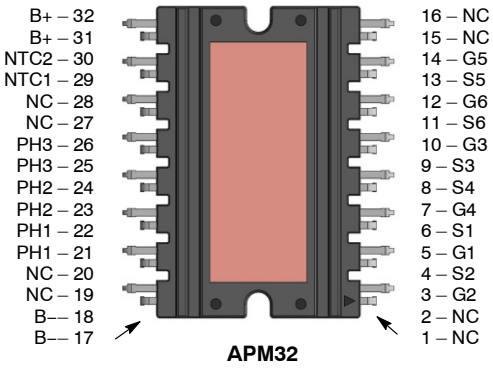
1200 V, 40 mΩ, 55 A
3-Phase Bridge Power Module

NVXK2VR40WXT2

$V_{(BR)DSS}$	$R_{DS(on)}$ Max	I_D Max
1200 V	59 mΩ @ 20 V	55 A



SiC MOSFET 3−Phase Bridge Module



APM32

Features

- DIP Silicon Carbide 3−Phase Bridge Power Module for On−Board Charger (OBC) for xEV Applications
- Creepage and Clearance per IEC 60664−1, IEC 60950−1
- Compact Design for Low Total Module Resistance
- Module Serialization for Full Traceability
- Lead Free, ROHS and UL94V−0 Compliant
- Automotive Qualified per AEC−Q101 and AQG324

Typical Applications

- PFC for On−Board Charger in xEV Applications

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

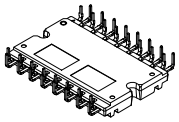
Parameter		Symbol	Value	Unit
Drain−to−Source Voltage		V_{DSS}	1200	V
Gate−to−Source Voltage		V_{GS}	+25/−15	V
Recommended Operation Values of Gate−to−Source Voltage, $T_J \le 175°C$		V_{GSop}	+20/−5	V
Continuous Drain Current (Note 1)	T_C = 25°C	I_D	55	A
Power Dissipation (Note 1)		P_D	319	W
Pulsed Drain Current (Note 2)	T_C = 25°C	I_{DM}	170	A
Single Pulse Surge Drain Current Capability	T_C = 25°C, t_p = 10 μs, R_G = 4.7 Ω	I_{DSC}	495	A
Operating Junction Temperature		T_J	−55 to 175	°C
Storage Temperature		T_{stg}	−40 to 125	°C
Source Current (Body Diode)		I_S	55	A
Single Pulse Drain−to−Source Avalanche Energy (Note 3)		E_{AS}	338	mJ

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS (Note 1)

Parameter	Symbol	Typ	Max	Unit
Thermal Resistance Junction−to−Case (Note 1)	$R_{\theta JC}$	0.37	0.47	°C/W
Thermal Resistance Junction−to−Sink (Note 1)	$R_{\Psi JS}$	0.84	0.95	°C/W

1. Particular conditions specified determine thermal resistance values shown. Infinite heatsink with T_C = 100°C for $R_{\theta JC}$. For $R_{\Psi JS}$ assembled to 3 mm thick aluminum heatsink with infinite cooling bottom surface at 85°C, through 38 μm thick TIM with 6.5 W/mK thermal conductivity.
2. Repetitive rating limited by maximum junction temperature and transconductance.
3. E_{AS} based on initial T_J = 25°C, L = 1 mH, I_{AS} = 26 A, V_{DD} = 120 V, V_{GS} = 18 V.



APM32
44.00x28.80x5.70
CASE MODHM

MARKING DIAGRAM

NVXK2VR40WXT2
ZZZ ATYWW
NNNNNNN

NVXK2VR40WXT2 = Specific Device Code
ZZZ = Lot Number
AT = Assembly Site & Test Location
Y = Year
W = Work Week
NNN = Serial Number

ORDERING INFORMATION

Device	Package	Shipping
NVXK2VR40WXT2	APM32	10 ea / Tube

PIN DESCRIPTION

Pin No.	Name	Description
1, 2, 15, 16, 19, 20, 27, 28	NC	Not Connected
3	G2	Q2 Gate
4	S2	Q2 Source
5	G1	Q1 Gate
6	S1	Q1 Source
7	G4	Q4 Gate
8	S4	Q4 Source
9	S3	Q3 Source
10	G3	Q3 Gate
11	S6	Q6 Source
12	G6	Q6 Gate
13	S5	Q5 Source
14	G5	Q5 Gate
17, 18	B–	Negative Power Terminal
21, 22	PH1	Phase 1 Output
23, 24	PH2	Phase 2 Output
25, 26	PH3	Phase 3 Output
29	NTC1	NTC pin1
30	NTC2	NTC pin2
31, 32	B+	Positive Power Terminal

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise stated)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain–to–Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1 mA		1200	–	–	V
Drain–to–Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}$ / T_J	I_D = 1 mA, referenced to 25°C		–	450	–	mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 1200 V	T_J = 25°C	–	–	100	μA
			T_J = 175°C	–	–	1	mA
Gate–to–Source Leakage Current	I_{GSS}	V_{GS} = +25/–15 V, V_{DS} = 0 V		–	–	±1	μA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS} , I_D = 10 mA		1.8	3	4.3	V
Recommended Gate Voltage	V_{GOP}			–5		+20	V
Drain–to–Source On Resistance	$R_{DS(on)}$	V_{GS} = 20 V, I_D = 35 A, T_J = 25°C		–	40	59	mΩ
Drain–to–Source On Resistance	$R_{DS(on)}$	V_{GS} = 20 V, I_D = 35 A, T_J = 175°C		–	71	–	mΩ
Forward Transconductance	g_{FS}	V_{DS} = 20 V, I_D = 35 A		–	20	–	S
CHARGES, CAPACITANCES & GATE RESISTANCE							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 800 V		–	1789	–	pF
Output Capacitance	C_{OSS}			–	139	–	
Reverse Transfer Capacitance	C_{RSS}			–	12.5	–	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise stated) (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
CHARGES, CAPACITANCES & GATE RESISTANCE						
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = −5/20 V, V_{DS} = 600 V, I_D = 47 A	–	106	–	nC
Threshold Gate Charge	$Q_{G(TH)}$		–	18	–	
Gate−to−Source Charge	Q_{GS}		–	34	–	
Gate−to−Drain Charge	Q_{GD}		–	26	–	
Gate−Resistance	R_G	V_{GS} = 0 V, f = 1 MHz	–	2	–	Ω
INDUCTIVE SWITCHING CHARACTERISTICS						
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = −5 / 20 V, V_{DS} = 800 V, I_D = 47 A, R_G = 4.7 Ω, Inductive load	–	17	–	ns
Rise Time	t_r		–	20	–	
Turn−Off Delay Time	$t_{d(OFF)}$		–	30	–	
Fall Time	t_f		–	9	–	
Turn−On Switching Loss	E_{ON}		–	366	–	μJ
Turn−Off Switching Loss	E_{OFF}		–	200	–	μJ
Total Switching Loss	E_{tot}		–	566	–	μJ
DRAIN−SOURCE DIODE CHARACTERISTICS						
Continuous Drain−Source Diode Forward Current (Note 1)	I_{SD}	V_{GS} = −5 V, T_J = 25°C	–	–	55	A
Pulsed Drain−Source Diode Forward Current (Note 2)	I_{SDM}	V_{GS} = −5 V, T_J = 25°C	–	–	170	A
Forward Diode Voltage	V_{SD}	V_{GS} = −5 V, I_{SD} = 17.5 A, T_J = 25°C	–	3.7	–	V
Reverse Recovery Time	t_{RR}	V_{GS} = −5 V, dI_S/dt = 1000 A/μs, I_{SD} = 17.5 A	–	24	–	ns
Peak Reverse Recovery Current	I_{RRM}		–	10.4	–	A
Charge Time	t_a		–	12.4	–	ns
Discharge Time	t_b		–	11.6	–	ns
Reverse Recovery Charge	Q_{RR}		–	125	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse test: pulse width ≤300 μs, duty ratio ≤2%.

COMPONENTS

Component	Description	Type	Quantity	Specification
NTC	10 kΩ, ±3% Case Size 0603	Discrete	1	B Constants $B_{25/50}$: 3590 $B_{25/85}$ = 3635 $B_{25/100}$ = 3650 ±3%

TYPICAL CHARACTERISTICS

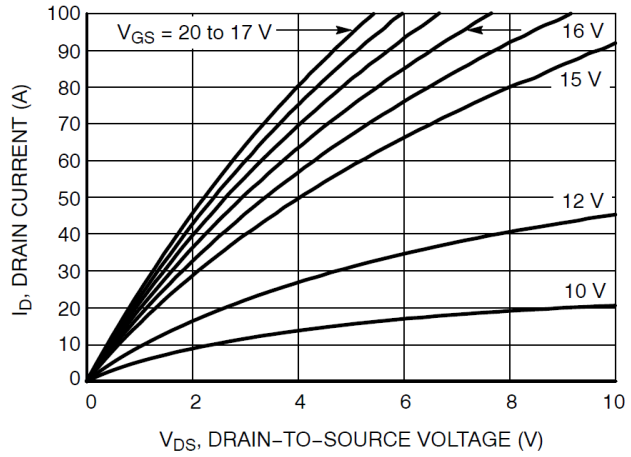


Figure 1. On−Region Characteristics

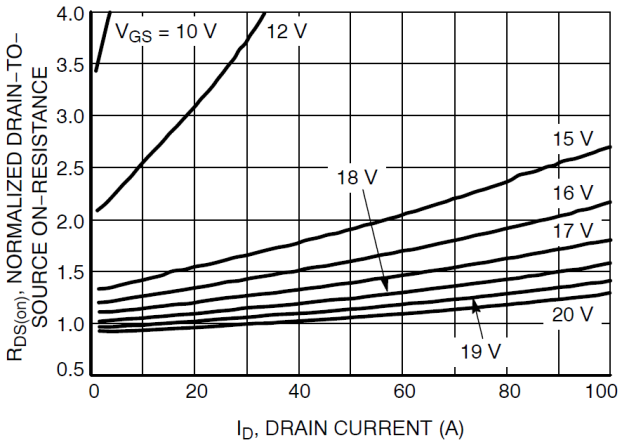


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

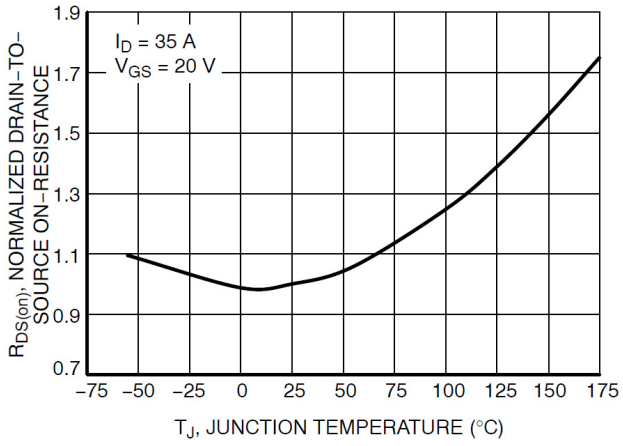


Figure 3. On−Resistance Variation with Temperature

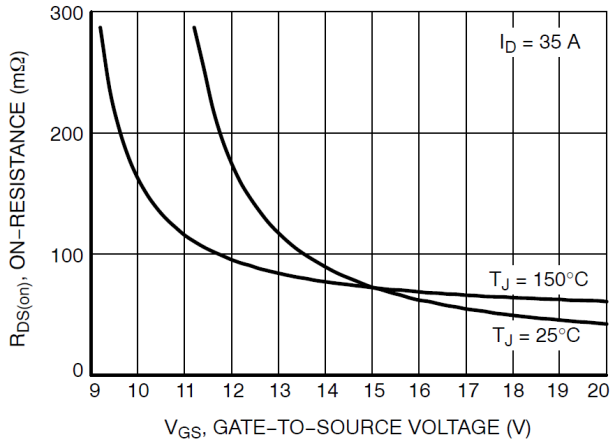


Figure 4. On−Resistance vs. Gate−to−Source Voltage

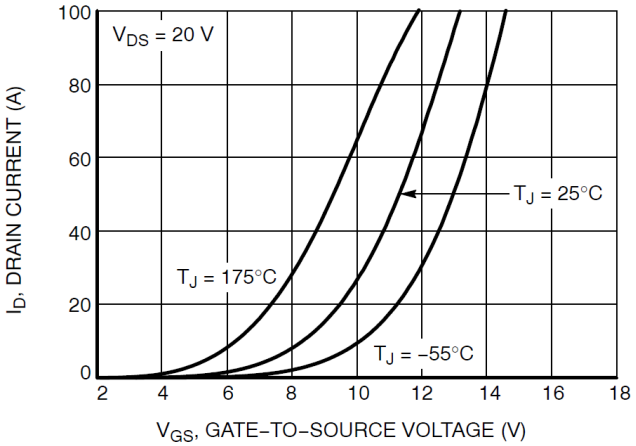


Figure 5. Transfer Characteristics

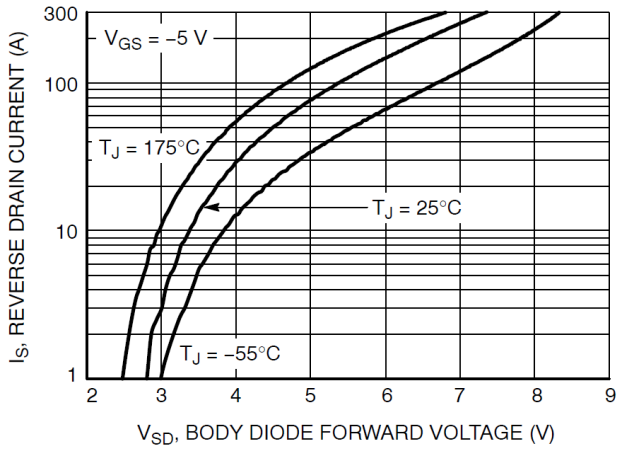


Figure 6. Diode Forward Voltage vs. Current

TYPICAL CHARACTERISTICS (CONTINUED)

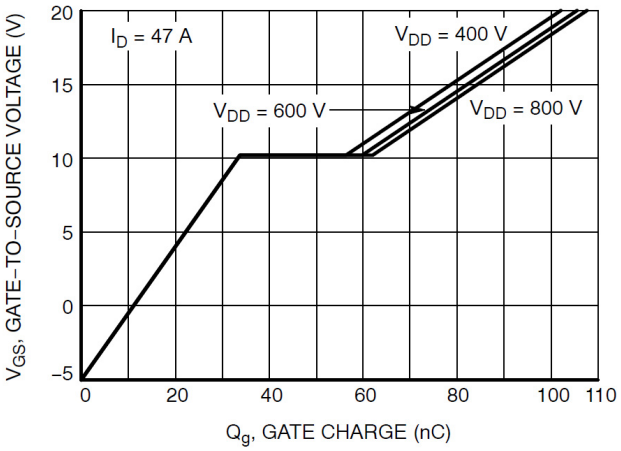


Figure 7. Gate−to−Source Voltage vs. Total Charge

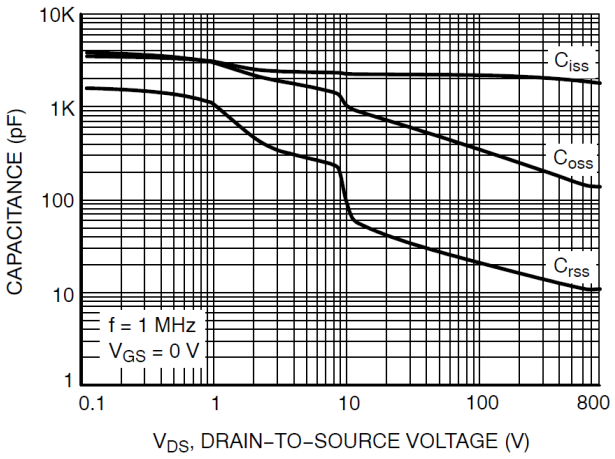


Figure 8. Capacitance vs. Drain−to−Source Voltage

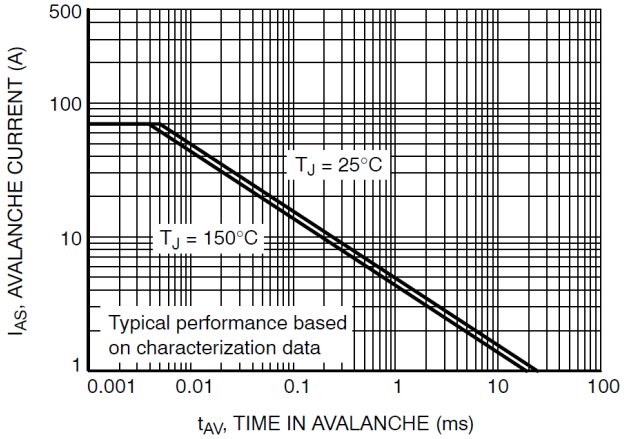


Figure 9. Unclamped Inductive Switching Capability

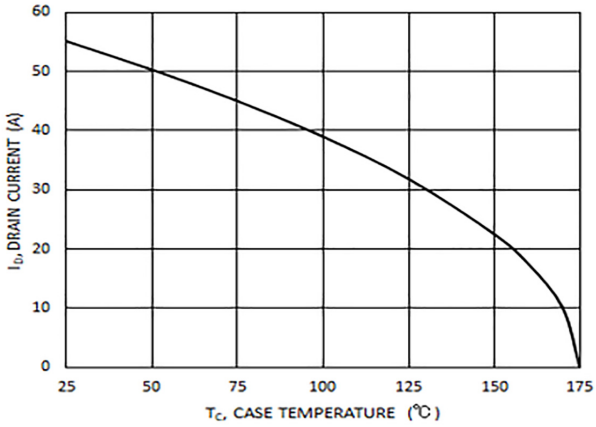


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

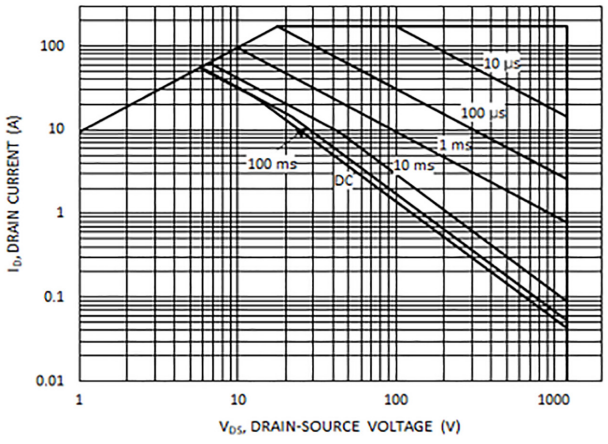


Figure 11. Safe Operating Area

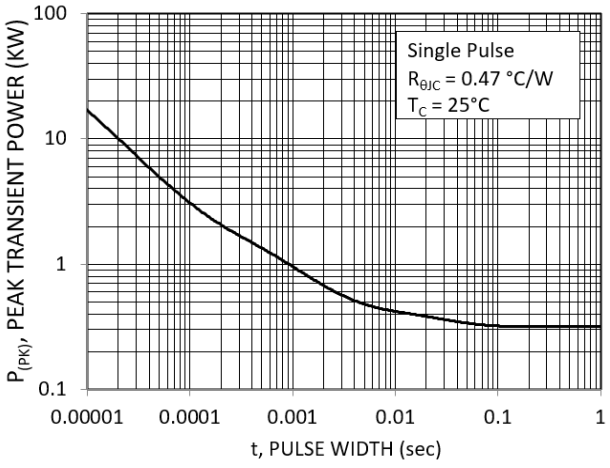


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (CONTINUED)

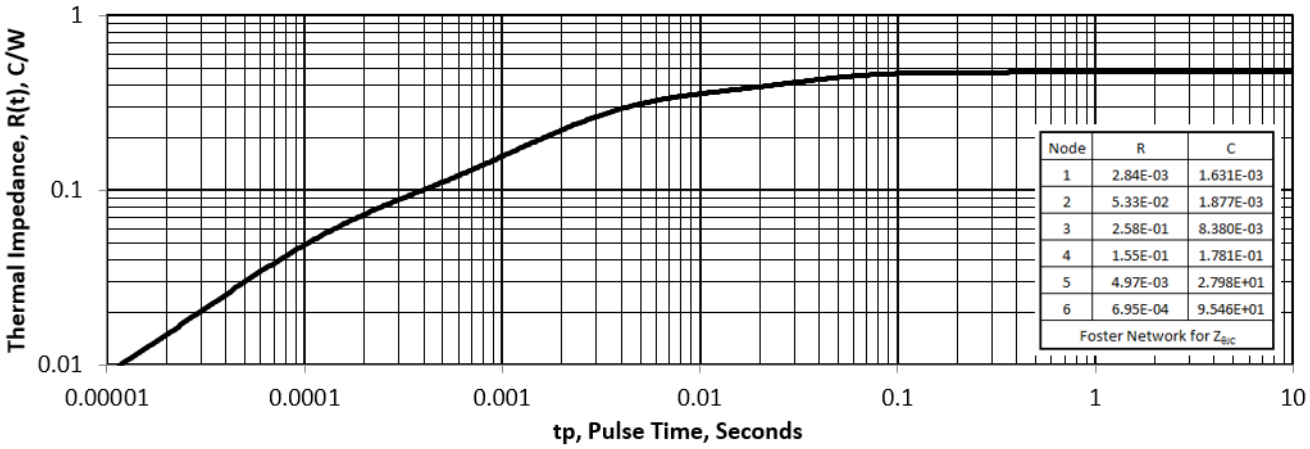
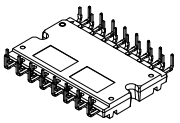


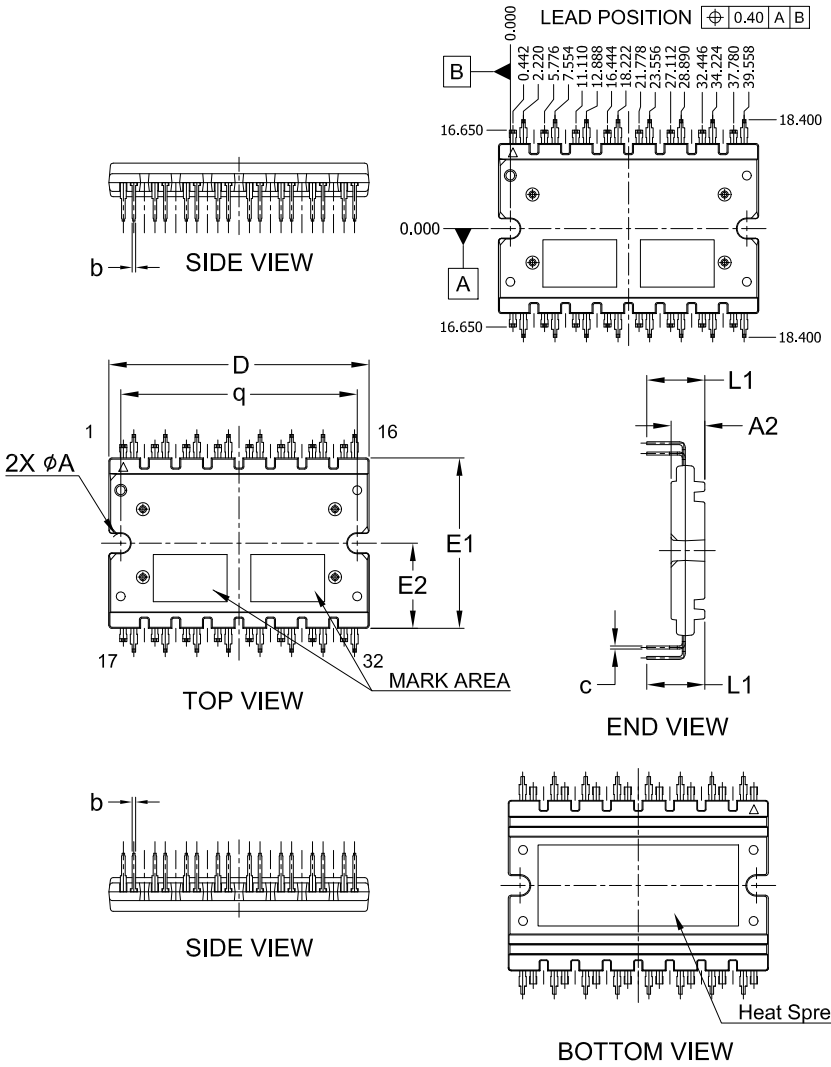
Figure 13. Thermal Response

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



APM32 44.00x28.80x5.70
CASE MODHM
ISSUE A

DATE 01 AUG 2023



NOTES:

1. DIMENSIONING AND TOLERANCING PER. ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A2	5.60	5.70	5.80
b	0.50	0.60	0.70
c	0.45	0.50	0.60
D	43.80	44.00	44.20
E1	28.60	28.80	29.00
E2	14.25	14.40	14.55
L1	9.50	9.80	10.10
q	39.85	40.00	40.15
ϕA	3.20	3.30	3.40

GENERIC MARKING DIAGRAM*

XXXXXXXXXXXXXXXXX
ZZZ ATYWW
NNNNNNN

XXXX = Specific Device Code
ZZZ = Lot ID
AT = Assembly & Test Location
Y = Year
W = Work Week
NNN = Serial Number

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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