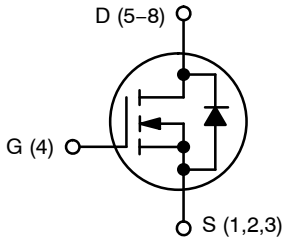
MOSFET - Power, Single N-Channel, Logic Level, μ8FL

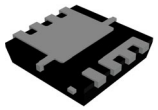
80 V, 5.3 mΩ, 79 A

NVTFWS005N08XL

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
80 V	5.3 mΩ @ 10 V	79 A
	8.4 mΩ @ 4.5 V	



N–CHANNEL MOSFET



WDFNW8
(μ8FL)
CASE 515AP

Features

- Low Q_{RR}, Soft Recovery Body Diode
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- AEC–Q101 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Synchronous Rectification (SR) in DC–DC and AC–DC
- Primary Switch in Isolated DC–DC Converter
- Motor Drives
- Automotive 48 V System

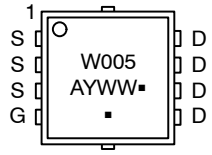
MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter		Symbol	Value	Unit
Drain–to–Source Voltage		V_{DSS}	80	V
Gate–to–Source Voltage		V_{GS}	±20	V
Continuous Drain Current (Note 1)	T_C = 25°C	I_D	79	A
	T_C = 100°C		56	
Power Dissipation (Note 1)	T_C = 25°C	P_D	82	W
	T_C = 100°C		41	
Pulsed Drain Current	T_C = 25°C, t_p = 100 μs	I_{DM}	290	A
Pulsed Source Current (Body Diode)		I_{SM}	290	
Operating Junction and Storage Temperature Range		T_J, T_{STG}	−55 to +175	°C
Source Current (Body Diode)		I_S	118	A
Single Pulse Avalanche Energy (I_{PK} = 34 A) (Note 3)		E_{AS}	57	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)		T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Actual continuous current will be limited by thermal & electromechanical application board design.
3. Surface mounted on FR4 board using a 1 in^2, 1 oz. Cu pad.
4. $R_{\theta JA}$ is determined by the users board design.

MARKING DIAGRAM



W005 = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb–Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NVTFWS005N08XLTAG	WDFN8 (μ8FL)	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	1.8	°C/W
Thermal Resistance, Junction−to−Ambient (Notes 5, 6)	$R_{\theta JA}$	46	

5. Surface−mounted on FR4 board using a 1 in^2, 1 oz. Cu pad.
6. $R_{\theta JA}$ is determined by the user's board design.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1 mA	80			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	I_D = 1 mA. Referenced to 25°C		31		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80 V			1	μA
		V_{DS} = 80 V, T_J = 125°C			250	
Gate−to−Source Leakage Current	I_{GSS}	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
ON CHARACTERISTICS						
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 17 A		4.3	5.3	mΩ
		V_{GS} = 4.5 V, I_D = 14 A		5.7	8.4	
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 85 μA	1.5		2.1	V
Gate Threshold Voltage Temperature Coefficient	$\Delta V_{GS(TH)}/\Delta T_J$	V_{GS} = V_{DS}, I_D = 85 μA		−6.4		mV/°C
Forward Transconductance	g_{FS}	V_{DS} = 5 V, I_D = 17 A		113		S
CHARGES, CAPACITANCES & GATE RESISTANCE						
Input Capacitance	C_{ISS}	V_{GS} = 0 V, V_{DS} = 40 V, f = 1 MHz		1800		pF
Output Capacitance	C_{OSS}			450		
Reverse Transfer Capacitance	C_{RSS}			14		
Output Charge	Q_{OSS}			33		nC
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DD} = 40 V; I_D = 17 A		14		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DD} = 40 V; I_D = 17 A		28		
Threshold Gate Charge	$Q_{G(TH)}$			3		
Gate−to−Source Charge	Q_{GS}			5		
Gate−to−Drain Charge	Q_{GD}			4		
Gate Plateau Voltage	V_{GP}			2.7		V
Gate Resistance	R_G	f = 1 MHz		0.6		Ω
SWITCHING CHARACTERISTICS						
Turn−On Delay Time	$t_{d(ON)}$	Resistive Load, V_{GS} = 0/10 V, V_{DD} = 64 V, I_D = 17 A, R_G = 2.5 Ω		10		ns
Rise Time	t_r			4		
Turn−Off Delay Time	$t_{d(OFF)}$			25		
Fall Time	t_f			3		
SOURCE−TO−DRAIN DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 17 A		0.8	1.2	V
		V_{GS} = 0 V, I_S = 17 A, T_J = 125°C		0.7		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI/dt = 1000 A/μs, I_S = 17 A, V_{DD} = 64 V		19		ns
Charge Time	t_a			11		
Discharge Time	t_b			9		
Reverse Recovery Charge	Q_{RR}			105		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

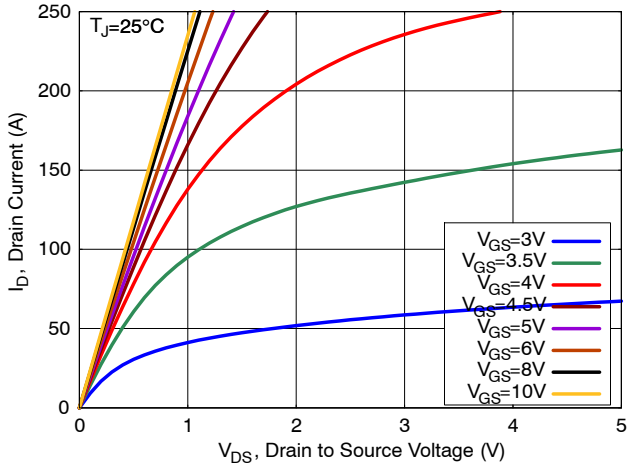


Figure 1. On−Region Characteristics

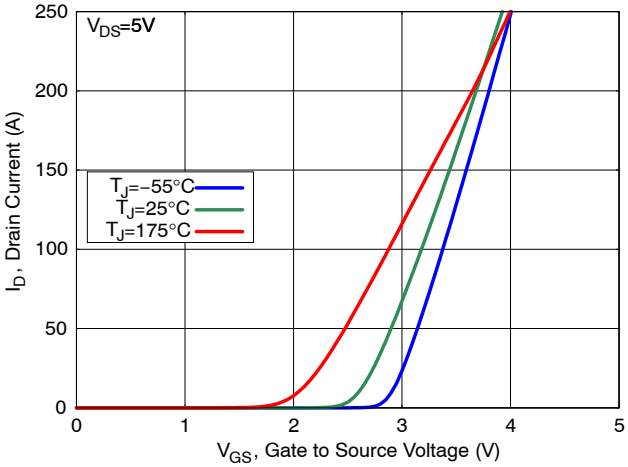


Figure 2. Transfer Characteristics

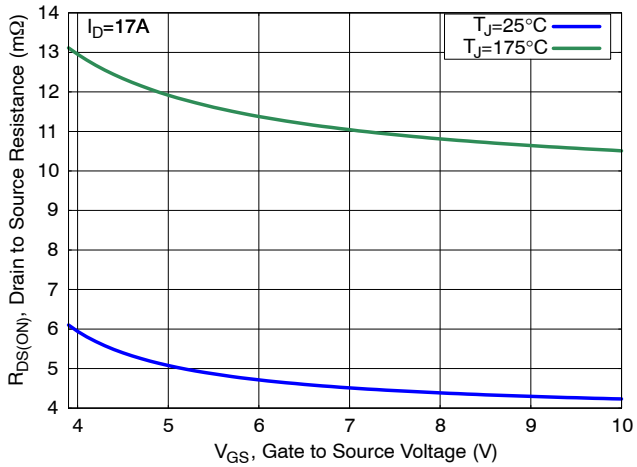


Figure 3. On−Resistance vs. Gate Voltage

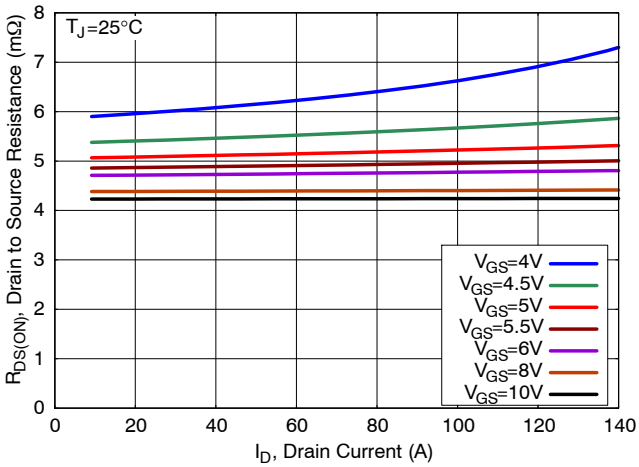


Figure 4. On−Resistance vs. Drain Current

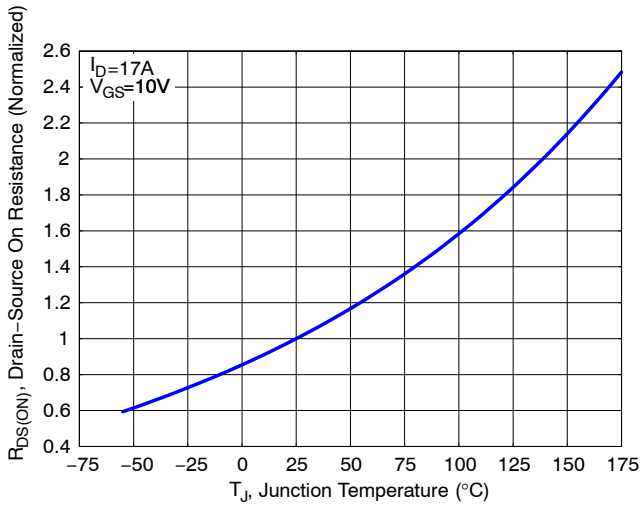


Figure 5. Normalized ON Resistance vs. Junction Temperature

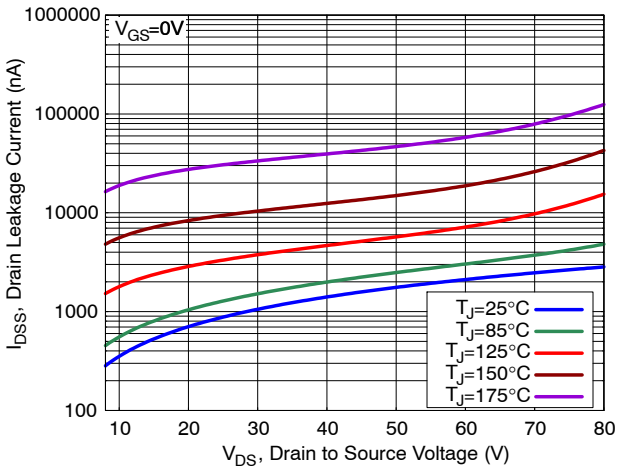


Figure 6. Drain Leakage Current vs. Drain Voltage

TYPICAL CHARACTERISTICS

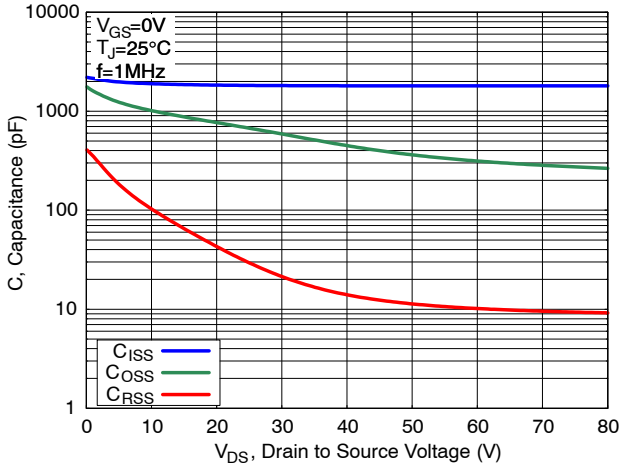


Figure 7. Capacitance Characteristics

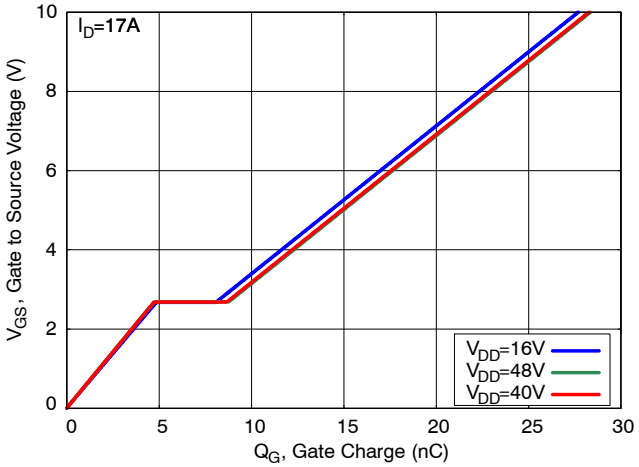


Figure 8. Gate Charge Characteristics

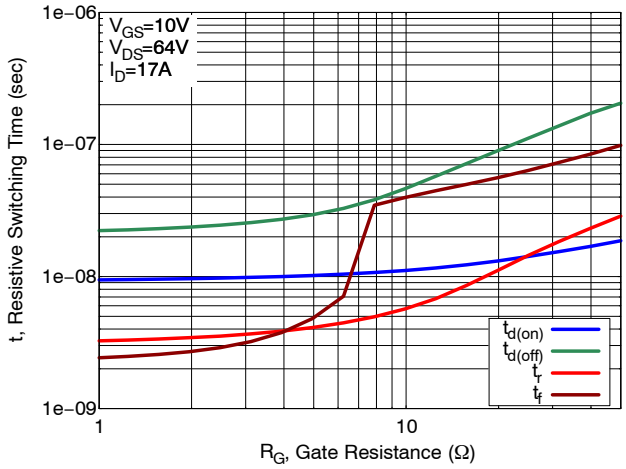


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

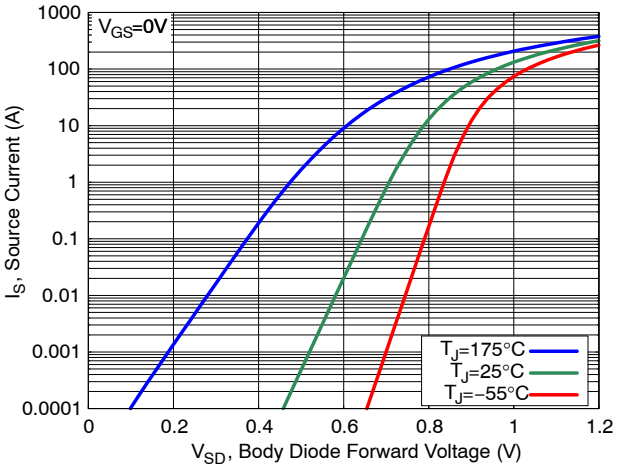


Figure 10. Diode Forward Characteristics

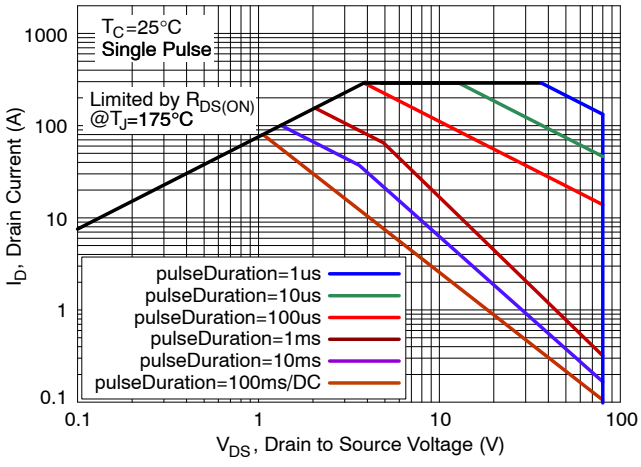


Figure 11. Safe Operating Area (SOA)

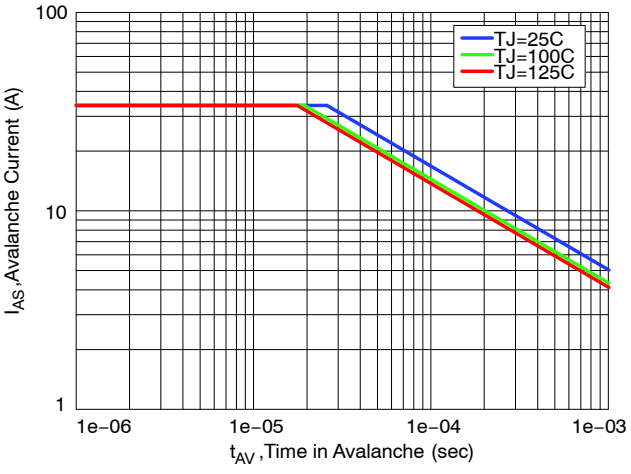


Figure 12. Avalanche Current vs. Pulse Time (UIS)

TYPICAL CHARACTERISTICS

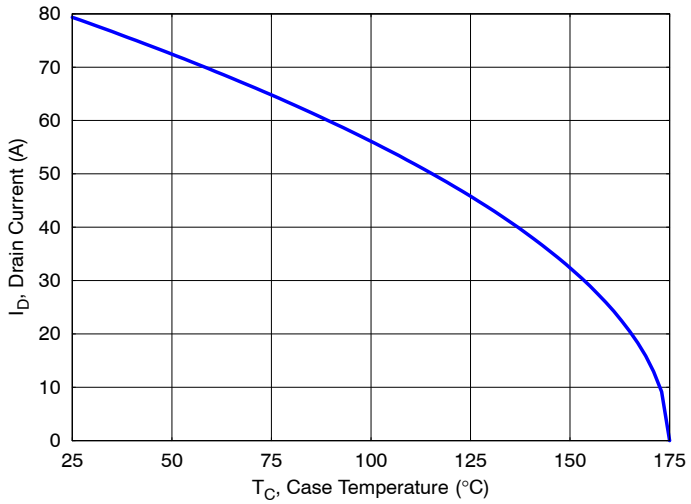


Figure 13. Maximum Current vs. Case Temperature

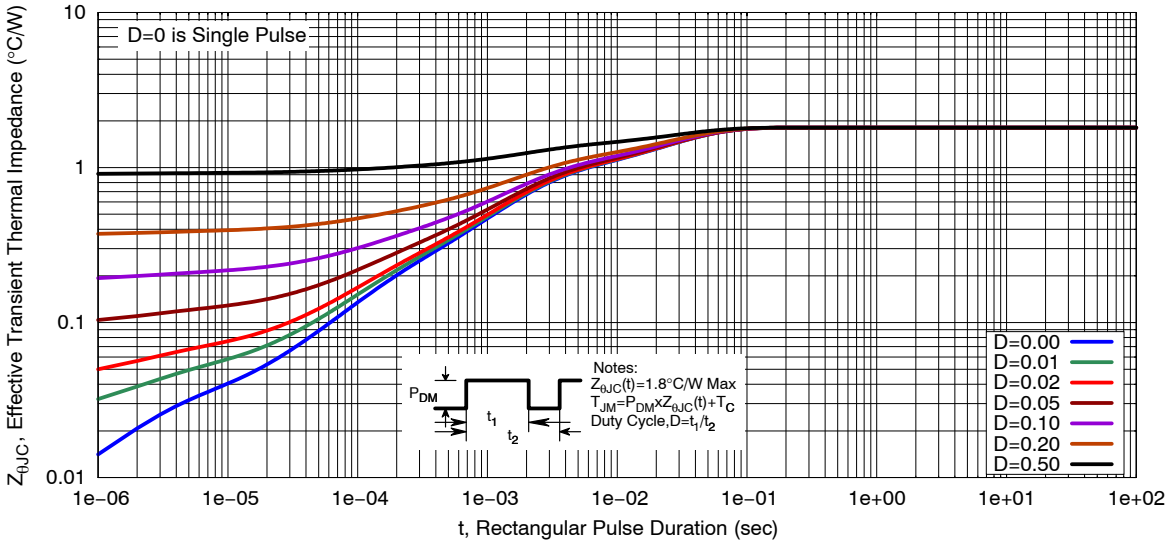
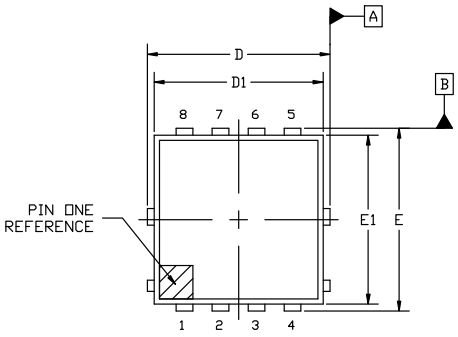


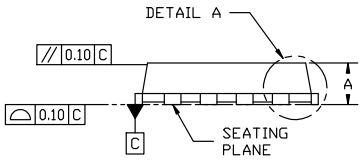
Figure 14. Transient Thermal Response

PACKAGE DIMENSIONS

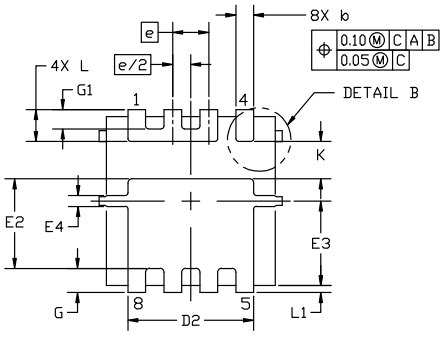
WDFNW8 3.30x3.30x0.75, 0.65P
CASE 515AP
ISSUE A



TOP VIEW



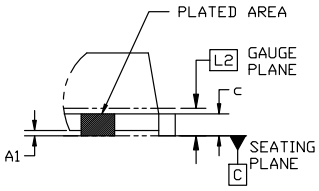
SIDE VIEW



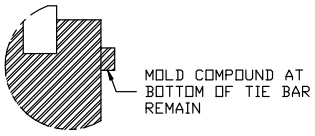
BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
4. FULL-CUT u8FL FUSED WF.

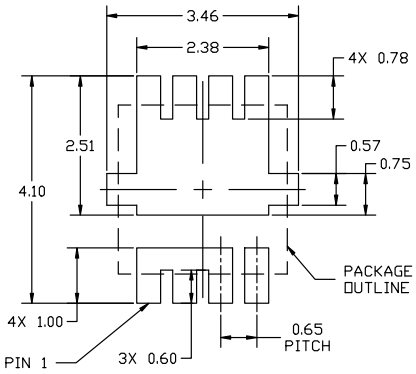


DETAIL "A"
SCALE 2:1



DETAIL "B"
SCALE 2:1

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	----	0.05
b	0.23	0.33	0.43
c	0.15	0.20	0.25
D	3.20	3.30	3.40
D1	2.95	3.13	3.30
D2	1.98	2.20	2.40
E	3.20	3.30	3.40
E1	2.80	3.00	3.15
E2	1.40	1.60	1.80
E3	1.35	1.50	1.60
E4	0.15	0.25	0.40
e	0.65 BSC		
G	0.30	0.43	0.55
G1	0.25	0.35	0.45
K	0.55	0.75	0.95
L	0.35	0.52	0.65
L1	0.06	0.15	0.30
L2	0.25 BSC		



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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