

# MOSFET - Power, Single N-Channel

60 V, 9 mΩ, 48 A

NVLJWS011N06CL

## Features

- Small Footprint for Compact Design
- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low  $Q_G$  and Capacitance to Minimize Driver Losses
- Wettable Flank Option for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

## MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			$V_{DS}$	60	V
Gate-to-Source Voltage			$V_{GS}$	$\pm 20$	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	$T_C = 25^\circ\text{C}$	$I_D$	48	A
		$T_C = 100^\circ\text{C}$		34	
Power Dissipation $R_{\theta JC}$ (Note 1)	Steady State	$T_C = 25^\circ\text{C}$	$P_D$	46	W
		$T_C = 100^\circ\text{C}$		23	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	$T_A = 25^\circ\text{C}$	$I_D$	12	A
		$T_A = 100^\circ\text{C}$		8.5	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)	Steady State	$T_A = 25^\circ\text{C}$	$P_D$	2.9	W
		$T_A = 100^\circ\text{C}$		1.4	
Pulsed Drain Current	$T_A = 25^\circ\text{C}$ , $t_p = 10 \mu\text{s}$		$I_{DM}$	233	A
Operating Junction and Storage Temperature Range			$T_J$ , $T_{stg}$	-55 to +175	$^\circ\text{C}$
Source Current (Body Diode)			$I_S$	38	A
Single Pulse Drain-to-Source Avalanche Energy ( $I_{L(pk)} = 2.3 \text{ A}$ )			$E_{AS}$	103	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			$T_L$	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

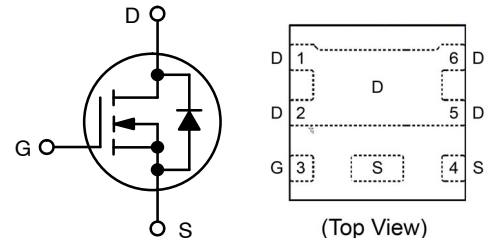
## THERMAL RESISTANCE

Parameter	Symbol	Value	Unit
Junction-to-Case	$R_{\theta JC}$	3.3	$^\circ\text{C/W}$
Junction-to-Ambient	$R_{\theta JA}$	52	

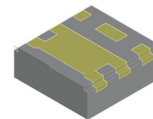
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
60 V	9 mΩ @ 10 V	48 A
	13 mΩ @ 4.5 V	

## ELECTRICAL CONNECTION



## N-CHANNEL MOSFET



WDFNW6 (2.05x2.05)  
CASE 515AD

## MARKING DIAGRAM



XXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week

## ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

# ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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## OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			27.5		mV/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 60\text{ V}$	$T_J = 25^\circ\text{C}$		10	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$		100	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

## ON CHARACTERISTICS (Note 4)

Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$		7.7	9	$\text{m}\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$		10.7	13	
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 34\text{ }\mu\text{A}$	1.2		2.0	V
Gate Threshold Voltage Temperature Coefficient	$V_{GS(TH)}/T_J$			-5.6		mV/°C
Forward Transconductance	$g_{FS}$	$V_{DS} = 6\text{ V}, I_D = 10\text{ A}$		39		S

## CHARGES AND CAPACITANCES

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 25\text{ V}$		912		pF
Output Capacitance	$C_{OSS}$			460		
Reverse Transfer Capacitance	$C_{RSS}$			8		
Total Gate Charge	$Q_{G(TOT)}$	$V_{DS} = 48\text{ V}; I_D = 10\text{ A}, V_{GS} = 4.5\text{ V}$		6.3		nC
Total Gate Charge	$Q_{G(TOT)}$	$V_{DS} = 48\text{ V}; I_D = 10\text{ A}, V_{GS} = 10\text{ V}$		13.6		nC
Threshold Gate Charge	$Q_{G(TH)}$			1.4		
Gate-to-Source Charge	$Q_{GS}$			2.5		
Gate-to-Drain Charge	$Q_{GD}$			1.4		
Plateau Voltage	$V_{GP}$			2.7		V

## SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 48\text{ V}, I_D = 10\text{ A}, R_G = 6\text{ }\Omega$		8.1		ns
Turn-Off Delay Time	$t_{d(OFF)}$			23.3		
Rise Time	$t_r$			3.0		
Fall Time	$t_f$			3.6		

## SOURCE-TO-DRAIN DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_{SD} = 10\text{ A}$	$T_J = 25^\circ\text{C}$		0.82	1.2	V
			$T_J = 125^\circ\text{C}$		0.69		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, dI/dt = 100\text{ A}/\mu\text{s}, I_{SD} = 10\text{ A}, V_{DS} = 48\text{ V}$		32		ns	
Charge Time	$t_a$			15.8			
Discharge Time	$t_b$			16			
Reverse Recovery Charge	$Q_{RR}$			20		nC	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

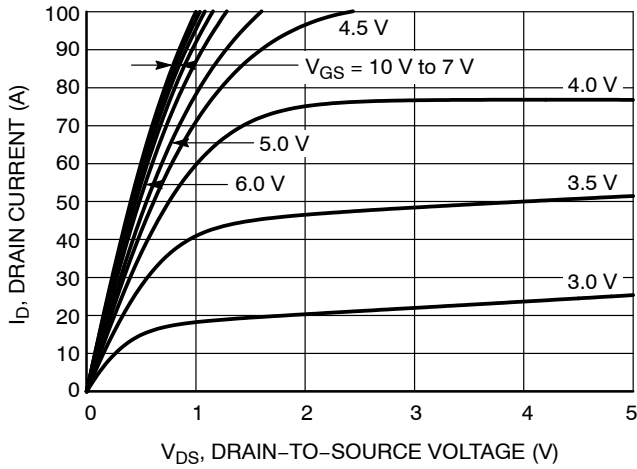


Figure 1. On-Region Characteristics

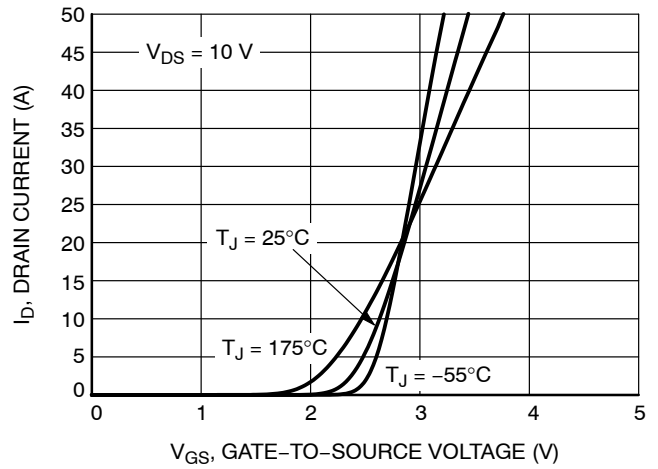


Figure 2. Transfer Characteristics

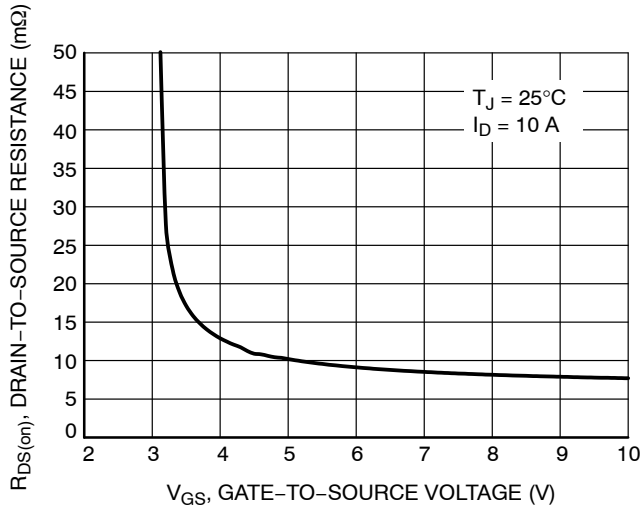


Figure 3. On-Resistance vs. Gate-to-Source Voltage

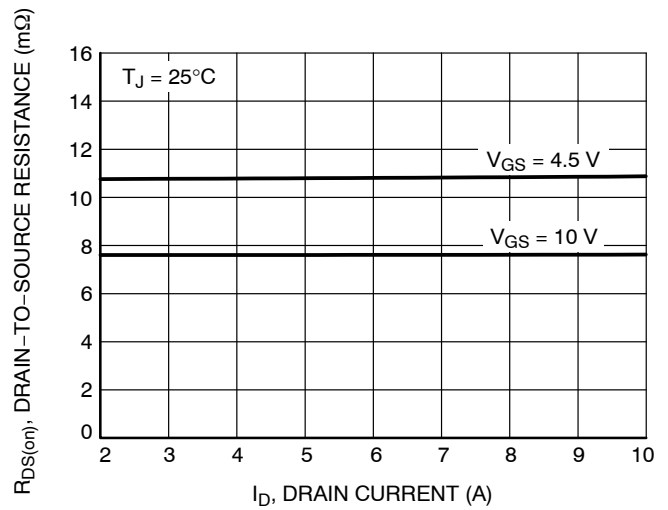


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

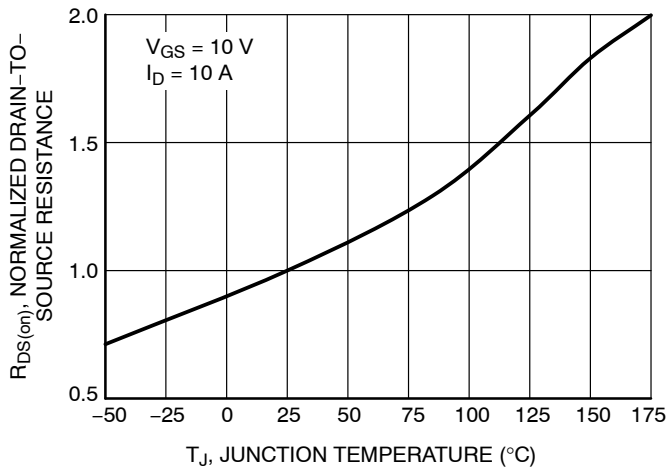


Figure 5. On-Resistance Variation with Temperature

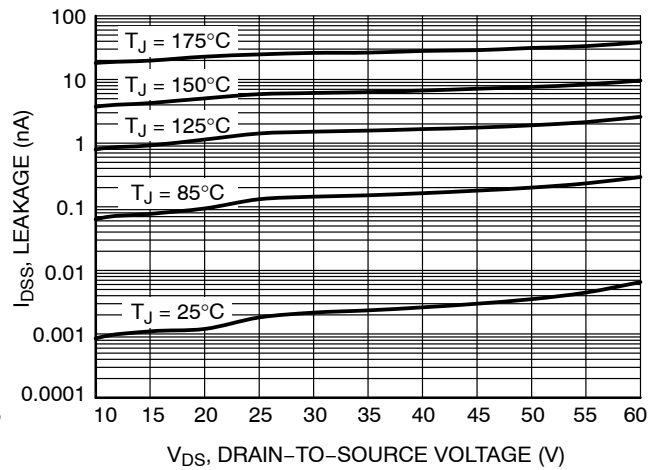


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

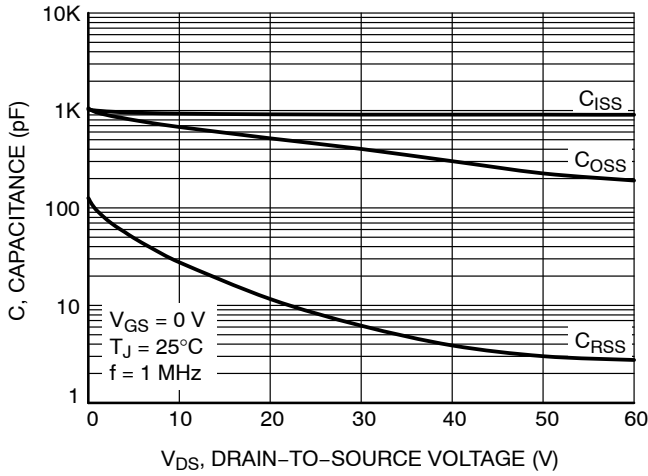


Figure 7. Capacitance Variation

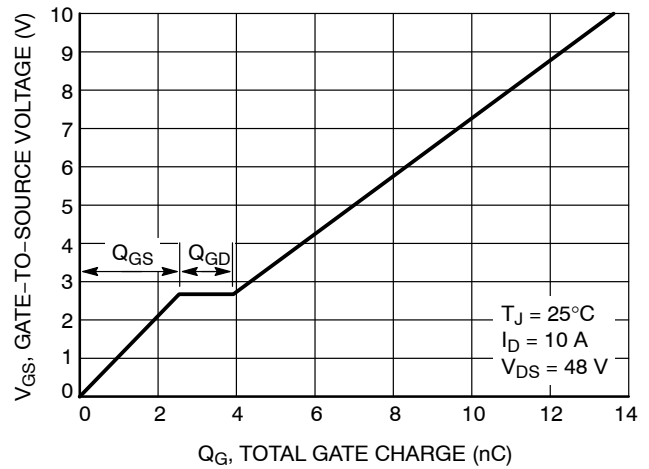


Figure 8. Gate-to-Source Voltage vs. Total Charge

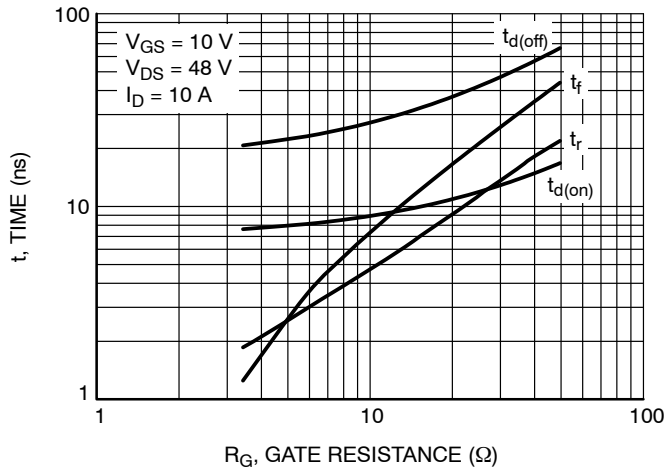


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

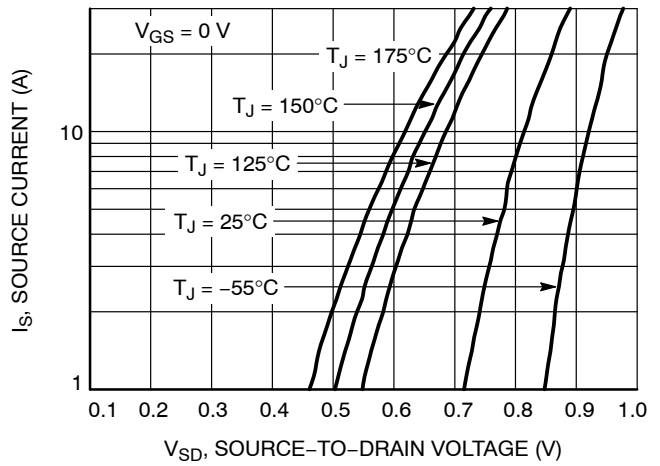


Figure 10. Diode Forward Voltage vs. Current

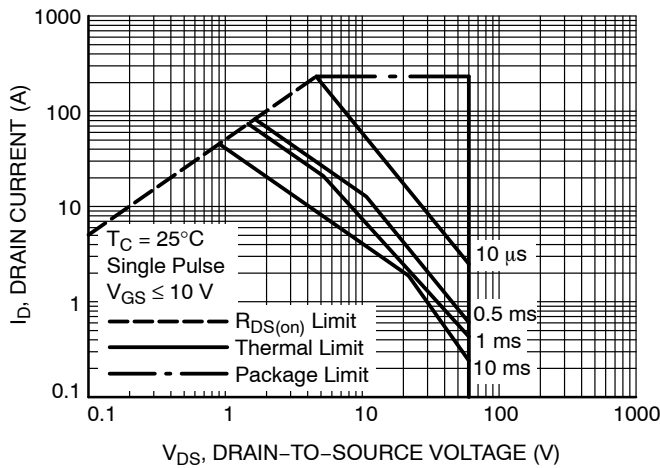


Figure 11. Maximum Rated Forward Biased Safe Operating Area

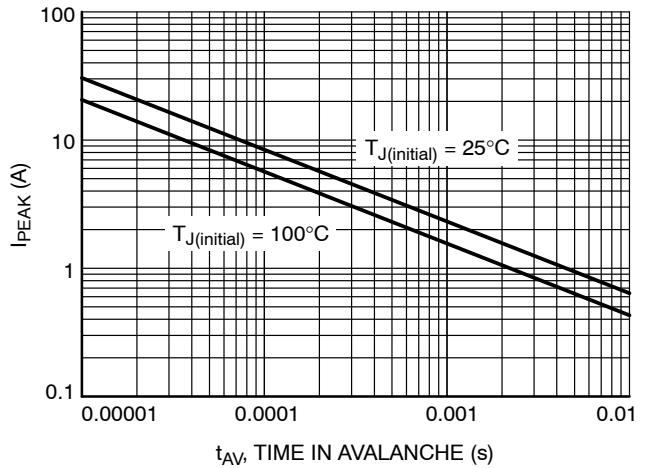


Figure 12. Maximum Drain Current vs. Time in Avalanche

# NVLJWS011N06CL

## TYPICAL CHARACTERISTICS

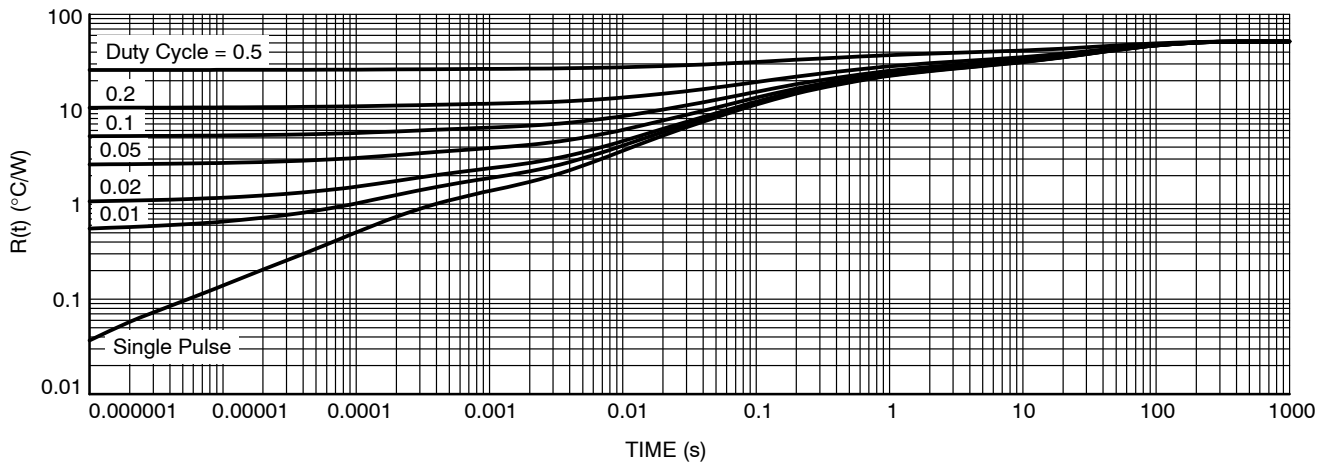


Figure 13. Transient Thermal Impedance

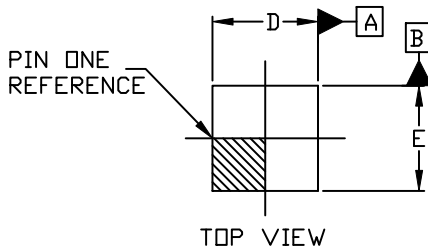
### DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping <sup>†</sup>
NVLJWS011N06CLTAG	011N	WDFNW6 (Pb-Free, Wettable Flanks)	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

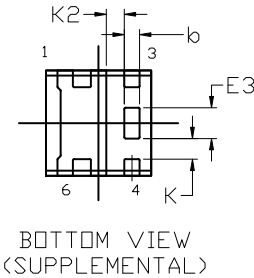
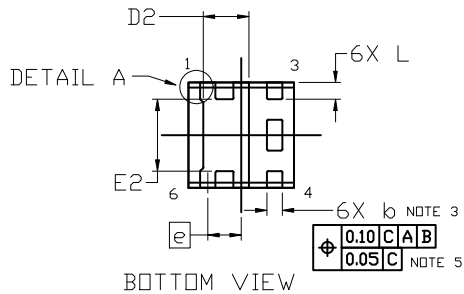
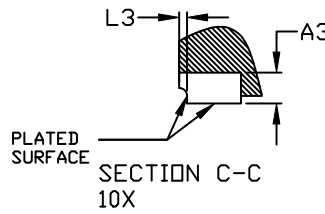
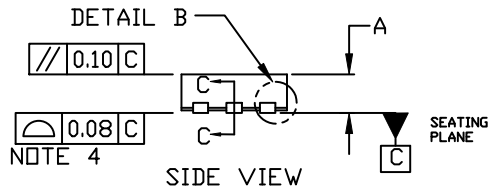
PACKAGE DIMENSIONS

WDFNW6 2.05x2.05, 0.65P  
CASE 515AD  
ISSUE O

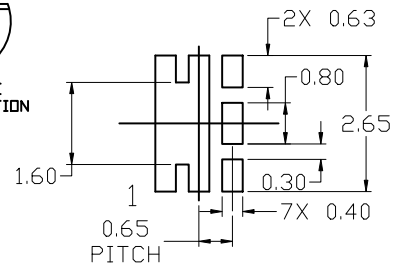
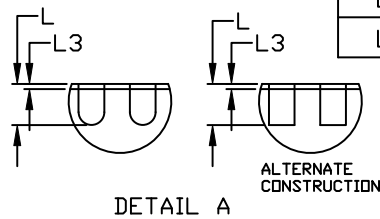
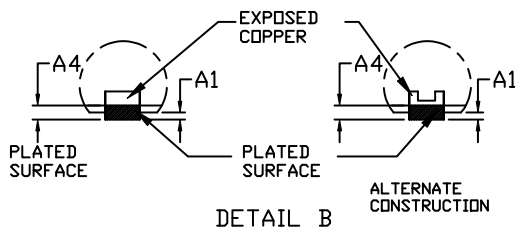


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION  $b$  APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. POSITIONAL TOLERANCE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	---	0.05
A3	0.20 REF		
A4	0.10	---	---
b	0.25	0.30	0.35
D	1.95	2.05	2.15
D2	0.84	0.89	0.94
E	1.95	2.05	2.15
E2	1.35	1.40	1.45
E3	0.55	0.60	0.65
e	0.65 BSC		
K	0.40 REF		
K2	0.35 REF		
L	0.275	0.325	0.375
L3	---	---	0.09



RECOMMENDED  
MOUNTING FOOTPRINT

\* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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