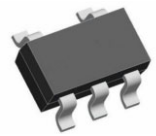
Single 2 A High-Speed, Low-Side Gate Driver

Product Preview

NCP51100



SOT23−5
CASE 527AH

The NCP51100 2 A gate driver is designed to drive an N−Channel enhancement−mode MOSFET in low −side switching applications by providing high peak current pulses during the short switching intervals. The driver is available with TTL input thresholds. Internal circuitry provides an under−voltage lockout function by holding the output LOW until the supply voltage is within the operating range. The NCP51100 delivers fast MOSFET switching performance, which helps maximize efficiency in high frequency power converter designs. NCP51100 drivers incorporate MillerDrive™ architecture for the final output stage. This bipolar−MOSFET combination provides high peak current during the Miller plateau stage of the MOSFET turn−on / turn−off process to minimize switching loss, while providing rail−to−rail voltage swing and reverse current capability. The NCP51100 is available in industry standard, 5−pin, SOT23.

Features

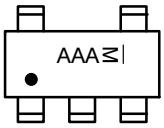
- Industry−Standard Pinouts
- 11 V to 18 V Operating Range
- 3 A Peak Sink/Source at V_{DD} = 12 V
- 2.5 A Sink / 1.8 A Source at V_{OUT} = 6 V
- 14 ns / 7 ns Typical Rise/Fall Times (1 nF Load)
- Under 20 ns Typical Propagation Delay Time
- MillerDrive™ Technology
- 5−Lead SOT23 Package
- Rated from –40°C to +125°C Ambient

Typical Applications

- Switch−Mode Power Supplies
- High−Efficiency MOSFET Switching
- Synchronous Rectifier Circuits
- DC−to−DC Converters
- Motor Control

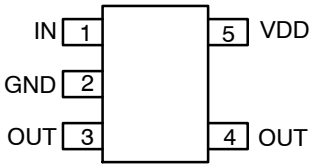
This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

MARKING DIAGRAM



AAA = Specific Device Code
M = Month Code

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping†
NCP51100ASNT1G	SOT23−5L	Tape & Reel 3000

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

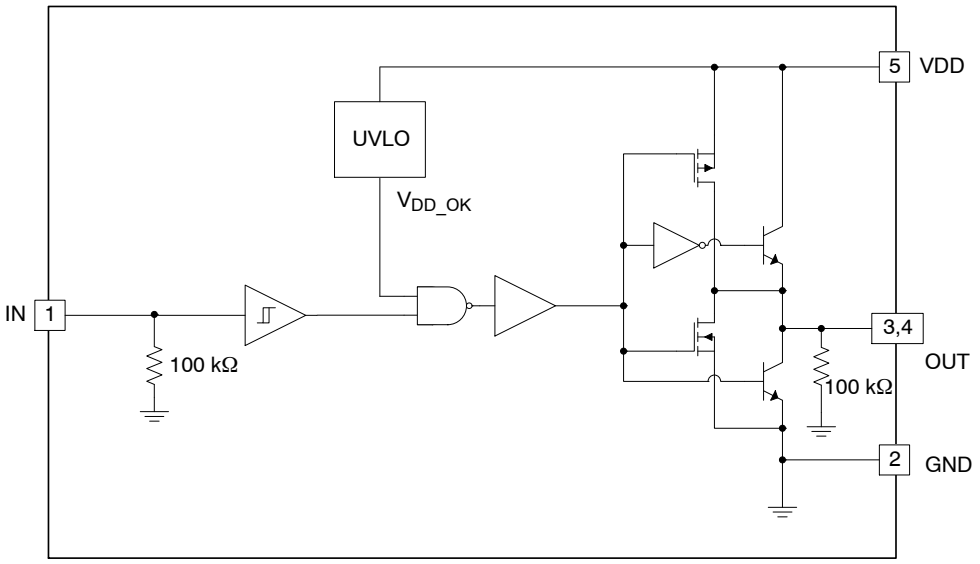


Figure 1. Internal Block Diagram

PIN CONNECTIONS

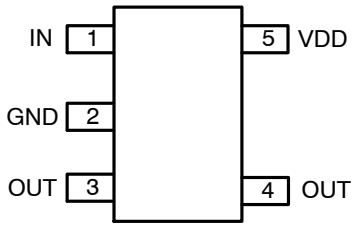


Figure 2. Pin Assignments − 5−Lead SOT23 (Top View)

PIN FUNCTION DESCRIPTION

Pin Name	Pin No.	I/O/x	Description
IN	1	I	**Non−inverting Input**
GND	2	x	**Ground.** Common ground reference for input and output circuits.
OUT	3, 4	O	**Gate Drive Output.** Held LOW unless required input(s) are present and VDD is above UVLO threshold.
VDD	5	x	**Supply Voltage.** Provides power to the IC.

OUTPUT LOGIC

NCP51100	
IN	**OUT**
0	0
1	1
No connection (Note 1)	0

1. Default input signal if no external connection is made.

MAXIMUM RATINGS (Note 2)

Symbol	Parameter		Min	Max	Unit
V_{DD}	VDD to PGND		−0.3	20.0	V
V_{IN}	IN to GND		GND − 0.3	V_{DD} + 0.3	V
V_{OUT}	OUT to GND		GND − 0.3	V_{DD} + 0.3	V
T_L	Lead Soldering Temperature (10 Seconds)		−	+260	°C
T_J	Junction Temperature		−	+150	°C
T_{STG}	Storage Temperature		−65	+150	°C
ESD_{HBM}	Electrostatic Discharge Capability (Note 3)	Human Body Model	−	3.5	kV
ESD_{CDM}		Charge Device Model	−	1	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. All voltage values are given with respect to GND pin.
3. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per JESD22−A114
   ESD Charged Device Model tested per JESD22−C101

THERMAL CHARACTERISTICS

Symbol	Rating	Value	Unit
θ_{JA}	Thermal Characteristics, 5L−SOT23 (Note 4) Thermal Resistance Junction−Air (Note 5)	157	°C/W
P_D	Power Dissipation (Note 5)	0.8	W

4. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
5. JEDEC standard: JESD51−2, JESD51−3. Mounted on 76.2 x 114.3 x 1.6 mm PCB (FR−4 glass epoxy material).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{DD}	Supply Voltage Range		11	18	V
V_{IN}	Input Voltage		0	V_{DD}	V
V_{OUT}	OUT to GND	Repetitive Pulse < 200 ns	−2.0	V_{DD} + 0.3	V
T_A	Operating Ambient Temperature		−40	+125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS

V_{CC} = 12 V, for typical values T_A = 25°C, for min/max values T_A = −40°C to +125°C, unless otherwise specified. (Notes 7, 8)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
SUPPLY						
V_{DD}	Operating Range		11	–	18.0	V
I_{DD}	Supply Current, Inputs Not Connected		–	0.55	0.8	mA
V_{ON}	Turn−On Voltage		9	10	11	V
V_{OFF}	Turn−Off Voltage		8	9	10	V
$V_{HYS\_ON, OFF}$	V_{ON} and V_{OFF} Hysteresis Voltage		–	1	–	V
t_{VDDON}	VDD ON Filter Debounce Time (Note 6)		–	5	7	μs
INPUTS						
V_{IL}	IN Logic LOW Threshold		0.8	1.2	–	V
V_{IH}	IN Logic HIGH Threshold		–	1.6	2.0	V
$V_{IN−HYST}$	TTL Logic Hysteresis Voltage		0.2	0.4	0.8	V
I_{IN}	Non−Inverting Input Current	IN from 0 to V_{DD}	−1	–	175	μA
OUTPUTS						
I_{SINK}	OUT Current, Mid−Voltage, Sinking (Note 6)	OUT at V_{DD}/2, C_{LOAD} = 0.1 μF, f = 1 kHz	–	2.5	–	A
I_{SOURCE}	OUT Current, Mid−Voltage, Sourcing (Note 6)	OUT at V_{DD}/2, C_{LOAD} = 0.1 μF, f = 1 kHz	–	−1.8	–	A
I_{PK_SINK}	OUT Current, Peak, Sinking (Note 6)	C_{LOAD} = 0.1 μF, f = 1 kHz	–	3	–	A
I_{PK_SOURCE}	OUT Current, Peak, Sourcing (Note 6)	C_{LOAD} = 0.1 μF, f = 1 kHz	–	−3	–	A
t_{RISE}	Output Rise Time (Note 8)	C_{LOAD} = 1000 pF	–	14	20	ns
t_{FALL}	Output Fall Time (Note 8)	C_{LOAD} = 1000 pF	–	7	17	ns
t_{D1}	Output Propagation Delay, TTL Inputs (Note 8)	0 to 5 V_{IN}, 1 V/ns Slew Rate	9	10	30	ns
t_{D2}		5 to 0 V_{IN}, 1 V/ns Slew Rate	9	14	30	ns
I_{RVS}	Output Reverse Current Withstand (Note 6)		–	500	–	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. This parameter, although guaranteed by design, is not tested in production.
7. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at T_J = T_A = 25°C.
8. See Timing Diagram of Figure 3.

TIMING DIAGRAMS

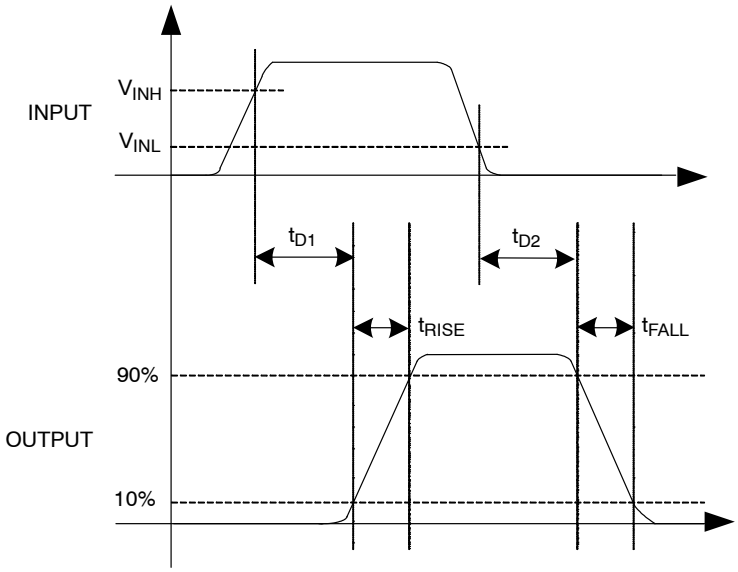


Figure 3. Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

(Typical characteristic are provide at 25°C and VDD = 12 V unless otherwise noted.)

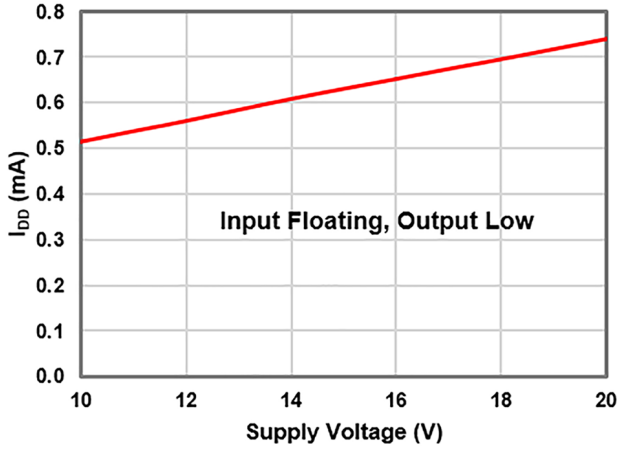


Figure 4. I_{DD} (Static) vs. Voltage

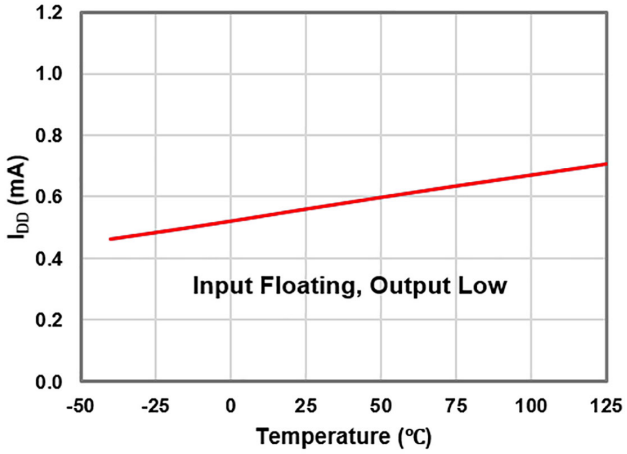


Figure 5. I_{DD} (Static) vs. Temperature

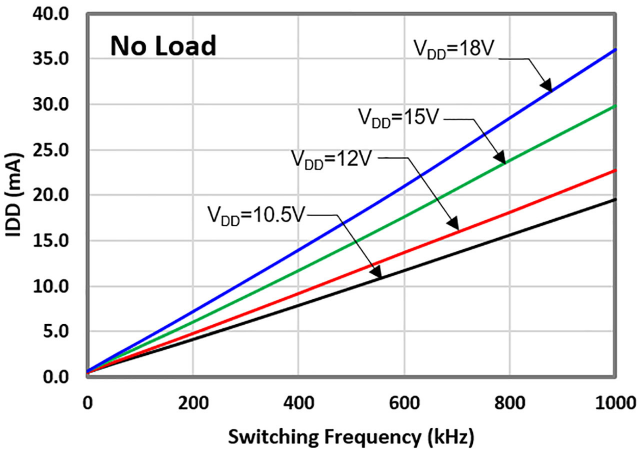


Figure 6. I_{DD} (No Load) vs. Frequency

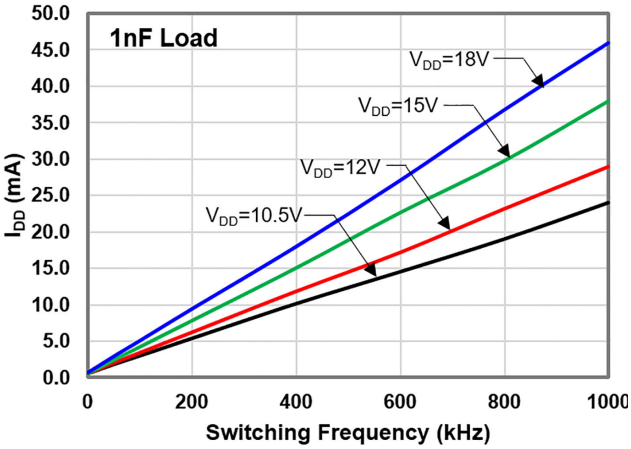


Figure 7. I_{DD} (1 nF Load) vs. Frequency

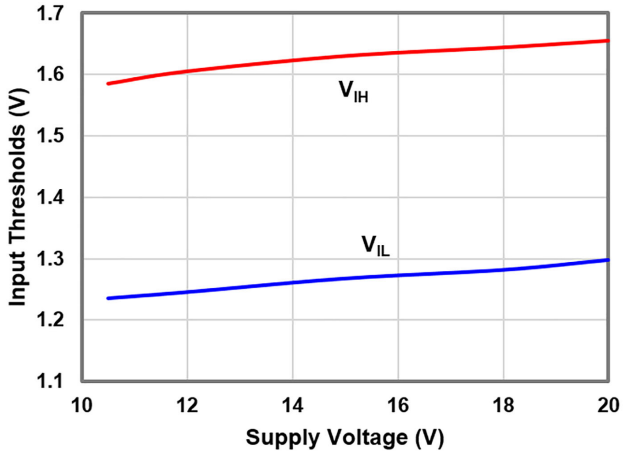


Figure 8. Input Threshold vs. Supply Voltage

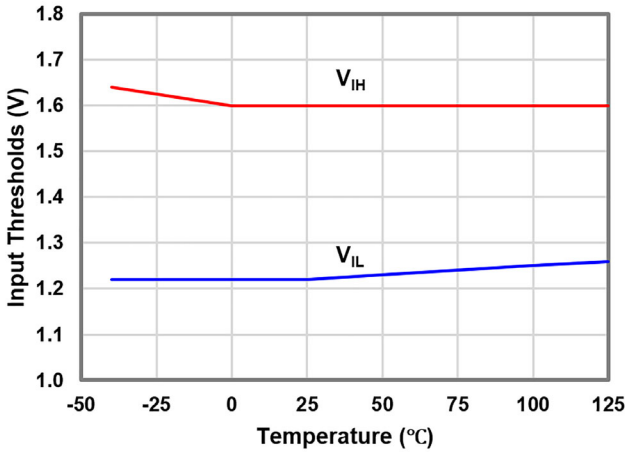


Figure 9. Input Thresholds vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(Typical characteristic are provide at 25°C and VDD = 12 V unless otherwise noted.)

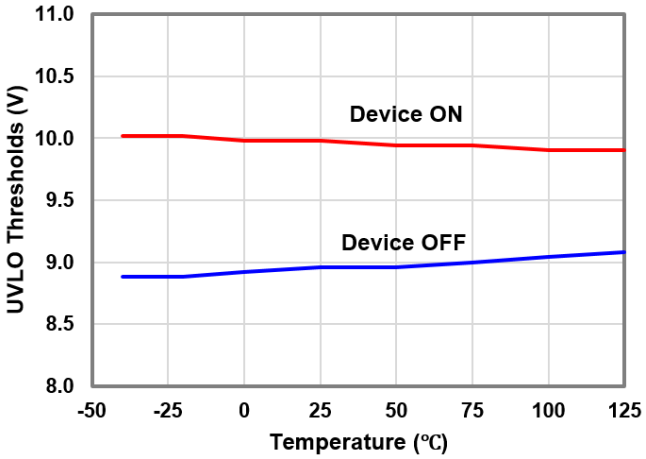


Figure 10. UVLO Threshold vs. Temperature

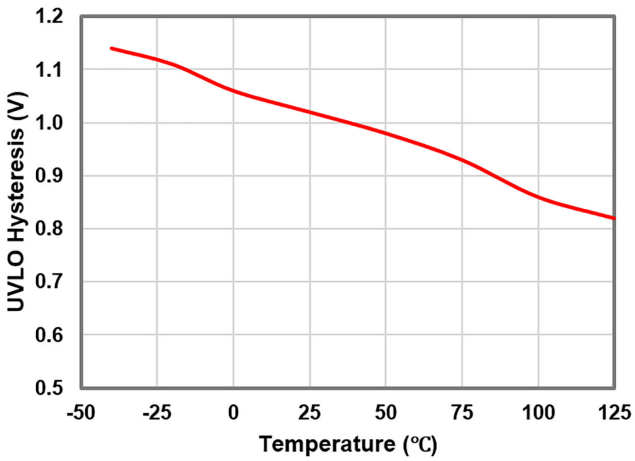


Figure 11. UVLO Hysterisis vs. Temperature

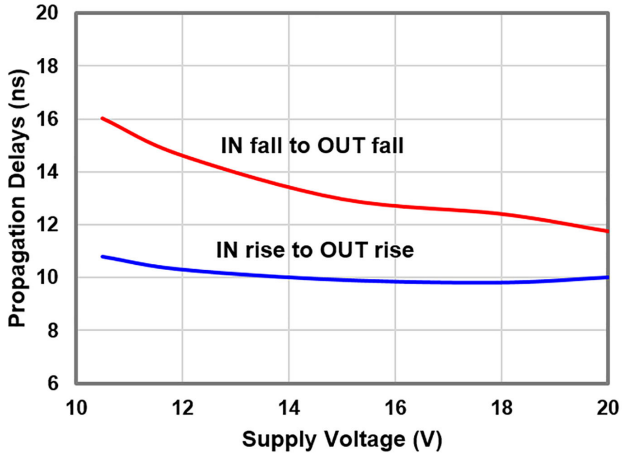


Figure 12. Propagation Delay vs. Supply Voltage

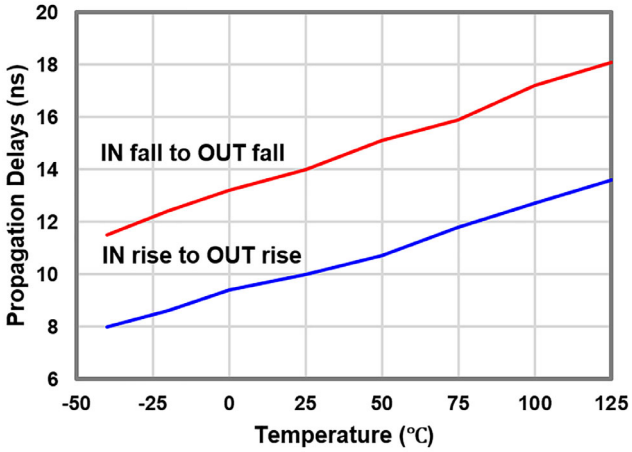


Figure 13. Propagation Delay vs. Temperature

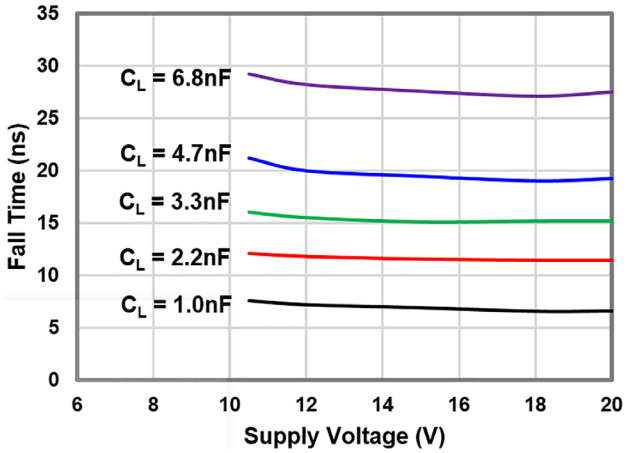


Figure 14. Fall Time vs. Supply Voltage

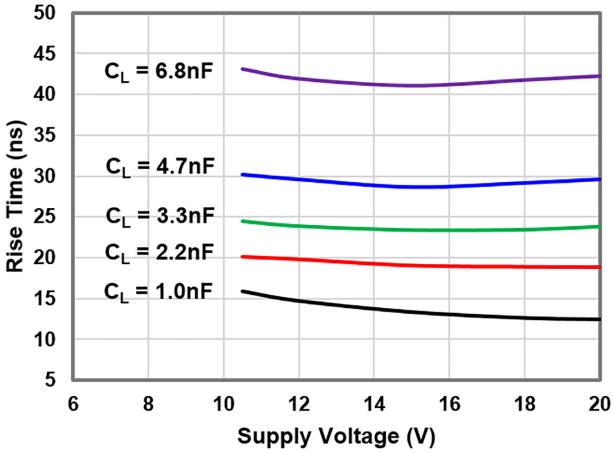


Figure 15. Rise Time vs. Supply Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(Typical characteristic are provide at 25°C and VDD = 12 V unless otherwise noted.)

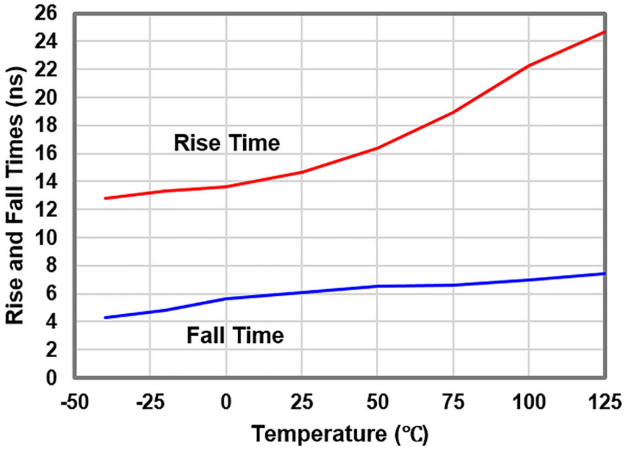


Figure 16. Rise and Fall Time vs. Temperature

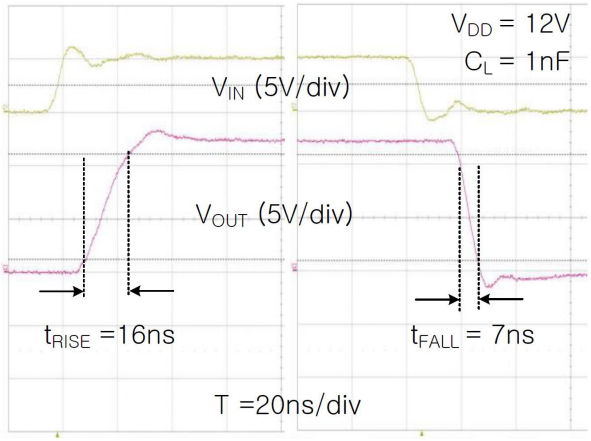


Figure 17. Rise / Fall Waveforms with 1 nF Load

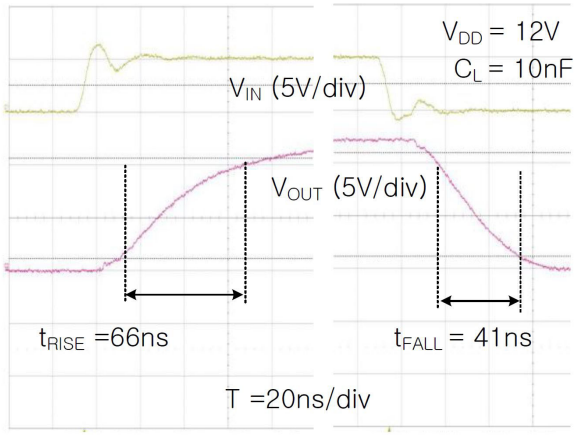


Figure 18. Rise / Fall Waveforms with 10 nF Load

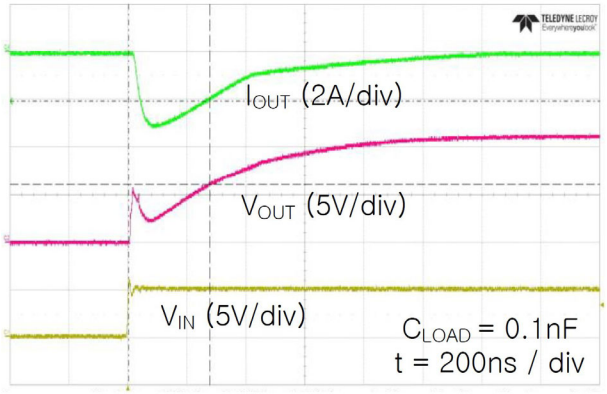


Figure 19. Quasi−Static Source Current with V_{DD} = 12 V

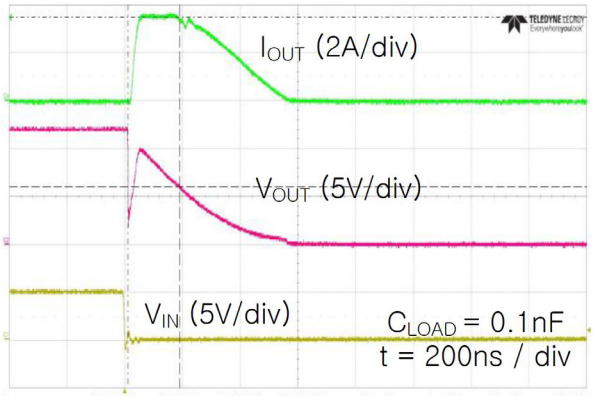


Figure 20. Quasi−Static Sink Current with V_{DD} = 12 V

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(Typical characteristic are provide at 25°C and VDD = 12 V unless otherwise noted.)

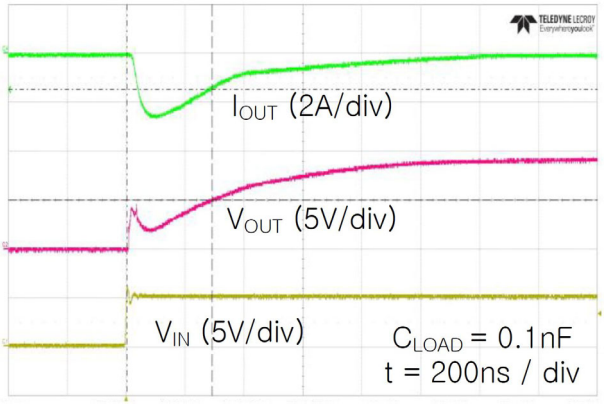


Figure 21. Quasi−Static Source Current with V_{DD} = 10 V

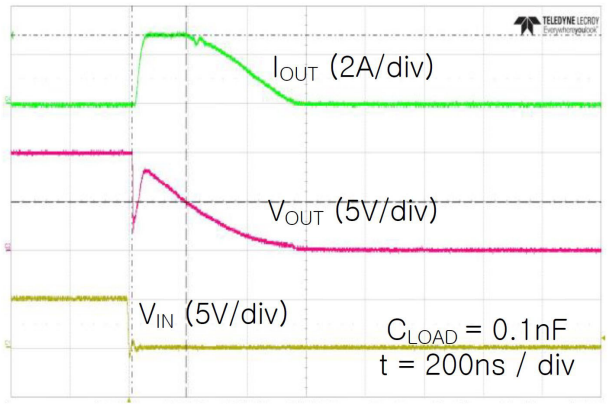


Figure 22. Quasi−Static Sink Current with V_{DD} = 10 V

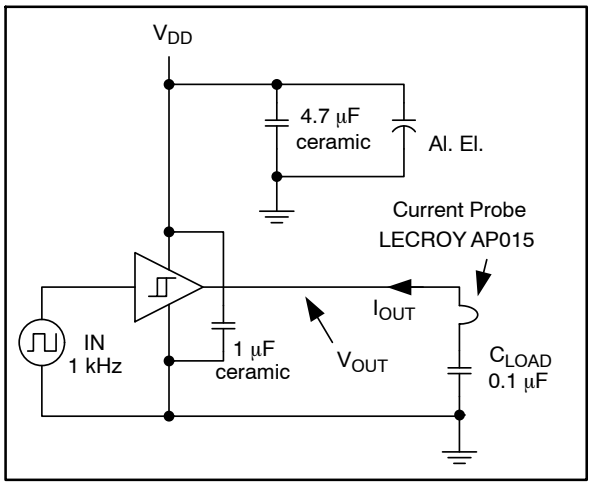


Figure 23. I_{DD} (1 nF Load) vs. Frequency

APPLICATION INFORMATION

Input Thresholds

The NCP51100 offers TTL input thresholds which meet industry−standard TTL logic thresholds, independent of the V_{DD} voltage and there is a hysteresis voltage of approximately 0.4 V. These levels permit the inputs to be driven from a range of input logic signal levels for which a voltage over 2 V is considered logic HIGH. The driving signal for the TTL inputs should have fast rising and falling edges with a slew rate of 6 V/μs or faster, so a rise time from 0 V to 3.3 V should be 550 ns or less. With reduced slew rate, circuit noise could cause the driver input voltage to exceed the hysteresis voltage and retrigger the driver input, causing erratic operation.

Static Supply Current

In these cases, the actual static IDD current is the value obtained from the curves plus this additional current. In the IDD (static) typical performance characteristics shown in Figure 4 and Figure 5, each curve is produced with both inputs floating and both outputs LOW to indicate the lowest static IDD current. For other states, additional current flows through the 100 kΩ resistors on the inputs and outputs shown in the block diagram of each part (see Figure 1). In these cases, the actual static IDD current is the value obtained from the curves plus this additional current.

MillerDrive™ Gate Drive Technology

NCP51100 drivers incorporate the MillerDrive architecture shown in Figure 24 for the output stage, a combination of bipolar and MOS devices capable of providing large currents over a wide range of supply voltage and temperature variations. The bipolar devices carry the bulk of the current as OUT swings between 1/3 to 2/3 V_{DD} and the MOS devices pull the output to the high or low rail.

The purpose of the MillerDrive architecture is to speed up switching by providing the highest current during the Miller plateau region when the gate−drain capacitance of the MOSFET is being charged or discharged as part of the turn−on / turn−off process. For applications that have zero voltage switching during the MOSFET turn−on or turn−off interval, the driver supplies high peak current for fast switching even though the Miller plateau is not present. This situation often occurs in synchronous rectifier applications because the body diode is generally conducting before the MOSFET is switched on.

The output pin slew rate is determined by V_{DD} voltage and the load on the output. It is not user adjustable, but if a slower rise or fall time at the MOSFET gate is needed, a series resistor can be added.

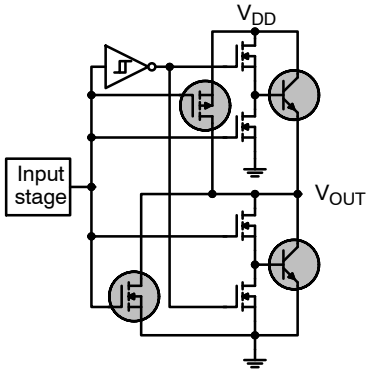


Figure 24. MillerDrive™ Output Architecture

Under−Voltage Lockout

The NCP51100 start−up logic is optimized to drive ground referenced N−channel MOSFETs with a under−voltage lockout (UVLO) function to ensure that the IC starts up in an orderly fashion. When V_{DD} is rising, yet below the 10 V operational level, this circuit holds the output LOW, regardless of the status of the input pins. After the part is active, the supply voltage must drop 1 V before the part shuts down. This hysteresis helps prevent chatter when low V_{DD} supply voltages have noise from the power switching. This configuration is not suitable for driving high−side P−channel MOSFETs because the low output voltage of the driver would turn the P−channel MOSFET on with V_{DD} below 10 V.

VDD Bypass Capacitor Guidelines

To enable this IC to turn a power device on quickly, a local, high−frequency, bypass capacitor C_{BYP} with low ESR and ESL should be connected between the VDD and GND pins with minimal trace length. This capacitor is in addition to bulk electrolytic capacitance of 10 μF to 47 μF often found on driver and controller bias circuits.

A typical criterion for choosing the value of C_{BYP} is to keep the ripple voltage on the V_{DD} supply ≤5%. Often this is achieved with a value ≥20 times the equivalent load capacitance C_{EQV}, defined here as Q_{gate}/V_{DD}. Ceramic capacitors of 0.1 μF to 1 μF or larger are common choices, as are dielectrics, such as X5R and X7R, which have good temperature characteristics and high pulse current capability.

If circuit noise affects normal operation, the value of C_{BYP} may be increased to 50−100 times the C_{EQV}, or C_{BYP} may be split into two capacitors. One should be a larger value, based on equivalent load capacitance, and the other a smaller value, such as 1−10 nF, mounted closest to the VDD and GND pins to carry the higher−frequency components of the current pulses.

Layout and Connection Guidelines

The NCP51100 incorporates fast−reacting input circuits, short propagation delays, and powerful output stages capable of delivering current peaks over 2 A to facilitate voltage transition times from under 10 ns to over 100 ns. The following layout and connection guidelines are strongly recommended:

- Keep high−current output and power ground paths separate from logic input signals and signal ground paths. This is especially critical when dealing with TTL−level logic thresholds.
- Keep the driver as close to the load as possible to minimize the length of high−current traces. This reduces the series inductance to improve high−speed switching, while reducing the loop area that can radiate EMI to the driver inputs and other surrounding circuitry.
- Many high−speed power circuits can be susceptible to noise injected from their own output or other external sources, possibly causing output re−triggering. These effects can be especially obvious if the circuit is tested in breadboard or non−optimal circuit layouts with long input, enable, or output leads. For best results, make connections to all pins as short and direct as possible.
- The turn−on and turn−off current paths should be minimized as discussed in the following sections.

Figure 25 shows the pulsed gate drive current path when the gate driver is supplying gate charge to turn the MOSFET on. The current is supplied from the local bypass capacitor, C_{BYP}, and flows through the driver to the MOSFET gate and to ground. To reach the high peak currents possible, the resistance and inductance in the path should be minimized. The localized C_{BYP} acts to contain the high peak current pulses within this driver−MOSFET circuit, preventing them from disturbing the sensitive analog circuitry in the PWM controller.

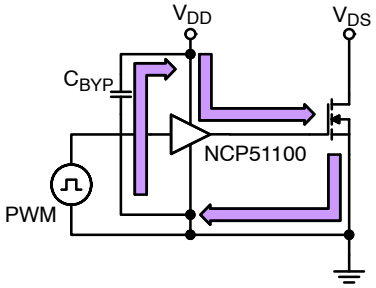


Figure 25. Current Path for MOSFET Turn−On

Figure 26 shows the current path when the gate driver turns the MOSFET off. Ideally, the driver shunts the current directly to the source of the MOSFET in a small circuit loop. For fast turn−off times, the resistance and inductance in this path should be minimized.

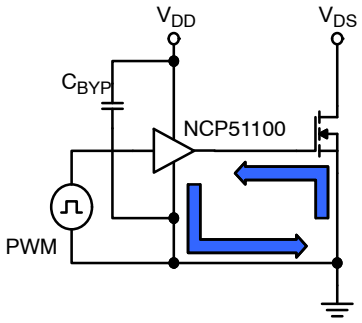


Figure 26. Current Path for MOSFET Turn−Off

Operational Waveforms

At power up, the driver output remains LOW until the V_{DD} voltage reaches the turn−on threshold. The magnitude of the OUT pulses rises with V_{DD} until steady−state V_{DD} is reached. The non−inverting operation illustrated in Figure 27 shows that the output remains LOW until the UVLO threshold is reached, then the output is in−phase with the input.

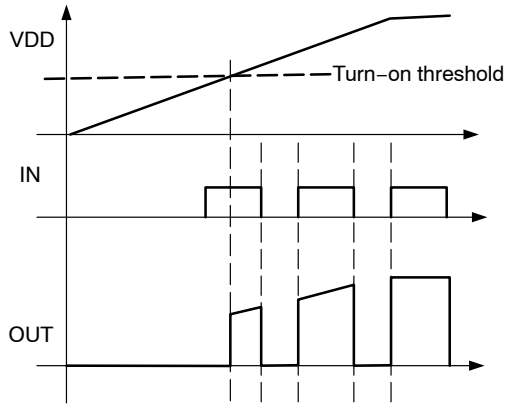


Figure 27. Start−Up Waveforms

Thermal Guidelines

Gate drivers used to switch MOSFETs and IGBTs at high frequencies can dissipate significant amounts of power. It is important to determine the driver power dissipation and the resulting junction temperature in the application to ensure that the part is operating within acceptable temperature limits.

The total power dissipation in a gate driver is the sum of three components; P_{GATE}, $P_{QUIESCENT}$, and $P_{DYNAMIC}$:

$$P_{total} = P_{gate} + P_{Dynamic} \quad \text{(eq. 1)}$$

Gate Driving Loss: The most significant power loss results from supplying gate current (charge per unit time) to switch the load MOSFET on and off at the switching frequency. The power dissipation that results from driving a MOSFET at a specified gate−source voltage, V_{GS}, with

gate charge, Q_G, at switching frequency, f_{SW}, is determined by:

$$P_{GATE} = Q_G \cdot V_{GS} \cdot f_{SW} \quad \text{(eq. 2)}$$

Dynamic Pre−drive / Shoot−through Current: A power loss resulting from internal current consumption under dynamic operating conditions, including pin pull−up / pull−down resistors, can be obtained using the graphs in Figure 6 and Figure 7 in Typical Performance Characteristics to determine the current $I_{DYNAMIC}$ drawn from V_{DD} under actual operating conditions:

$$P_{DYNAMIC} = I_{DYNAMIC} \cdot V_{DD} \quad \text{(eq. 3)}$$

Once the power dissipated in the driver is determined, the driver junction temperature rise with respect to the device lead can be evaluated using thermal equation:

$$T_J = P_{TOTAL}\,\Theta_{JL} + T_C \quad \text{(eq. 4)}$$

where

T_J = driver junction temperature;

θ_{JL} = thermal resistance from junction to lead; and

T_L = lead temperature of device in application

The power dissipated in a gate−drive circuit is independent of the drive−circuit resistance and is split proportionately among the resistances present in the driver, any discrete series resistor present, and the gate resistance internal to the power switching MOSFET. Power dissipated in the driver may be estimated using the following equation:

$$P_{PKG} = P_{TOTAL}\left(\frac{R_{OUT,\,Driver}}{R_{OUT,\,DRIVER} + R_{EXT} + R_{GATE,\,FET}}\right) \quad \text{(eq. 5)}$$

where

P_{PKG} = power dissipated in the driver package;

$R_{OUT,\,DRIVER}$ = estimated driver impedance derived from I_{OUT} vs. V_{OUT} waveforms;

R_{EXT} = external series resistance connected between the driver output and the gate of the MOSFET; and

$R_{GATE,\,FET}$ = resistance internal to the load MOSFET gate and source connections

TYPICAL APPLICATION DIAGRAMS

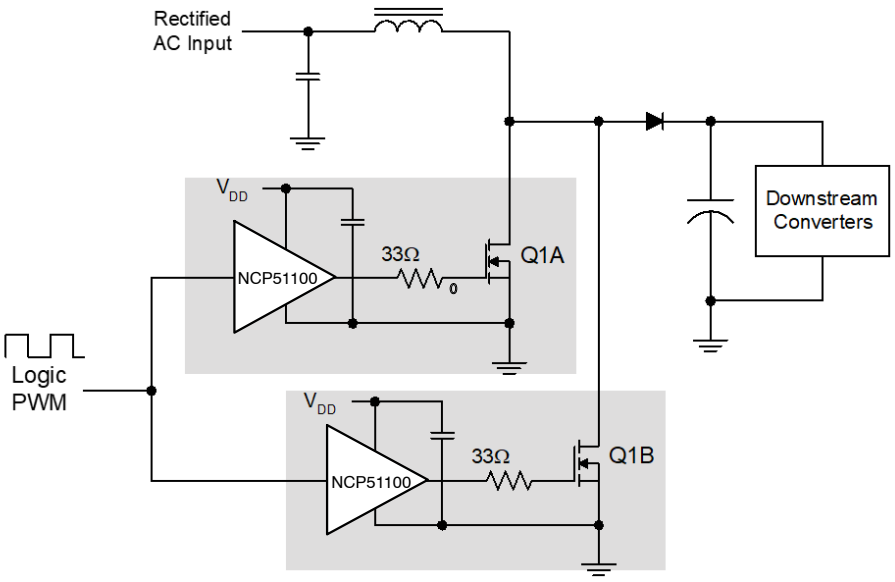


Figure 28. PFC Boost Circuit Utilizing Distributed Drivers for Parallel Power Switches Q1A and Q1B

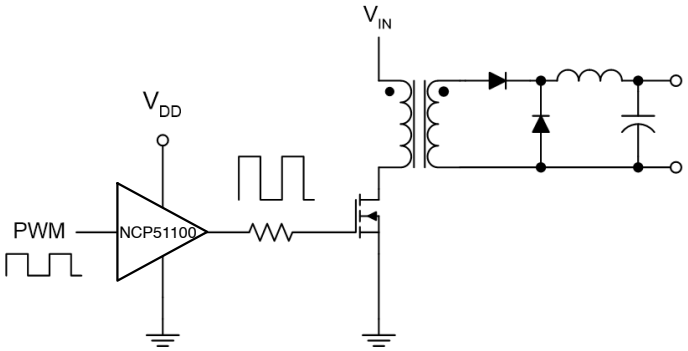


Figure 29. Driver for Forward Converter Low−Side Switch

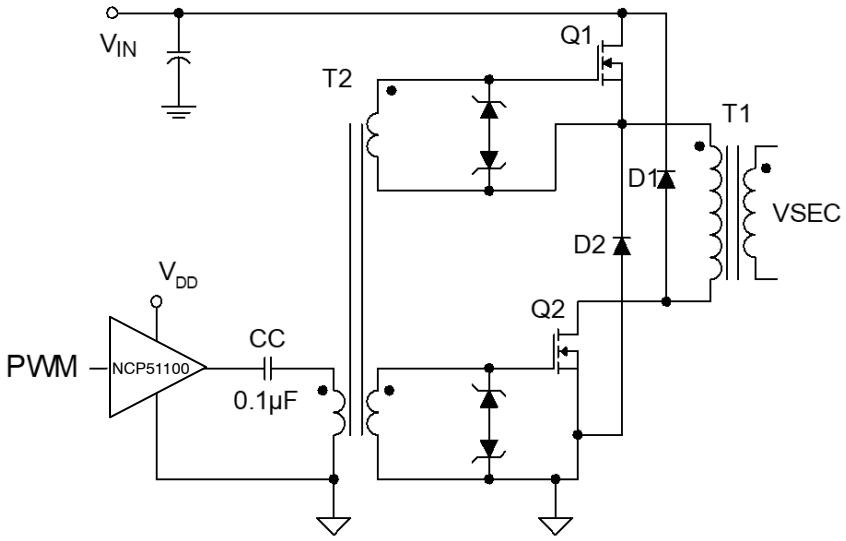
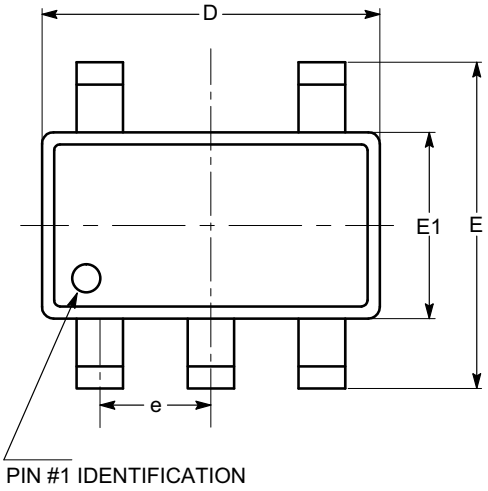


Figure 30. Driver for Two−Transistor, Forward−Converter Gate Transformer

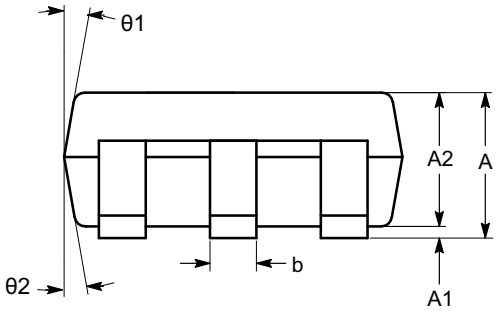
PACKAGE DIMENSIONS

SOT−23, 5 Lead
CASE 527AH−01
ISSUE O

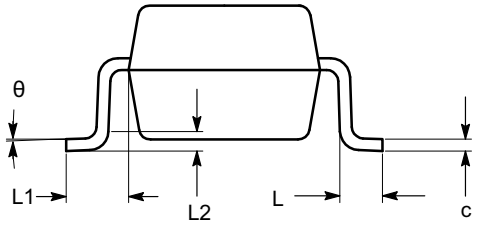


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	0.90		1.45
A1	0.00		0.15
A2	0.90	1.15	1.30
b	0.30		0.50
c	0.08		0.22
D		2.90 BSC	
E		2.80 BSC	
E1		1.60 BSC	
e		0.95 BSC	
L	0.30	0.45	0.60
L1		0.60 REF	
L2		0.25 REF	
θ	0°	4°	8°
θ1	5°	10°	15°
θ2	5°	10°	15°



SIDE VIEW



END VIEW

Notes:
(1) All dimensions in millimeters. Angles in degrees.
(2) Complies with JEDEC standard MO-178.

ALL DIMENSIONS ARE IN

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