NCP1218

PWM Controller with Adjustable Skip Level and External Latch Input

The NCP1218 represents a new, pin to pin compatible, generation of the successful 7−pin current mode NCP12XX product series. The controller allows for excellent standby power consumption by use of its adjustable skip mode and integrated high voltage startup FET. Internal frequency jittering, ramp compensation, timer−based fault detection and a latch input make this controller an excellent candidate for converters where ruggedness and component cost are the key constraints.

The Dynamic Self Supply (DSS) drastically simplifies the transformer design in avoiding the use of an auxiliary winding to supply the NCP1218. This feature is particularly useful in applications where the output voltage varies during operation (e.g. battery chargers). Due to its high voltage technology, the IC can be directly connected to the high voltage dc rail.

Features

- Fixed−Frequency 65 kHz Current−Mode Operation with Ramp Compensation
- Dynamic Self Supply Eliminates the Need for an Auxiliary Winding
- Timer−Based Fault Protection for Improved Overload Detection
- Cycle Skip Reduces Input Power in Standby Mode
- Latched Overload Protection
- Internal High Voltage Startup Circuit
- Accurate Current Limit Detector (±5%)
- Adjustable Skip Level
- Latch Input for Easy Implementation of Overvoltage and Overtemperature Protection
- Frequency Modulation for Softened EMI Signature
- 500 mA/800 mA Peak Source/Sink Current Drive Capability
- Pin to Pin Compatible with the Existing NCP12XX Series
- These Devices are Pb−Free and Halogen Free/BFR Free*

Typical Applications

- AC−DC Adapters for Notebooks, LCD Monitors
- Offline Battery Chargers
- Consumer Electronic Appliances STB, DVD, DVDR

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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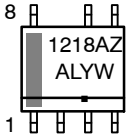
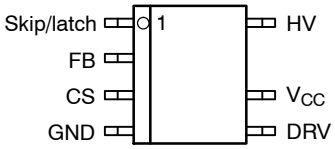
SOIC−7
D SUFFIX
CASE 751U

MARKING DIAGRAM



1218A = Specific Device Code
Z = Frequency (6 = 65 kHz)
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 19 of this data sheet.

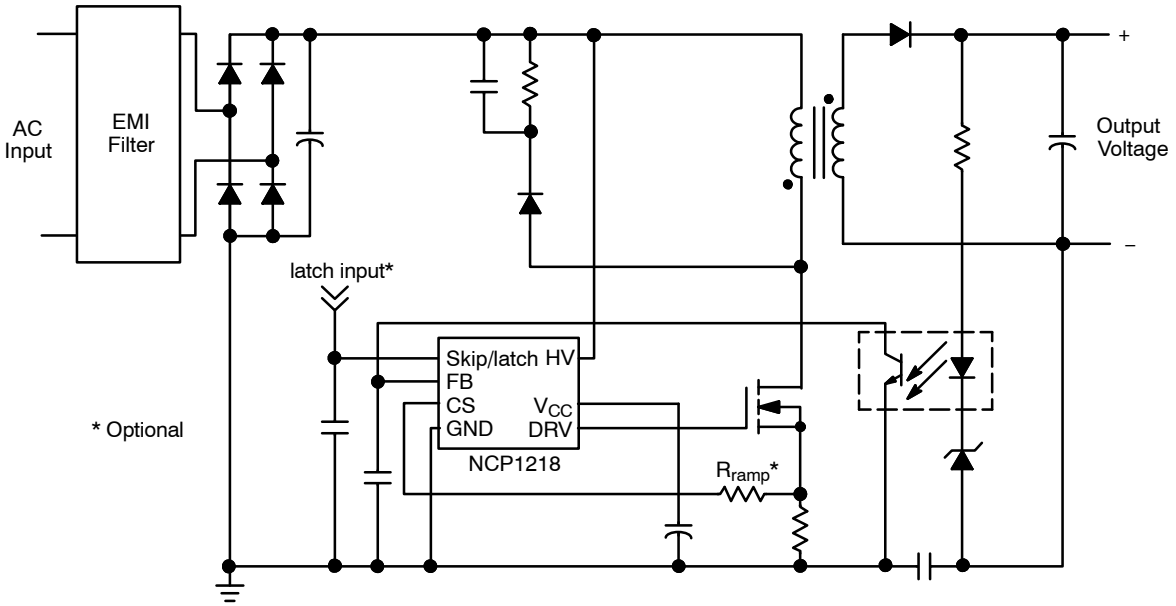


Figure 1. Typical Application Circuit

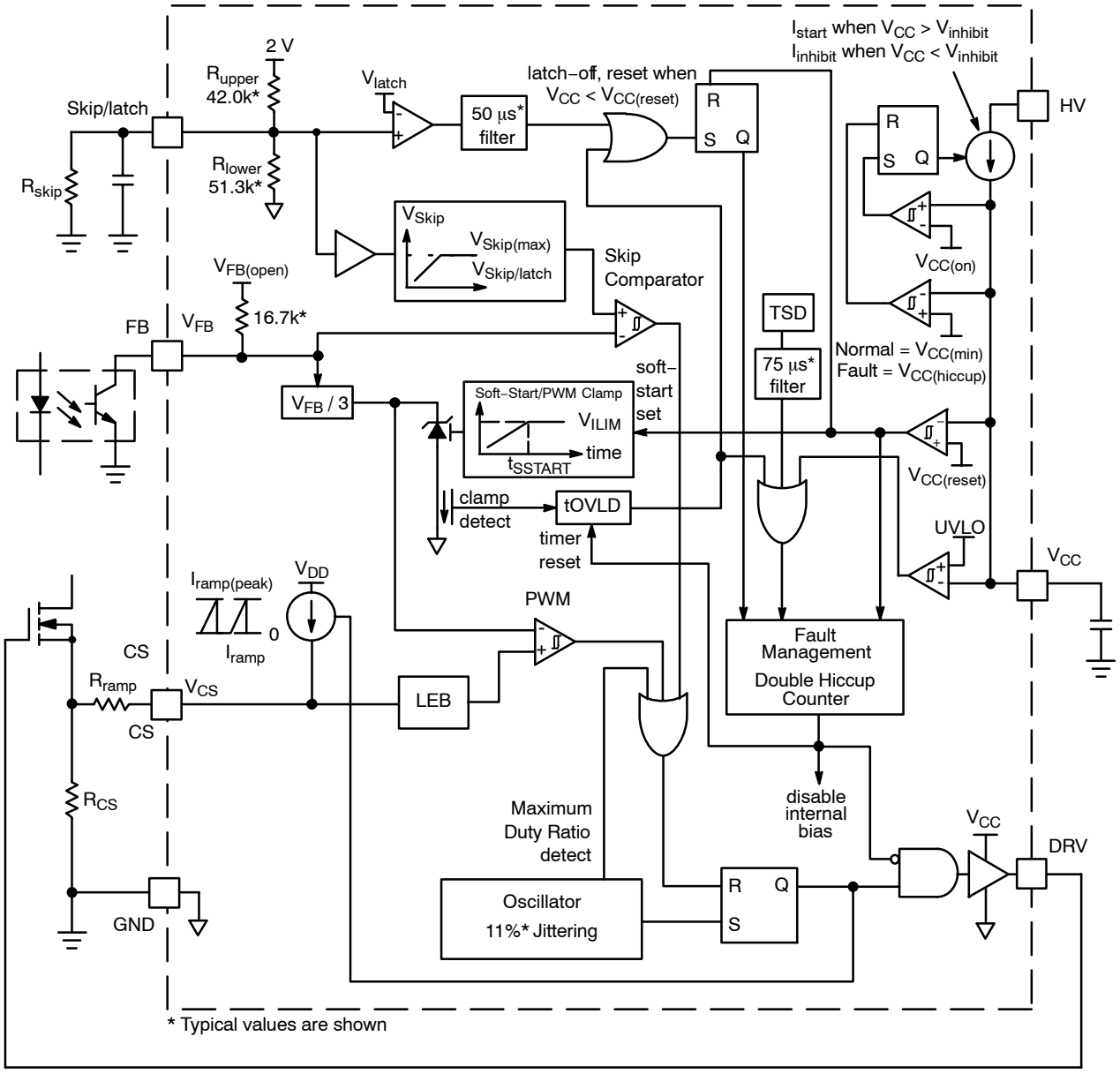


Figure 2. Functional Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin	Name	Description
1	Skip/Latch	This pin provides a latch input to permanently disable the device under a fault condition. It also allows the user to adjust the skip threshold. A resistor between this pin and GND provides noise immunity to the latch input and sets the skip threshold. The voltage on this pin is determined by the combination of the internal voltage divider and the external resistor to ground. The default skip threshold is 1.1 V (typical) if no external resistor is used. An internal clamp prevents the skip level from increasing above 1.3 V if the Skip/latch pin is pulled high to latch the controller.
2	FB	The voltage on this pin is proportional to the output load on the converter. An internal resistor divider sets the voltage on this pin above the regulation threshold (3 V) and an external optocoupler pulls the pin low to achieve regulation. While the FB voltage is above its regulation threshold, the overload timer is enabled. If the overload timer expires, the controller is latched. The converter enters skip mode if the FB voltage is below the skip threshold.
3	CS	A voltage ramp proportional to the primary current is applied to this pin. The maximum current is reached once the ramp voltage reaches 1 V (typical). A 100 μA (typical) current source provides ramp compensation. The amount of ramp compensation is adjusted with a series resistor between the CS pin and the current sense resistor.
4	GND	Analog ground.
5	DRV	Main output of the PWM Controller. DRV has a source resistance of 12.6 Ω (typical) and a sink resistance of 6.7 Ω (typical).
6	V_{CC}	Positive input supply. This pin connects to an external capacitor for energy storage. An internal current source supplies current from the HV pin to this pin. Once the V_{CC} voltage reaches $V_{CC(on)}$ (12.7 V typical), the current source turns off and the DRV is enabled. The current source turns on once V_{CC} falls to $V_{CC(min)}$ (9.9 V typical). This mode of operation is known as dynamic self supply (DSS). If the bias current consumption exceeds the startup current, and V_{CC} drops 0.5 V (typical) below $V_{CC(min)}$ the converter turns off and enters a double hiccup mode. If the V_{CC} voltage is below 0.67 V (typical) the startup current is reduced to 200 μA (typical), reducing power dissipation.
8	HV	This is the input of the high voltage startup regulator and connects directly to the bulk voltage. A controlled current source supplies current from this pin to the V_{CC} capacitor, eliminating the need for an external startup resistor. The charge current is 12.8 mA (typical).

Table 2. MAXIMUM RATINGS (Notes 1 – 4)

Rating	Symbol	Value	Unit
HV Voltage	V_{HV}	–0.3 to 500	V
HV Current	I_{HV}	100	mA
Supply Voltage	V_{CC}	–0.3 to 20	V
Supply Current	I_{CC}	100	mA
Skip/latch Voltage	$V_{Skip/latch}$	–0.3 to 9.5	V
Skip/latch Current	$I_{Skip/latch}$	100	mA
FB Voltage	V_{FB}	–0.3 to 5.0	V
FB Current	I_{FB}	100	mA
CS Voltage	V_{CS}	–0.3 to 5.0	V
CS Current	I_{CS}	100	mA
DRV Voltage	V_{DRV}	–0.3 to 20	V
DRV Current	I_{DRV}	–500 to 800	mA
Operating Junction Temperature	T_J	–40 to 150	°C
Storage Temperature Range	T_{stg}	–60 to 150	°C
Power Dissipation (T_A = 25°C, 2.0 Oz Cu, 1.0 Sq Inch Printed Circuit Copper Clad) D Suffix, Plastic Package Case 751U (SOIC–7) (Note 4)	P_D	0.92	W
Thermal Resistance, Junction to Ambient (2.0 Oz Cu Printed Circuit Copper Clad)			°C/W
D Suffix, Plastic Package Case 751U (SOIC–7)			
Junction to Air, Low conductivity PCB (Note 3)	$R_{\theta JA}$	177	
Junction to Lead, Low conductivity PCB (Note 3)	$R_{\theta JL}$	75	
Junction to Air, High conductivity PCB (Note 4)	$R_{\theta JA}$	136	
Junction to Lead, High conductivity PCB (Note 4)	$R_{\theta JL}$	69	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device series contains ESD protection and exceeds the following tests:
   Pins 1– 6: Human Body Model 3000 V per JEDEC JESD22–A114–F.
   Machine Model Method 300 V per JEDEC JESD22–A115–A.
   Pin 8 is the HV startup of the device and is rated to the maximum rating of the part, or 500 V.
2. This device contains Latch–Up protection and exceeds ±100 mA per JEDEC Standard JESD78.
3. As mounted on a 40x40x1.5 mm FR4 substrate with a single layer of 80 mm^2 of 2 oz copper traces and heat spreading area. As specified for a JEDEC 51 low conductivity test PCB. Test conditions were under natural convection or zero air flow.
4. As mounted on a 40x40x1.5 mm FR4 substrate with a single layer of 650 mm^2 of 2 oz copper traces and heat spreading area. As specified for a JEDEC 51 high conductivity test PCB. Test conditions were under natural convection or zero air flow.

Table 3. ELECTRICAL CHARACTERISTICS (V_{HV} = 60 V, V_{CC} = 11.3 V, V_{FB} = 2 V, $V_{Skip/latch}$ = 0 V, V_{CS} = 0 V, V_{DRV} = open, C_{CC} = 0.1 μF, for typical values T_J = 25°C, for min/max values, T_J is −40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
STARTUP AND SUPPLY CIRCUITS						
Supply Voltage						V
Startup Threshold	V_{CC} Increasing	$V_{CC(on)}$	11.2	12.7	13.8	
Minimum Operating Voltage	V_{CC} Decreasing	$V_{CC(MIN)}$	9.0	9.9	10.8	
Undervoltage Lockout	V_{CC} Decreasing	UVLO	8.4	9.4	10.6	
Double Hiccup Threshold	V_{CC} Decreasing	$V_{CC(hiccup)}$	4.9	5.7	6.3	
Logic Reset Voltage	V_{CC} Decreasing	$V_{CC(reset)}$	–	4.0	–	
UVLO Filter Delay		$t_{UVLO(delay)}$	–	50	–	μs
Inhibit Threshold Voltage	$I_{inhibit}$ = 500 μA	$V_{inhibit}$	0.35	0.67	0.90	V
Inhibit Bias Current	V_{CC} = 0 V	$I_{inhibit}$	100	200	350	μA
Minimum Startup Voltage	I_{start} = 0.5 mA, V_{CC} = $V_{CC(on)}$ − 0.5 V	$V_{start(min)}$	–	20	28	V
Startup Current	V_{CC} = $V_{CC\ (on)}$ − 0.5 V	I_{start}	5.5	12.8	18.5	mA
Startup Circuit Reverse Current	V_{HV} = 0 V, V_{CC} = 14 V	$I_{HV(reverse)}$	–	–	100	μA
Off−State Leakage Current	V_{HV} = 500 V, V_{CC} = 14 V	$I_{HV(off)}$	–	12	50	μA
Breakdown Voltage (Note 5)	I_{HV} = 50 μA	$V_{BR(DS)}$	500	–	–	V
Supply Current						mA
Device Disabled/Fault	$V_{Skip/latch}$ = 5.2 V, V_{FB} = open	I_{CC1}	–	0.6	0.8	
Device Enabled/No Switching	$V_{Skip/latch}$ = open, V_{FB} = 0 V	I_{CC2}	–	1.4	2.1	
Device Switching	$V_{Skip/latch}$ = open, C_{DRV} = 1000 pF	I_{CC3}	–	2.2	2.7	
CURRENT SENSE						
Current Sense Voltage Threshold	Apply voltage step on CS pin	V_{ILIM}	0.95	1.0	1.05	V
Leading Edge Blanking Duration		t_{LEB}	100	184	330	ns
Propagation Delay	V_{CS} > V_{ILIM} to 50% DRV turns off, C_{DRV} = 1000 pF	t_{delay}	–	59	150	ns
Ramp Compensation Peak Current		$I_{ramp(peak)}$	–	100	–	μA
Ramp Compensation Valley Current		$I_{ramp(valley)}$	–	0	–	μA
FEEDBACK INPUT						
Open Feedback Voltage		$V_{FB(open)}$	3.2	3.6	3.9	V
Internal Pull−up Resistance		R_{FB}	–	16.7	–	kΩ
Feedback Pull−up Current	V_{FB} = 0 V	I_{FB}	141	280	392	μA
Feedback to Current Set Point Ratio		I_{ratio}	–	3.0	–	
SOFT−START						
Soft−Start Period	Measured at 0.9 V_{ILIM}	t_{SSTART}	–	4.8	–	ms
OSCILLATOR						
Oscillator Frequency	T_J = 25°C	f_{OSC}	61.75	65	68.25	kHz
	T_J = −40°C to 85°C		58	–	71	
	T_J = −40°C to 125°C		55	–	71	
Frequency Modulation in Percentage of f_{OSC}			–	±11	–	%
Frequency Modulation Period			–	11.5	–	ms
Maximum Duty Ratio		D	75	80	85	%

5. Guaranteed by the $I_{HV(off)}$ test.

Table 3. ELECTRICAL CHARACTERISTICS (V_{HV} = 60 V, V_{CC} = 11.3 V, V_{FB} = 2 V, $V_{Skip/latch}$ = 0 V, V_{CS} = 0 V, V_{DRV} = open, C_{CC} = 0.1 μF, for typical values T_J = 25°C, for min/max values, T_J is −40°C to 125°C, unless otherwise noted)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
GATE DRIVE						
Drive Resistance DRV Sink DRV Source	 V_{FB} = 0 V, V_{DRV} = 1 V V_{DRV} = V_{CC} − 1 V	 R_{SNK} R_{SRC}	 2.0 6.0	 6.7 12.6	 13 25	Ω
Rise Time (10% to 90%)	C_{DRV} = 1000 pF (10% to 90%)	t_r	–	30	–	ns
Fall Time (90% to 10%)	C_{DRV} = 1000 pF (90% to 10%)	t_f	–	20	–	ns
LATCH INPUT						
Latch Voltage Threshold		V_{latch}	3.4	3.9	4.6	V
Latch Filter Delay	$V_{Skip/latch}$ = 5.2 V, apply voltage step on Skip/latch pin	$t_{latch(delay)}$	–	50	–	μs
CYCLE SKIP						
Default Skip Threshold	V_{FB} increasing, $V_{Skip/latch}$ = Open	V_{skip}	0.9	1.1	1.3	V
Skip Clamp Voltage	V_{FB} increasing, $V_{Skip/latch}$ = 2.0 V	$V_{skip(MAX)}$	1.1	1.3	1.5	V
Skip Comparator Hysteresis	V_{FB} decreasing, $V_{Skip/latch}$ = 0.5 V	$V_{skip(HYS1)}$	–	75	–	mV
Skip Clamp Comparator Hysteresis	V_{FB} decreasing, $V_{Skip/latch}$ = 2.0 V	$V_{skip(HYS2)}$	–	75	–	mV
Skip Current	$V_{Skip/latch}$ = 0 V	I_{skip}	30	47	56	μA
FAULTS PROTECTION						
Thermal Shutdown (Note 6)	Temperature Increasing	T_{SHDN}	–	155	–	°C
Thermal Shutdown Hysteresis	Temperature Decreasing	$T_{SHDN(HYS)}$	–	40	–	°C
Thermal Shutdown Delay		$T_{SHDN(delay)}$	–	75	–	μs
Overload Timer	Apply voltage step on FB pin	t_{OVLD}	–	350	–	ms

6. Guaranteed by design only.

TYPICAL CHARACTERISTICS

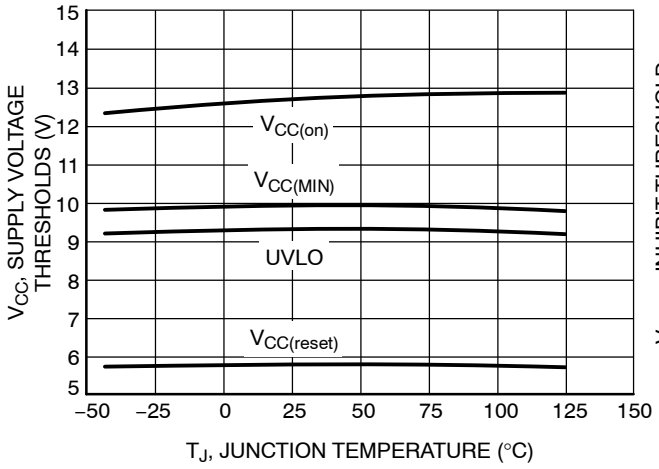


Figure 3. Supply Voltage Thresholds vs. Junction Temperature

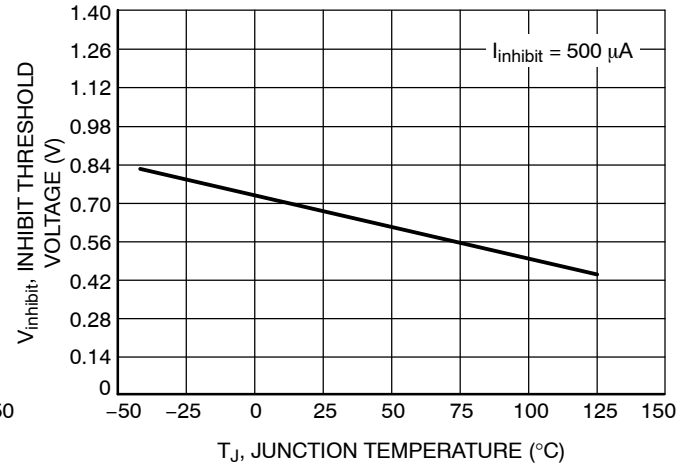


Figure 4. Inhibit Threshold Voltage vs. Junction Temperature

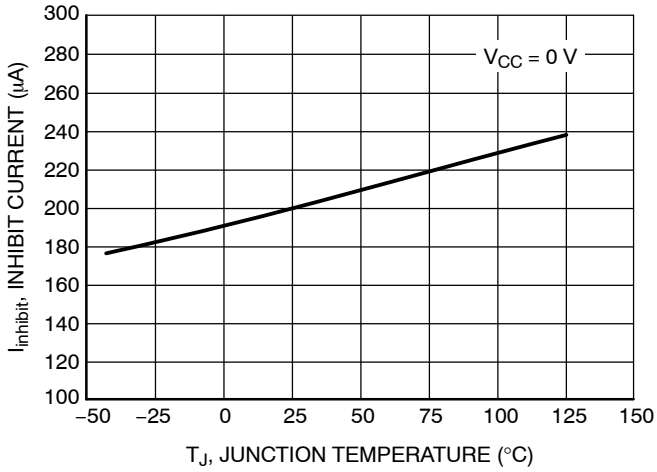


Figure 5. Inhibit Current vs. Junction Temperature

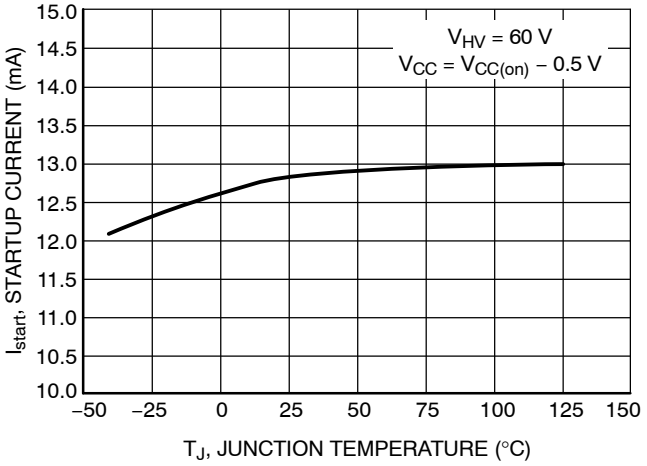


Figure 6. Startup Current vs. Junction Temperature

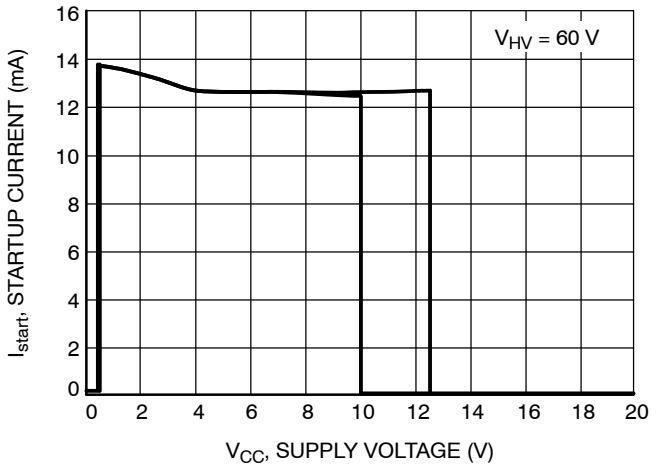


Figure 7. Startup Current vs. Supply Voltage

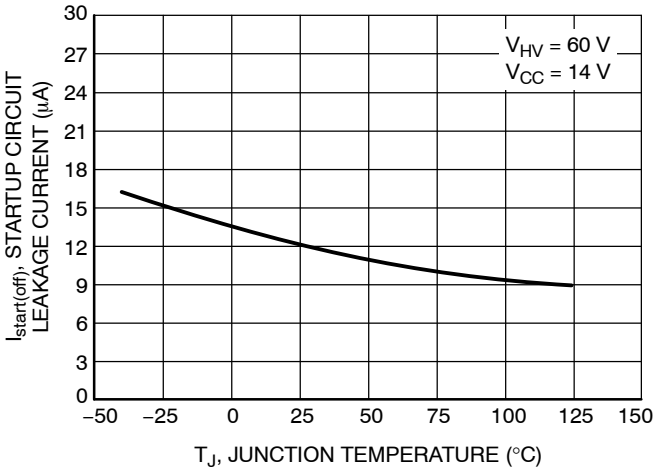


Figure 8. Startup Circuit Leakage Current vs. Junction Temperature

TYPICAL CHARACTERISTICS

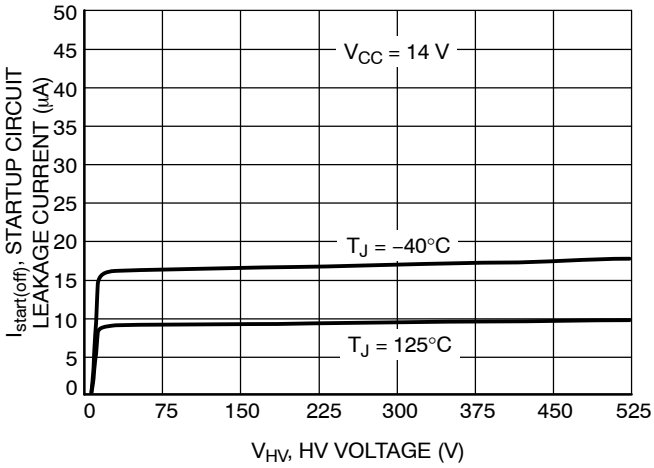


Figure 9. Startup Circuit Leakage Current vs. HV Voltage

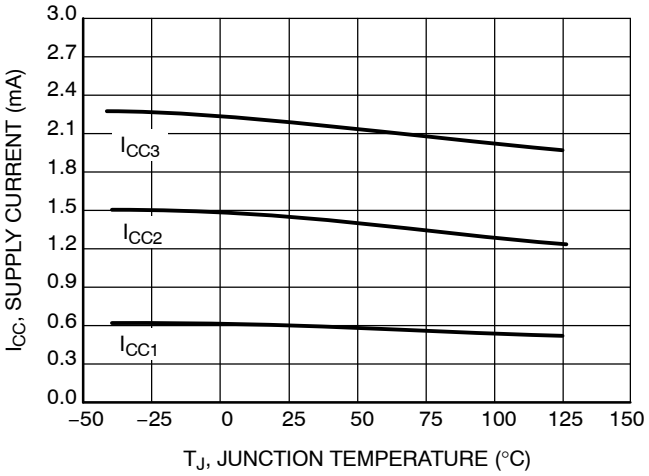


Figure 10. Supply Current vs. Junction Temperature

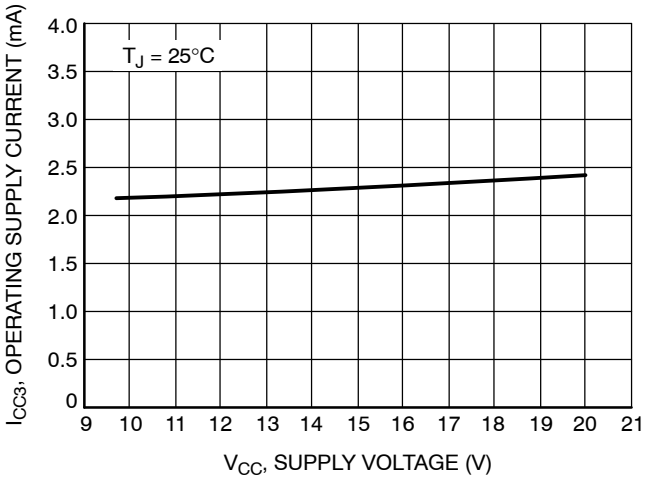


Figure 11. Operating Supply Current vs. Supply Voltage

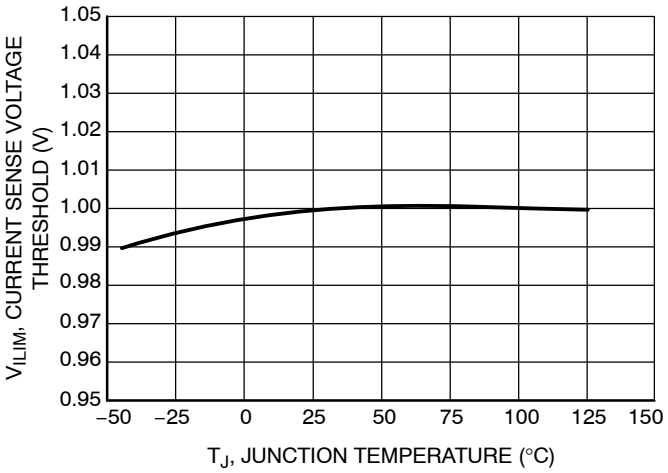


Figure 12. Current Sense Voltage Threshold vs. Junction Temperature

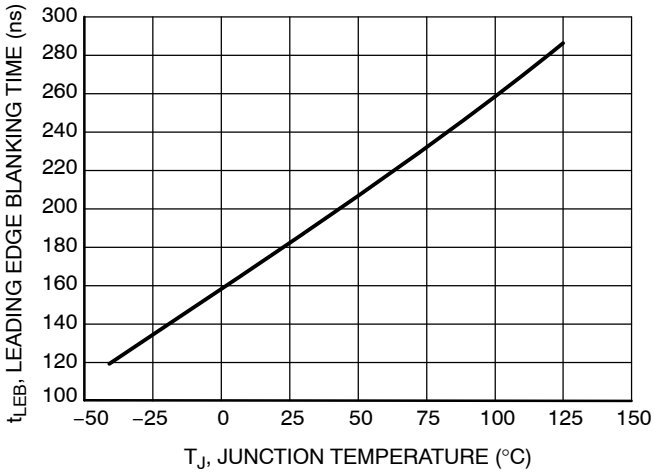


Figure 13. Leading Edge Blanking Time vs. Junction Temperature

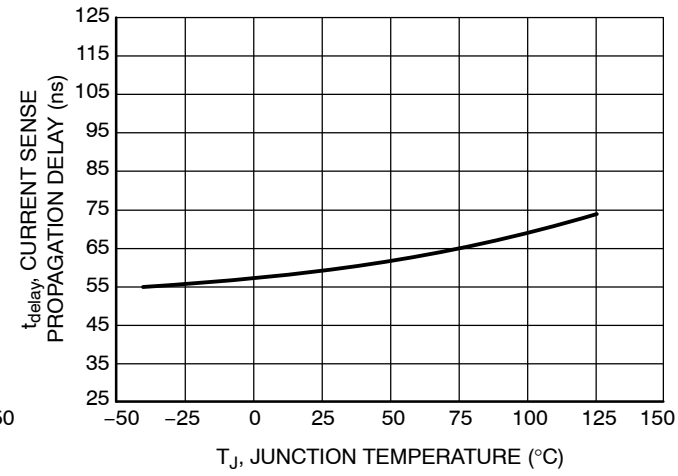


Figure 14. Current Sense Propagation Delay vs. Junction Temperature

TYPICAL CHARACTERISTICS

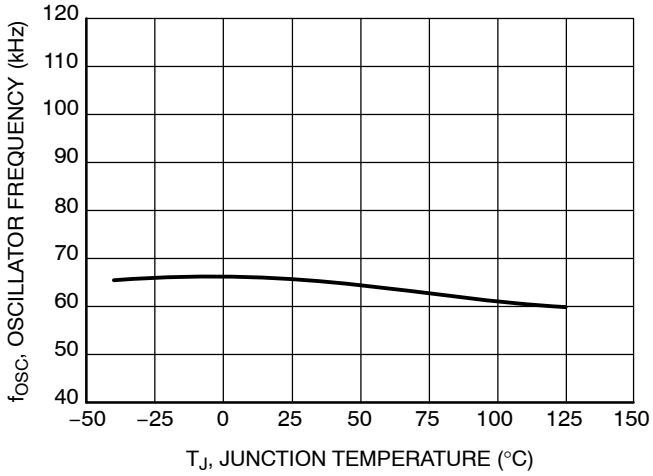


Figure 15. Oscillator Frequency vs. Junction Temperature

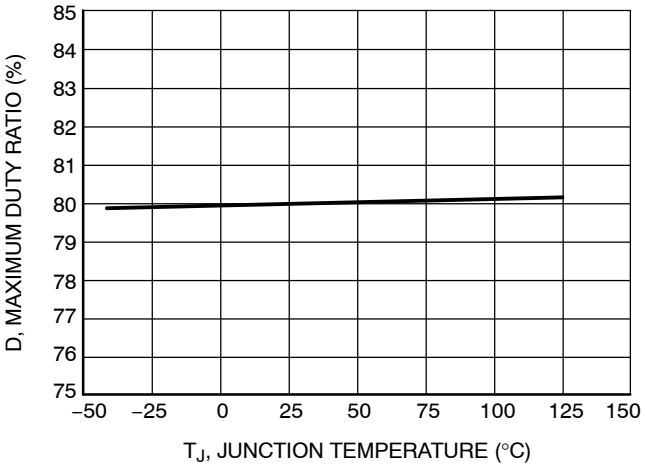


Figure 16. Maximum Duty Ratio vs. Junction Temperature

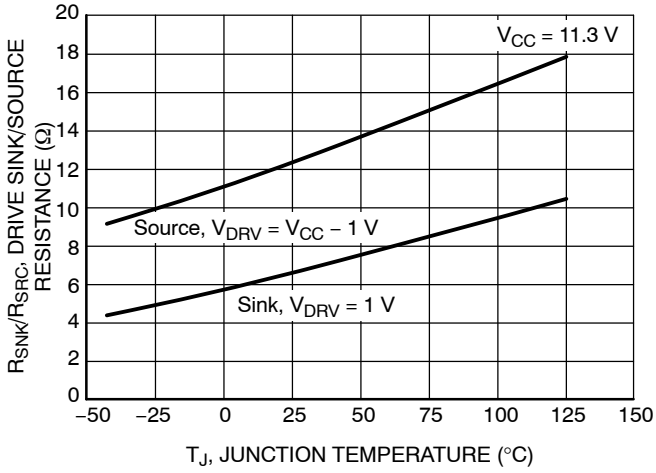


Figure 17. Drive Sink and Source Resistances vs. Junction Temperature

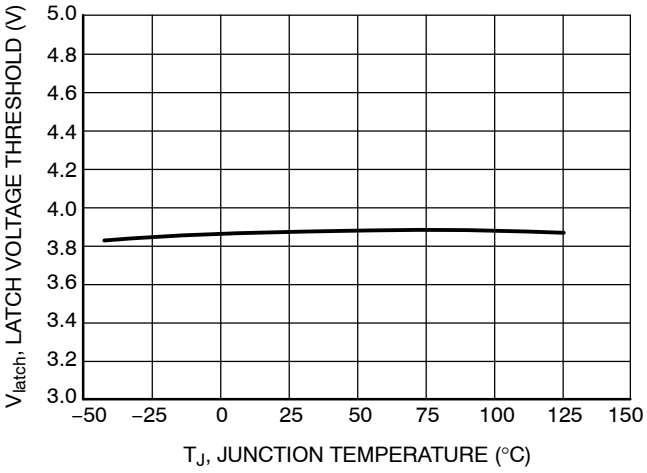


Figure 18. Latch Voltage Threshold vs. Junction Temperature

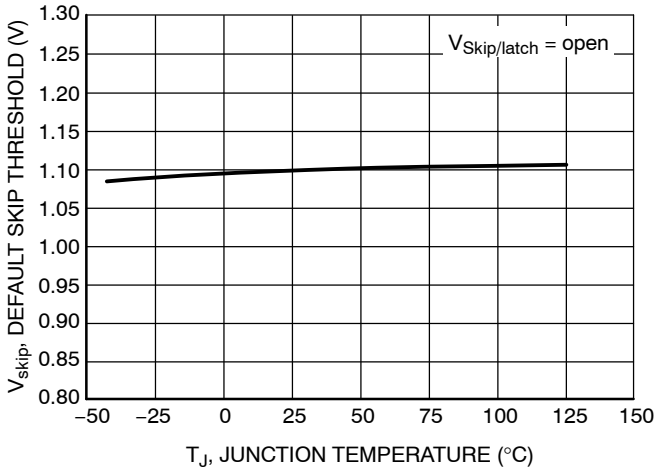


Figure 19. Default Skip Threshold vs. Junction Temperature

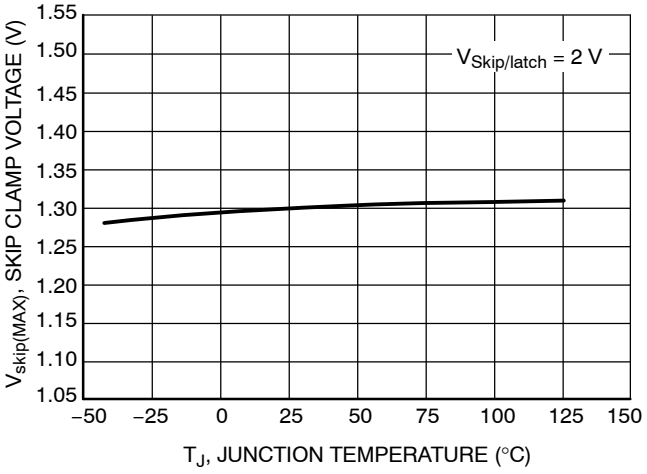


Figure 20. Skip Clamp Voltage vs. Junction Temperature

TYPICAL CHARACTERISTICS

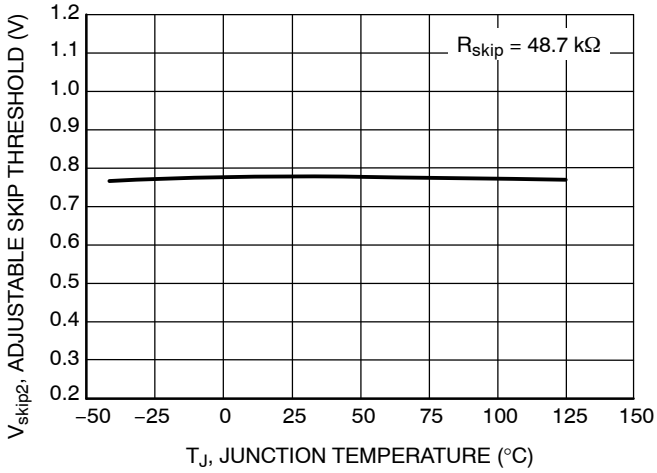


Figure 21. Adjustable Skip Threshold vs. Junction Temperature

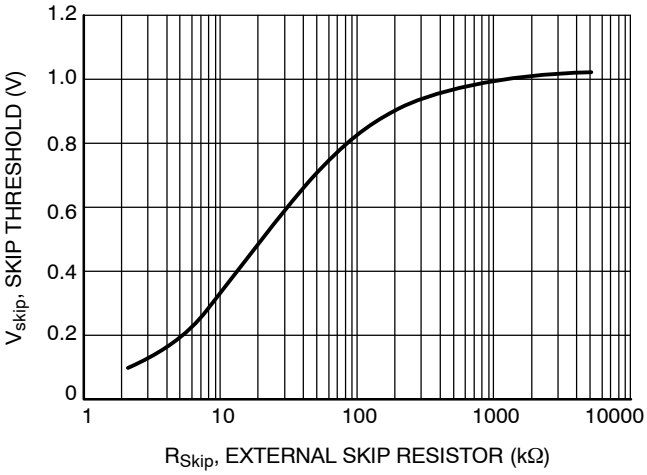


Figure 22. Skip Threshold vs. Skip Resistor

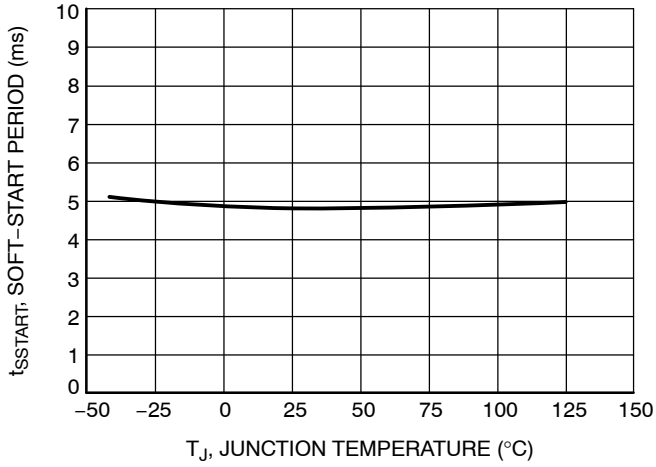


Figure 23. Soft−Start Period vs. Junction Temperature

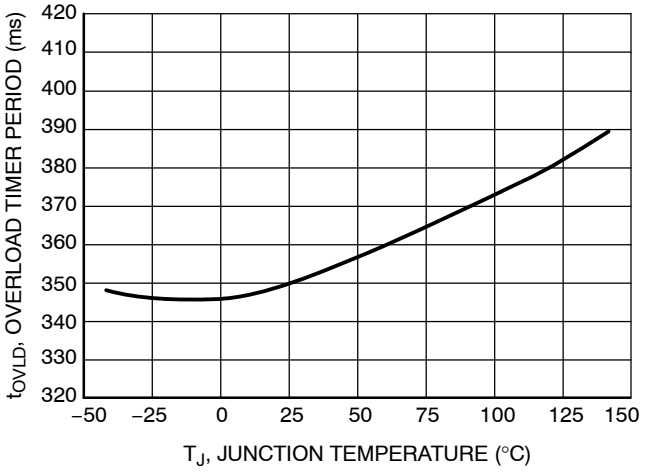


Figure 24. Overload Timer Period vs. Junction Temperature

DETAILED OPERATING DESCRIPTION

The NCP1218 is part of a product family of current mode controllers designed for ac−dc applications requiring low standby power. The controller operates in skip or burst mode at light load. Its high integration reduces component count resulting in a more compact and lower cost power supply.

The internal high voltage startup circuit with dynamic self supply (DSS) allows the controller to operate without an auxiliary supply, simplifying the transformer design. This feature is particularly useful in applications where the output voltage varies during operation (e.g. printer adapters).

Other features found in the NCP1218 are frequency jittering, adjustable ramp compensation, timer based fault detection and a dedicated latch input.

High Voltage Startup Circuit

The NCP1218 internal high voltage startup circuit eliminates the need for external startup components and provides a faster startup time compared to an external startup resistor. The startup circuit consists of a constant current source that supplies current from the HV pin to the supply capacitor on the V_{CC} pin (C_{CC}). The HV pin is rated at 500 V allowing direct connection to the bulk capacitor. The start−up current (I_{start}) is typically 12.8 mA.

The startup current source is disabled once the V_{CC} voltage reaches $V_{CC(on)}$, typically 12.7 V. The controller is then biased by the V_{CC} capacitor. The current source is enabled once the V_{CC} voltage decays to its minimum operating threshold ($V_{CC(MIN)}$) typically 9.9 V. If the supply current consumption exceeds the startup current, V_{CC} will decay below $V_{CC(MIN)}$. The NCP1218 has an undervoltage lockout (UVLO) to prevent operation at low V_{CC} levels. The UVLO threshold is typically 9.4 V. The DRV signal is immediately disabled upon reaching UVLO. It is re−enabled if V_{CC} increases above UVLO before the 50 μs (typical) timer expires. Otherwise, the controller enters double hiccup mode.

The controller enters a double hiccup mode if a thermal shutdown or UVLO fault is detected. A double hiccup fault disables the DRV signal, sets the controller in a low current mode and allows V_{CC} to discharge to $V_{CC(hiccup)}$, typically 5.7 V. This cycle is repeated twice to minimize power dissipation in external components during a fault event. Figures 25 and 26 show double hiccup mode operation with a fault occurring while the startup circuit is disabled and enabled, respectively. A soft−start sequence is initiated the second time V_{CC} reaches $V_{CC(on)}$. If the fault is present or the controller is latched upon reaching $V_{CC(on)}$, the controller stays in hiccup mode. During this mode, V_{CC} never drops below 4 V, the controller logic reset level. This prevents latched faults from being cleared unless power to the controller is completely removed (i.e. unplugging the supply from the AC line). The NCP1218 latches off after the overload timer expires if an overload fault is detected. In this case, V_{CC} cycles between $V_{CC(on)}$ and $V_{CC(hiccup)}$ without enabling the DRV signal until the power to the controller is reset.

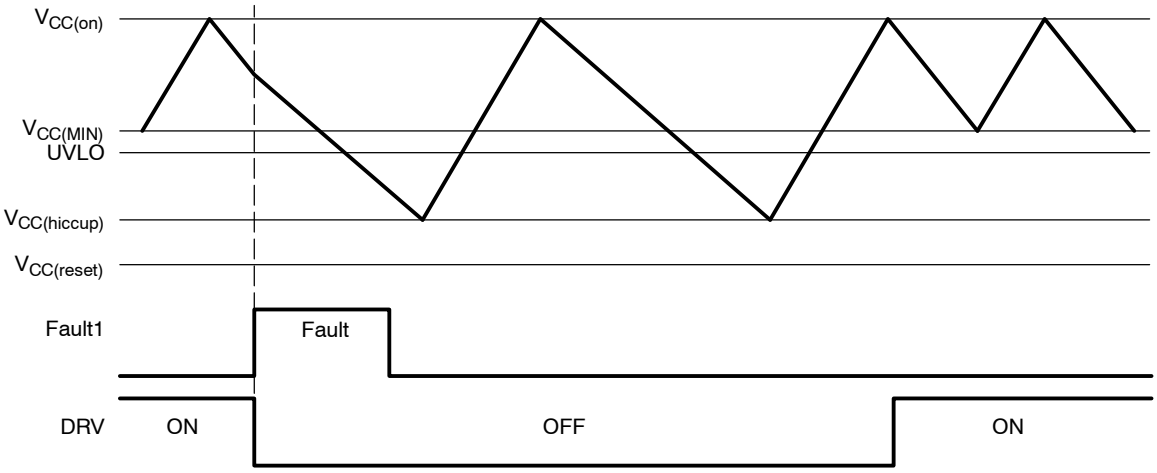


Figure 25. V_{CC} Double Hiccup Operation with a Fault Occurring While the Startup Circuit is Disabled.

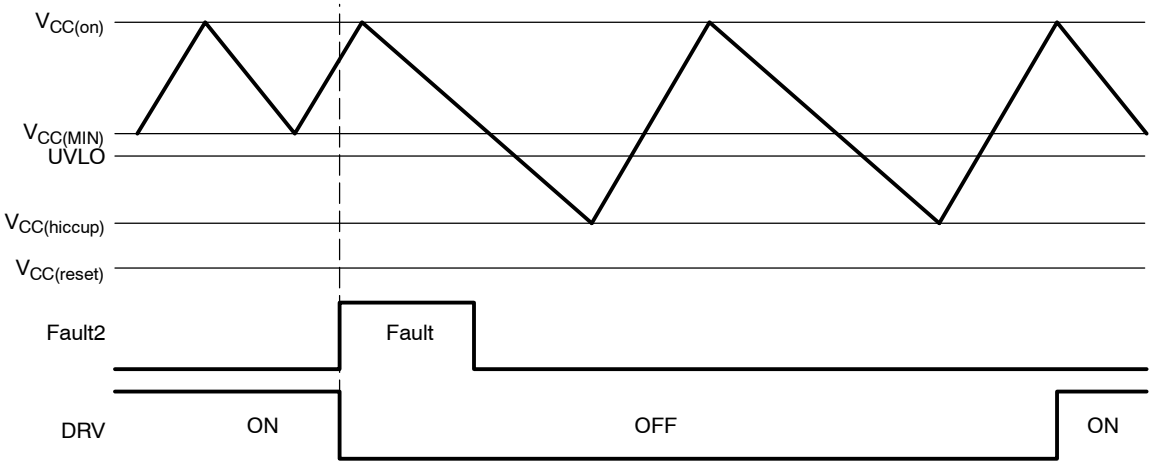


Figure 26. V_{CC} Double Hiccup Operation with a Fault Occurring While the Startup Circuit is Enabled

An internal supervisory circuit monitors the V_{CC} voltage to prevent the controller from dissipating excessive power if the V_{CC} pin is accidentally grounded. A lower level current source ($I_{inhibit}$) charges C_{CC} from 0 V to $V_{inhibit}$, typically 0.67 V. Once V_{CC} exceeds $V_{inhibit}$, the startup current source is enabled. This behavior is illustrated in Figure 27. This slightly increases the total time to charge V_{CC}, but it is generally not noticeable.

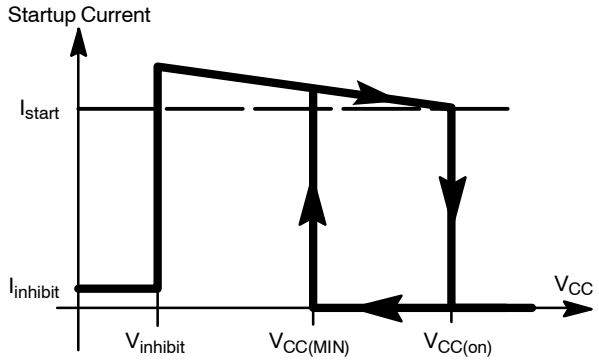


Figure 27. Startup Current at Various V_{CC} Levels

The start−up circuit is rated at a maximum voltage of 500 V. If the device operates in the DSS mode, power dissipation should be controlled to avoid exceeding the maximum power dissipation of the controller. If dissipation on the controller is excessive, a resistor can be placed in series with the HV pin. This will reduce power dissipation on the controller and transfer it to the series resistor.

Standby mode losses and normal mode power dissipation can be reduced by biasing the controller with an auxiliary winding. The auxiliary winding needs to maintain V_{CC} above $V_{CC(MIN)}$ once the startup circuit is disabled.

The power dissipation of the controller when operated in DSS mode, P_{DSS}, can be calculated using equation 1, where I_{CC3} is the operating current of the NCP1218 during switching and V_{HV} is the voltage at the HV pin. The HV pin is most often connected to the bulk capacitor.

$$P_{DSS} = I_{CC3} \cdot (V_{HV} - V_{CC}) \qquad \text{(eq. 1)}$$

In comparison, the power dissipation when the startup circuit is disabled and V_{CC} is being supplied by the auxiliary winding is a function of the V_{CC} voltage. This is shown in Equation 2.

$$P_{AUX} = I_{CC3} \cdot V_{CC} \qquad \text{(eq. 2)}$$

It is recommended that an external filter capacitor be placed as close as possible to the V_{CC} pin to improve the noise immunity.

Soft−Start Operation

Figures 28 and 29 show how the soft−start feature is included in the pulse−width modulation (PWM) comparator. When the NCP1218 starts up, a soft−start voltage V_{SSTART} begins at 0 V. V_{SSTART} increases gradually from 0 V to 1.0 V in 4.8 ms and stays at 1.0 V afterward. V_{SSTART} is compared with the divided by 3 feedback pin voltage ($V_{FB}/3$). The lesser of V_{SSTART} and ($V_{FB}/3$) becomes the modulation voltage, V_{PWM}, in the PWM duty ratio generation. Initially, ($V_{FB}/3$) is above 1.0 V because the FB pin is brought to $V_{FB(open)}$, typically 3.6 V, by the internal pullup resistor. As a result, V_{PWM} is limited by the soft−start function and slowly ramps up the duty ratio (and therefore the primary current) for the initial 4.8 ms. This provides a greatly reduced stress on the power devices during startup.

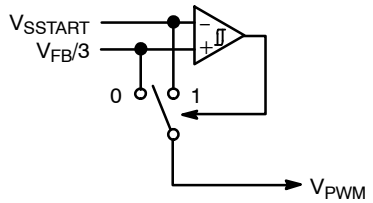


Figure 28. V_{PWM} is the lesser of V_{SSTART} and ($V_{FB}/3$)

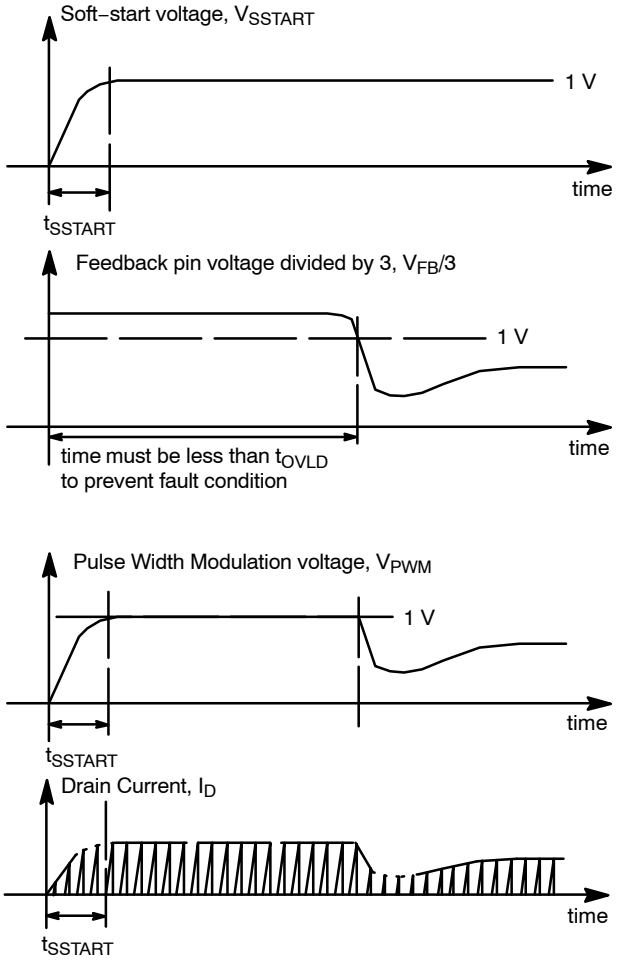


Figure 29. Soft−Start (Time = 0 at V_{CC} = $V_{CC(on)}$)

Current−Mode Pulse Width Modulation

The NCP1218 is a current−mode, fixed frequency pulse width modulation controller with ramp compensation. The PWM block of the NCP1218 is shown in Figure 30. The DRV signal is enabled by a clock pulse. At this time, current begins to flow in the power MOSFET and the sense resistor. A corresponding voltage is generated on the CS pin of the device, ranging from very low to as high as the maximum modulation voltage, V_{PWM} (maximum of 1 V). This sets the primary current on a cycle−by−cycle basis. Equation 3 gives the maximum drain current, $I_{D(MAX)}$, where R_{CS} is the current sense resistor value and V_{ILIM} is the current sense voltage threshold.

$$I_{D(MAX)} = \frac{V_{ILIM}}{R_{CS}} \qquad \text{(eq. 3)}$$

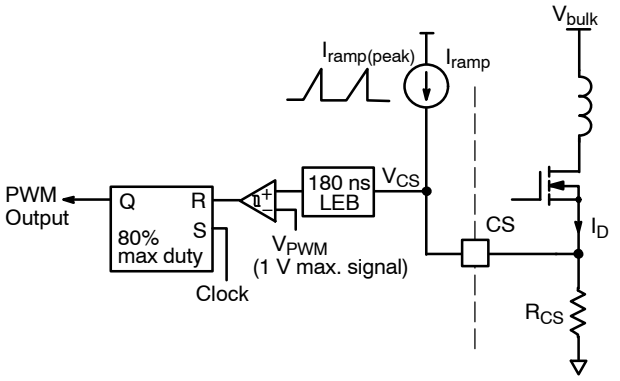


Figure 30. Current−Mode Implementation

Figure 31 shows the timing diagram for the current−mode pulse width modulation operation. An internal clock sets the output RS latch, pulling the DRV pin high. The latch is then reset when the voltage on the CS pin intersects the modulation voltage, V_{PWM}. This generates the duty ratio of the DRV pulse. The maximum duty ratio is internally limited to 80% (typical) by the output RS latch.

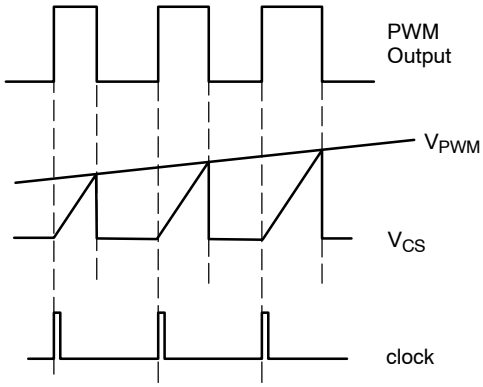


Figure 31. Current−Mode Timing Diagram

The V_{PWM} voltage is the scaled representation of the FB pin voltage. The scale factor, I_{ratio}, is 3. The FB pin voltage is provided by an external error amplifier, whose output is a function of the power supply output. An FB signal between V_{skip} and 3 V determines the duty ratio of the controller output. The FB voltage operates in a closed loop with the output voltage to regulate the power supply.

It is recommended that an external filter capacitor be placed as close to the FB pin as possible to improve the noise immunity.

Ramp Compensation

Ramp compensation is a known mean to cure subharmonic oscillations. These oscillations take place at half the switching frequency and occur only during continuous conduction mode (CCM) with a duty ratio greater than 50%. To lower the current loop gain, one usually injects 50 to 75% of the inductor current down slope. The NCP1218 generates an internal current ramp that is synchronized with the clock. This current ramp is then routed to the CS pin. Figures 32 and 33 depict how the ramp is generated and utilized. Ramp compensation is simply formed by placing a resistor, R_{ramp}, between the CS pin and the sense resistor.

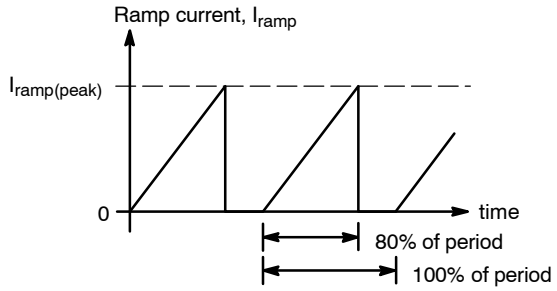


Figure 32. Internal Ramp Compensation Current Source

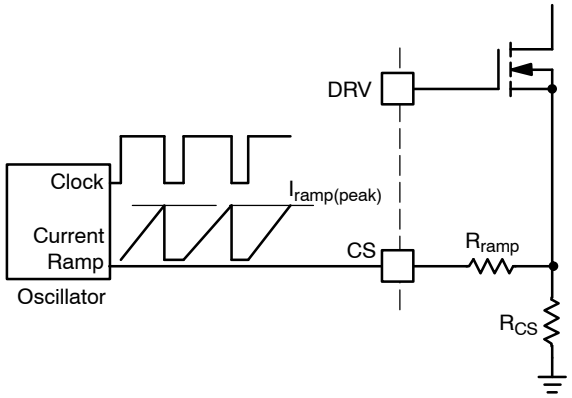


Figure 33. Inserting a Resistor in Series with the Current Sense Information Provides Ramp Compensation

In order to calculate the value of the ramp compensation resistor, R_{ramp}, the off time primary current slope, $S_{off,primary}$ must be calculated using Equation 4,

$$S_{off,primary} = \frac{(V_{out} + V_f) \cdot \left(\frac{N_P}{N_S}\right)}{L_P} \quad \text{(eq. 4)}$$

where V_{out} is the converter output voltage, V_f is the forward diode drop of the secondary diode, N_P/N_S is the primary to secondary turns ratio, and L_P is the primary inductance of the transformer. The value of R_{ramp} can be calculated using Equation 5,

$$R_{ramp} = \frac{\left(S_{off,primary} \times R_{CS}\right) \cdot \%slope}{\left(\frac{I_{ramp(peak)} \times f_{OSC}}{D}\right)} \quad \text{(eq. 5)}$$

where R_{CS} is the current sense resistor and %slope is the percentage of the current downslope to be used for ramp compensation.

The NCP1218 has a peak ramp compensation current of 100 μA. A frequency of 65 kHz with an 80% maximum duty ratio corresponds to an 8.1 μA/μs ramp. For a typical flyback design, let's assume that the primary inductance is 350 μH, the converter output is 19 V, the V_f of the output diode is 1 V and the N_P:N_S ratio is 10:1. The off time primary current slope is given by Equation 6.

$$\frac{(V_{out} + V_f)\left(\frac{N_P}{N_S}\right)}{L_P} = 571\,\frac{mA}{\mu s} \quad \text{(eq. 6)}$$

When projected over an R_{CS} of 0.1 Ω (for example), this becomes 57 mV/μs. If we select 50% of the downslope as the required amount of ramp compensation, then we shall inject 28.5 mV/μs. Therefore, R_{ramp} is simply equal to Equation 7.

$$R_{ramp} = \frac{28.5\,\frac{mV}{\mu s}}{8.1\,\frac{\mu A}{\mu s}} = 3.5\ k\Omega \quad \text{(eq. 7)}$$

Ramp compensation greater than 50% of the inductor down slope can be used if necessary; however, overcompensating will degrade the transient response of the system. The addition of ramp compensation also reduces the total available output power of the system.

Internal Oscillator

The internal oscillator of the NCP1218 provides the clock signal that sets the DRV signal high and limits the duty ratio to 80% (typical). The oscillator has a fixed frequency of 65 kHz. The NCP1218 employs frequency jittering to smooth the EMI signature of the system by spreading the energy of the main switching component across a range of frequencies. An internal low frequency oscillator continuously varies the switching frequency of the controller by ±11%. The period of modulation is 11.5 ms, typical. Figure 34 illustrates the oscillator frequency modulation.

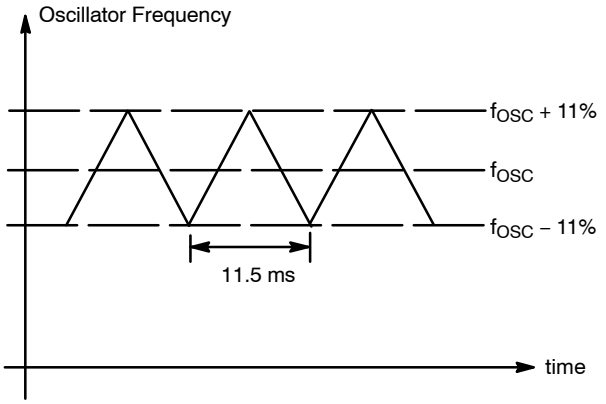


Figure 34. Oscillator Frequency Modulation

Gate Drive

The output drive of the NCP1218 is designed to directly drive the gate of an n−channel power MOSFET. The DRV pin is capable of sourcing 500 mA and sinking 800 mA of drive current. It has typical rise and fall times of 30 ns and 20 ns, respectively, driving a 1 nF capacitive load.

The power dissipation of the output stage while driving the capacitance of the power MOSFET must be considered when calculating the NCP1218 power dissipation. The driver power dissipation can be calculated using Equation 8,

$$P_{DRV} = f_{OSC} \cdot Q_G \cdot V_{CC} \qquad \text{(eq. 8)}$$

where Q_G is the gate charge of the power MOSFET.

External Latch Input

Board level protection functionality is often incorporated using external circuits to suit a specific application. An external fault condition can be used to disable the controller by bringing the voltage on the Skip/latch pin above the latch threshold, V_{latch} (3.9 V typical). When an external fault condition is detected, the DRV signal is stopped, and the controller enters low current operation mode. The external capacitor C_{CC} discharges and V_{CC} drops until $V_{CC(hiccup)}$ is reached. The high voltage startup circuit turns on and I_{start} charges C_{CC} until $V_{CC(on)}$ is reached. V_{CC} cycles between $V_{CC(on)}$ and $V_{CC(hiccup)}$ until V_{CC} reaches $V_{CC(reset)}$. Voltage must be removed from the HV pin, disabling the startup current and allowing C_{CC} to discharge to $V_{CC(reset)}$. Therefore, the controller is reset by unplugging the power supply from the wall to allow V_{bulk} to discharge. Figure 35 illustrates the timing diagram of V_{CC} in the latch−off condition.

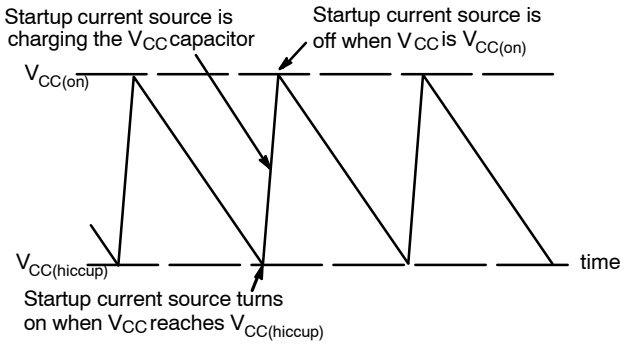


Figure 35. Latch−off V_{CC} Timing Diagram

The external latch feature allows the circuit designers to implement different kinds of latching protection. Figure 36 shows an example circuit in which a bipolar transistor is used to pull the Skip/latch pin above the latch threshold. The R_{LIM} value is chosen to prevent the Skip/latch pin from exceeding the maximum rated voltage. The NCP1219 applications note (AND8393/D) details several simple circuits to implement overtemperature protection (OTP) and overvoltage protection (OVP).

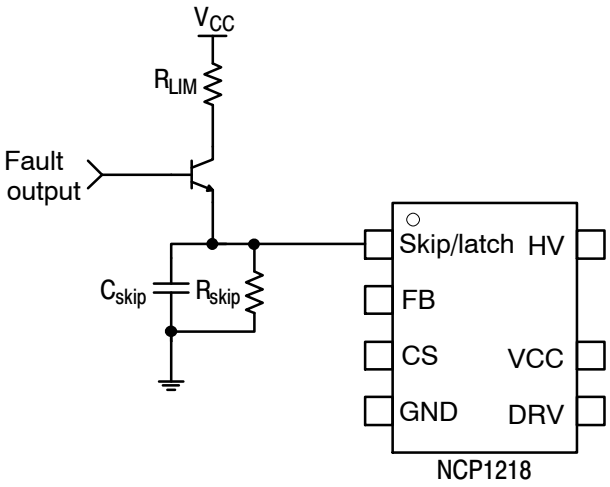


Figure 36. Circuit Example of an External Latch−off Circuit

An internal blanking filter prevents fast voltage spikes caused by noise from latching the part. However, it is recommended that an external filter capacitor be placed as close as possible to the Skip/latch pin to further improve the noise immunity.

Skip Cycle Operation

During standby or light load operation the duty ratio on the controller becomes very small. At this point, a significant portion of the power dissipation is related to the power MOSFET switching on and off. To reduce this power dissipation, the NCP1218 “skips” pulses when the FB level drops below the skip threshold. The level at which this occurs is completely adjustable by setting a resistor on the Skip/latch pin.

By discontinuing pulses, the output voltage slowly drops and the FB voltage rises. When the FB voltage rises above the V_{skip} level, DRV is turned back on. This feature produces the timing diagram shown in Figure 37.

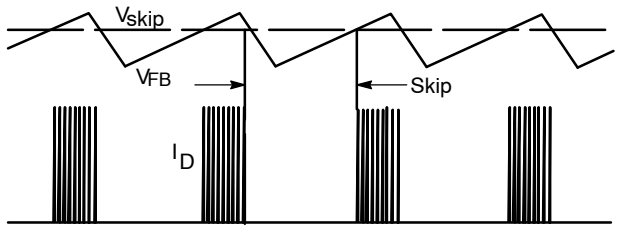


Figure 37. Skip Operation

Skip peak current, $\%I_{CSSKIP}$, is the percentage of the maximum peak current at which the controller enters skip mode. $\%I_{CSSKIP}$ can be any value from 0 to 43% as defined by Equation 9. However, the higher $\%I_{CSSKIP}$ is, the greater the drain current when skip is entered. This increases acoustic noise. Conversely, the lower $\%I_{CSSKIP}$ is, the larger the percentage of energy is expended turning the switch on and off. Therefore, it is important to adjust $\%I_{CSSKIP}$ to the optimal level for a given application.

$$\%I_{CSSKIP} = \frac{V_{skip}}{3\ V} \cdot 100 \qquad \text{(eq. 9)}$$

Figure 38 shows the details of the Skip/latch pin circuitry. The voltage on the Skip/latch pin determines the voltage required on the FB pin to place the controller into skip mode. If the pin is left open, the default skip threshold is 1.1 V. This corresponds to a 37% $\%I_{CSSKIP}$ ($\%I_{CSSKIP}$ = 1.1 V / 3.0 V * 100% = 37%). Therefore, the controller will enter skip mode when the peak current is less than 37% of the maximum peak current.

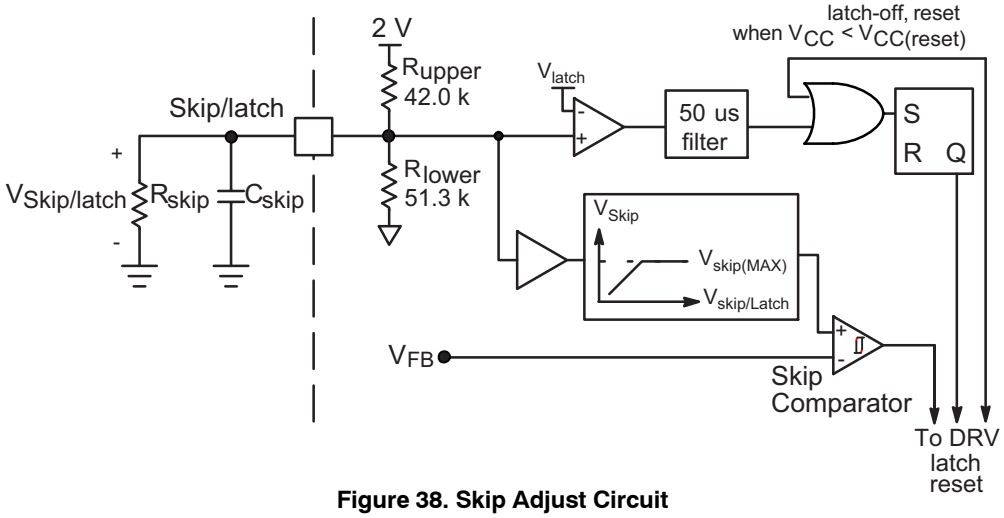


Figure 38. Skip Adjust Circuit

The skip level is reduced by placing an external resistor, R_{skip}, between the Skip/latch and GND pins. Figure 39 summarizes the operating voltage regions of the Skip/latch pin.

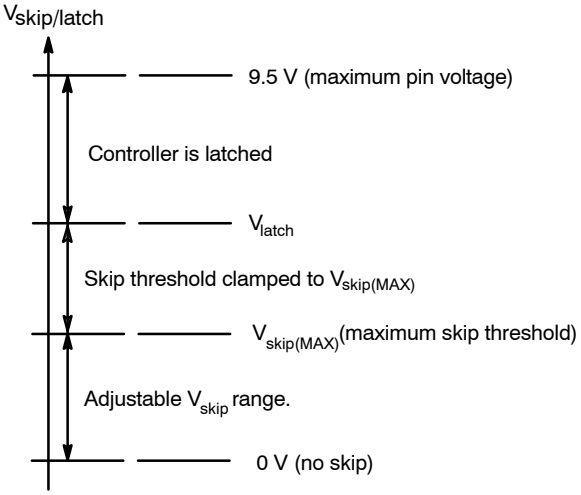


Figure 39. NCP1218 VSkip/latch Pin Operating Regions

Within the adjustable V_{skip} range, the skip level changes according to Equation 10.

$$V_{skip} = \frac{2\ V \cdot (R_{lower} \parallel R_{skip})}{(R_{lower} \parallel R_{skip}) + R_{upper}} \qquad \text{(eq. 10)}$$

An internal clamp limits the skip threshold ($V_{skip(MAX)}$) to 1.3 V. Increasing the voltage on the Skip/latch pin beyond the value of the internal clamp will induce no further change in the skip level. This prevents the act of disabling the controller in the presence of an external latch event from causing it to enter skip mode. The relationship between $\%I_{CSSKIP}$, $V_{Skip/latch}$, V_{skip}, and R_{skip} is summarized in Table 4.

Table 4. $\%I_{CSskip}$ and Skip Threshold Relationship with R_{skip}

$\%ICS_{skip}$	$V_{Skip/latch}$	V_{skip}	R_{skip}	Comment
0%	0 V	0 V	0 Ω	Never skips
12%	0.36 V	0.36 V	11.8 kΩ	–
25%	0.75 V	0.75 V	52.3 kΩ	–
37%	1.10 V	1.10 V	Open	Default Skip Threshold
43%	2.00 V	1.30 V	–	No further increase in Skip threshold
43 %	3.00 V	1.30 V	–	No further increase in Skip threshold

External Non−Latched Shutdown

Figure 40 summarizes the operating regions of the FB pin. An external non−latched shutdown can be easily implemented by simply pulling FB below the skip level. This is an inherent feature of the standby skip operation, allowing additional flexibility in the SMPS design.

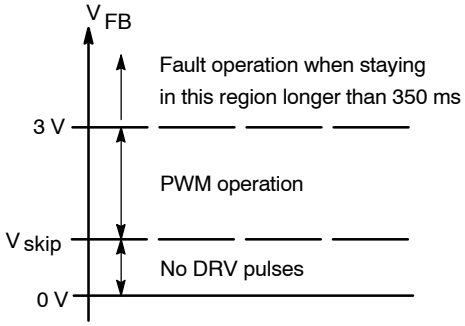


Figure 40. NCP1218 Operation Threshold

Figure 41 shows an example implementation of a non−latched shutdown circuit using a bipolar transistor to pull the FB pin low.

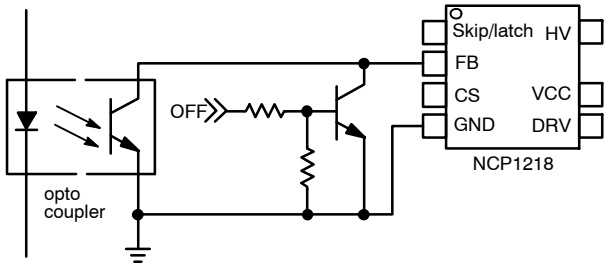


Figure 41. Example Circuit for Non−Latched Shutdown

Overload Protection

Figure 42 details the timer based fault detection circuitry. When an overload (or short circuit) event occurs, the output voltage collapses and the optocoupler does not conduct current. This opens the FB pin and V_{FB} is internally pulled higher than 3.0 V. Since $V_{FB}/3$ is greater than 1 V, the controller activates an error flag and starts a timer, t_{OVLD} (350 ms typical). If the output recovers during this time, the timer is reset and the device continues to operate normally.

However, if the fault lasts for more than 350 ms, then the driver latches off and the device remains in V_{CC} hiccup mode described earlier.

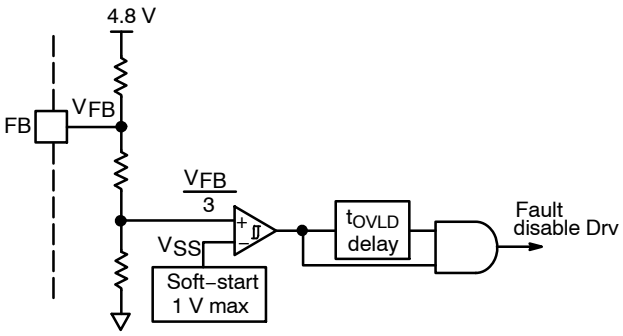


Figure 42. Block Diagram of Timer−Based Fault Detection

The NCP1218 also has an internal temperature shutdown circuit. If the junction temperature of the controller reaches 155°C (typical), the driver turns off and the controller enters double hiccup mode.

Table 5. ORDERING INFORMATION

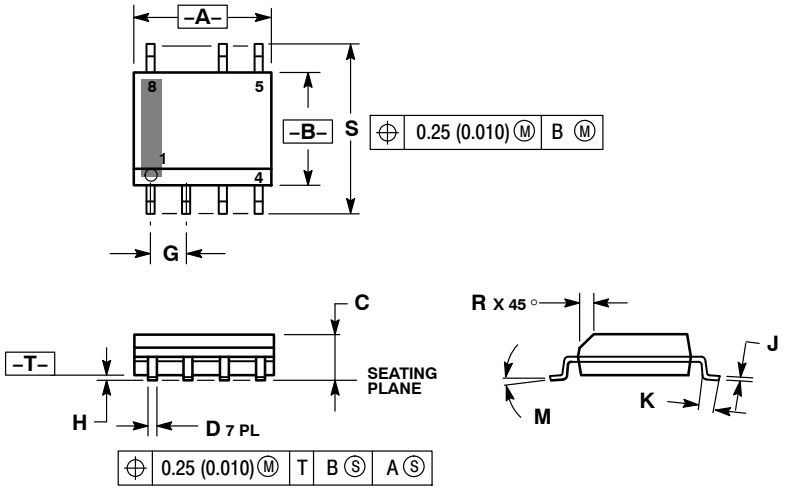
Device	Frequency	Package	Shipping†
NCP1218AD65R2G	65 kHz	SOIC−7 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

SOIC–7
CASE 751U–01
ISSUE E

DATE 20 OCT 2009

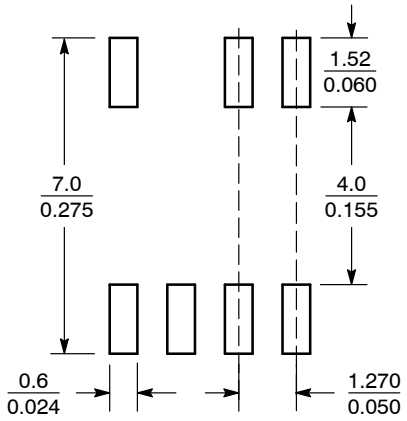
SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B ARE DATUMS AND T IS A DATUM SURFACE.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

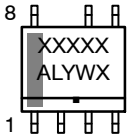
SOLDERING FOOTPRINT*



SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM



XXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb–Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “ ▪”, may or may not be present.

STYLES ON PAGE 2

SOIC−7
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ISSUE E

DATE 20 OCT 2009

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6.
7. NOT USED
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. NOT USED
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. NOT USED
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. NOT USED
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5.
6.
7. NOT USED
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6.
7. NOT USED
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. NOT USED
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR (DIE 1)
2. BASE (DIE 1)
3. BASE (DIE 2)
4. COLLECTOR (DIE 2)
5. COLLECTOR (DIE 2)
6. EMITTER (DIE 2)
7. NOT USED
8. COLLECTOR (DIE 1)

STYLE 9:
PIN 1. EMITTER (COMMON)
2. COLLECTOR (DIE 1)
3. COLLECTOR (DIE 2)
4. EMITTER (COMMON)
5. EMITTER (COMMON)
6. BASE (DIE 2)
7. NOT USED
8. EMITTER (COMMON)

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. NOT USED
8. GROUND

STYLE 11:
PIN 1. SOURCE (DIE 1)
2. GATE (DIE 1)
3. SOURCE (DIE 2)
4. GATE (DIE 2)
5. DRAIN (DIE 2)
6. DRAIN (DIE 2)
7. NOT USED
8. DRAIN (DIE 1)

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