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KSB1151

Feature

- Low Collector-Emitter Saturation Voltage
- Large Collector Current
- High Power Dissipation : P_C=1.3W (T_a=25°C)
- Complement to KSD 1691



PNP Epitaxial Silicon Transistor

Absolute Maximum Ratings $T_C=25^{\circ}C$ unless otherwise noted

Symbol	Parameter	Value	Units
V_{CBO}	Collector-Base Voltage	- 60	V
V_{CEO}	Collector-Emitter Voltage	- 60	V
V_{EBO}	Emitter-Base Voltage	- 7	V
I _C	Collector Current (DC)	- 5	Α
I _{CP}	*Collector Current (Pulse)	- 8	Α
I _B	Base Current	- 1	Α
P _C	Collector Dissipation (T _a =25°C)	1.3	W
	Collector Dissipation (T _C =25°C)	20	W
TJ	Junction Temperature	150	°C
T _{STG}	Storage Temperature	- 55 ~ 150	°C

^{*} PW≤10ms, Duty Cycle≤50%

Electrical Characteristics $T_C=25^{\circ}C$ unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Тур.	Max.	Units
I _{CBO}	Collector Cut-off Current	$V_{CB} = -50V, I_{E} = 0$			- 10	μΑ
I _{EBO}	Emitter Cut-off Current	$V_{EB} = -7V, I_{C} = 0$			- 10	μΑ
h _{FE1}	* DC Current Gain	$V_{CE} = -1V, I_{C} = -0.1A$	60			
h_{FE2}		$V_{CE} = -1V, I_{C} = -2A$	100	200	400	
h _{FE3}		$V_{CE} = -2V, I_{C} = -5A$	50			
V _{CE} (sat)	* Collector-Emitter Saturation Voltage	$I_C = -2A$, $I_B = -0.2A$		- 0.14	- 0.3	V
V _{BE} (sat)	* Base-Emitter Saturation Voltage	$I_C = -2A$, $I_B = -0.2A$		- 0.9	- 1.2	V
t _{ON}	Turn On Time	$V_{CC} = -10V, I_{C} = -2A$		0.15	1	μs
t _{STG}	Storage Time	$I_{B1} = -I_{B2} = 0.2A$		0.78	2.5	μs
t _F	Fall Time	$RL = 5\Omega$		0.18	1	μs

^{*} Pulse test: PW≤350μs, Duty Cycle≤2% Pulsed

h_{FE} Classification

Classification	0	Y	G
h _{FE2}	100 ~ 200	160 ~ 320	200 ~ 400

Typical Characteristics

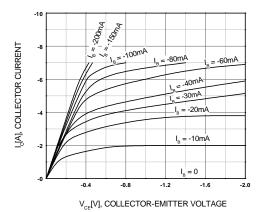


Figure 1. Static Characteristic

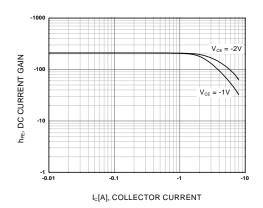


Figure 2. DC current Gain

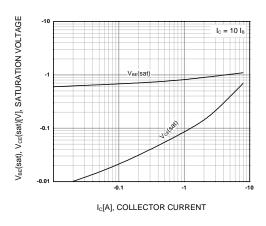


Figure 3. Collector-Emitter Saturation Voltage Base-Emitter Saturation Voltage

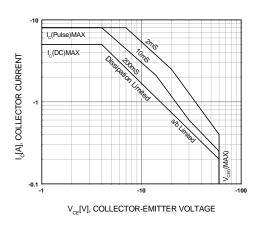


Figure 4. Forward Bias Operating Area

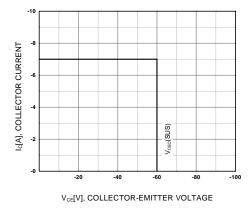


Figure 5. Reverse Bias Safe Operating Area

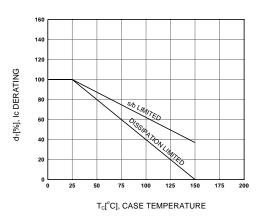


Figure 6. Derating Curve of Safe Operating Areas

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Typical Characteristics (Continued)

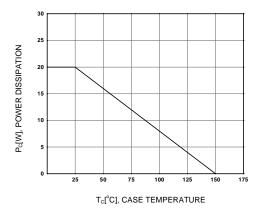
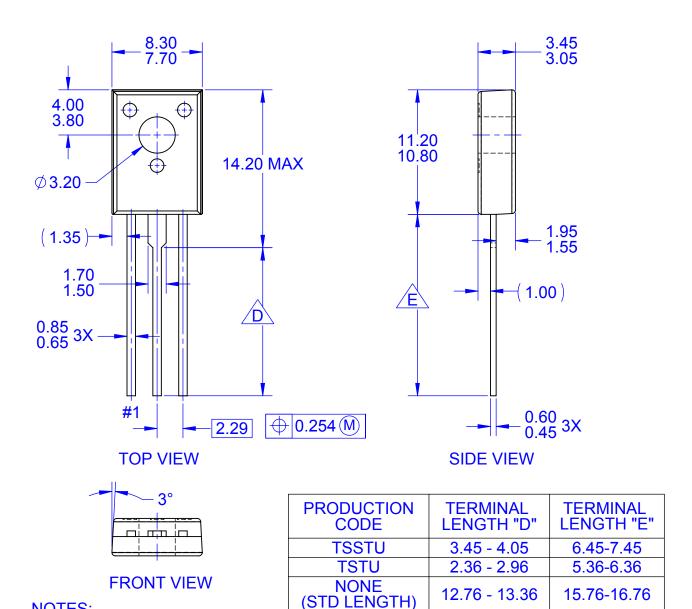


Figure 7. Power Derating

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