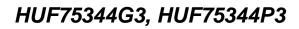
**ON Semiconductor** 

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#### Data Sheet

#### October 2013

### N-Channel UltraFET Power MOSFET 55 V, 75 A, 8 mΩ

These N-Channel power MOSFETs are manufactured using the innovative UltraFET process. This advanced process technology achieves the lowest possible onresistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and batteryoperated products.

Formerly developmental type TA75344.

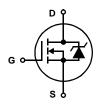
### **Ordering Information**

PART NUMBER	PACKAGE	BRAND
HUF75344G3	TO-247	75344G
HUF75344P3	TO-220AB	75344P

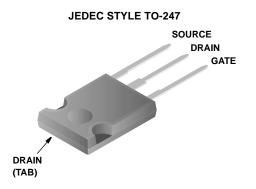
#### Features

- 75A, 55V
- Simulation Models
  - Temperature Compensated PSPICE® and SABER™ Models
  - Thermal Impedance PSPICE and SABER Models Available on the web at: www.fairchildsemi.com
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
  - TB334, "Guidelines for Soldering Surface Mount Components to PC Boards"

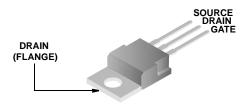
#### Symbol



### Packaging



JEDEC TO-220AB



All ON Semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

## Absolute Maximum Ratings $T_C = 25^{\circ}C$ , Unless Otherwise Specified

		UNITS
Drain to Source Voltage (Note 1)V <sub>DSS</sub>	55	V
Drain to Gate Voltage (R <sub>GS</sub> = 20kΩ) (Note 1) V <sub>DGR</sub>	55	V
Gate to Source Voltage	<u>+20</u>	V
Drain Current		
Continuous (Figure 2)	75	A
Pulsed Drain Current	Figure 4	
Pulsed Avalanche Rating E <sub>AS</sub>	Figure 6	
Power Dissipation P <sub>D</sub>	285	W
Derate Above 25 <sup>o</sup> C	1.90	W/ <sup>o</sup> C
Operating and Storage Temperature	-55 to 175	°C
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10sTL	300	°C
Package Body for 10s, See Techbrief 334	260	Oo

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1.  $T_J = 25^{\circ}C$  to  $150^{\circ}C$ .

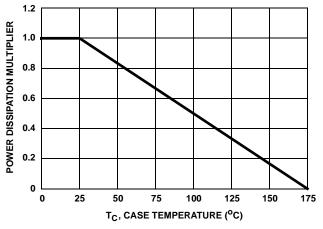
PARAMETER	SYMBOL	TEST	CONDITIONS	MIN	TYP	MAX	UNITS
OFF STATE SPECIFICATIONS		1		1	1	1	1
Drain to Source Breakdown Voltage	BV <sub>DSS</sub>	I <sub>D</sub> = 250μA, V <sub>GS</sub> = 0V (Figure 11)		55	-	-	V
Zero Gate Voltage Drain Current	IDSS	V <sub>DS</sub> = 50V, V <sub>GS</sub> =	0V	-	-	1	μA
		$V_{DS} = 45V, V_{GS} = 0V, T_{C} = 150^{\circ}C$		-	-	250	μA
Gate to Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20V		-	-	±100	nA
ON STATE SPECIFICATIONS						1	1
Gate to Source Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250µA (Figure 10)		2	-	4	V
Drain to Source On Resistance	rDS(ON)	I <sub>D</sub> = 75A, V <sub>GS</sub> = 10V (Figure 9)		-	6.5	8.0	mΩ
THERMAL SPECIFICATIONS		1				I	
Thermal Resistance Junction to Case	$R_{\theta JC}$	(Figure 3)		-	-	0.52	°C/W
Thermal Resistance Junction to Ambient	R <sub>θJA</sub>	TO-247		-	-	30	°C/W
		TO-220		-	-	62	°C/W
SWITCHING SPECIFICATIONS (V <sub>GS</sub> = 10 <sup>-</sup>	V)	1				I	
Turn-On Time	tON	$V_{DD}$ = 30V, I <sub>D</sub> ≅ 75A, $R_{L}$ = 0.4Ω, $V_{GS}$ = 10V, $R_{GS}$ = 3.0Ω		-	-	187	ns
Turn-On Delay Time	<sup>t</sup> d(ON)			-	13	-	ns
Rise Time	t <sub>r</sub>			-	125	-	ns
Turn-Off Delay Time	td(OFF)			-	46	-	ns
Fall Time	t <sub>f</sub>			-	57	-	ns
Turn-Off Time	<sup>t</sup> OFF			-	-	147	ns
GATE CHARGE SPECIFICATIONS						1	1
Total Gate Charge	Q <sub>g(TOT)</sub>	$V_{GS} = 0V$ to 20V	V <sub>DD</sub> = 30V,	-	175	210	nC
Gate Charge at 10V	Q <sub>g(10)</sub>	$V_{GS} = 0V$ to 10V	I <sub>D</sub> ≅ 75A,	-	90	108	nC
Threshold Gate Charge	Q <sub>g(TH)</sub>	$V_{GS} = 0V \text{ to } 2V$	$R_{L} = 0.4\Omega$ $I_{g(REF)} = 1.0mA$	-	5.9	7.0	nC
Gate to Source Gate Charge	Q <sub>gs</sub>		(Figure 13)	-	14	-	nC
Reverse Transfer Capacitance	Q <sub>gd</sub>			-	39	-	nC
CAPACITANCE SPECIFICATIONS		1		I		1	1
Input Capacitance	C <sub>ISS</sub>	$V_{DS} = 25V, V_{GS} = 0V,$ f = 1MHz (Figure 12)		-	3200	-	pF
Output Capacitance	C <sub>OSS</sub>			-	1170	-	pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			-	310	-	pF

# **Electrical Specifications** $T_C = 25^{\circ}C$ , Unless Otherwise Specified

#### Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V <sub>SD</sub>	I <sub>SD</sub> = 75A	-	-	1.25	V
Reverse Recovery Time	t <sub>rr</sub>	$I_{SD} = 75A$ , $dI_{SD}/dt = 100A/\mu s$	-	-	105	ns
Reverse Recovered Charge	Q <sub>RR</sub>	$I_{SD} = 75A$ , $dI_{SD}/dt = 100A/\mu s$	-	-	210	nC

# **Typical Performance Curves**





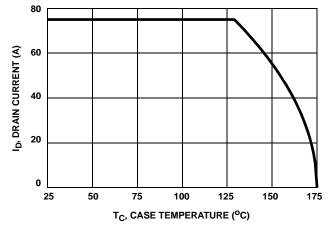


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

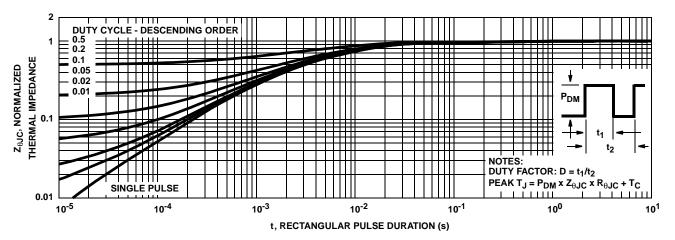


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

# Typical Performance Curves (Continued)

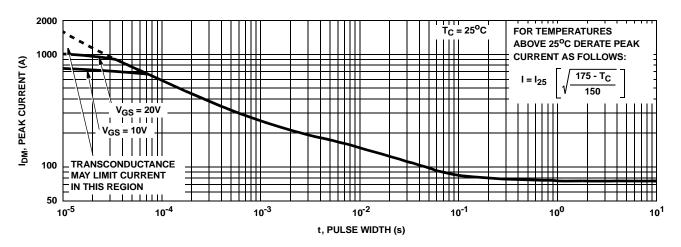


FIGURE 4. PEAK CURRENT CAPABILITY

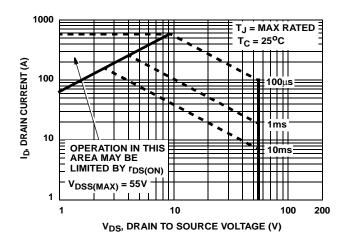


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA

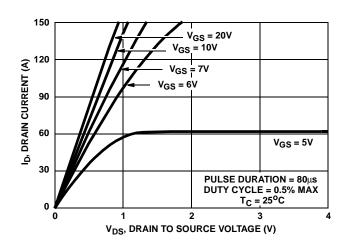
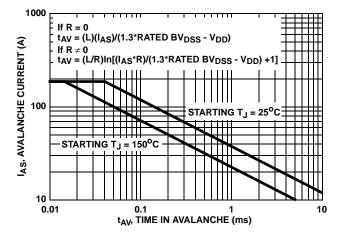
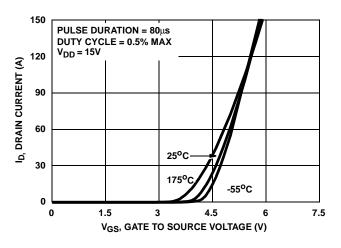


FIGURE 7. SATURATION CHARACTERISTICS



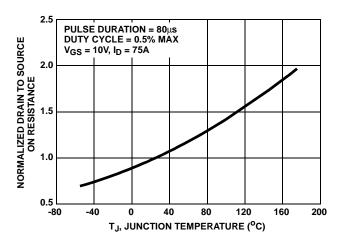
NOTE: Refer to ON Semiconductor Application Notes AN9321 and AN9322.





#### FIGURE 8. TRANSFER CHARACTERISTICS

#### Typical Performance Curves (Continued)





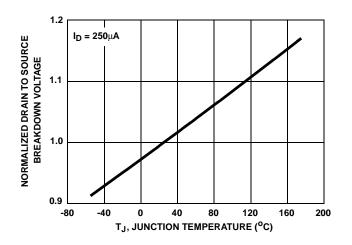


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

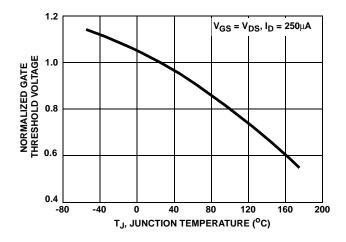


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

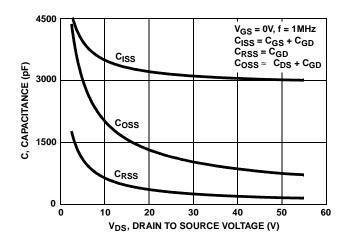
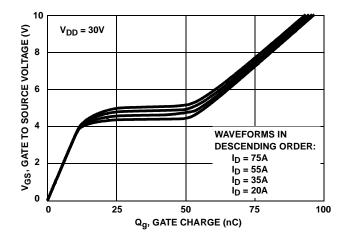


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to ON Semiconductor Application Notes AN7254 and AN7260. FIGURE 13. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

# Test Circuits and Waveforms

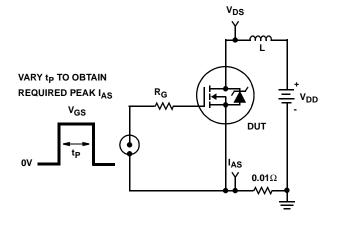


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

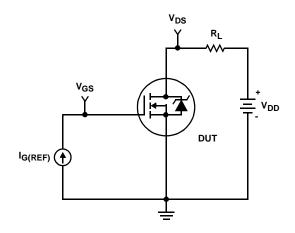


FIGURE 16. GATE CHARGE TEST CIRCUIT

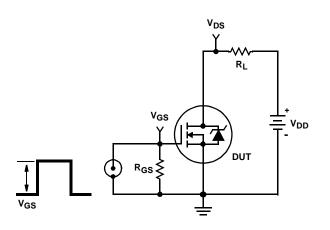


FIGURE 18. SWITCHING TIME TEST CIRCUIT

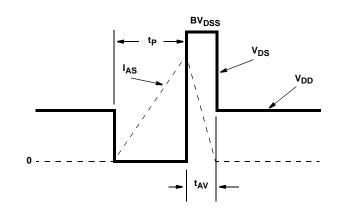
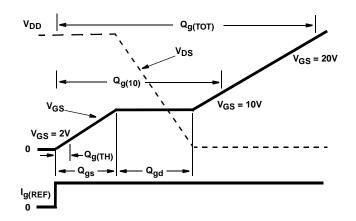


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS





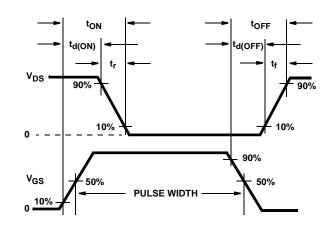


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

#### **PSPICE Electrical Model**

.SUBCKT HUF75337 2 1 3 ; rev 3 Feb 1999

CA 12 8 4.9e-9 CB 15 14 4.75e-9 CIN 6 8 2.85e-9

DBODY 7 5 DBODYMOD DBREAK 5 11 DBREAKMOD DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 59.7 EDS 14 8 5 8 1 EGS 13 8 6 8 1 ESG 6 10 6 8 1 EVTHRES 6 21 19 8 1 EVTERP 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 1e-9 LGATE 1 9 2.6e-9 LSOURCE 3 7 1.1e-9 KGATE LSOURCE LGATE 0.0085

MMED 16 6 8 8 MMEDMOD MSTRO 16 6 8 8 MSTROMOD MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1 RDRAIN 50 16 RDRAINMOD 1.94e-3 RGATE 9 20 0.36 RLDRAIN 2 5 10 RLGATE 1 9 26 RLSOURCE 3 7 11 RSLC1 5 51 RSLCMOD 1e-6 RSLC2 5 50 1e3 RSOURCE 8 7 RSOURCEMOD 3.5e-3 RVTHRES 22 8 RVTHRESMOD 1 RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD S1B 13 12 13 8 S1BMOD S2A 6 15 14 13 S2AMOD S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))\*(PWR(V(5,51)/(1e-6\*400),3))}

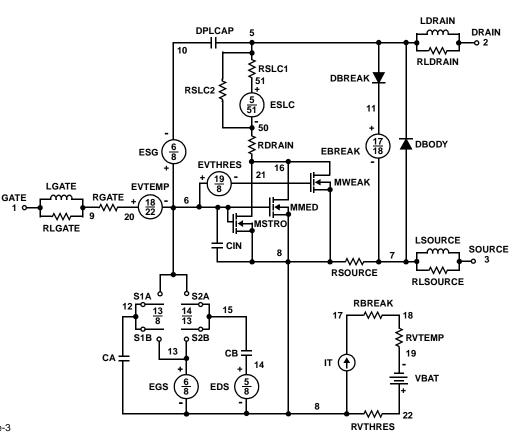
.MODEL DBODYMOD D (IS = 2.95e-12 RS = 2.6e-3 TRS1 = 1.05e-3 TRS2 = 5.0e-7 CJO = 5.19e-9 TT = 5.9e-8 M = 0.55) .MODEL DBREAKMOD D (RS = 1.65e-1 IKF = 30 TRS1 = 1.15e-4 TRS2 = 2.27e-6) .MODEL DPLCAPMOD D (CJO = 5.40e-9 IS = 1e-30 N=1 M = 0.88) .MODEL MMEDMOD NMOS (VTO = 3.29 KP = 5.5 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 0.36) .MODEL MSTROMOD NMOS (VTO = 3.83 KP = 123 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u) .MODEL MWEAKMOD NMOS (VTO = 2.90 KP = 0.04 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u) .MODEL RBREAKMOD RES (TC1 = 1.15e-3 TC2 = 2.0e-7) .MODEL RBREAKMOD RES (TC1 = 1.37e-2 TC2 = 3.85e-5) .MODEL RSLCMOD RES (TC1 = 1.45e-4 TC2 = 2.11e-6) .MODEL RSUCCEMOD RES (TC1 = 0 TC2 = 0) .MODEL RVTHRESMOD RES (TC1 = -3.7e-3 TC2 = -1.6e-5) .MODEL RVTHRESMOD RES (TC1 = -2.4e-3 TC2 = 7e-7) .MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -6.9 VOFF= -3.9) MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -6.9 VOFF= -6.9)

MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -3.9 VOFF = -6.9) MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.99 VOFF = 2.39)

.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 2.39 VOFF= -2.99)

#### .ENDS

NOTE: For further discussion of the PSPICE model, consult A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.



#### SABER Electrical Model

#### REV 3 February 1999

template huf75344 n2, n1, n3 electrical n2, n1, n3 var i iscl d..model dbodymod = (is = 2.95e-12, cjo = 5.19e-9, tt = 5.90e-8, m = 0.55) d..model dbreakmod = () LDRAIN DPLCAP DRAIN d..model dplcapmod = (cjo = 5.40e-9, is = 1e-30, n = 1, m = 0.88) 5 m..model mmedmod = (type=\_n, vto = 3.29, kp = 5.5, is = 1e-30, tox = 1) o 2 10 m..model mstrongmod = (type=\_n, vto = 3.83, kp = 123, is = 1e-30, tox = 1) RLDRAIN m..model mweakmod = (type=\_n, vto = 2.90, kp = 0.04, is = 1e-30, tox = 1) ≥ RSLC1 RDBREAK sw\_vcsp..model s1amod = (ron = 1e-5, roff = 0.1, von = -6.9, voff = -3.9) 51 RSLC2≥ sw\_vcsp..model s1bmod = (ron = 1e-5, roff = 0.1, von = -3.9, voff = -6.9) 72 ۶ RDBODY sw\_vcsp..model s2amod = (ron = 1e-5, roff = 0.1, von = -2.99, voff = 2.39) Ŧ ISCL sw\_vcsp..model s2bmod = (ron = 1e-5, roff = 0.1, von = 2.39, voff = -2.99) DBREAK 50 c.ca n12 n8 = 4.9e-9 71 6 8 c.cb n15 n14 = 4.75e-9 ESG 11 c.cin n6 n8 = 2.85e-9 EVTHRES 16 21 <u>19</u> 8 MWEAK EVTEMP LGATE d.dbody n7 n71 = model=dbodymod DBODY RGATE GATE d.dbreak n72 n11 = model=dbreakmod 6 18 22 EBREAK i MMED d.dplcap n10 n5 = model=dplcapmod 1 C 9 20 \*\*\* Hi€mstro RLGATE i.it n8 n17 = 1 18 LSOURCE CIN SOURCE 8 I.Idrain n2 n5 = 1e-9 -0 - 3 l.lgate n1 n9 = 2.6e-9 RSOURCE RLSOURCE l.lsource n3 n7 = 1.1e-9 k.kl i(l.lgate) i(l.lsource) = I(l.lgate), I(l.lsource), 0.0085 ⁰S2A S1A RBREAK <u>14</u> 13 15 17  $\sim$ 18 m.mmed n16 n6 n8 n8 = model=mmedmod, I = 1u, w = 1u m.mstrong n16 n6 n8 n8 = model=mstrongmod, I = 1u, w = 1u RVTEMP o S2B S1B m.mweak n16 n21 n8 n8 = model=mweakmod, I = 1u, w = 1u 13 CB 19 CA: IT 14 res.rbreak n17 n18 = 1, tc1 = 1.15e-3, tc2 = 2e-7 res.rdbody n71 n5 = 2.6e-3, tc1 = 1.05e-3, tc2 = 5e-7 VBAT <u>6</u> 8 EGS 5 FDS res.rdbreak n72 n5 = 1.65e-1, tc1 = 1.15e-4, tc2 = 2.27e-6 res.rdrain n50 n16 = 1.94e-3, tc1 = 1.37e-2, tc2 = 3.85e-5 8 res.rgate n9 n20 = 0.36 22 res.rldrain n2 n5 = 10 RVTHRES res.rlgate n1 n9 = 26 res.rlsource n3 n7 = 11 res.rslc1 n5 n51 = 1e-6, tc1 = 1.45e-4, tc2 = 2.11e-6 res.rslc2 n5 n50 = 1e3 res.rsource n8 n7 = 3.5e-3, tc1 = 0, tc2 = 0 res.rvtemp n18 n19 = 1, tc1 = -2.4e-3, tc2 = 7e-7 res.rvthres n22 n8 = 1, tc1 = -3.7e-3, tc2 = -1.6e-5 spe.ebreak n11 n7 n17 n18 = 59.7 spe.eds n14 n8 n5 n8 = 1 spe.egs n13 n8 n6 n8 = 1 spe.esg n6 n10 n6 n8 = 1 spe.evtemp n20 n6 n18 n22 = 1 spe.evthres n6 n21 n19 n8 = 1 sw\_vcsp.s1a n6 n12 n13 n8 = model=s1amod sw\_vcsp.s1b n13 n12 n13 n8 = model=s1bmod sw\_vcsp.s2a n6 n15 n14 n13 = model=s2amod sw\_vcsp.s2b n13 n15 n14 n13 = model=s2bmod v.vbat n22 n19 = dc = 1 equations { i(n51-n50) + = iscl(v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))\*((abs(v(n5,n51)\*1e6/400))\*\*3))

# SPICE Thermal Model

#### REV 5 February 1999

#### HUF75344

CTHERM1 th 6 5.0e-3 CTHERM2 6 5 1.0e-2 CTHERM3 5 4 1.3e-2 CTHERM4 4 3 1.5e-2 CTHERM5 3 2 2.2e-2 CTHERM6 2 tl 8.5e-2

RTHERM1 th 6 6.0e-4 RTHERM2 6 5 3.5e-3 RTHERM3 5 4 2.5e-2 RTHERM4 4 3 4.8e-2 RTHERM5 3 2 1.6e-1 RTHERM6 2 tl 1.8e-1

# SABER Thermal Model

SABER thermal model HUF75344

template thermal\_model th tl thermal\_c th, tl { ctherm.ctherm1 th 6 = 5.0e-3 ctherm.ctherm2 6 5 = 1.0e-2 ctherm.ctherm3 5 4 = 1.3e-2

ctherm.ctherm4 4 3 = 1.5e-2ctherm.ctherm5 3 2 = 2.2e-2ctherm.ctherm6 2 tl = 5.5e-2

rtherm.rtherm1 th 6 = 6.0e-4 rtherm.rtherm2 6 5 = 3.5e-3 rtherm.rtherm3 5 4 = 2.5e-2 rtherm.rtherm4 4 3 = 4.8e-2 rtherm.rtherm5 3 2 = 1.6e-1 rtherm.rtherm6 2 tl = 1.8e-1 }

JUNCTION th Q RTHERM1 CTHERM1 6 RTHERM2 CTHERM2 5 **RTHERM3** CTHERM3 4 RTHERM4 CTHERM4 3 RTHERM5 CTHERM5 2 RTHERM6 CTHERM6 CASE tl Ŷ

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