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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FAIRCHILD™

January 2016

FQP3P50

P-Channel QFET® MOSFET

-500 V, -2.7 A, 4.9 Ω

Description

This P-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

Features

- -2.7 A, -500 V, $R_{DS(on)}$ = 4.9 Ω (Max.) @ V_{GS} = -10 V, I_D = -1.35 A
- Low Gate Charge (Typ. 18 nC)
- Low Crss (Typ 9.5 pF)
- 100% Avalanche Tested

TO-220

Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter		FQP3P50	Unit
V_{DSS}	Drain-Source Voltage		-500	V
I_D	Drain Current - Continuous (T_C = 25°C)		-2.7	A
	- Continuous (T_C = 100°C)		-1.71	A
I_{DM}	Drain Current - Pulsed	(Note 1)	-10.8	A
V_{GS}	Gate-Source Voltage		± 30	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	250	mJ
I_{AR}	Avalanche Current	(Note 1)	-2.7	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	8.5	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	-4.5	V/ns
P_D	Power Dissipation (T_C = 25°C)		85	W
	- Derate above 25°C		0.68	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum lead temperature for soldering, 1/8" from case for 5 seconds		300	°C

Thermal Characteristics

Symbol	Parameter	FQP3P50	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	1.47	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	°C/W

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Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQP3P50	FQP3P50	TO-220	Tube	N/A	N/A	50 units

Elerical Characteristics $T_C = 25°C$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0$ V, $I_D = -250$ μA	-500	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = -250$ μA, Referenced to 25°C	--	0.42	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -500$ V, $V_{GS} = 0$ V	--	--	-1	μA
		$V_{DS} = -400$ V, $T_C = 125°C$	--	--	-10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = -30$ V, $V_{DS} = 0$ V	--		-100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = 30$ V, $V_{DS} = 0$ V	--		100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = -250$ μA	-3.		-5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -10$ V, $I_D = -1.5$ A	--	3.9	4.9	Ω
g_{FS}	Forward Transconductance	$V_{DS} = -50$ V, $I_D = -35$	--	2.35	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 25$ V, $V_{GS} = 0$ V,	--	510	660	pF
C_{oss}	Output Capacitance	$f = 1.0$ MHz	--	70	90	pF
C_{rss}	Reverse Transfer Capacitance		--	9.5	12	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -250$ V, $I_D = -2.7$ A, $R_G = 25$ Ω,	--	12	35	ns
t_r	Turn-On Rise Time		--	56	120	ns
$t_{d(off)}$	Turn-Off Delay Time		--	35	80	ns
t_f	Turn-Off Fall Time	(Note 4)	--	45	100	ns
Q_g	Total Gate Charge	$V_{DS} = -400$ V, $I_D = -2.7$ A,	--	18	23	nC
Q_{gs}	Gate-Source Charge	$V_{GS} = -10$ V	--	3.6	--	nC
Q_{gd}	Gate-Drain Charge	(Note 4)	--	9.2	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	-2.7	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	-10.8	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0$ V, $I_S = -2.7$ A	--	--	-5.0	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0$ V, $I_S = -2.7$ A,	--	270	--	ns
Q_{rr}	Reverse Recovery Charge	$dI_F / dt = 100$ A/μs	--	1.5	--	μC

Notes:

1. Repetitive rating : pulse-width limited by maximum junction temperature.

2. $L = 62$ mH, $I_{AS} = -2.7$ A, $V_{DD} = -50$ V, $R_G = 25$ Ω, starting $T_J = 25°C$.

3. $I_{SD} \leq -2.7$ A, di/dt ≤ 200 A/μs , $V_{DD} \leq BV_{DSS}$, starting $T_J = 25°C$.

4. Essentially independent of operating temperature.
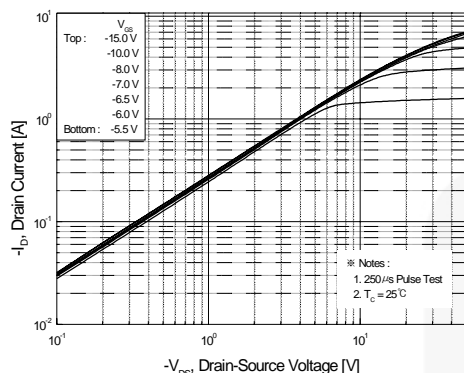
Typical Characteristics
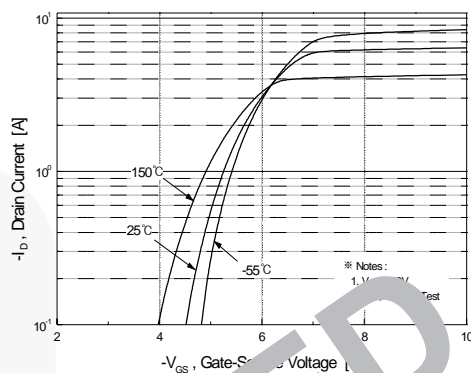

Figure 1. On-Region Characteristics

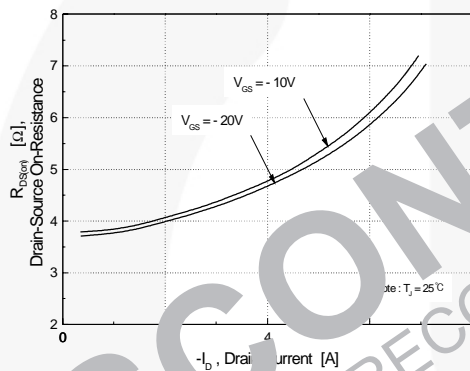**Figure 2. Transfer Characteristics**

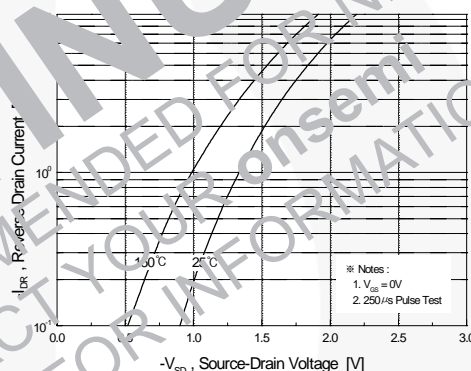**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**

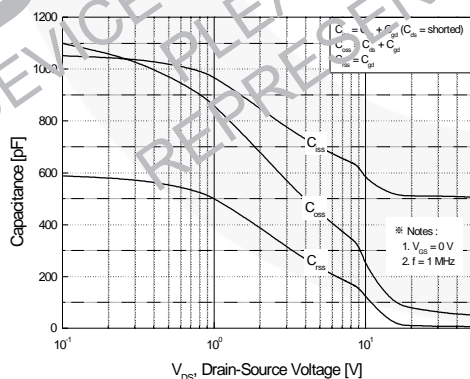**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**
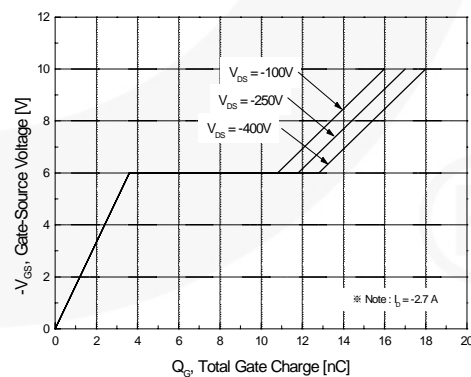

Figure 5. Capacitance Characteristics

Figure 6. Gate Charge Characteristics

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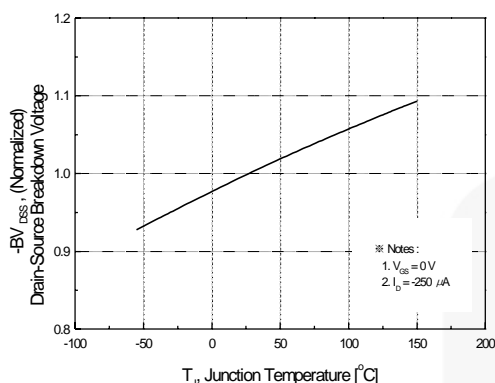
Typical Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature
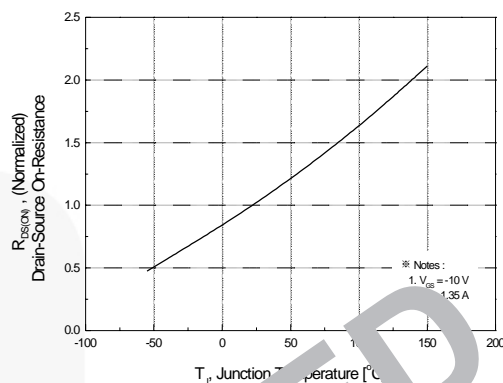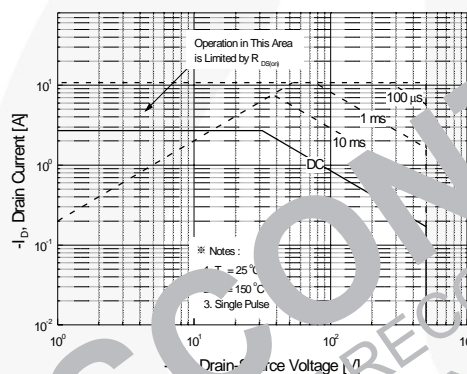

Figure 8. On-Resistance Variation vs. Temperature
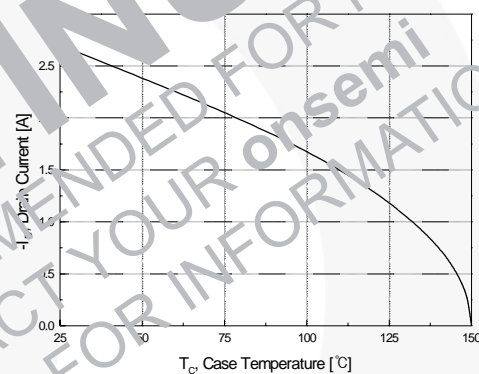

Figure 9. Maximum Safe Operating Area

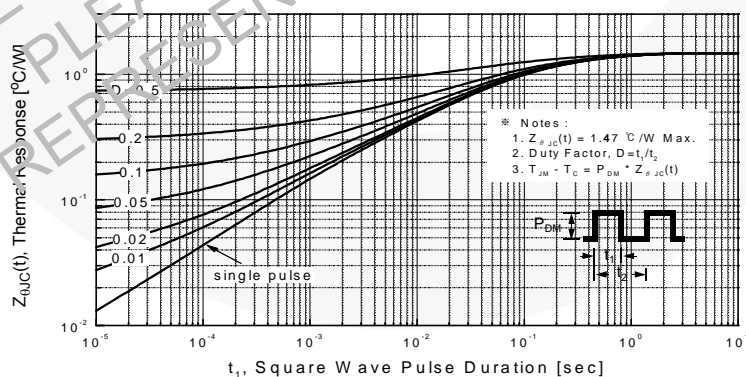**Figure 10. Maximum Drain Current vs. Case Temperature**

Figure 11. Transient Thermal Response Curve

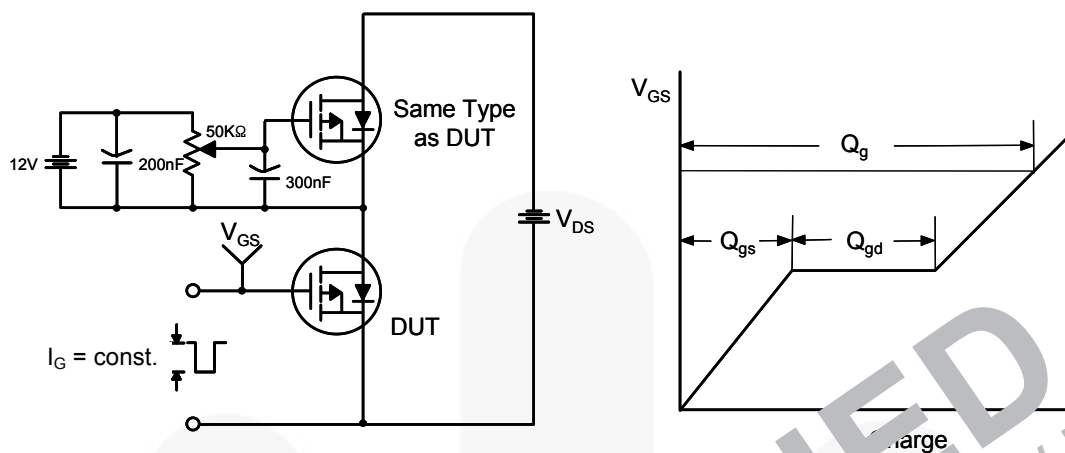Figure 12. Gate Charge Test Circuit & Waveform
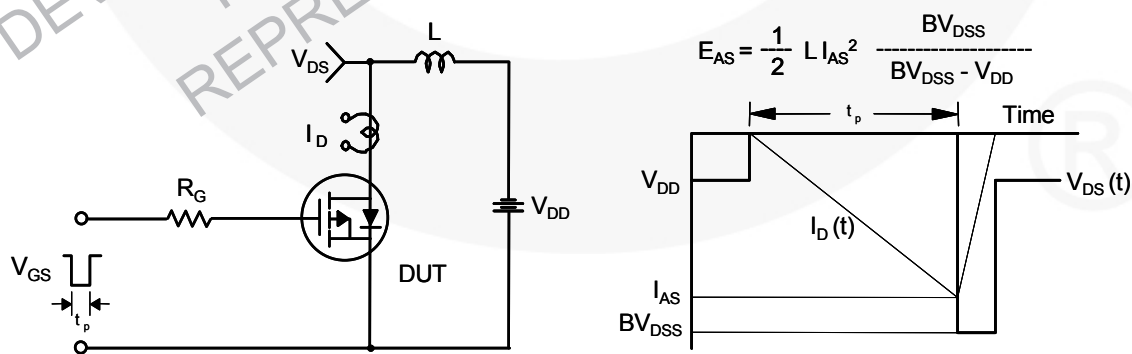

Figure 13. Resistive Switching Test Circuit & Waveforms

$$E_{AS} = \frac{1}{2} L I_{AS}^2 \; \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

V_{DS}

DUT

I_{SD}

L

Driver

R_G

Compliment of DUT
(N-Channel)

V_{GS}

dv/dt controlled by R_G

controlled by pulse period

V_{DD}

V_{GS}
(Driver)

$D = \dfrac{\text{Gate Pulse Width}}{\text{Gate Pulse Period}}$

10V

I_{SD}
(DUT)

Body Diode Reverse Current

I_{RM}

di/dt

I_{FM} , Body Diode Forward Current

V_{DS}
(DUT)

V_{SD}

Body Diode
Forward Voltage Drop

V_{DD}

Body Diode Recovery dv/dt
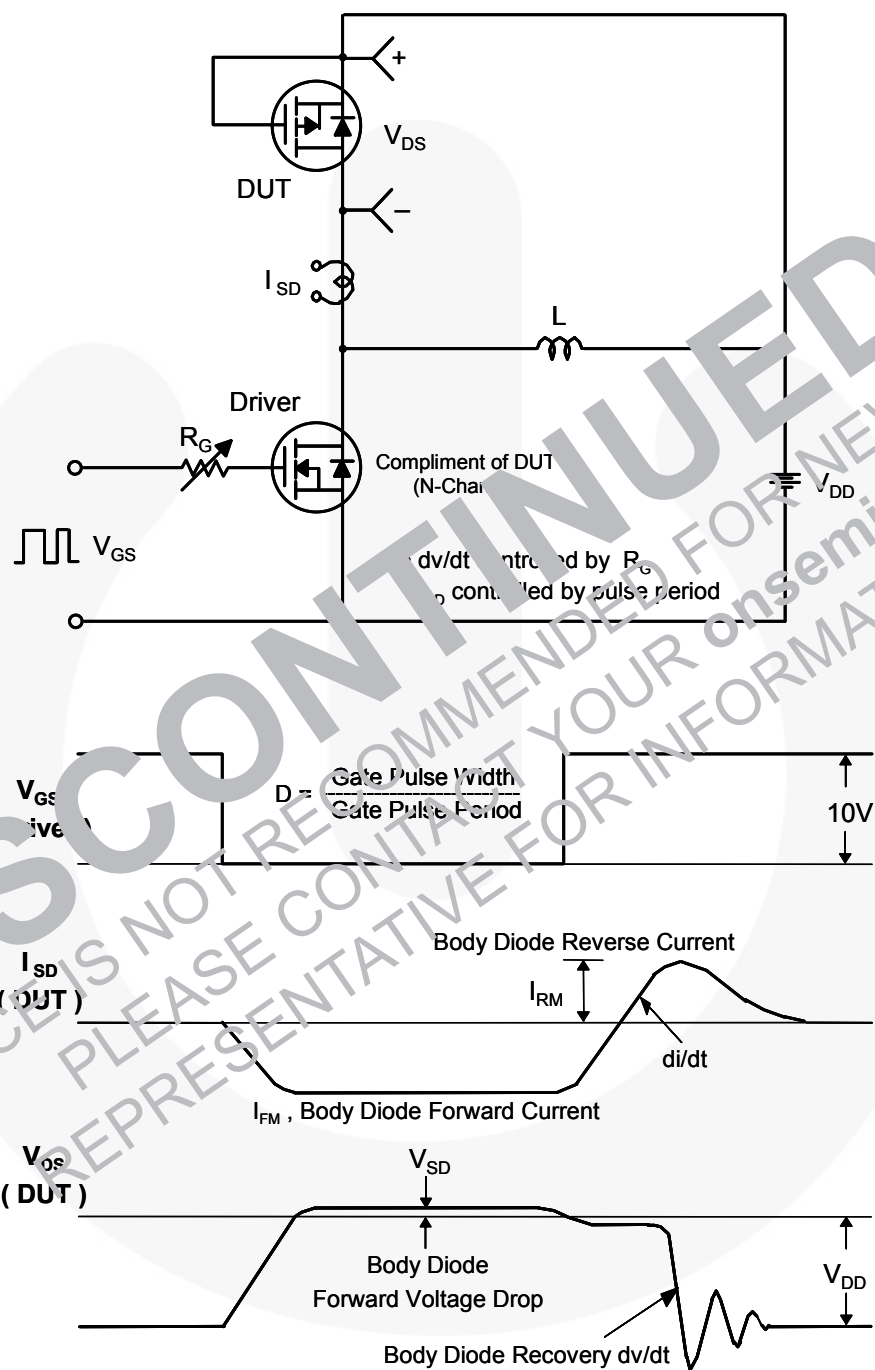
Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions

NOTES:
A) CONFORMS TO JEDEC TO-220
   VARIATION AB EXCEPT WHERE NOTED
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS ARE EXCLUSIVE OF BURRS,
   MOLD FLASH, AND TIE BAR EXTRUSIONS.
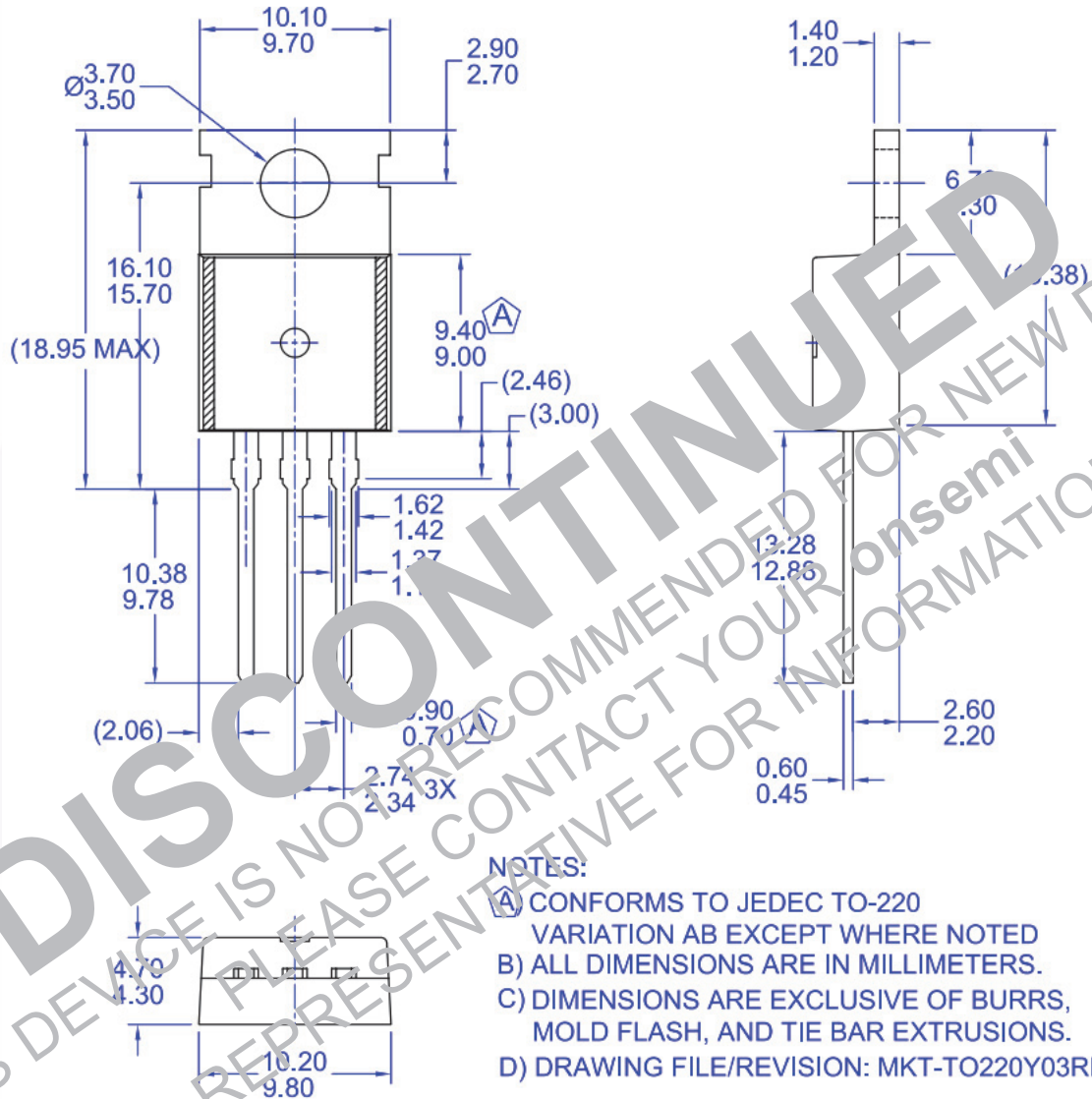D) DRAWING FILE/REVISION: MKT-TO220Y03REV1

Figure 16. TO220, Molded, 3-Lead, Jedec Variation AB

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Datasheet Identification	Product Status	Definition
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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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Mouser Electronics

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