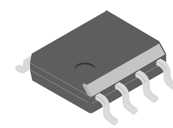
3.3 V LVDS, 1-Bit, High-Speed Differential Driver

FIN1017



SOIC8
CASE 751EB

General Description

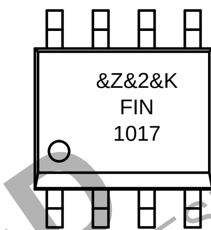
This single driver is designed for high−speed interconnects utilizing Low Voltage Differential Signaling (LVDS) technology. The driver translates LVTTL signal levels to LVDS levels with a typical differential output swing of 350 mV, which provides low EMI at ultra−low power dissipation even at high frequencies. This device is ideal for high−speed transfer of clock or data.

The FIN1017 can be paired with any other LVDS receiver.

Features

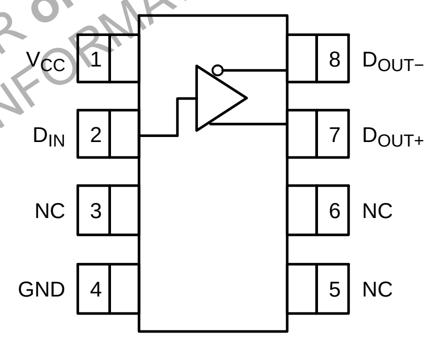
- Greater than 600 Mbs Data Rate
- 3.3 V Power Supply Operation
- 0.5 ns Maximum Differential Pulse Skew
- 1.5 ns Maximum Propagation Delay
- Low Power Dissipation
- Power−Off Protection
- Meets or Exceeds the TIA/EIA−644 LVDS Standard
- Flow−Through Pinout Simplifies PCB Layout
- 8−Lead SOIC Package Saves Space
- This Device is Pb−Free, Halide Free and is RoHS Compliant

MARKING DIAGRAM



&Z = Assembly Plant Code
&2 = 2−Digit Date Code
&K = 2−Digits Lot Run Traceability Code
FIN1017 = Specific Device Code

PIN CONFIGURATION



PIN CONFIGURATION

Pin# SOIC	Name	Description
2	DIN	LVTTL Data Input
7	D_{OUT+}	Non−inverting Driver Output
8	D_{OUT-}	Inverting Driver Output
1	V_{CC}	Power Supply
4	GND	Ground
3, 5, 6	NC	No Connect

FUNCTIONAL TABLE

Input	Outputs	
D_{IN}	D_{OUT+}	D_{OUT-}
LOW	LOW	HIGH
HIGH	HIGH	LOW
OPEN	LOW	HIGH

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	−0.5	+4.6	V
D_{IN}	DC Input Voltage	−0.5	+6.0	V
D_{OUT}	DC Output Voltage	−0.5	+4.7	V
I_{OSD}	Driver Short−Circuit Current, Continuous	−	10	mA
T_{STG}	Storage Temperature Range	−65	+150	°C
T_J	Max Junction Temperature	−	+150	°C
T_L	Lead Temperature (Soldering, 10 Seconds)	−	+260	°C
ESD	Human Body Model, JESD22−A114	−	6500	V
	Bus Pins D_{OUT+}/D_{OUT-} to GND	−	10500	
	Machine Model, JESD22−A115	−	350	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	3.0	3.6	V
V_{IN}	Input Voltage	0	V_{CC}	V
T_A	Operating Temperature	−40	+85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (Over−supply voltage and operating temperature ranges, unless otherwise specified. All typical values are at T_A = 25°C and with V_{CC} = 3.3 V.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OD}	Output Differential Voltage	R_L = 100 Ω, See Figure 1	250	350	450	mV
ΔV_{OD}	VOD Magnitude Change from Differential LOW−to−HIGH		−	−	25	mV
V_{OS}	Offset Voltage		1.125	1.250	1.375	V
ΔV_{OS}	Offset Magnitude Change from Differential LOW−to−HIGH		−	−	25	mV
I_{OFF}	Power−Off Output Current	V_{CC} = 0 V, V_{OUT} = 0 V or 3.6 V	−	−	±20	mA
I_{OS}	Short−Circuit Output Current	V_{OUT} = 0 V	−	−	−8	mA
		V_{OD} = 0 V	−	−	±8	
V_{IH}	Input HIGH Voltage		2	−	V_{CC}	V
V_{IL}	Input LOW Voltage		GND	−	0.8	V
I_{IN}	Input Current	V_{IN} = 0 V or V_{CC}	−	−	±20	mA
$I_{I(OFF)}$	Power−Off Input Current	V_{CC} = 0 V, V_{IN} = 0 V or 3.6 V	−	−	±20	mA
V_{IK}	Input Clamp Voltage	I_{IK} = −18 mA	−1.5	−	−	V
I_{CC}	Power Supply Current	No Load, V_{IN} = 0 V or V_{CC}	−	−	8	mA
		R_L = 100 Ω, V_{IN} = 0 V or V_{CC}	−	−	10	mA
C_{IN}	Input Capacitance		−	4	−	pF
C_{OUT}	Output Capacitance		−	6	−	pF

AC ELECTRICAL CHARACTERISTICS (Over−supply voltage and operating temperature ranges, unless otherwise specified. All typical values are at T_A = 25°C and with V_{CC} = 3.3 V.)

Symbol	Parameter	Test Conditions	Min	Max	Unit
t_{PLHD}	Differential Propagation Delay, LOW−to−HIGH	R_L = 100 Ω, CL = 10 pF, see Figure 2 and Figure 3	0.5	1.5	ns
t_{PHLD}	Differential Propagation Delay, HIGH−to−LOW		0.5	1.5	ns
t_{TLHD}	Differential Output Rise Time (20% to 80%)		0.4	1.0	ns
t_{THLD}	Differential Output Fall Time (80% to 20%)		0.4	1.0	ns
$t_{SK(P)}$	Pulse Skew $\|t_{PLH} − t_{PHL}\|$		−	0.5	ns
$t_{SK(PP)}$	Part−to−Part Skew (Note 1)		−	1.0	ns

1. $t_{SK(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices switching in the same direction (either LOW−to−HIGH or HIGH−to−LOW) when both devices operate with the same supply voltage, same temperature, and have identical test circuits.

TEST DIAGRAMS

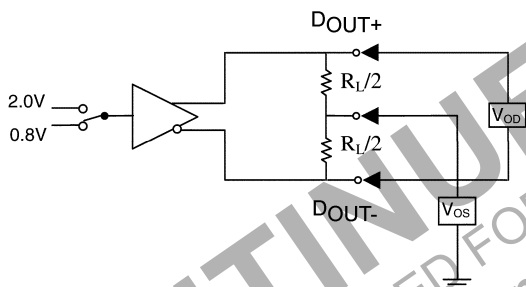
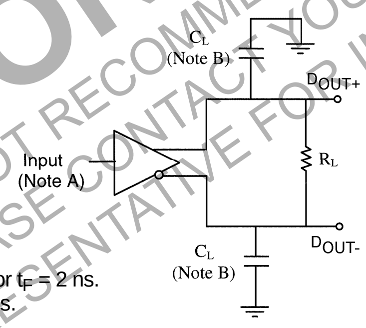


Figure 1. Differential Driver DC Test Circuit



NOTES:
A. All input pulses have frequency = 10 MHz, t_R or t_F = 2 ns.
B. CL includes all probe and fixture capacitances.

Figure 2. Differential Driver Propagation Delay and Transition Time Test Circuit

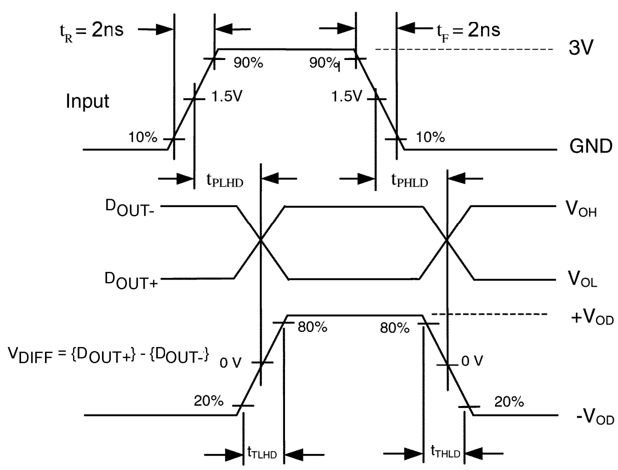


Figure 3. AC Waveforms

TYPICAL PERFORMANCE CHARACTERISTICS

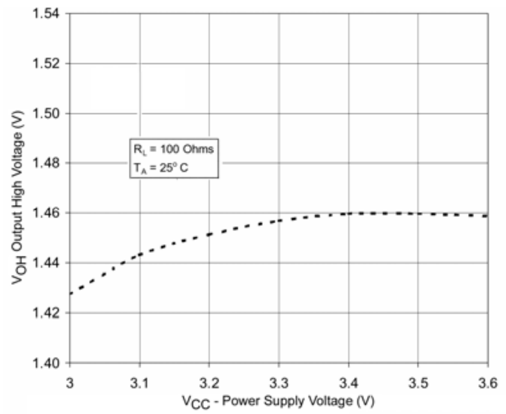


Figure 4. Output High Voltage vs. Power Supply Voltage

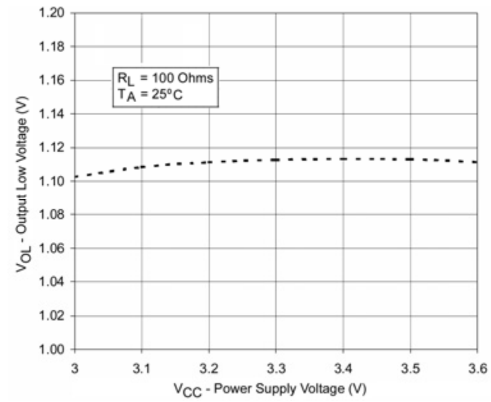


Figure 5. Output Low Voltage vs. Power Supply Voltage

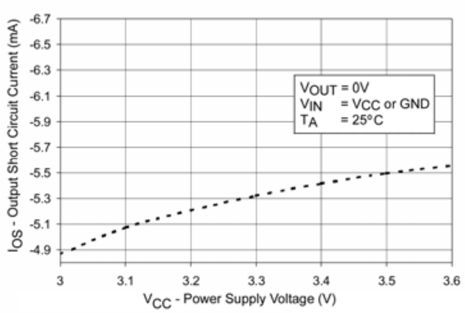


Figure 6. Output Short Circuit Current vs. Power Supply Voltage

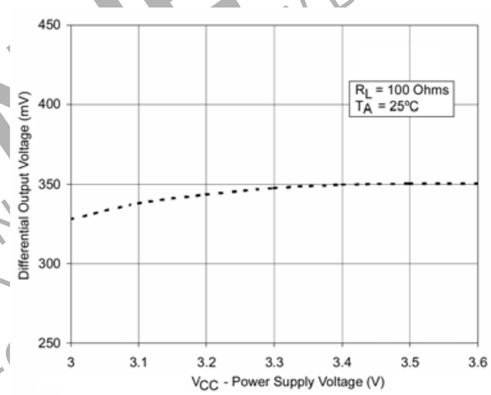


Figure 7. Differential Output Voltage vs. Power Supply Voltage

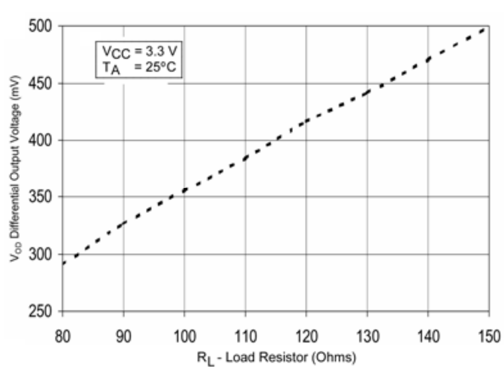


Figure 8. Differential Output Voltage vs. Load Resistor

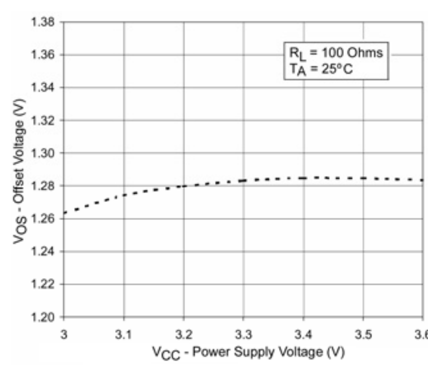


Figure 9. Offset Voltage vs. Power Supply Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

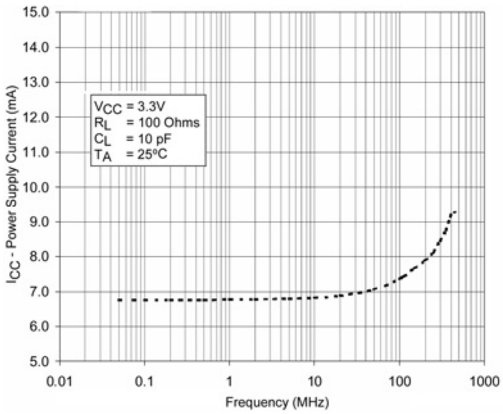


Figure 10. Power Supply Current vs. Frequency

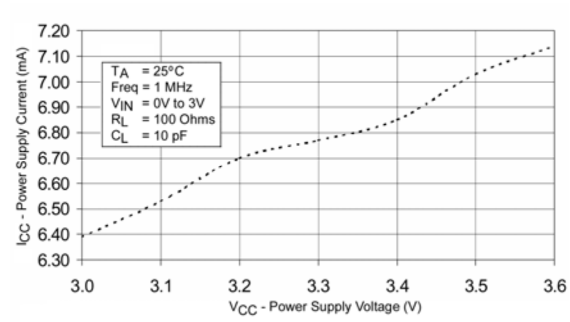


Figure 11. Power Supply Current vs. Power Supply Voltage

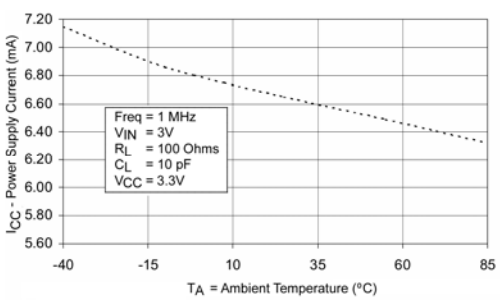


Figure 12. Power Supply Current vs. Ambient Temperature

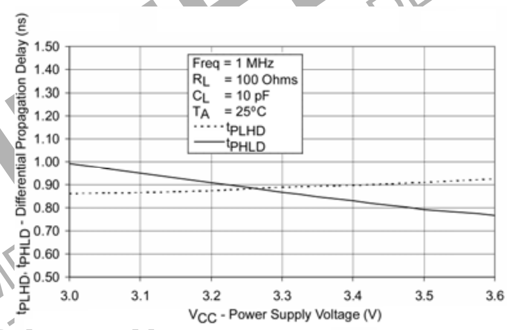


Figure 13. Differential Propagation Delay vs. Power Supply

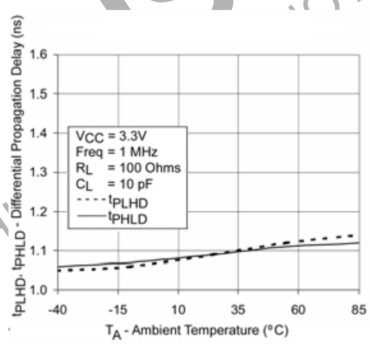


Figure 14. Differential Propagation Delay vs. Ambient Temperature

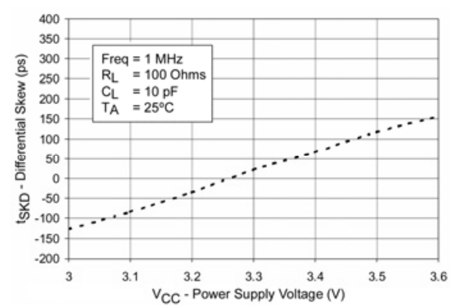


Figure 15. Differential Pulse Skew ($t_{PLH} - t_{PHL}$) vs. Power Supply Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

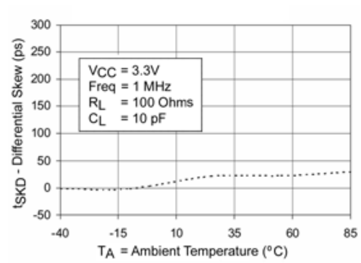


Figure 16. Differential Pulse Skew ($t_{PLH} - t_{PHL}$) vs. Ambient Temperature

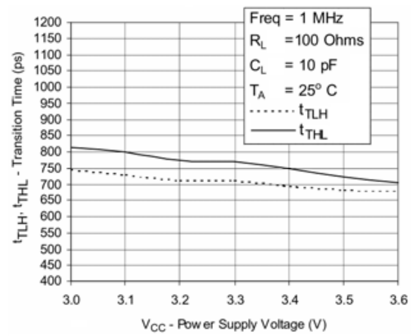


Figure 17. Transition Time vs. Power Supply Voltage

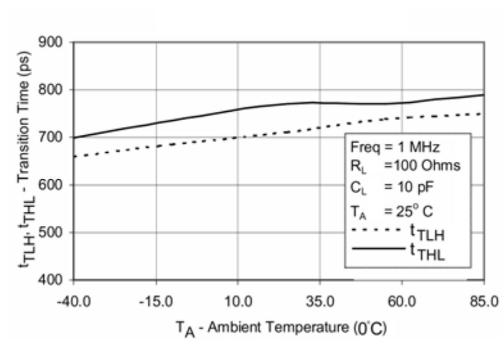


Figure 18. Transition Time vs. Ambient Temperature

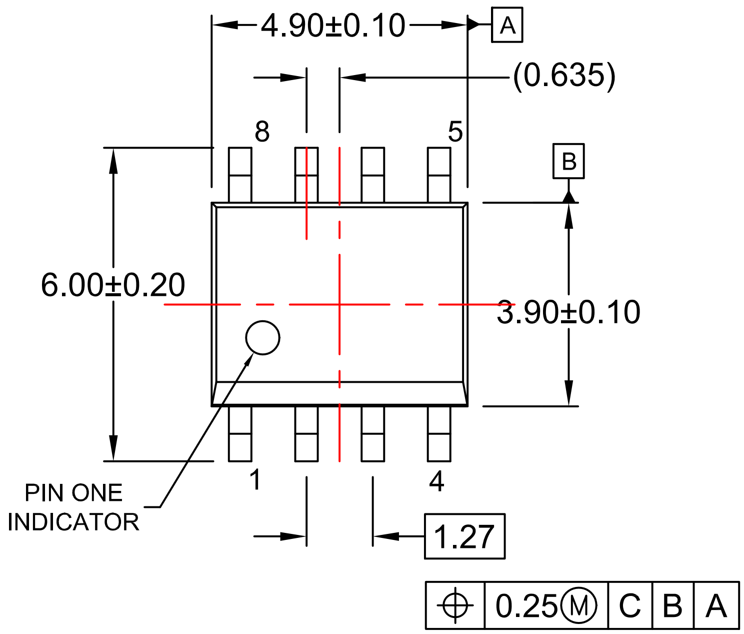
ORDERING INFORMATION

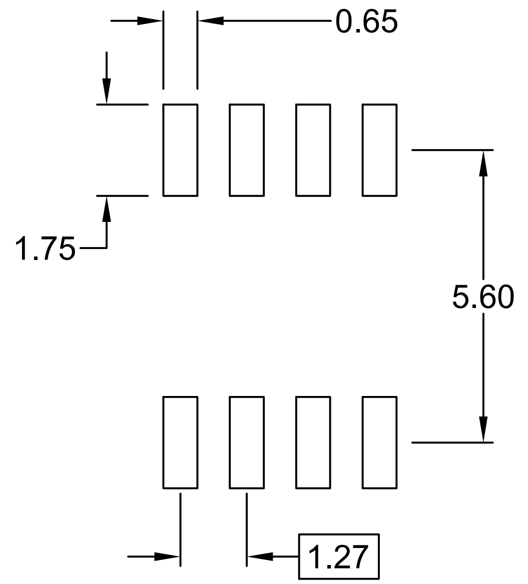
Part Number	Operating Range Temperature	Package	Shipping†
FIN1017MX	−40 to +85°C	8−Lead Small Outline Integrated Circuit (SOIC), JEDEC MS−012, 0.150 inch Narrow (Pb−Free, Halide Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

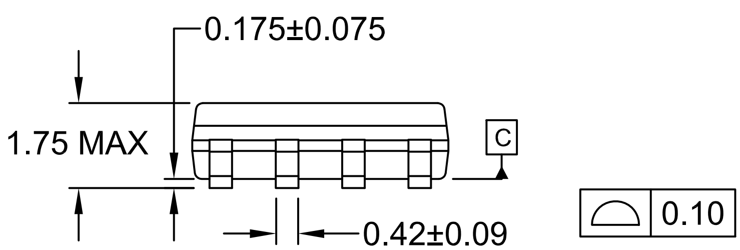
SOIC8
CASE 751EB
ISSUE A

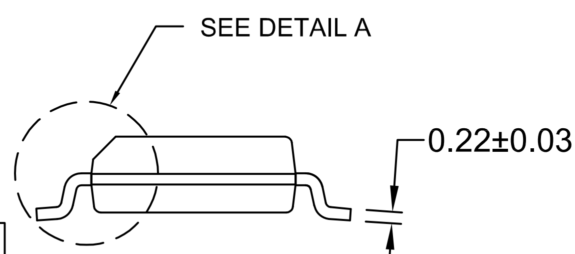
DATE 24 AUG 2017



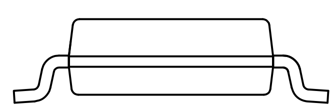


LAND PATTERN RECOMMENDATION

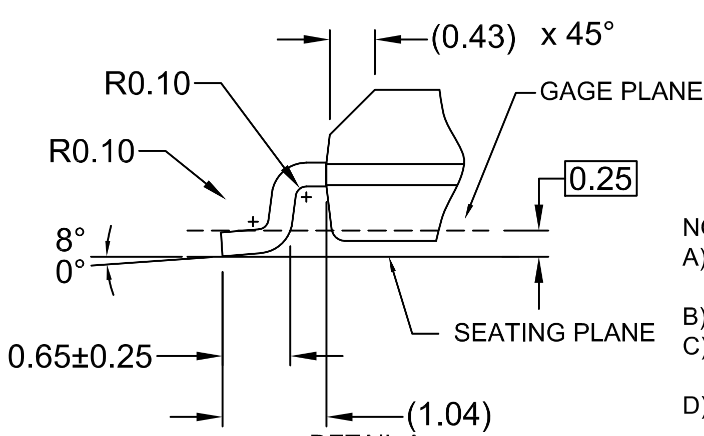




OPTION A - BEVEL EDGE



OPTION B - NO BEVEL EDGE



DETAIL A
SCALE: 2:1

NOTES:
A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M

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