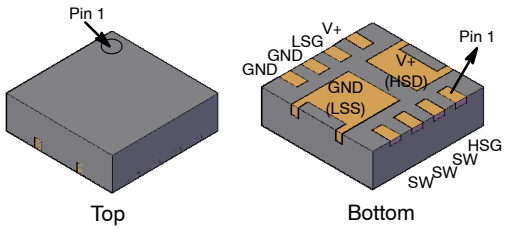
MOSFET – Dual, N-Channel, Asymmetric, Power Clip, POWERTRENCH®, 30 V

FDPC8013S



PQFN8 3.3 × 3.3, 0.65P
CASE 483AZ

General Description

This device includes two specialized N−Channel MOSFETs in a dual package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous SyncFET™ (Q2) have been designed to provide optimal power efficiency.

Features

Q1: N−Channel

- Max $R_{DS(on)}$ = 9.6 mΩ at V_{GS} = 4.5 V, I_D = 10 A

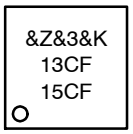
Q2: N−Channel

- Max $R_{DS(on)}$ = 2.7 mΩ at V_{GS} = 4.5 V, I_D = 22 A
- Low Inductance Packaging Shortens Rise/Fall Times, Resulting in Lower Switching Losses
- MOSFET Integration Enables Optimum Layout for Lower Circuit Inductance and Reduced Switch Node Ringing
- RoHS Compliant

Applications

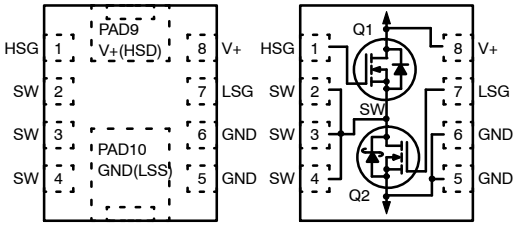
- Computing
- Communications
- General Purpose Point of Load

MARKING DIAGRAM



&Z	= Assembly Plant Code
&3	= 3−Digit Date Code
&K	= 2−Digits Lot Run Traceability Code
13CF15CF	= Device Code

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping†
FDPC8013S	PQFN8	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

MOSFET MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter		Q1	Q2	Unit
V_{DS}	Drain to Source Voltage		30	30	V
V_{GS}	Gate to Source Voltage		±20	±20	V
I_D	Drain Current	– Continuous (Package limited) T_C = 25°C	20	55	A
		– Continuous T_A = 25°C	13 (Note 1a)	26 (Note 1b)	
		– Pulsed	40	100	
E_{AS}	Single Pulse Avalanche Energy (Note 3)		21	97	mJ
P_D	Power Dissipation for Single Operation	T_A = 25°C	1.6 (Note 1a)	2.0 (Note 1b)	W
		T_A = 25°C	0.8 (Note 1c)	0.9 (Note 1d)	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		–55 to +150		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Characteristic	Value	Value	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	77 (Note 1a)	63 (Note 1b)	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	151 (Note 1c)	135 (Note 1d)	
$R_{\theta JC}$	Thermal Resistance, Junction to Case	5.0	3.5	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

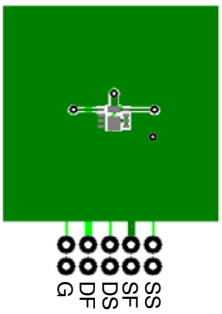
Symbol	Parameter	Test Condition	Type	Min	Typ	Max	Unit
OFF CHARACTERISTICS							
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V I_D = 1 mA, V_{GS} = 0 V	Q1 Q2	30 30	– –	– –	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C I_D = 10 mA, referenced to 25°C	Q1 Q2	– –	16 20	– –	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V V_{DS} = 24 V, V_{GS} = 0 V	Q1 Q2	– –	– –	1 500	μA μA
I_{GSS}	Gate to Source Leakage Current, Forward	V_{GS} = 20 V, V_{DS} = 0 V V_{GS} = 20 V, V_{DS} = 0 V	Q1 Q2	– –	– –	100 100	nA nA
ON CHARACTERISTICS							
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA V_{GS} = V_{DS}, I_D = 1 mA	Q1 Q2	1.2 1.2	1.5 1.7	3.0 3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C I_D = 10 mA, referenced to 25°C	Q1 Q2	– –	–5 –6	– –	mV/°C
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 10 V, I_D = 13 A V_{GS} = 4.5 V, I_D = 10 A V_{GS} = 10 V, I_D = 13 A, T_J = 125°C	Q1	– – –	4.6 6.7 6.6	6.4 9.6 9.2	mΩ
		V_{GS} = 10 V, I_D = 26 A V_{GS} = 4.5 V, I_D = 22 A V_{GS} = 10 V, I_D = 26 A ,T_J = 125°C	Q2	– –	1.4 2.0 1.9	1.9 2.7 2.6	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 13 A V_{DS} = 5 V, I_D = 26 A	Q1 Q2	– –	53 168	– –	S
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	Q1: V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	Q1 Q2	– –	827 2785	– –	pF
C_{oss}	Output Capacitance	Q2: V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	Q1 Q2	– –	333 997	– –	pF
C_{rss}	Reverse Transfer Capacitance		Q1 Q2	– –	44 128	– –	pF
R_g	Gate Resistance		Q1 Q2	– –	0.5 0.5	– –	Ω

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

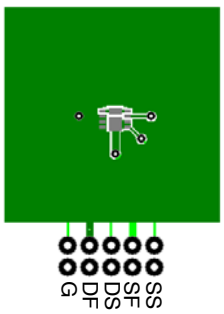
Symbol	Parameter	Test Condition		Type	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS								
$t_{d(on)}$	Turn−On Delay Time	Q1: V_{DD} = 15 V, I_D = 13 A, R_{GEN} = 6 Ω Q2: V_{DD} = 15 V, I_D = 26 A, R_{GEN} = 6 Ω		Q1 Q2	– –	6 11	– –	ns
t_r	Rise Time			Q1 Q2	– –	2 5	– –	ns
$t_{d(off)}$	Turn−Off Delay Time			Q1 Q2	– –	16 30	– –	ns
t_f	Fall Time			Q1 Q2	– –	2 4	– –	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V	Q1 V_{DD} = 15 V, I_D = 13 A Q2 V_{DD} = 15 V, I_D = 26 A	Q1 Q2	– –	13 44	– –	nC
		V_{GS} = 0 V to 4.5 V		Q1 Q2	– –	6 21	– –	nC
Q_{gs}	Gate to Source Gate Charge			Q1 Q2	– –	2.2 7.2	– –	nC
Q_{gd}	Gate to Drain “Miller” Charge			Q1 Q2	– –	1.9 6.6	– –	nC
DRAIN−SOURCE DIODE CHARACTERISTICS								
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 13 A (Note 2) V_{GS} = 0 V, I_S = 26 A (Note 2)		Q1 Q2	– –	0.80 0.77	1.2 1.2	V
t_{rr}	Reverse Recovery Time	Q1: I_F = 13 A, di/dt = 100 A/μs Q2: I_F = 26 A, di/dt = 300 A/μs		Q1 Q2	– –	22 29	– –	ns
Q_{rr}	Reverse Recovery Charge			Q1 Q2	– –	7 30	– –	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

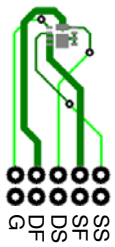
1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user’s board design.



a. 77°C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 63°C/W when mounted on a 1 in^2 pad of 2 oz copper



c. 151°C/W when mounted on a minimum pad of 2 oz copper

d. 135°C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. Q1: E_{AS} of 21 mJ is based on starting T_J = 25°C; N−ch: L = 1.2 mH, I_{AS} = 6 A, V_{DD} = 23 V, V_{GS} = 10 V. 100% test at L= 0.1 mH, I_{AS} = 14.5 A.
   Q2: E_{AS} of 97 mJ is based on starting T_J = 25°C; N−ch: L = 0.6 mH, I_{AS} = 18 A, V_{DD} = 23 V, V_{GS} = 10 V. 100% test at L= 0.1 mH, I_{AS} = 32.9 A.
4. As an N−ch device, the negative V_{gs} rating is for low duty cycle pulse occurence only. No continuous rating is implied.

TYPICAL CHARACTERISTICS (Q1 N−CHANNEL) (T_J = 25°C unless otherwise noted)

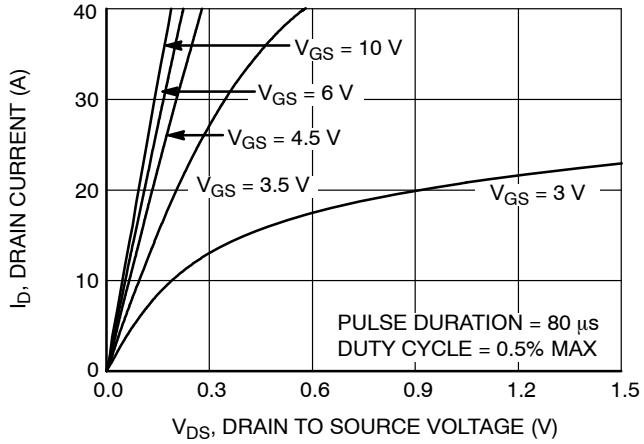


Figure 1. On−Region Characteristics

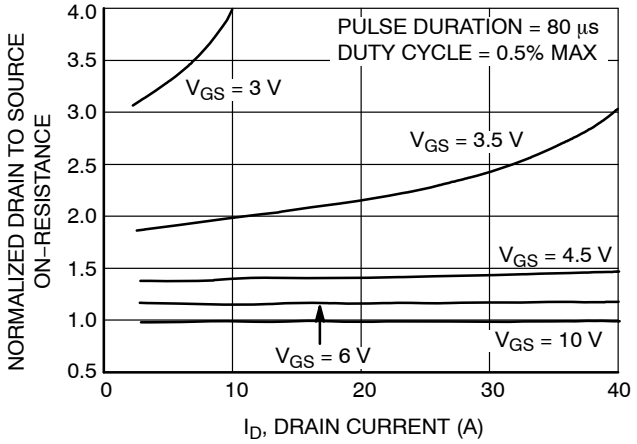


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

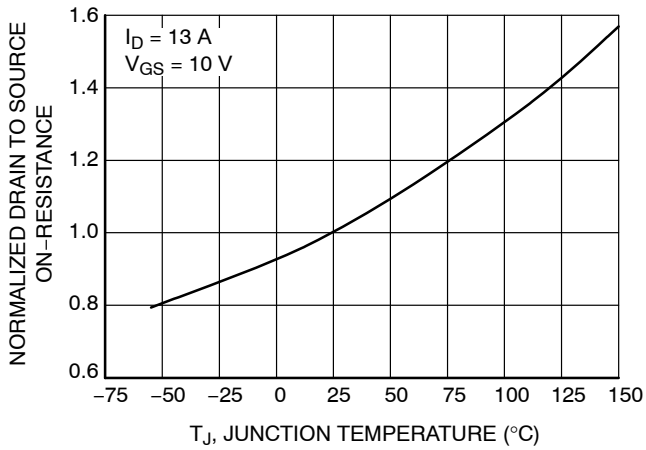


Figure 3. Normalized On−Resistance vs. Junction Temperature

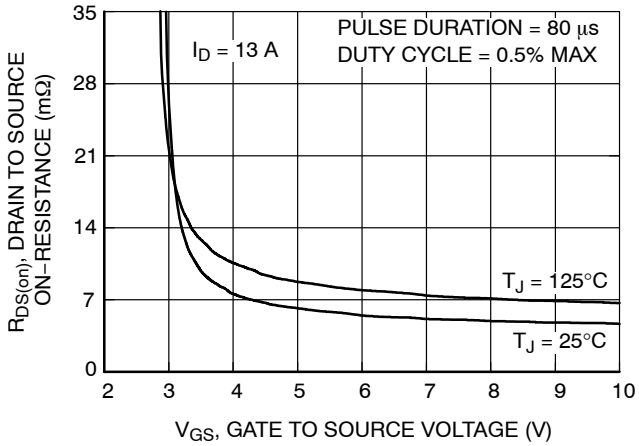


Figure 4. On−Resistance vs. Gate to Source Voltage

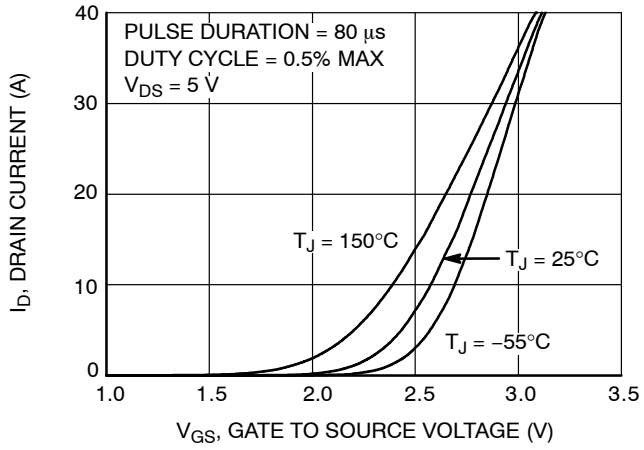


Figure 5. Transfer Characteristics

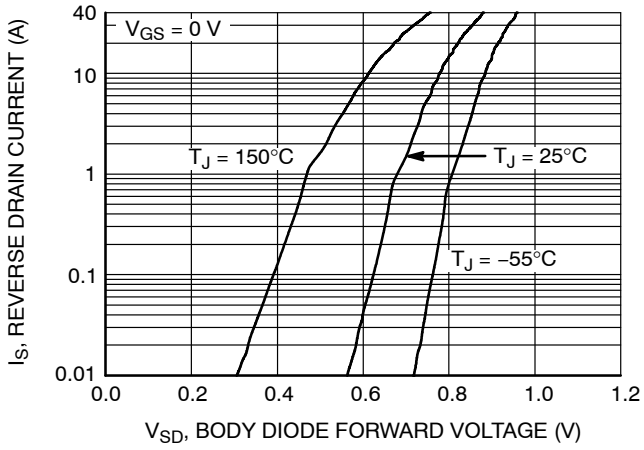


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (Q1 N−CHANNEL) (T_J = 25°C unless otherwise noted) (continued)

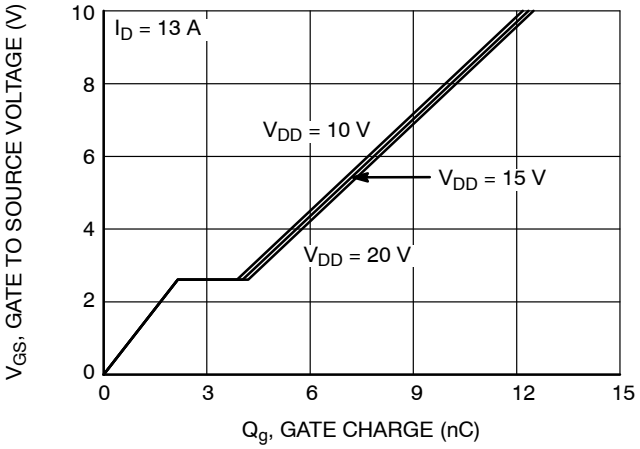


Figure 7. Gate Charge Characteristics

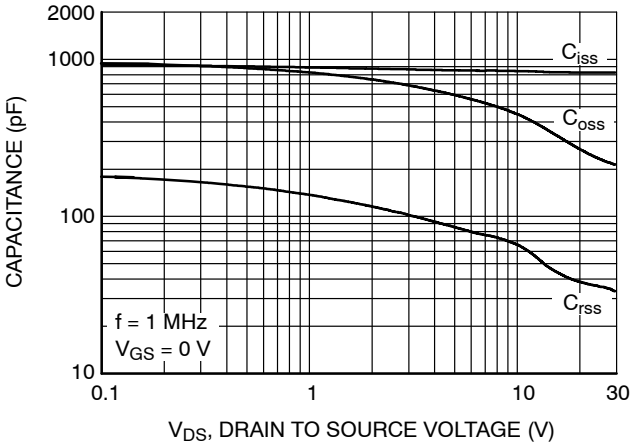


Figure 8. Capacitance vs. Drain to Source Voltage

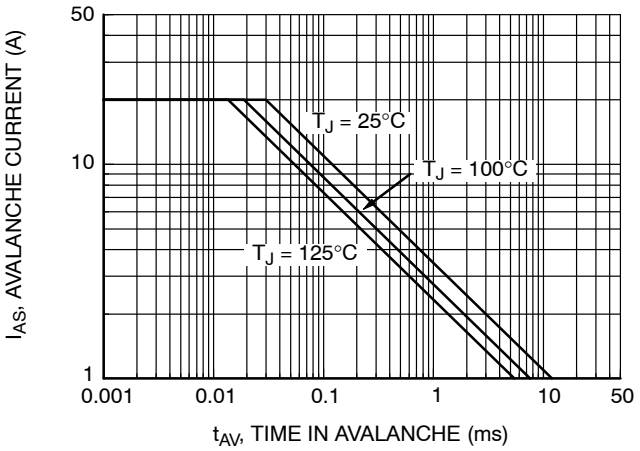


Figure 9. Unclamped Inductive Switching Capability

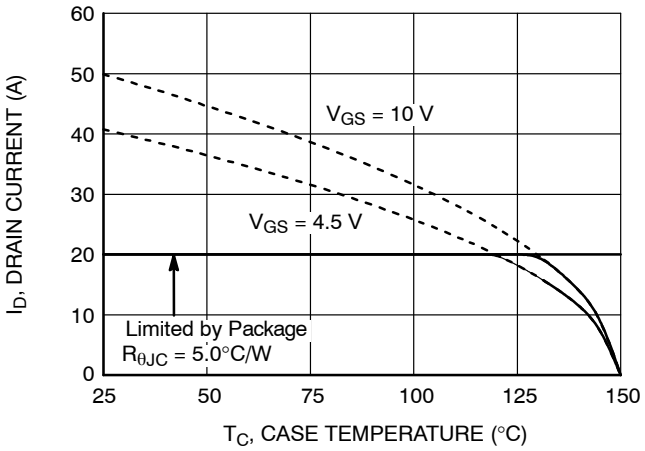


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

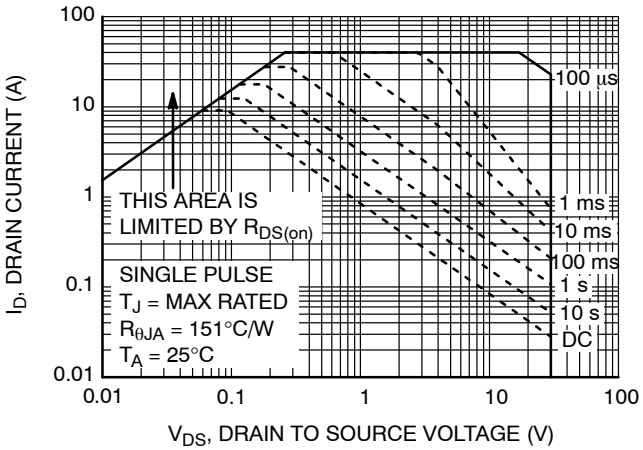


Figure 11. Forward Bias Safe Operating Area

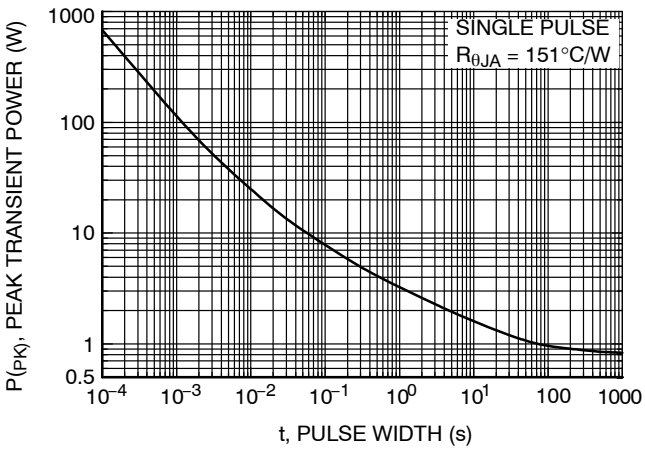


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (Q1 N−CHANNEL) (T_J = 25°C unless otherwise noted) (continued)

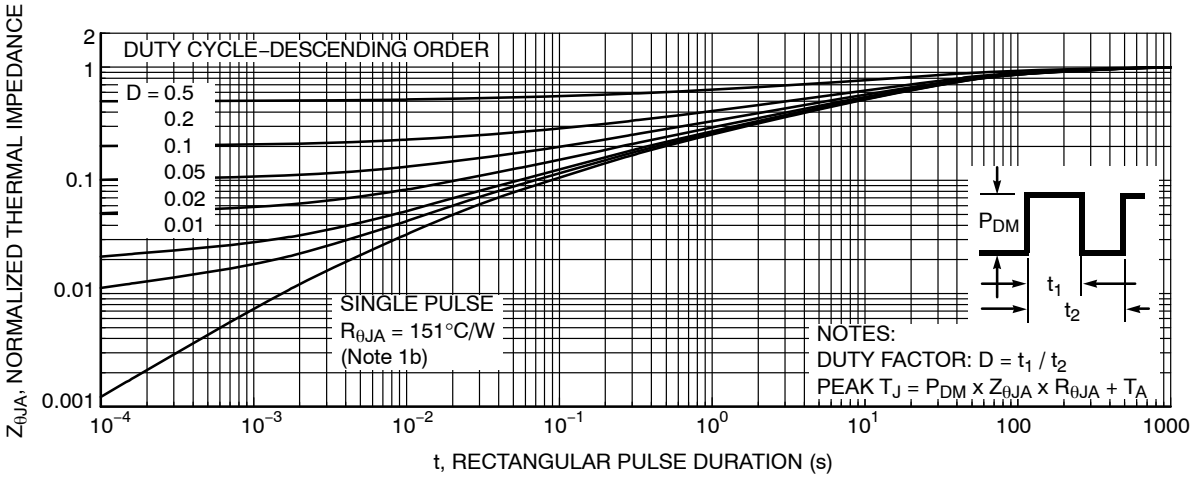


Figure 13. Junction−to−Ambient Transient Thermal Response Curve

TYPICAL CHARACTERISTICS (Q2 N−CHANNEL) (T_J = 25°C unless otherwise noted)

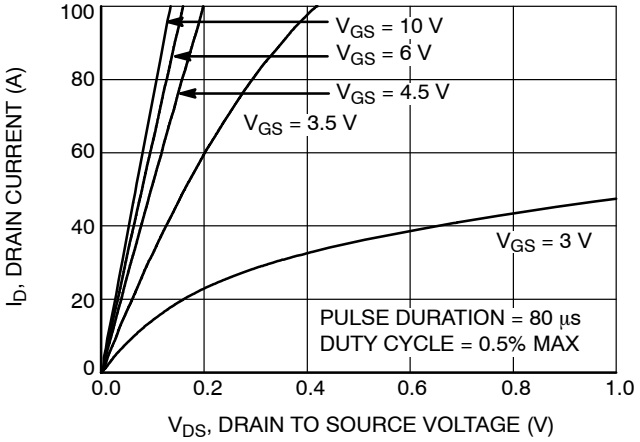


Figure 14. On−Region Characteristics

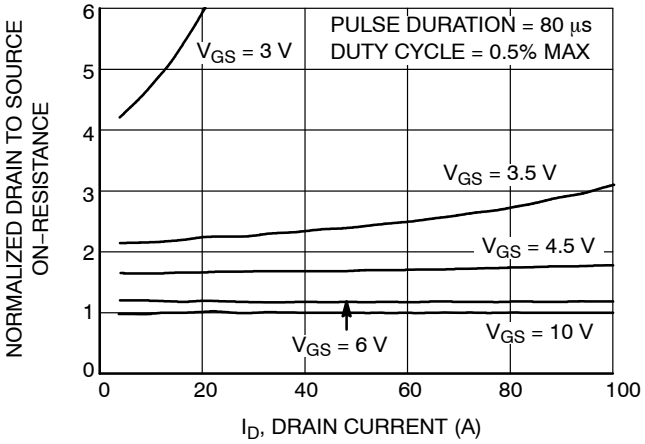


Figure 15. Normalized On−Resistance vs. Drain Current and Gate Voltage

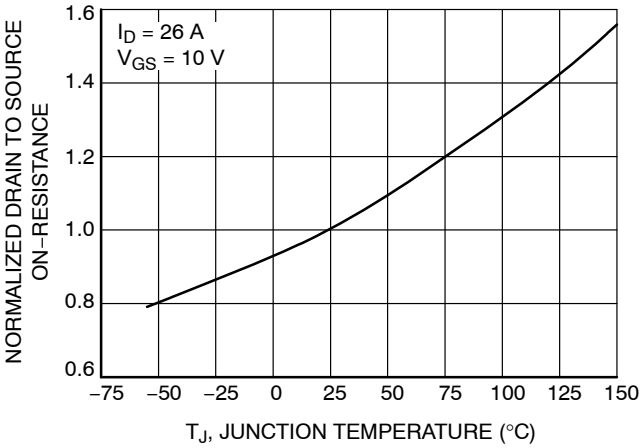


Figure 16. Normalized On−Resistance vs. Junction Temperature

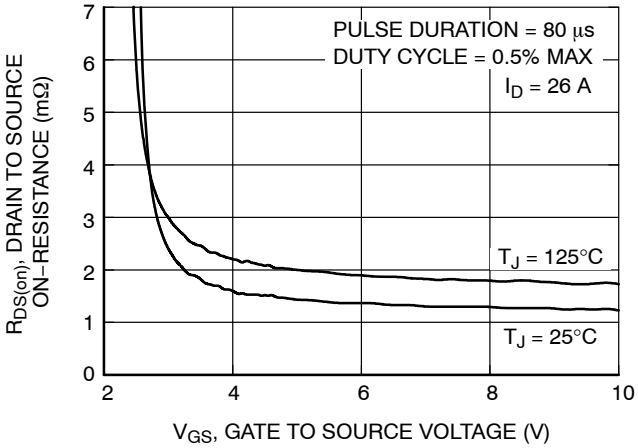


Figure 17. On−Resistance vs. Gate to Source Voltage

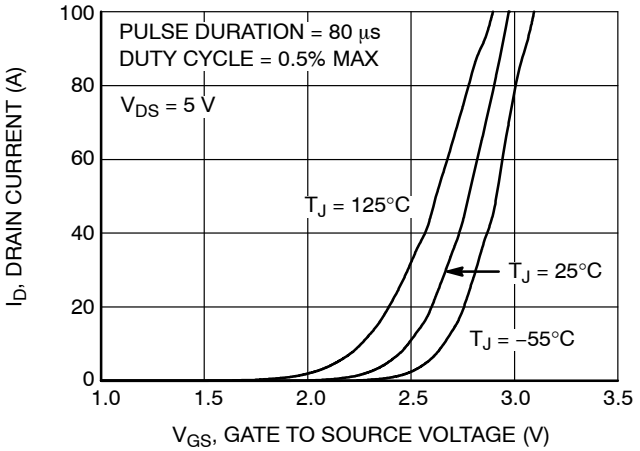


Figure 18. Transfer Characteristics

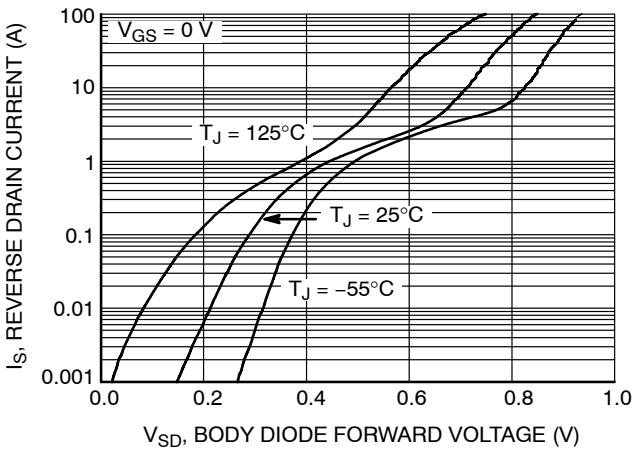


Figure 19. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (Q2 N−CHANNEL) (T_J = 25°C unless otherwise noted) (continued)

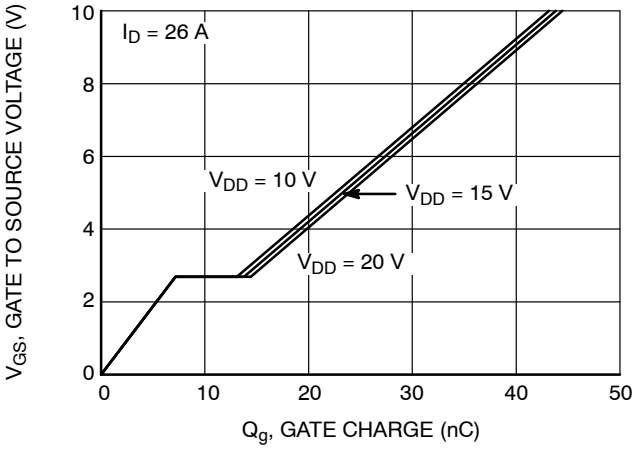


Figure 20. Gate Charge Characteristics

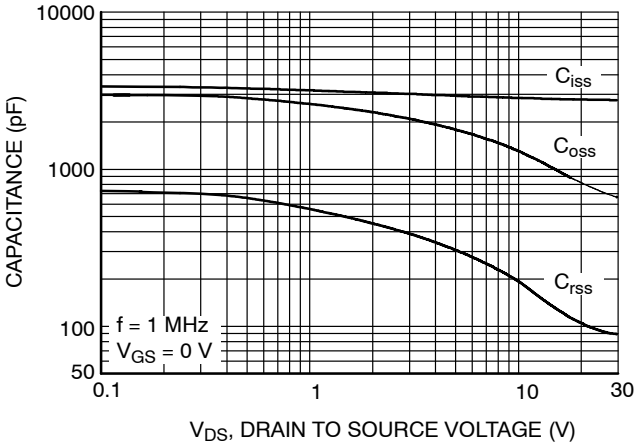


Figure 21. Capacitance vs. Drain to Source Voltage

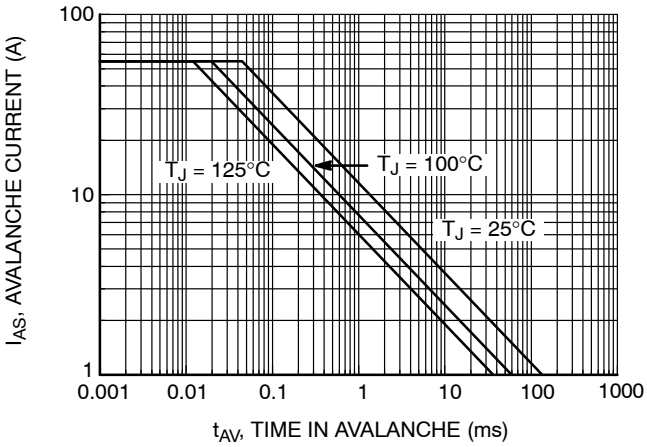


Figure 22. Unclamped Inductive Switching Capability

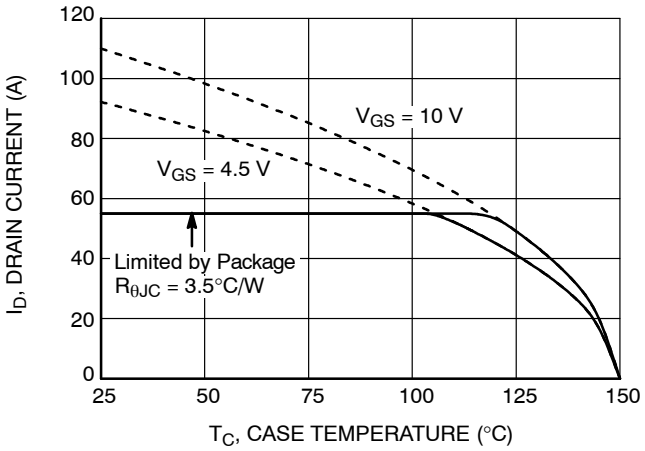


Figure 23. Maximum Continuous Drain Current vs. Ambient Temperature

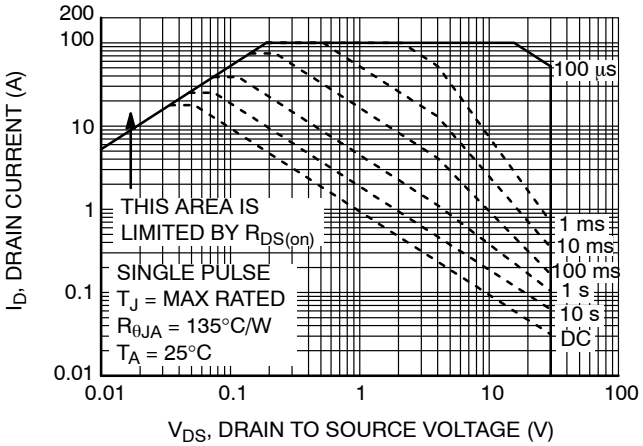


Figure 24. Forward Bias Safe Operating Area

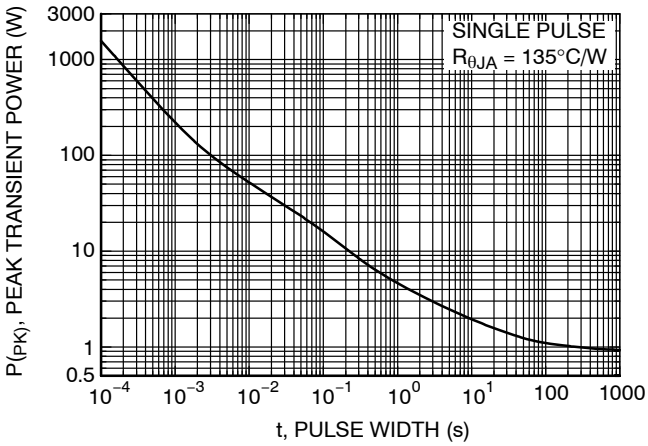


Figure 25. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (Q2 N−CHANNEL) (T_J = 25°C unless otherwise noted) (continued)

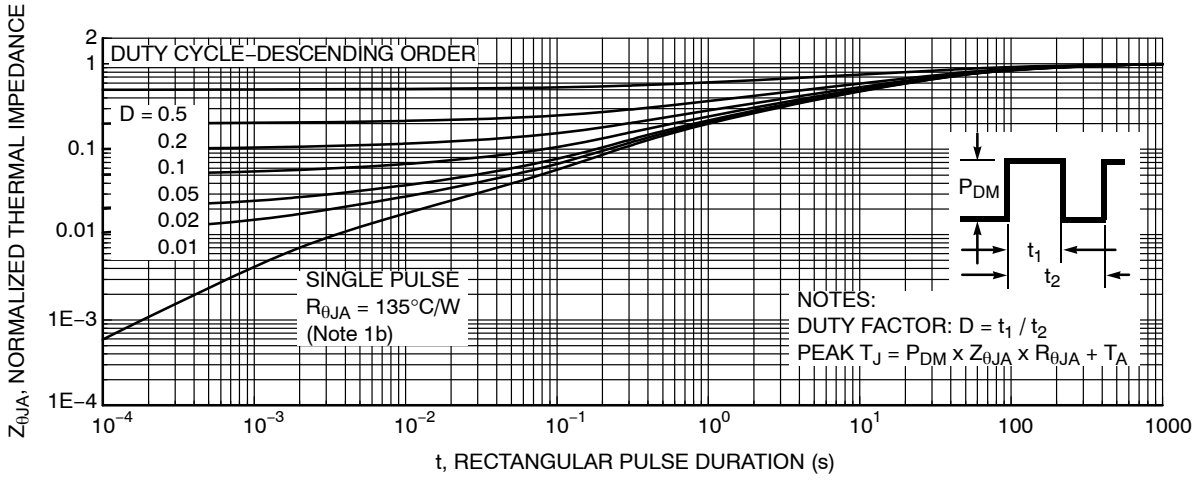


Figure 26. Junction−to−Ambient Transient Thermal Response Curve

TYPICAL CHARACTERISTICS (continued)

SyncFET Schottky Body Diode Characteristics

onsemi's SyncFET process embeds a Schottky diode in parallel with POWERTRENCH MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 27 shows the reverse recovery characteristic of the FDPC8013S.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

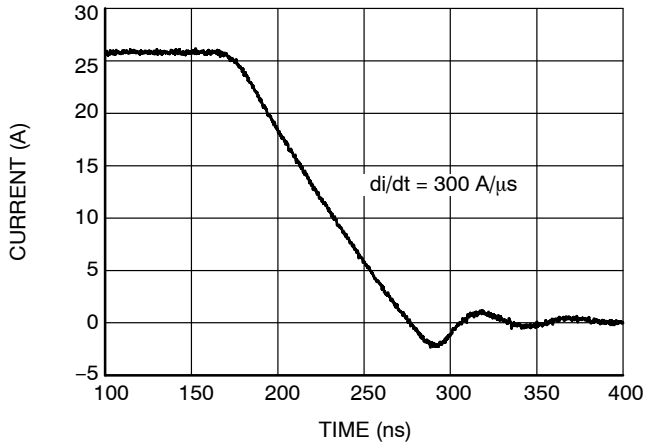


Figure 27. FDPC8013S SyncFET Body Diode Reverse Recovery Characteristics

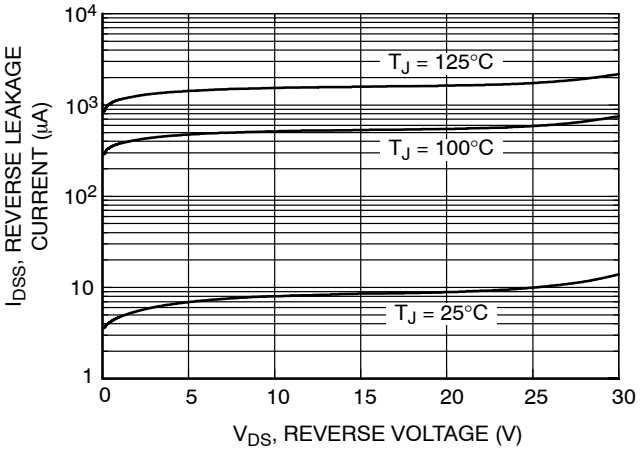
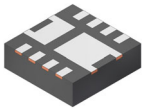
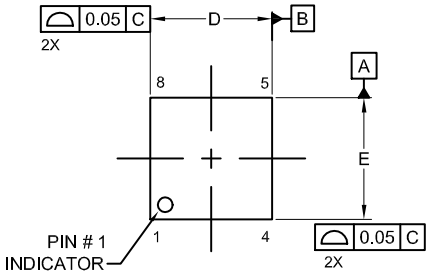


Figure 28. SyncFET Body Diode Reverse Leakage vs. Drain−Source Voltage

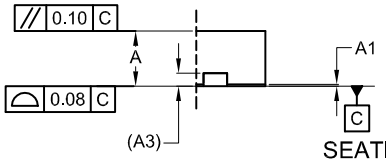


PQFN8 3.3X3.3, 0.65P
CASE 483AZ
ISSUE B

DATE 14 FEB 2022



TOP VIEW

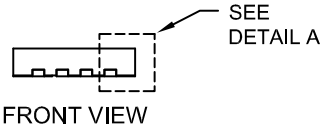


DETAIL 'A'
SCALE 2:1

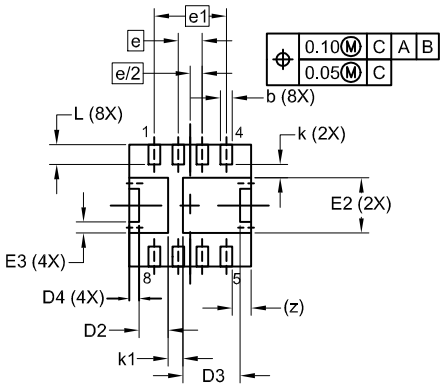
SEATING PLANE

NOTES:

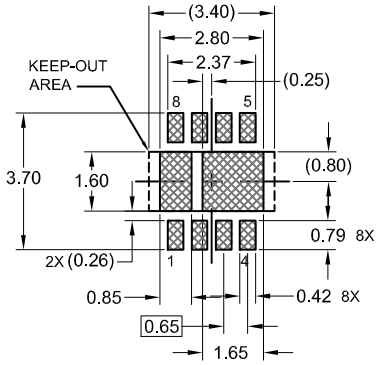
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS DO NOT INCLUDE BURSS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.



FRONT VIEW



BOTTOM VIEW



LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	--	0.05
A3		0.20 REF	
b	0.27	0.32	0.37
D	3.20	3.30	3.40
D2	0.69	0.79	0.89
D3	1.45	1.55	1.65
D4	0.16	0.26	0.36
E	3.20	3.30	3.40
E2	1.40	1.50	1.60
E3		0.30 REF	
e		0.65 BSC	
e1		1.95 BSC	
e/2		0.325 BSC	
k		0.36 REF	
k1		0.40 REF	
L	0.44	0.54	0.64
z		0.52 REF	

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DESCRIPTION:	**PQFN8 3.3X3.3, 0.65P**		**PAGE 1 OF 1**

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