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STK682-010-E

Thick Film Hybrid IC

2-phase Stepping Motor Driver

Overview

The STK682-010-E is a hybrid IC for use as a Bipolar, 2-phase stepping motor driver with PWM current control.

Function

- Output on-resistance (High side 0.3 Ω , Low side 0.25 Ω , Total 0.55 Ω ; Ta = 25°C, I_O = 2.5A)
- VMmax=36V(DC), Iopmax=3.0A
- 2, 1-2, W1-2, 2W1-2, 4W1-2, 8W1-2, 16W1-2, 32W1-2 phase excitation are selectable
- With built-in automatic half current maintenance energizing function
- Over current protection circuit
- Thermal shutdown circuit
- Input pull down resistance
- With reset pin and enable pin

Specifications

Absolute Maximum Ratings at Tc = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	VMmax		36.0	V
Peak output current	Iopmax		3.0	A
Logic input voltage	VINmax		6.0	V
VREF input voltage	VREFmax		6.0	V
Operating substrate temperature	Tc		-20 to +105	°C
Storage temperature	Tstg		-40 to +125	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

ORDERING INFORMATION

See detailed ordering and shipping information on page 20 of this data sheet.

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Recommended Operating Conditions at $T_c = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range	VM		9.0 to 32.0	V
Logic input voltage range	VIN		0 to 5.0	V
VCC input voltage range	VCC		0 to 5.0	V
VREF input voltage range	VREF		0 to 3.0	V
Output current1	Io1	1-2 Phase-ex, $T_c \leq 90^\circ\text{C}$	3.0	A
Output current2	Io2	1-2 Phase-ex, $T_c=105^\circ\text{C}$	2.5	A
Output current3	Io3	2 Phase-ex, $T_c=105^\circ\text{C}$	1.8	A

Electrical Characteristics at $T_c = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$

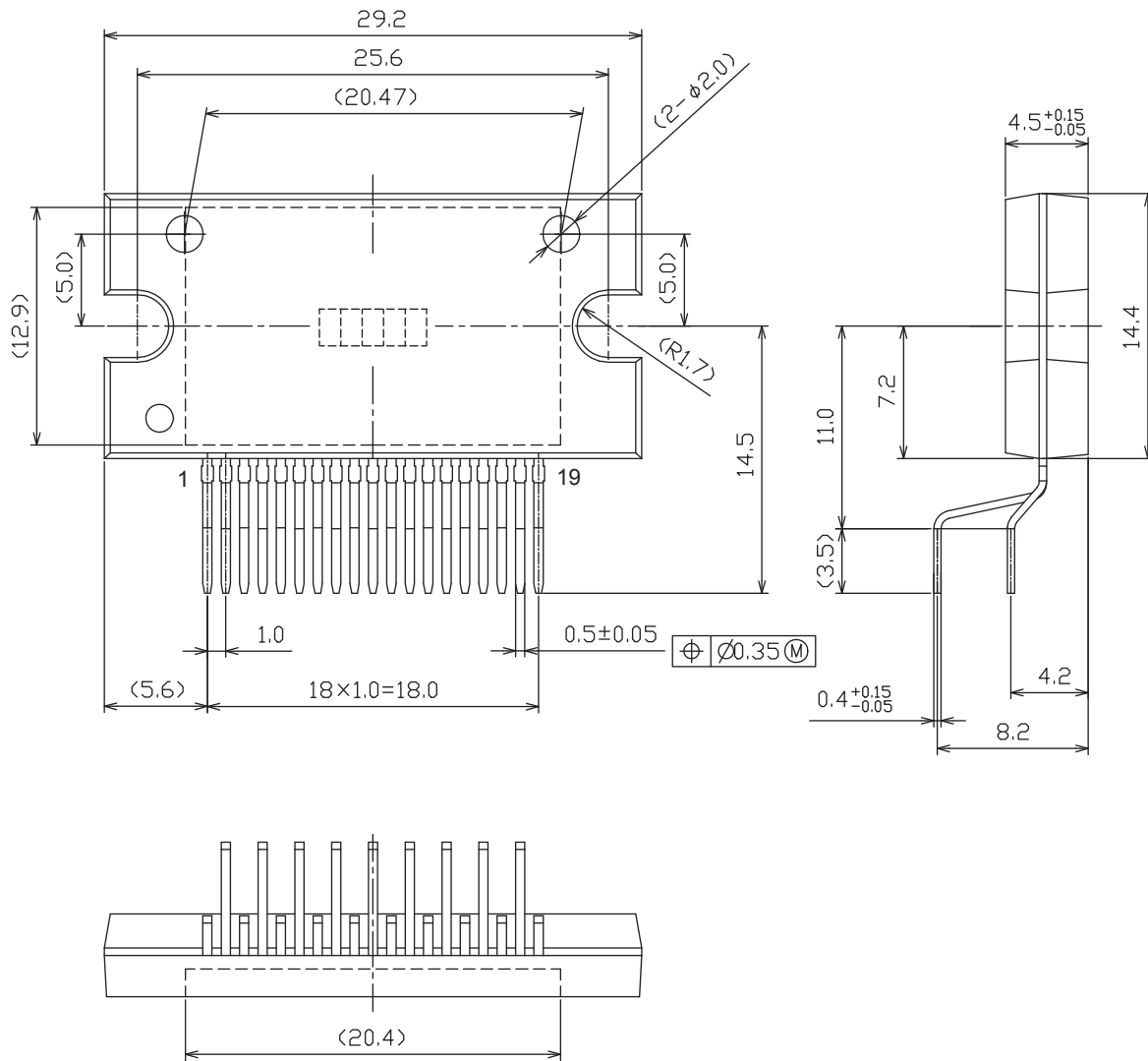
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Standby mode current drain	IMstn	VCC="L"		70	100	μA
Current drain	IM	VCC="H", ENABLE="H" No Load		3.3	4.6	mA
Thermal shutdown temperature	TSD	Design guarantee	150	180	210	$^\circ\text{C}$
Thermal hysteresis width	ΔTSD	Design guarantee		40		$^\circ\text{C}$
Logic pin input current	linL1	VIN=0.8V	3	8	15	μA
	linH1	VIN=5V	30	50	70	μA
VCC pin input current	VCC	15pin=5V	51	83	115	μA
Logic input high-level voltage	Vinh	Pins 2,3,16,17,18,19	2.0			V
Logic input low-level voltage	Vinl	Pins 2,3,16,17,18,19			0.8	V
FDT pin high-level voltage	Vfdth	Pin 6	3.5			V
FDT pin middle-level voltage	Vfdtm	Pin 6	1.1		3.1	V
FDT pin low-level voltage	Vfdtl	Pin 6			0.8	V
Chopping frequency	Fch	C1=100pF	58	83	108	kHz
Chopping frequency	Iosc1			10		μA
Chopping oscillator circuit threshold voltage	Vtup1			1		V
	Vtdown1			0.5		V
VREF pin input voltage	Iref	VREF=1.5V, CLK=10kHz	-0.5			μA
DOWN output residual voltage	VoIDO	I _{down} =1mA, CLK=Low		40		mV
Hold current switching frequency	Falert			1.6		Hz
Blanking time	Tb1			1		μs
Output block						
Output on-resistance	Ronu	I _O =2.0A, high-side ON resistance		0.30	0.42	Ω
	Rond	I _O =2.0A, low-side ON resistance		0.25	0.35	Ω
Output leakage current	Ioleak	VM=36V			50	μA
Diode forward voltage	VD	ID=-2.0A		1.1	1.4	V
Current setting reference voltage	VRF	VREF=1.5V, Current ratio 100%		300		mV
Output short-circuit protection block						
Timer latch time	Tscp			256		μs

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Package Dimensions

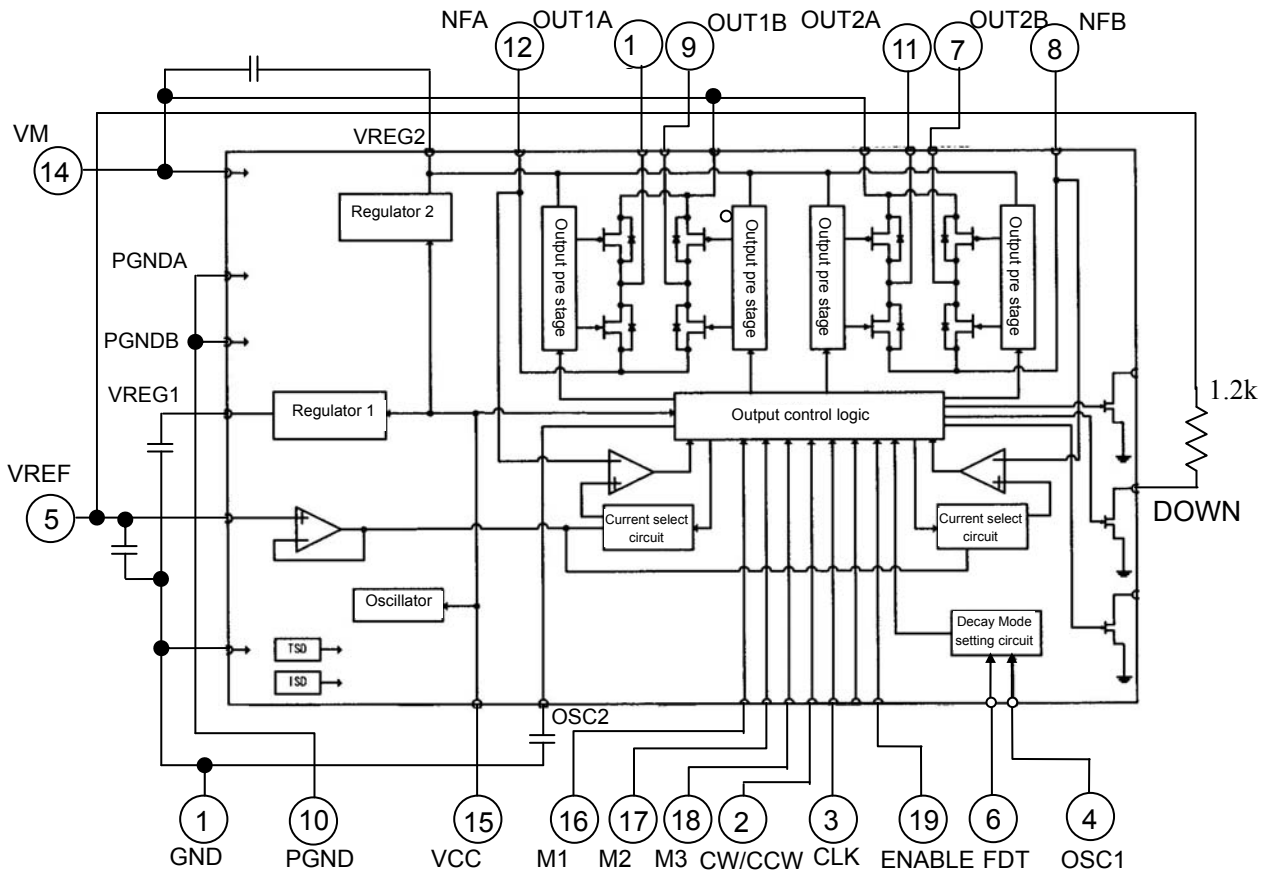
unit : mm

SIP19 29.2x14.4
CASE 127CF
ISSUE 0

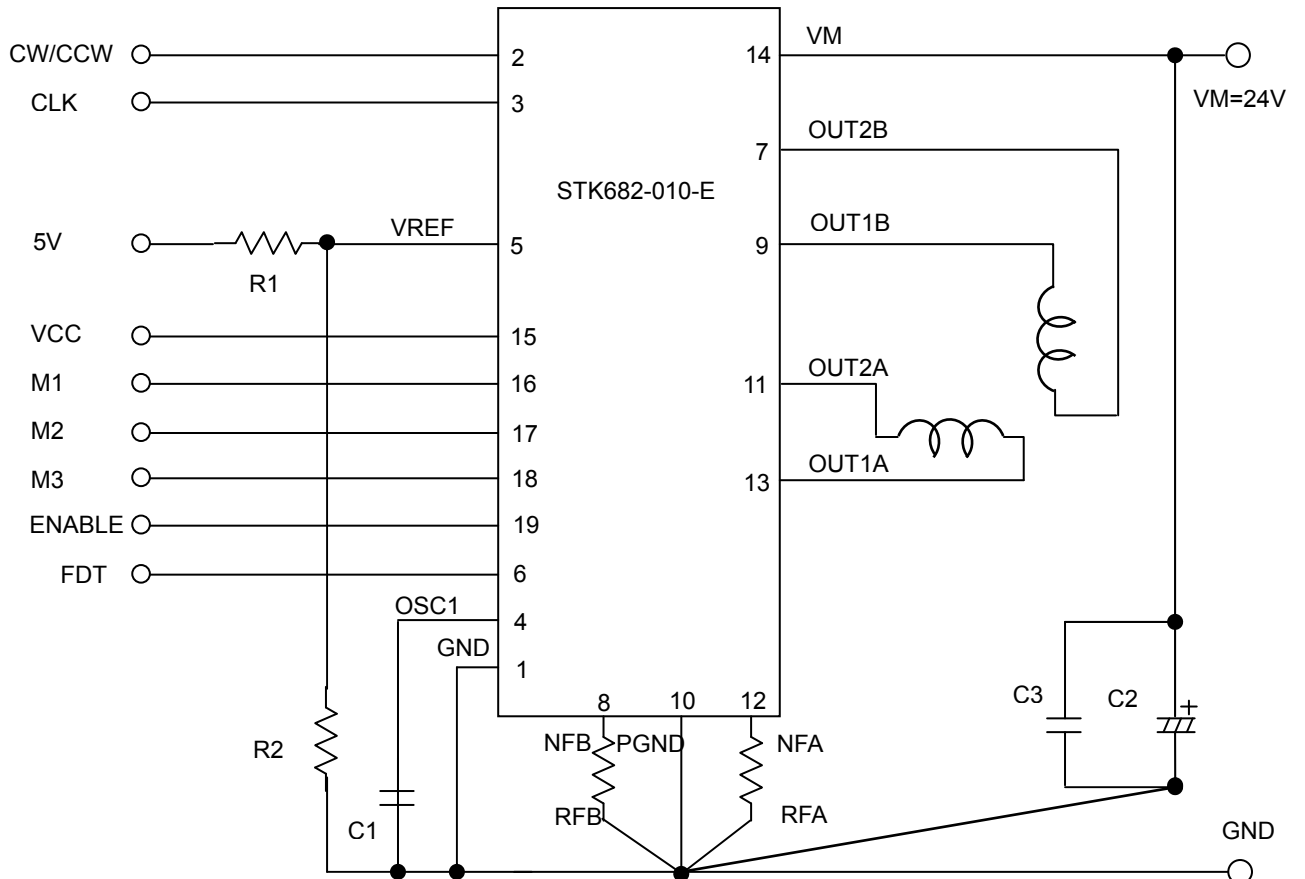


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Block diagram



Application Circuit Example



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Pin Functions

Pin No.	Pin symbol	Pin Functions
1	GND	Circuit GND
2	CW/CCW	Forward / Reverse signal input
3	CLK	Clock pulse signal input
4	OSC1	Chopping frequency setting capacitor connection
5	VREF	Constant-current control reference voltage input
6	FDT	Decay mode select voltage input
7	OUT2B	B phase OUTB output
8	NFB	B phase current sense resistance connection
9	OUT1B	B phase OUTA output
10	PGND	Power GND
11	OUT2A	A phase OUTB output
12	NFA	A phase current sense resistance connection
13	OUT1A	A phase OUTA output
14	VM	Motor supply connection
15	VCC	Chip enable input
16	M1	Excitation-mode switching pin
17	M2	
18	M3	
19	ENABLE	Output enable signal input

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Equivalent circuit diagram

Pin No.	Pin type	Equivalent Circuit Diagram
3 2 19 18 17 16	CLK CW/CCW ENABLE M3 M2 M1	
15	VCC	<p>Internal reset Input pin</p>
13 10 14 12 11 9 8 7	OUT1A PGND VM NFA OUT2A OUT1B NFB OUT2B	
5	VREF	
4	OSC1	
6	FDT	

Description of functions

(1) Excitation setting method

Set the excitation setting as shown in the following table by setting M1 pin, M2 pin and M3 pin

Input signal			MODE (Excitation)	Initial position	
M3	M2	M1		A phase current	B phase current
L	L	L	2 Phase	100%	-100%
L	L	H	1-2 Phase	100%	0%
L	H	L	W1-2 Phase	100%	0%
L	H	H	2W1-2 Phase	100%	0%
H	L	L	4W1-2 Phase	100%	0%
H	L	H	8W1-2 Phase	100%	0%
H	H	L	16W1-2 Phase	100%	0%
H	H	H	32W1-2 Phase	100%	0%

The initial position is also the default state at start-up and excitation position at counter-reset in each excitation mode

(2) Output current setting

Output current is set as shown below by the VREF pin (applied voltage) and a resistance value between NFA (B) pin and GND.

$$I_{OUT} = (VREF / 5) / \text{NFA (B) resistance}$$

* The setting value above is a 100% output current in each excitation mode.

(Example) When VREF=1.5V and NFA (B) resistance is 0.3 Ω, the setting current is shown below.

$$I_{OUT} = (1.5 \text{ V} / 5) / 0.3 \Omega = 1.0 \text{ A}$$



(3) Chip enable terminal/ VCC function

When Chip enable terminal/ VCC pin is at low levels, the IC enters stand-by mode, all logic is reset and output is turned OFF.

When Chip enable terminal/ VCC pin is at high levels, the stand-by mode is released

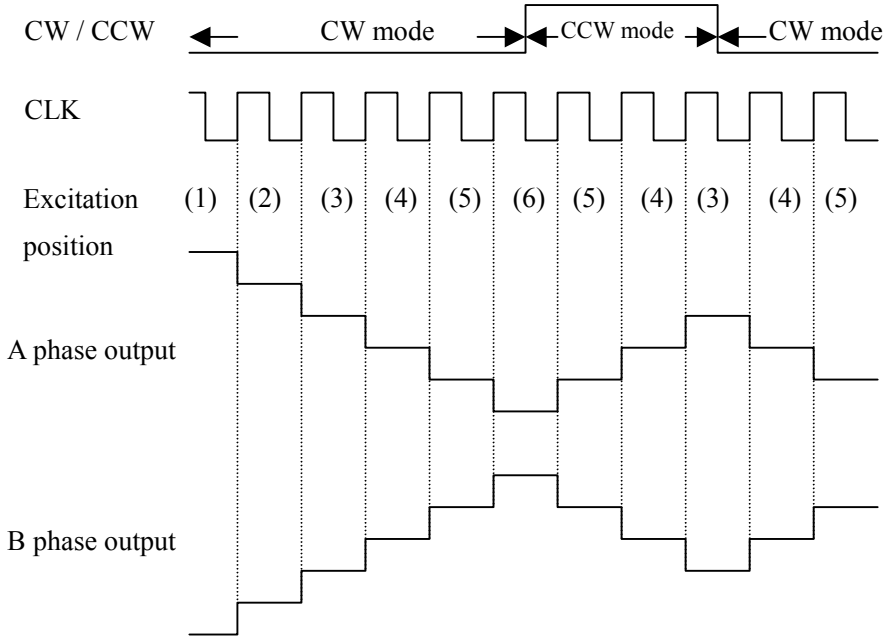
(4) Step pin function

CLK pin step signal input allows advancing excitation step

Input		Operation
VCC	CLK	
L	*	Stand-by mode
H		Excitation step feed
H		Excitation step hold

(5) Forward / reverse switching function

CW/CCW	Operation
L	CW
H	CCW

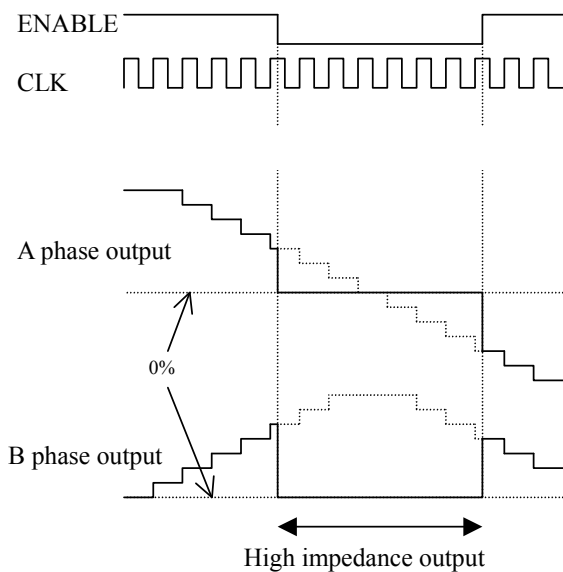


The internal D/A converter proceeds by a bit on the rising edge of the step signal input to the CLK pin. In addition, CW and CCW mode are switched by CW and CCW pin setting.

In CW mode, the B phase current is delayed by 90° relative to the A phase current. In CCW mode, the B phase current is advanced by 90° relative to the A phase current.

(6) Output enable function

When the ENABLE pin is set Low, the output is forced OFF and goes to high impedance. However, the internal logic circuits are operating, so the excitation position proceeds when the CLK is input. Therefore, when ENABLE pin is returned to High, the output level conforms to the excitation position proceeded by the CLK input.



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(7) DECAY mode

The DECAY mode of the output current becomes only MIXED DECAY.

FDT voltage	DECAY method
3.5V to	SLOW DECAY
1.1V to 3.1V or OPEN	MIXED DECAY
to 0.8V	FAST DECAY

(8) Chopping frequency setting function

Chopping frequency is set as shown below by a capacitor between OSC1 pin and GND.

$$F_{ch} = 1 / (C1 + 20pF / 10 \times 10^{-6}) \text{ (Hz)}$$

(Example) When $C_{osc1} = 100pF$, the chopping frequency is shown below.

$$F_{ch} = 1 / ((20 + 100) \times 10^{-12} / 10 \times 10^{-6}) \text{ (Hz)} = 83.3 \text{ (kHz)}$$

Note

- The 20pF is a stray capacitance which is involved by the package of STK682-010-E.

(9) Output short-circuit protection circuit

Build-in output short-circuit protection circuit makes output to enter in stand-by mode. This function prevents the IC from damaging when the output shorts circuit by a voltage short or a ground short, etc. When output short state is detected, short-circuit detection circuit starts the operating and output is once turned OFF. After the timer latch time (typ : 256 μ s), output is turned ON again. Still the output is at short state, the output is turned OFF and fixed in stand-by mode.

When output is fixed in stand-by mode by output short protection circuit, output is released the latch by setting Chip enable terminal/ $V_{CC} = "L"$

(10) Internal DOWN pin

The DOWN pin is an open drain connection.

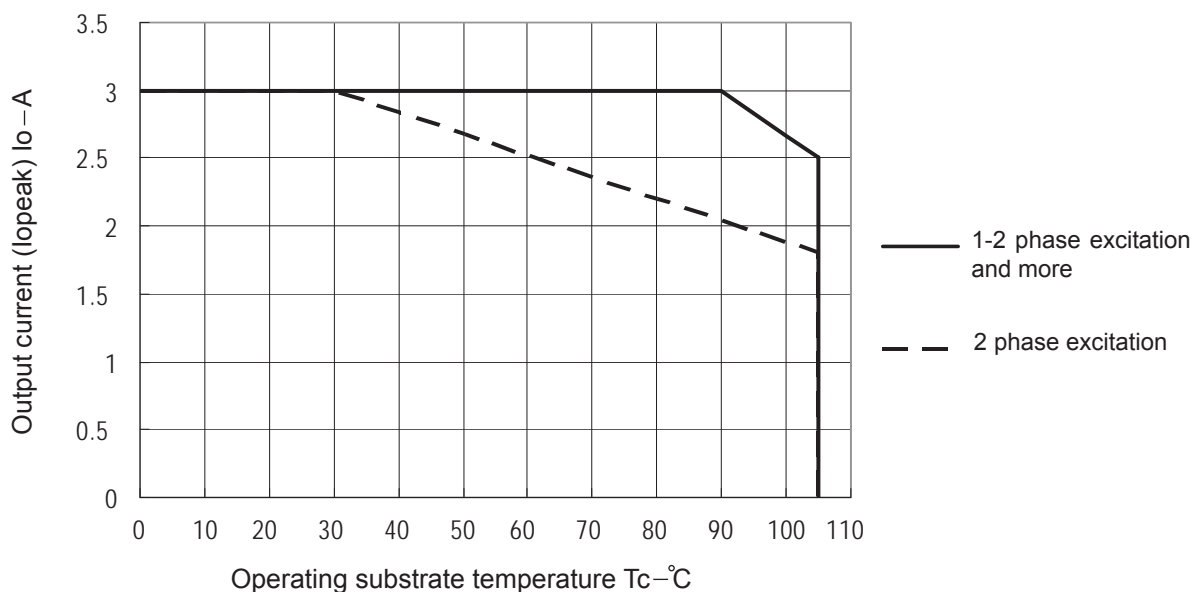
This pin is turned ON when no rising edge of CLK between the input signals while a period determined by a capacitor between OSC2 and GND, and outputs at low levels.

The DOWN pin output in once turned ON, is turned OFF at the next rising edge of CLK.

Holding current switching time (0.6sectyp) is set by an internal capacitor between OSC2 pin and GND.

(11) Output current tolerance

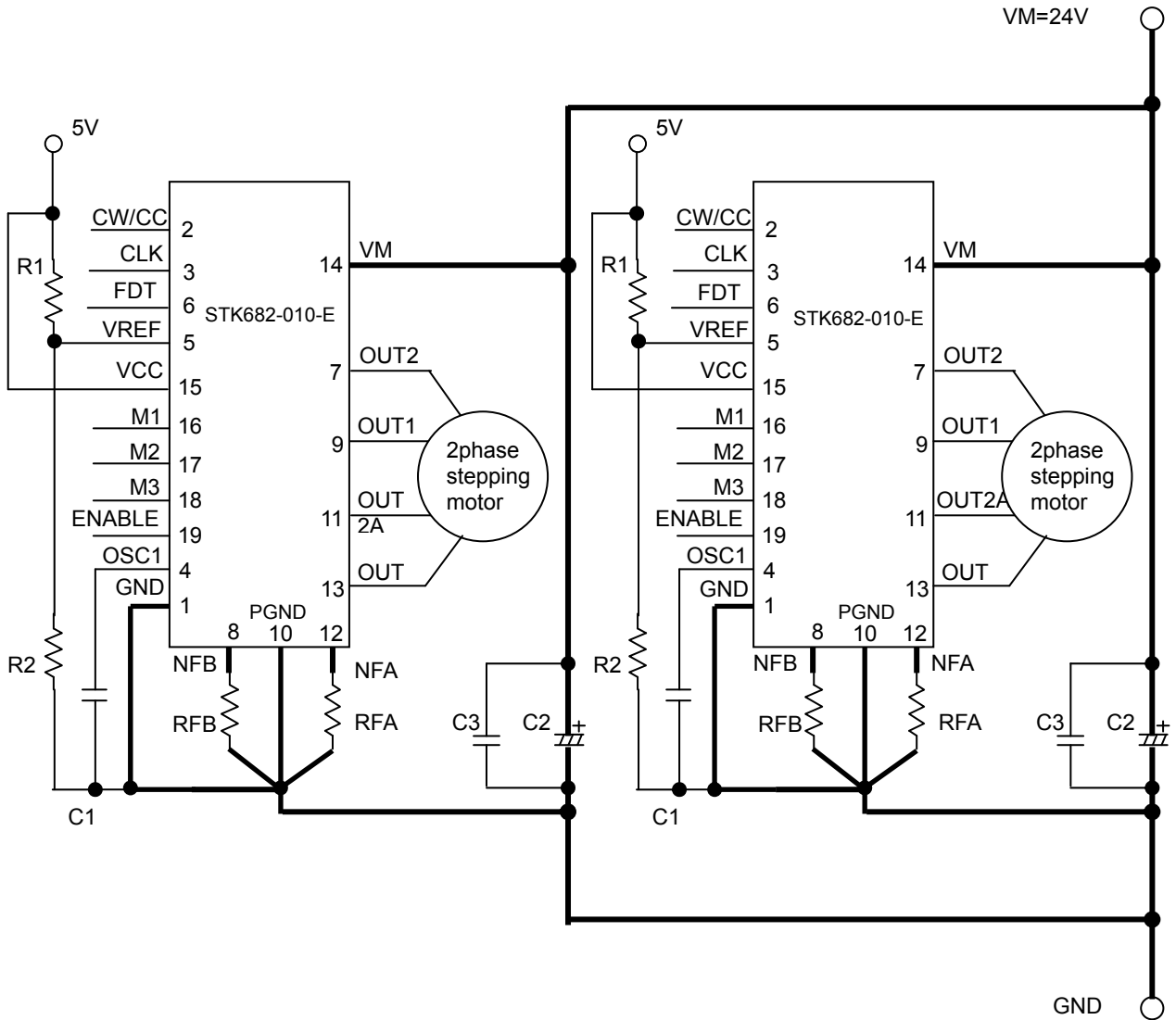
STK682-010-E Output current tolerance $I_o - T_c$



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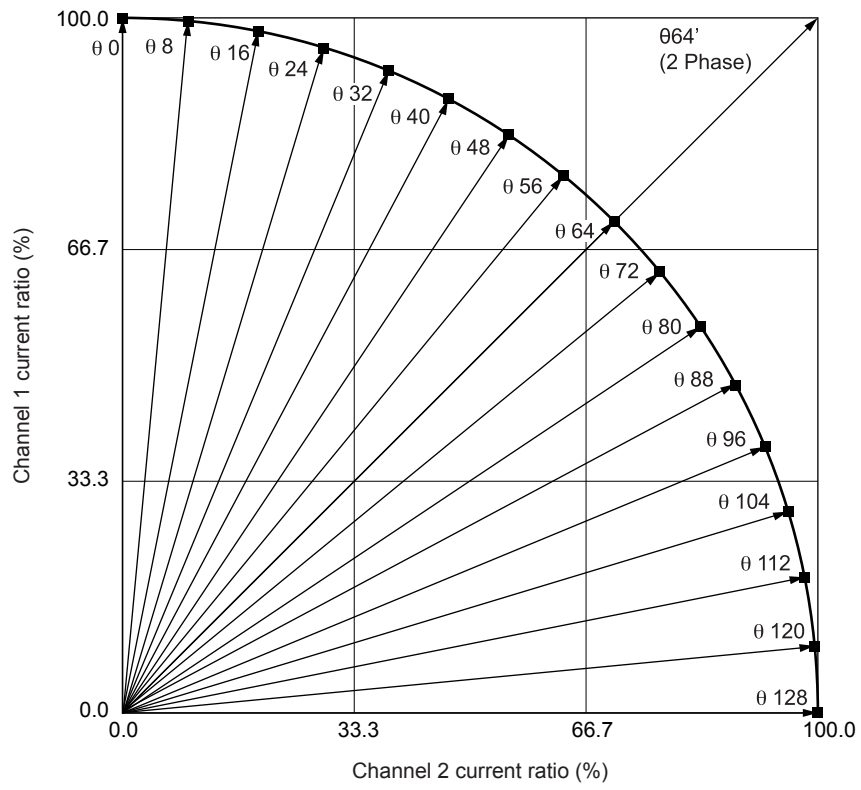
(12) When mounting multiple drivers on a single PC board

When mounting multiple drivers on a single PC board, the GND design should mount a VCC decoupling capacitor, C2 and C3, for each driver to stabilize the GND potential of the other drivers. The key wiring points are as follows.



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(13) Output current vector locus (1 step normalized 90°)



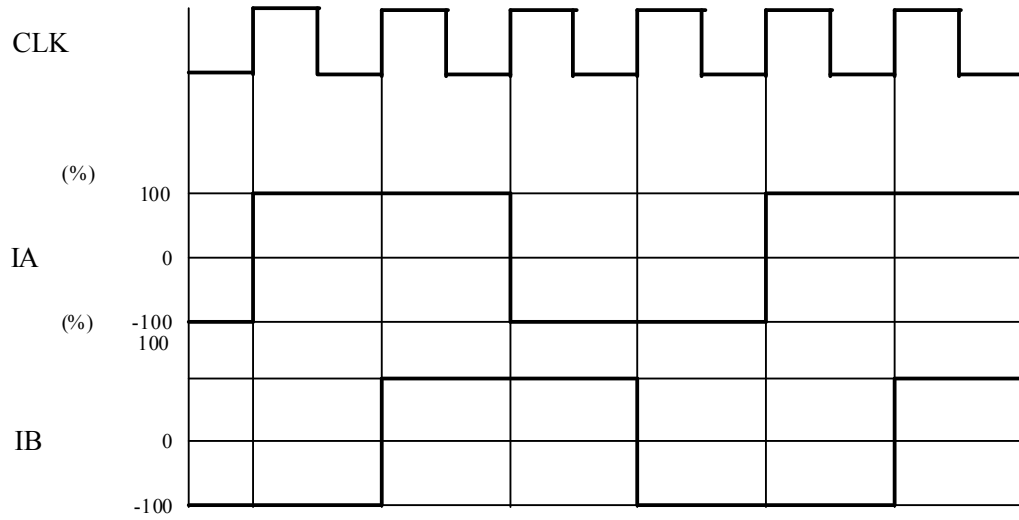
STK682-010-E

(14) Current setting ratio in each excitation mode

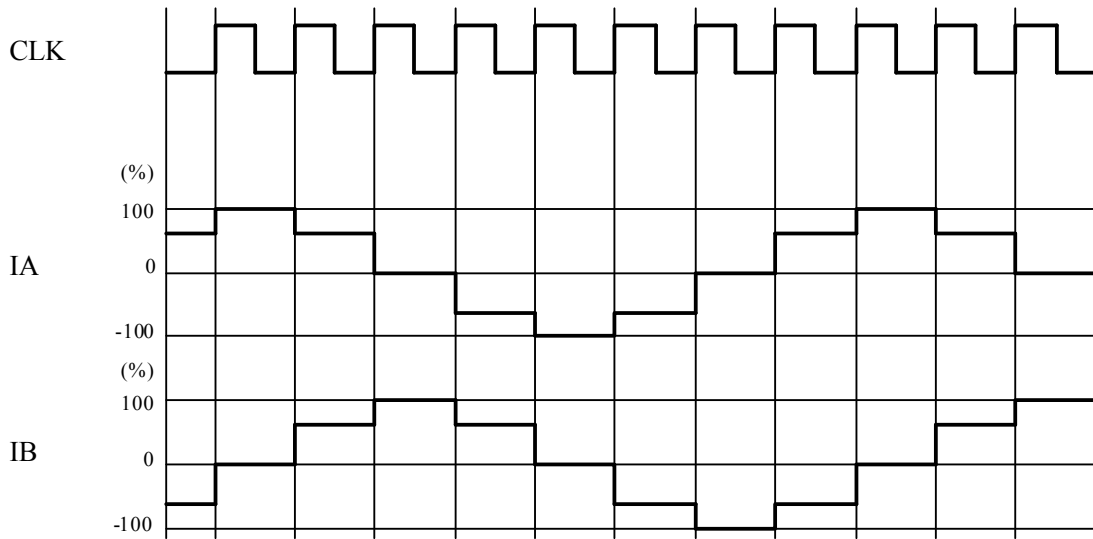
STEP	2W1-2 phase(%)		6W1-2 phase(%)		8W1-2 phase(%)		4W1-2 phase(%)		2W1-2 phase(%)		W1-2 phase(%)		1-2 phase(%)		2 phase(%)		STEP	2W1-2 phase(%)		6W1-2 phase(%)		8W1-2 phase(%)		4W1-2 phase(%)		2W1-2 phase(%)		W1-2 phase(%)		1-2 phase(%)		2 phase(%)	
	Ach	Bch	Ach	Bch	Ach	Bch	Ach	Bch	Ach	Bch	Ach	Bch	Ach	Bch	Ach	Bch		Ach	Bch	Ach	Bch	Ach	Bch	Ach	Bch	Ach	Bch	Ach	Bch	Ach	Bch	Ach	Bch
00	100	0	100	0	100	0	100	0	100	0	100	0	100	0	065	70	72																
01	100	1													066	69	72	69	72														
02	100	2	100	2											067	68	73																
03	100	4													068	67	74	67	74	67	74												
04	100	5	100	5	100	5									069	66	75																
05	100	6													070	65	76	65	76														
06	100	7	100	7											071	64	77																
07	100	9													072	63	77	63	77	63	77	63	77										
08	100	10	100	10	100	10	100	10							073	62	78																
09	99	11													074	62	79	62	79														
010	99	12	99	12											075	61	80																
011	99	13													076	60	80	60	80	60	80												
012	99	15	99	15	99	15									077	59	81																
013	99	16													078	58	82	58	82														
014	99	17	99	17											079	57	82																
015	98	18													080	56	83	56	83	56	83	56	83	56	83								
016	98	20	98	20	98	20	98	20	98	20					081	55	84																
017	98	21													082	53	84	53	84														
018	98	22	98	22											083	52	85																
019	97	23													084	51	86	51	86	51	86												
020	97	24	97	24	97	24									085	50	86																
021	97	25													086	49	87	49	87														
022	96	27	96	27											087	48	88																
023	96	28													088	47	88	47	88	47	88	47	88										
024	96	29	96	29	96	29	96	29							089	46	89																
025	95	30													090	45	89	45	89														
026	95	31	95	31											091	44	90																
027	95	33													092	43	90	43	90	43	90												
028	94	34	94	34	94	34									093	42	91																
029	94	35													094	41	91	41	91														
030	93	36	93	36											095	39	92																
031	93	37													096	38	92	38	92	38	92	38	92	38	92	38	92						
032	92	38	92	38	92	38	92	38	92	38	92	38			097	37	93																
033	92	39													098	36	93	36	93														
034	91	41	91	41											099	35	94																
035	91	42													0100	34	94	34	94	34	94												
036	90	43	90	43	90	43									0101	33	95																
037	90	44													0102	31	95	31	95														
038	89	45	89	45											0103	30	95																
039	89	46													0104	29	96	29	96	29	96	29	96										
040	88	47	88	47	88	47	88	47							0105	28	96																
041	88	48													0106	27	96	27	96														
042	87	49	87	49											0107	25	97																
043	86	50													0108	24	97	24	97	24	97												
044	86	51	86	51	86	51									0109	23	97																
045	85	52													0110	22	98	22	98														
046	84	53	84	53											0111	21	98																
047	84	55													0112	20	98	20	98	20	98	20	98	20	98	20	98						
048	83	56	83	56	83	56	83	56	83	56					0113	18	98																
049	82	57													0114	17	99	17	99														
050	82	58	82	58											0115	16	99																
051	81	59													0116	15	99	15	99	15	99												
052	80	60	80	60	80	60									0117	13	99																
053	80	61													0118	12	99	12	99														
054	79	62	79	62											0119	11	99																
055	78	62													0120	10	100	10	100	10	100	10	100										
056	77	63	77	63	77	63	77	63							0121	9	100																
057	77	64													0122	7	100	7	100														
058	76	65	76	65											0123	6	100																
059	75	66													0124	5	100	5	100	5	100												
060	74	67	74	67	74	67									0125	4	100																
061	73	68													0126	2	100	2	100														
062	72	69	72	69											0127	1	100																
063	72	70													0128	0	100	0	100	0	100	0	100	0	100	0	100	0	100				
064	71	71	71	71	71	71	71	71	71	71	71	71	71	71																			

(15) Current wave example in each excitation mode (2 phase, 1-2 phase, W1-2 phase, 4W1-2 phase)

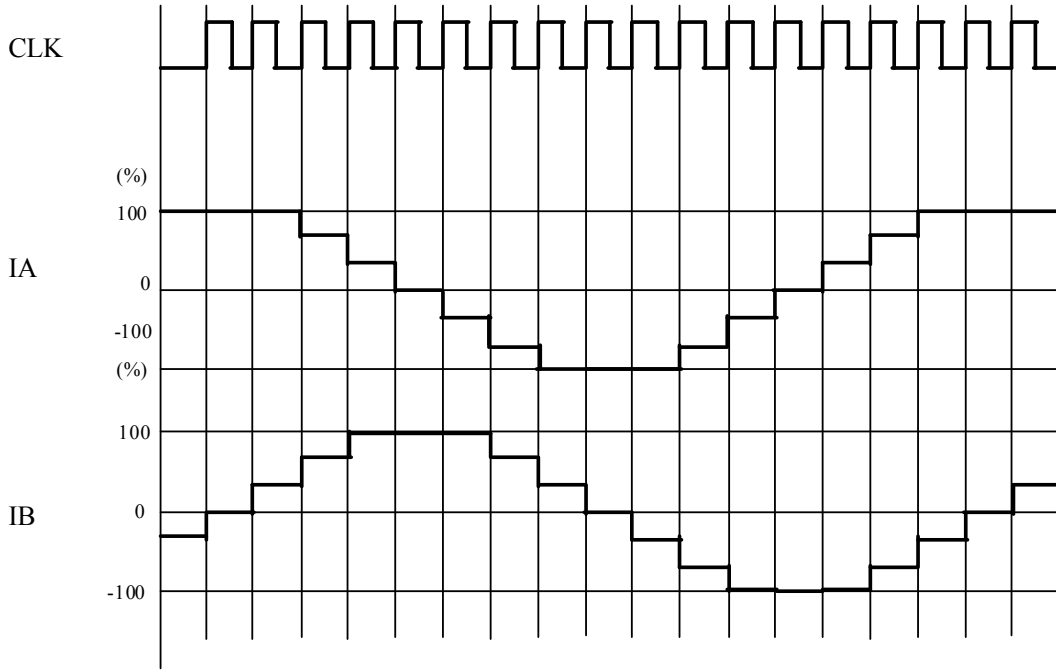
2 phase excitation (CW mode)



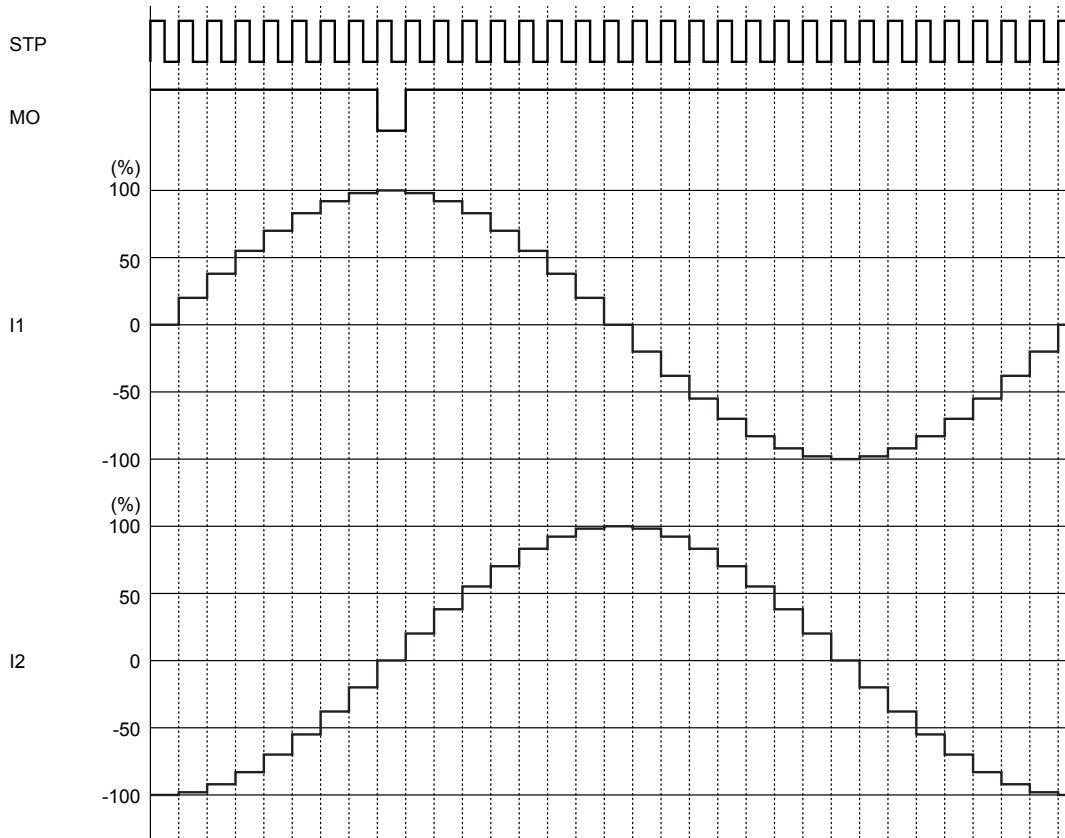
1-2 phase excitation (CW mode)



W1-2 phase excitation (CW mode)



4W1-2 phase excitation (CW mode)

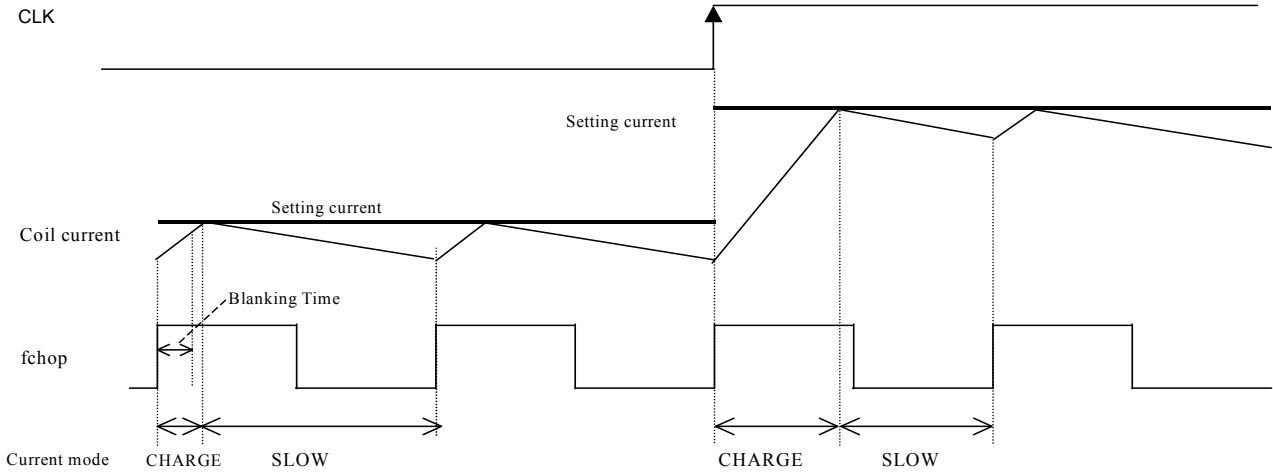


(16) Current control operation

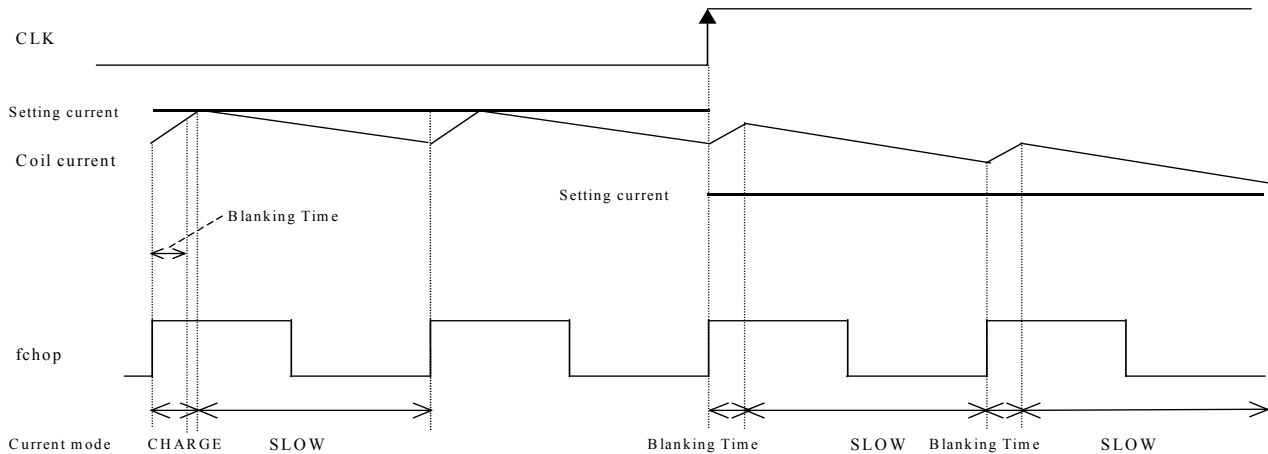
SLOW DECAY current control operation

When FDT pin voltage is a voltage over 3.5 V, the constant-current control is operated in SLOW DECAY mode.

(Sine-wave increasing direction)



(Sine-wave decreasing direction)



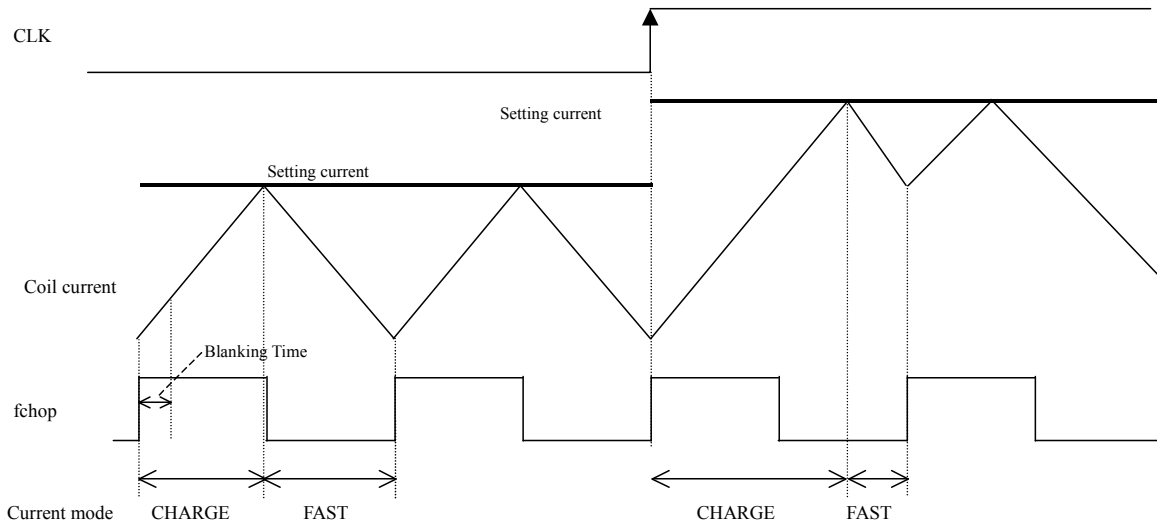
Each of current modes operates with the follow sequence.

- The IC enters CHARGE mode at a rising edge of the chopping oscillation.
(A period of CHARGE mode (Blanking Time) is forcibly present in approximately 1 μ s, regardless of the current value of the coil current (ICOIL) and set current (IREF)).
- After the period of the blanking time, the IC operates in CHARGE mode until $ICOIL \geq IREF$. After that, the mode switches to the SLOW DECAY mode and the coil current is attenuated until the end of a chopping period.
At the constant-current control in SLOW DECAY mode, following to the setting current from the coil current may take time (or not follow) for the current delay attenuation.

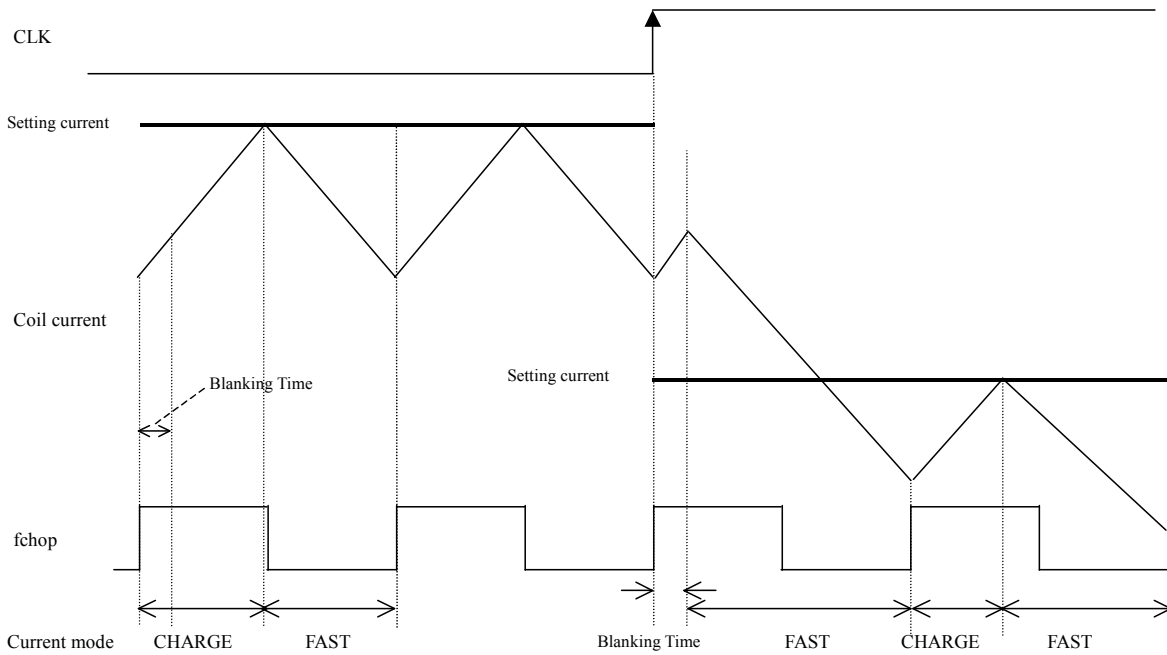
FAST DECAY current control operation

When FDT pin voltage is a voltage under 0.8V, the constant-current control is operated in FAST DECAY mode.

(Sine-wave increasing direction)



(Sine-wave decreasing direction)



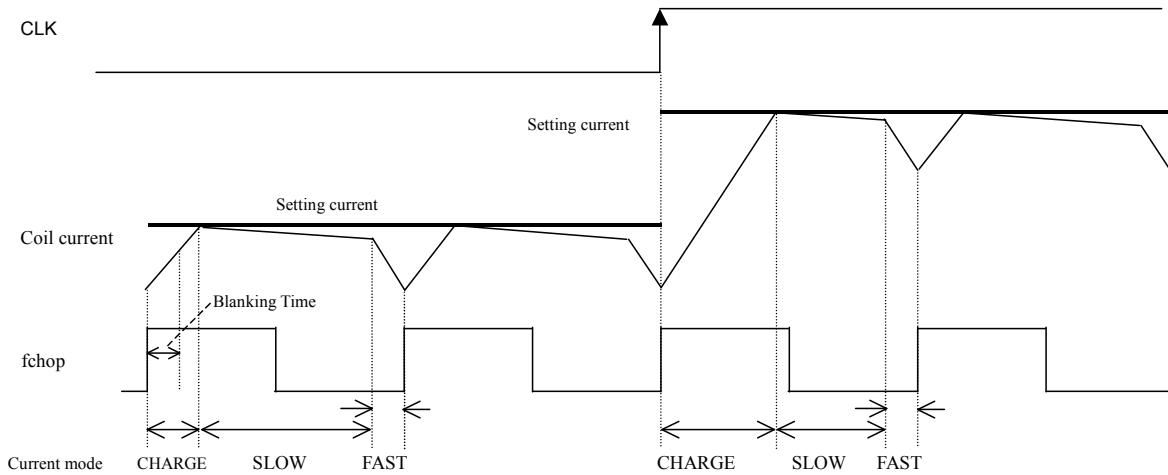
Each of current modes operates with the follow sequence.

The IC enters CHARGE mode at a rising edge of the chopping oscillation. (A period of CHARGE mode (Blanking Time) is forcibly present in approximately 1 μ s, regardless of the current value of the coil current (ICOIL) and set current (IREF)).

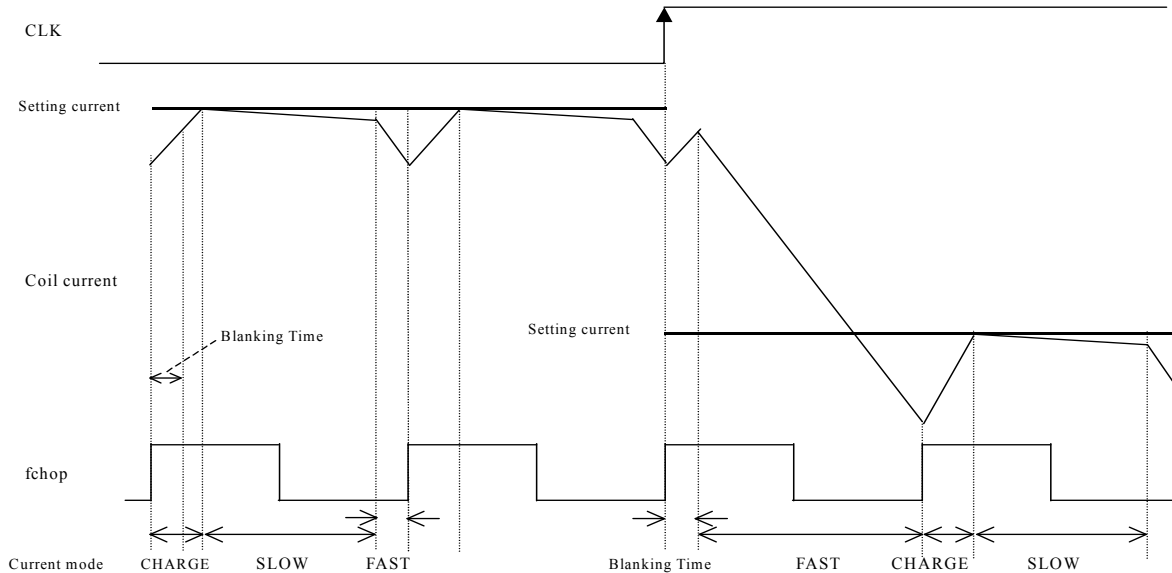
After the period of the blanking time, The IC operates in CHARGE mode until $ICOIL \geq IREF$. After that, the mode switches to the FAST DECAY mode and the coil current is attenuated until the end of a chopping period. At the constant-current control in FAST DECAY mode, following to the setting current from the coil current takes short-time for the current fast attenuation, but, the current ripple value may be higher.

MIXED DECAY current control operation

(Sine-wave increasing direction)



(Sine-wave decreasing direction)



Each of current modes operates with the follow sequence.

The IC enters CHARGE mode at a rising edge of the chopping oscillation.

(A period of CHARGE mode (Blanking Time) is forcibly present in approximately 1 μ s, regardless of the current value of the coil current (ICOIL) and set current (IREF)).

In a period of Blanking Time, the coil current (ICOIL) and the setting current (IREF) are compared.

If an $ICOIL = IREF$ state exists during the charge period:

The IC operates in CHAGE mode until $ICOIL \geq IREF$. After that, it switches to SLOW DECAY mode and then switches to FAST DECAY mode in the last approximately 1 μ s of the period.

If no $ICOIL = IREF$ state exists during the charge period:

The IC switches to FAST DECAY mode and the coil current is attenuated with the FAST DECAY operation until the end of a chopping period.

The above operation is repeated.

Normally, in the sine wave increasing direction the IC operates in SLOW (+FAST) DECAY mode, and in the sine wave decreasing direction the IC operates in FAST DECAY mode until the current is attenuated and reaches the set value and the IC operates in SLOW (+FAST) DECAY mode.

Power Dissipation

Power dissipation calculation of STK682-010-E following becomes.

2-phase excitation

$$Pd=IOH \times (Ronu + Rond)^2$$

1-2-phase excitation

$$Pd=0.71 \times IOH \times (Ronu + Rond)^2$$

Please by substituting from electrical characteristic table value of Rond and Ronu.

Thermal design

[Operating range in which a heat sink is not used]

Use of a heat sink to lower the operating substrate temperature of the HIC (Hybrid IC) is effective in increasing the quality of the HIC.

The size of heat sink for the HIC varies depending on the magnitude of the average power loss, PdAV, within the HIC. The value of PdAV increases as the output current increases. To calculate PdAV, refer to “Calculating Internal HIC Loss for the STK672-640C-E in the specification document.

Calculate the internal HIC loss, PdAV, assuming repeat operation such as shown in Figure 1 below, since conduction during motor rotation and off time both exist during actual motor operations,

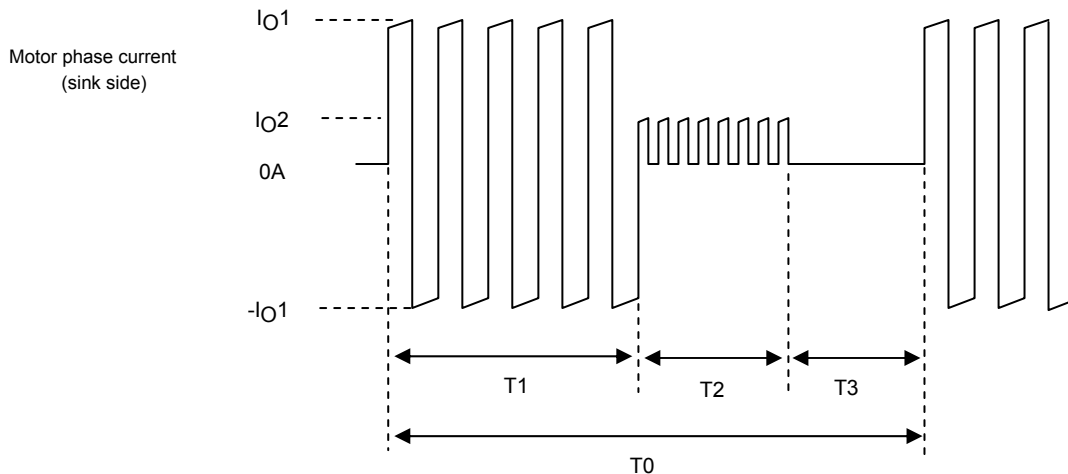


Figure 1 Motor Current Timing

- T1 : Motor rotation operation time
- T2 : Motor hold operation time
- T3 : Motor current off time
- T2 may be reduced, depending on the application.
- T0 : Single repeated motor operating cycle
- IO1 and IO2 : Motor current peak values

Due to the structure of motor windings, the phase current is a positive and negative current with a pulse form.

Note that figure 1 presents the concepts here, and that the on/off duty of the actual signals will differ.

The hybrid IC internal average power dissipation PdAV can be calculated from the following formula.

$$PdAV = (T1 \times P1 + T2 \times P2 + T3 \times 0) \cdot TO \text{ ----- (I)}$$

(Here, P1 is the PdAV for IO1 and P2 is the PdAV for IO2)

If the value calculated using Equation (I) is 1.5W or less, and the ambient temperature, Ta, is 60°C or less, there is no need to attach a heat sink. Refer to Figure 2 for operating substrate temperature data when no heat sink is used.

[Operating range in which a heat sink is used]

Although a heat sink is attached to lower Tc if PdAV increases, the resulting size can be found using the value of c-a in Equation (II) below and the graph depicted in Figure 3.

$$c-a = (Tc \text{ max} - Ta) \cdot PdAV \text{ ----- (II)}$$

Tc max : Maximum operating substrate temperature =105°C

Ta : HIC ambient temperature

Although a heat sink can be designed based on equations (I) and (II) above, be sure to mount the HIC in a set and confirm that the substrate temperature, Tc, is 105°C or less.

Figure 2 Substrate temperature rise, ΔT_c (no heat sink) - Internal average power dissipation, PdAV

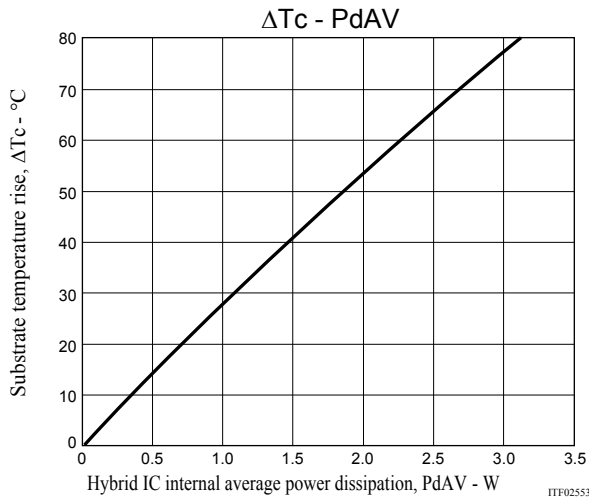
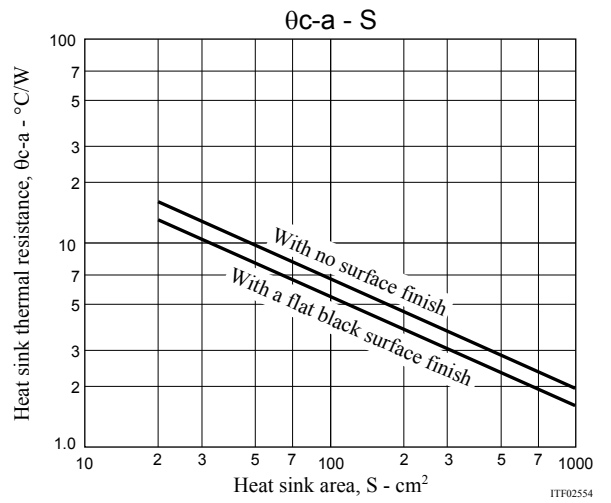
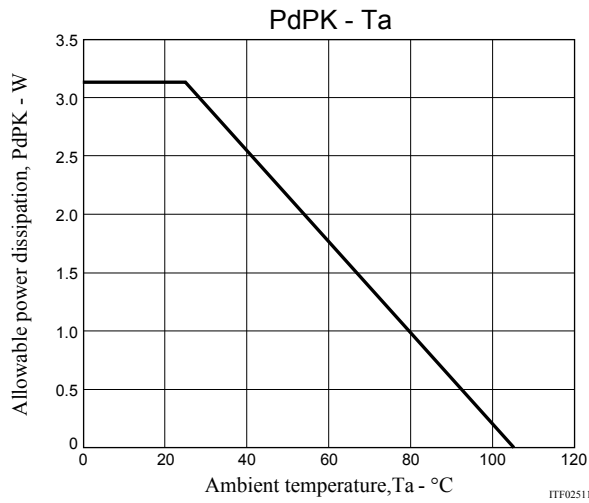


Figure 3 Heat sink area (Board thickness: 2mm) - θ_{c-a}



Mitigated Curve of Package Power Loss, PdPK, vs. Ambient Temperature, Ta
 Package power loss, PdPK, refers to the average internal power loss, PdAV, allowable without a heat sink.
 The figure below represents the allowable power loss, PdPK, vs. fluctuations in the ambient temperature, Ta.
 Power loss of up to 3.1W is allowable at Ta=25°C, and of up to 1.75W at Ta=60°C.

Allowable power dissipation, PdPK(no heat sink) - Ambient temperature, Ta



STK682-010-E

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
STK682-010-E	SIP-19 (Pb-Free)	15 / Tube

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