



LC87F2R04A

CMOS IC 4K-byte FROM and 128-byte RAM integrated 8-bit 1-chip Microcontroller

ON Semiconductor®

<http://onsemi.com>

Overview

The LC87F2R04A is an 8-bit microcontroller that, integrates on a single chip a number of hardware features such as 4K-byte flash ROM, 128-byte RAM, an On-chip-debugger, 16-bit timers/counters, two 8-bit timers, an asynchronous/synchronous SIO interface, an 8-channel AD converter, an internal reset and an interrupt feature.

Features

■Flash ROM

- 4096 × 8 bits
- Capable of on-board programming with wide range (2.2 to 5.5V) of voltage source.
- Block-erasable in 128 byte units
- Writable in 2-byte units

■RAM

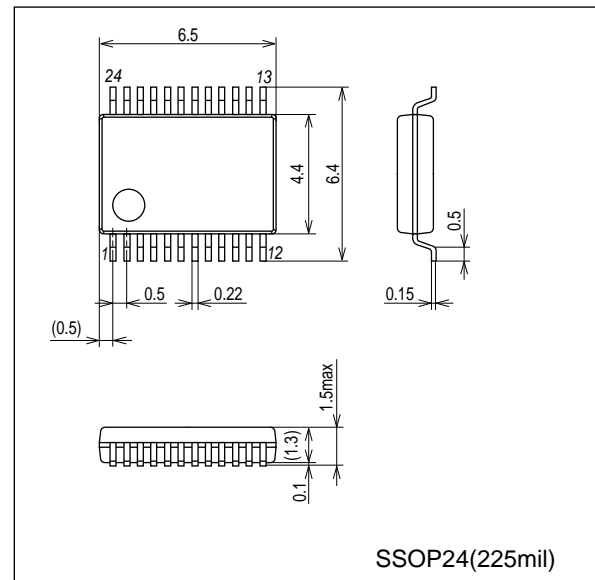
- 128 × 9 bits

■Package Form

- SSOP24(225mil): Lead-/Halogen-free type
- MFP24S(300mil): Lead-/Halogen-free type (discontinued)
- SSOP24(275mil): Lead-/Halogen-free type (build-to-order)
- VCT24(3mm×3mm): Lead-/Halogen-free type (build-to-order)

Package Dimensions

unit : mm (typ)
3287



* This product is licensed from Silicon Storage Technology, Inc. (USA).

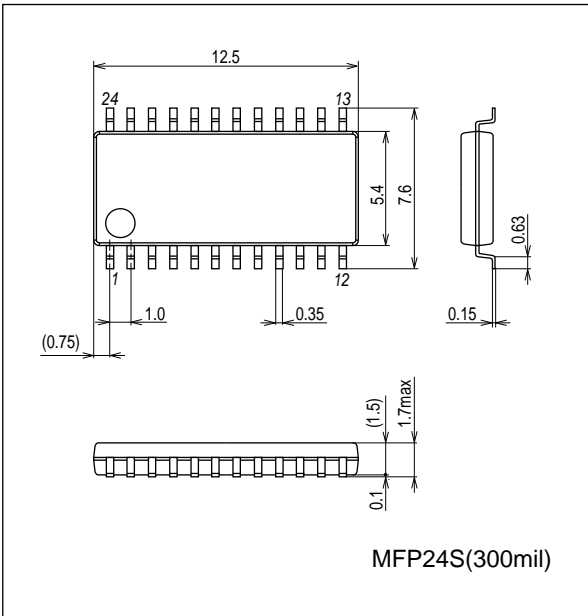
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Package Dimensions

unit : mm (typ)

3112B

(discontinued)

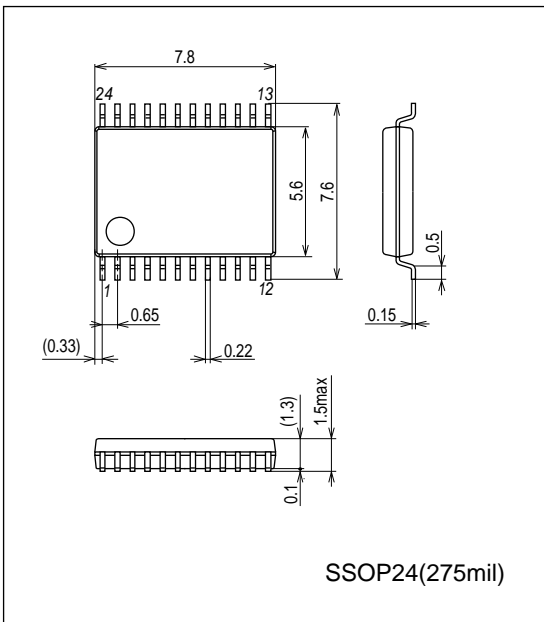


Package Dimensions

unit : mm (typ)

3175C

(build-to-order)

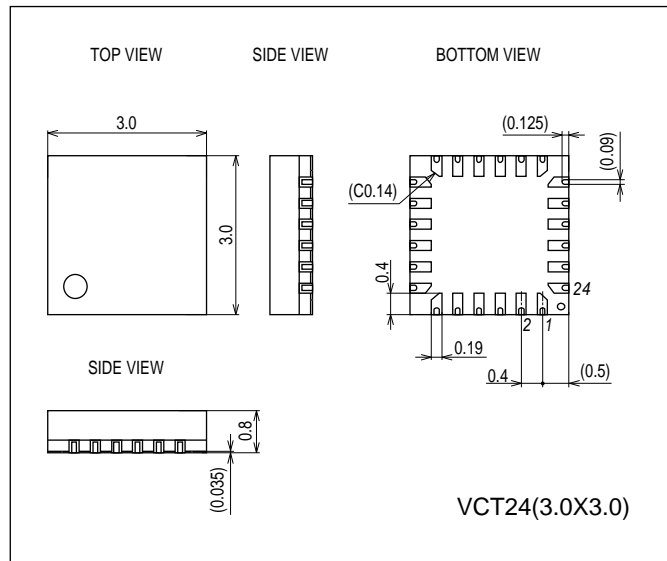


Package Dimensions

unit : mm (typ)

3366

(build-to-order)



■ Minimum Bus Cycle

- 83.3ns (12MHz at $V_{DD}=2.7V$ to 5.5V)
- 100ns (10MHz at $V_{DD}=2.2V$ to 5.5V)

Note: The bus cycle time here refers to the ROM read speed.

■ Minimum Instruction Cycle Time

- 250ns (12MHz at $V_{DD}=2.7V$ to 5.5V)
- 300ns (10MHz at $V_{DD}=2.2V$ to 5.5V)

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■ Ports

- Normal withstand voltage I/O ports
 - Ports whose I/O direction can be designated in 1-bit units 11 (P1n, P20, P21, P70)
 - Ports whose I/O direction can be designated in 4-bit units 8 (P0n)
- Dedicated oscillator ports/input ports 2 (CF1, CF2)
- Reset pin 1 ($\overline{\text{RES}}$)
- Power pins 2 (V_{SS1} , V_{DD1})

■ Timers

- Timer 0: 16-bit timer/counter with a capture register.
 - Mode 0: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) × 2 channels
 - Mode 1: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) + 8-bit counter (with an 8-bit capture register)
 - Mode 2: 16-bit timer with an 8-bit programmable prescaler (with a 16-bit capture register)
 - Mode 3: 16-bit counter (with a 16-bit capture register)
- Timer 6: 8-bit timer with a 6-bit prescaler (with toggle outputs)
- Timer 7: 8-bit timer with a 6-bit prescaler (with toggle outputs)

■ SIO

- SIO1: 8-bit asynchronous/synchronous serial interface
 - Mode 0: Synchronous 8-bit serial I/O (2- or 3-wire configuration, 2 to 512 tCYC transfer clocks)
 - Mode 1: Asynchronous serial I/O (half-duplex, 8 data bits, 1 stop bit, 8 to 2048 tCYC baudrates)
 - Mode 2: Bus mode 1 (start bit, 8 data bits, 2 to 512 tCYC transfer clocks)
 - Mode 3: Bus mode 2 (start detect, 8 data bits, stop detect)

■ AD Converter: 12 bits/8 bits × 8 channels

- 12/8 bits AD converter resolution selectable

■ Remote Control Receiver Circuit (sharing pins with P73, INT3, and T0IN)

- Noise rejection function (noise filter time constant selectable from 1 tCYC/32 tCYC/128 tCYC)

■ Watchdog Timer

- External RC watchdog timer
- Interrupt and reset signals selectable

■ Interrupts

- 12 sources, 8 vector addresses
 - 1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
 - 2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

| No. | Vector Address | Level | Interrupt Source |
|-----|----------------|--------|------------------|
| 1 | 00003H | X or L | INT0 |
| 2 | 0000BH | X or L | INT1 |
| 3 | 00013H | H or L | INT2/T0L/INT4 |
| 4 | 0001BH | H or L | INT3 |
| 5 | 00023H | H or L | T0H |
| 6 | 0002BH | H or L | None |
| 7 | 00033H | H or L | None |
| 8 | 0003BH | H or L | SIO1 |
| 9 | 00043H | H or L | ADC/T6/T7 |
| 10 | 0004BH | H or L | Port 0 |

- Priority levels $X > H > L$
- Of interrupts of the same level, the one with the smallest vector address takes precedence.

■ Subroutine Stack Levels: 64levels (The stack is allocated in RAM.)

■ High-speed Multiplication/Division Instructions

- 16 bits × 8 bits (5 tCYC execution time)
- 24 bits × 16 bits (12 tCYC execution time)
- 16 bits ÷ 8 bits (8 tCYC execution time)
- 24 bits ÷ 16 bits (12 tCYC execution time)

■ Oscillation Circuits

- Internal oscillation circuits
 - Medium-speed RC oscillation circuit: For system clock (1MHz)
 - Multifrequency RC oscillation circuit: For system clock (8MHz)
- External oscillation circuits
 - Hi-speed CF oscillation circuit: For system clock, with internal Rf

■ System Clock Divider Function

- Can run on low current.
- The minimum instruction cycle selectable from 300ns, 600ns, 1.2μs, 2.4μs, 4.8μs, 9.6μs, 19.2μs, 38.4μs, and 76.8μs (at a main clock rate of 10MHz).

■ Internal reset function

- Power-on reset (POR) function
 - 1) POR reset is generated only at power-on time.
 - 2) The POR release level can be selected from 8 levels (1.67V, 1.97V, 2.07V, 2.37V, 2.57V, 2.87V, 3.86V, and 4.35V) through option configuration.
- Low-voltage detection reset (LVD) function
 - 1) LVD and POR functions are combined to generate resets when power is turned on and when power voltage falls below a certain level.
 - 2) The use/disuse of the LVD function and the low voltage threshold level (7 levels: 1.91V, 2.01V, 2.31V, 2.51V, 2.81V, 3.79V, 4.28V).

■ Standby Function

- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
 - 1) Oscillation is not halted automatically.
 - 2) There are three ways of resetting the HALT mode.
 - (1) Setting the reset pin to the low level
 - (2) System resetting by watchdog timer or low-voltage detection
 - (3) Occurrence of an interrupt
- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
 - 1) The CF, RC and crystal oscillators automatically stop operation.
 - 2) There are four ways of resetting the HOLD mode.
 - (1) Setting the reset pin to the lower level.
 - (2) System resetting by watchdog timer or low-voltage detection
 - (3) Having an interrupt source established at either INT0, INT1, INT2, INT4* INT0 and INT1 HOLD mode reset is available only when level detection is set.
 - (4) Having an interrupt source established at port 0.

■ On-chip Debugger

- Supports software debugging with the IC mounted on the target board.
- Software break point setting for debugger.
- Stepwise execution on debugger.
- Real time RAM data monitoring function on debugger.

All the RAM data map can be monitored on screen when the program is running.
(The RAM & SFR data can be changed by screen patch when the program is running)
- Two channels of on-chip debugger pins are available to be compatible with small pin count devices.
DBGP0 (P0), DBGP1 (P1)

■ Data Security Function (flash versions only)

- Protects the program data stored in flash memory from unauthorized read or copy.

Note: This data security function does not necessarily provide absolute data security.

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■Development Tools

- On-chip debugger: TCB87 TypeB+LC87F2R04A
: TCB87 TypeC (3 wire version) +LC87F2R04A

■Programming Boards

| Package | Programming boards |
|----------------|--------------------|
| MFP24S(300mil) | W87F2GM |
| SSOP24(225mil) | W87F2GS |
| SSOP24(275mil) | build-to-order |
| VCT24 | build-to-order |

■Flash ROM Programmer

| Maker | | Model | Supported Version | Device |
|---|--------------------------|--|--------------------------------------|------------|
| Flash Support Group, Inc. (FSG) | Single | AF9708 AF9709/AF9709B/AF9709C (including Ando Electric Co., Ltd. models) | Rev 03.11 or later | LC87F2L08A |
| | Ganged | AF9723/AF9723B(Main unit) (including Ando Electric Co., Ltd. models) | - | - |
| | | AF9833(Unit) (including Ando Electric Co., Ltd. models) | - | - |
| Flash Support Group, Inc. (FSG) + Our company (Note 1) | Onboard single/ganged | AF9101/AF9103(Main unit) (FSG) SIB87(Interface driver) (Our company) | (Note 2) | - |
| Our company | Single/ganged | SKK/SKK Type B (SANYO FWS) | Application version 1.05 or later | LC87F2R04A |
| | Onboard single/ganged | SKK-DBG Type B (SANYO FWS) | Chip data version 2.22 or later | |

For information about AF-Series:

Flash Support Group, Inc.
TEL: +81-53-459-1050
E-mail: sales@j-fsg.co.jp

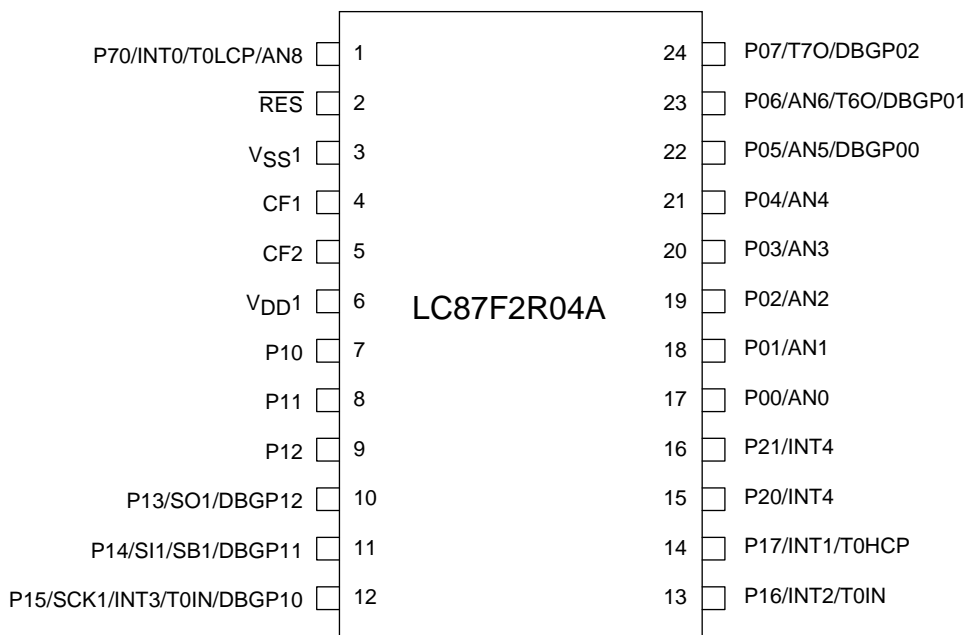
Note1: On-board-programmer from FSG (AF9101/AF9103) and serial interface driver from Our company (SIB87) together

can give a PC-less, standalone on-board-programming capabilities.

Note2: It needs a special programming devices and applications depending on the use of programming environment.
Please ask FSG or Our company for the information.

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Pin Assignment



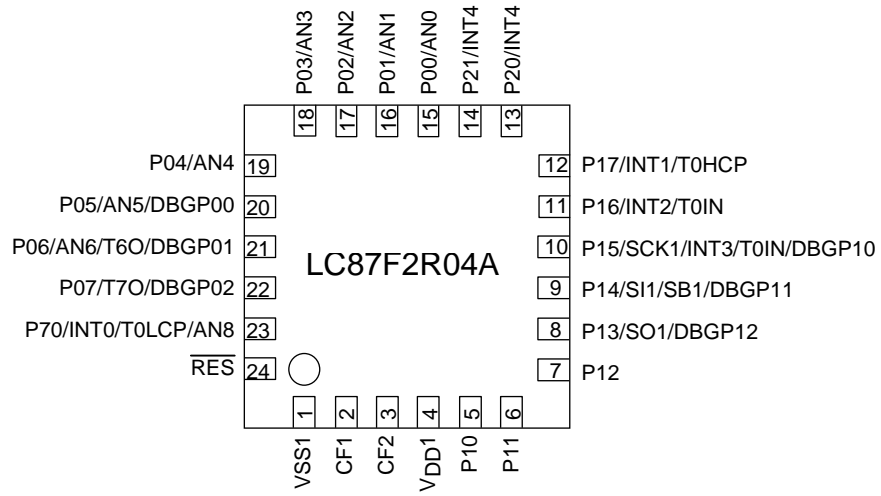
Top view

MFP24S(300mil) "Lead-/Halogen-free Type" (discontinued)
 SSOP24(225mil) "Lead-/Halogen-free Type"
 SSOP24(275mil) "Lead-/Halogen-free Type" (build-to-order)

| MFP24S SSOP24 | NAME |
|------------------|---------------------------|
| 1 | P70/INT0/T0LCP/AN8 |
| 2 | $\overline{\text{RES}}$ |
| 3 | VSS1 |
| 4 | CF1 |
| 5 | CF2 |
| 6 | VDD1 |
| 7 | P10 |
| 8 | P11 |
| 9 | P12 |
| 10 | P13/SO1/DBGP12 |
| 11 | P14/SI1/SB1/DBGP11 |
| 12 | P15/SCK1/INT3/T0IN/DBGP10 |

| MFP24S SSOP24 | NAME |
|------------------|--------------------|
| 13 | P16/INT2/T0IN |
| 14 | P17/INT1/T0HCP |
| 15 | P20/INT4 |
| 16 | P21/INT4 |
| 17 | P00/AN0 |
| 18 | P01/AN1 |
| 19 | P02/AN2 |
| 20 | P03/AN3 |
| 21 | P04/AN4 |
| 22 | P05/AN5/DBGP00 |
| 23 | P06/AN6/T6O/DBGP01 |
| 24 | P07/T7O/DBGP02 |

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Top view

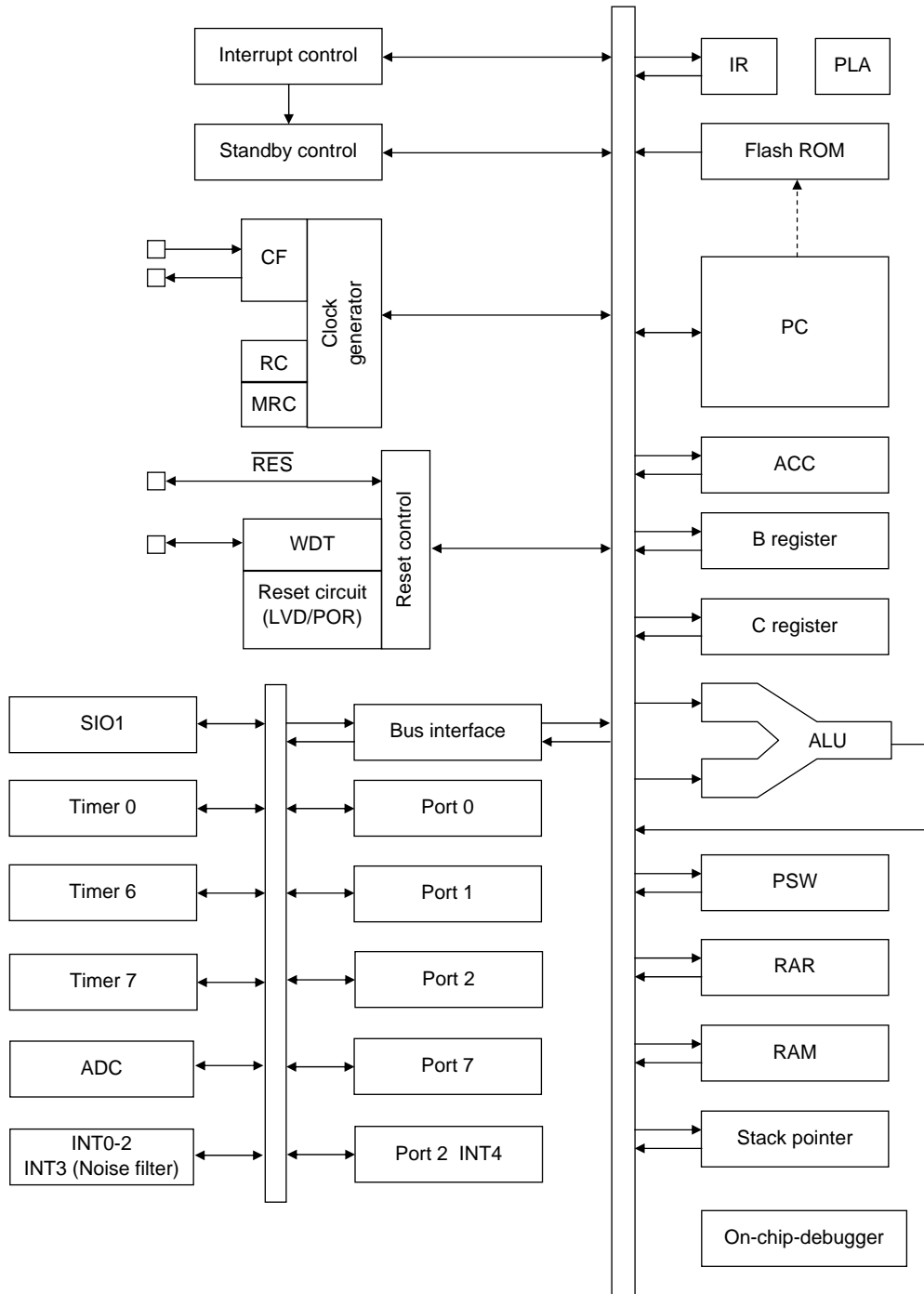
VCT24(3.0x3.0) "Lead-/Halogen-free Type" (build-to-order)

| VCT24 | NAME |
|-------|---------------------------|
| 1 | V _{SS} 1 |
| 2 | CF1 |
| 3 | CF2 |
| 4 | VDD1 |
| 5 | P10 |
| 6 | P11 |
| 7 | P12 |
| 8 | P13/SO1/DBGP12 |
| 9 | P14/SI1/SB1/DBGP11 |
| 10 | P15/SCK1/INT3/T0IN/DBGP10 |
| 11 | P16/INT2/T0IN |
| 12 | P17/INT1/T0HCP |

| VCT24 | NAME |
|-------|--------------------|
| 13 | P20/INT4 |
| 14 | P21/INT4 |
| 15 | P00/AN0 |
| 16 | P01/AN1 |
| 17 | P02/AN2 |
| 18 | P03/AN3 |
| 19 | P04/AN4 |
| 20 | P05/AN5/DBGP00 |
| 21 | P06/AN6/T6O/DBGP01 |
| 22 | P07/T7O/DBGP02 |
| 23 | P70/INT0/T0LCP/AN8 |
| 24 | RES |

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System Block Diagram



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Pin Description

| Pin Name | I/O | Description | Option | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------------------|--------|---|------------------|---------|---------|------------------|---------|---------|------|--------|--------|---------|---------|---------|------|--------|--------|--------|---------|---------|------|--------|--------|--------|---------|---------|-----|
| V _{SS} 1 | - | - power supply pins | No | | | | | | | | | | | | | | | | | | | | | | | | |
| V _{DD} 1 | - | + power supply pin | No | | | | | | | | | | | | | | | | | | | | | | | | |
| Port 0 P00 to P07 | I/O | <ul style="list-style-type: none"> • 8-bit I/O port • I/O specifiable in 4-bit units • Pull-up resistors can be turned on and off in 4-bit units. • HOLD reset input • Port 0 interrupt input • Pin functions P06: Timer 6 toggle output P07: Timer 7 toggle output P00(AN0) to P06(AN6): AD converter input P05(DBGP00) to P07(DBGP02): On-chip debugger 0 port | Yes | | | | | | | | | | | | | | | | | | | | | | | | |
| Port 1 P10 to P17 | I/O | <ul style="list-style-type: none"> • 8-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1-bit units. • Pin functions P13: SIO1 data output P14: SIO1 data input/bus I/O P15: SIO1 clock I/O/INT3 input (with noise filter)/timer 0 event input/timer 0H capture input P16: INT2 input/HOLD reset input/timer 0 event input/timer 0L capture input P17: INT1 input/HOLD reset input/timer 0H capture input P15(DBGP10) to P13(DBGP12): On-chip debugger 1 port Interrupt acknowledge types <table border="1" style="margin-top: 5px;"> <thead> <tr> <th></th> <th>Rising</th> <th>Falling</th> <th>Rising & Falling</th> <th>H level</th> <th>L level</th> </tr> </thead> <tbody> <tr> <td>INT1</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>enable</td> <td>enable</td> </tr> <tr> <td>INT2</td> <td>enable</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>disable</td> </tr> <tr> <td>INT3</td> <td>enable</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>disable</td> </tr> </tbody> </table> | | Rising | Falling | Rising & Falling | H level | L level | INT1 | enable | enable | disable | enable | enable | INT2 | enable | enable | enable | disable | disable | INT3 | enable | enable | enable | disable | disable | Yes |
| | Rising | Falling | Rising & Falling | H level | L level | | | | | | | | | | | | | | | | | | | | | | |
| INT1 | enable | enable | disable | enable | enable | | | | | | | | | | | | | | | | | | | | | | |
| INT2 | enable | enable | enable | disable | disable | | | | | | | | | | | | | | | | | | | | | | |
| INT3 | enable | enable | enable | disable | disable | | | | | | | | | | | | | | | | | | | | | | |
| Port 2 P20 to P21 | I/O | <ul style="list-style-type: none"> • 2-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1-bit units. • Pin functions P20 to P21: INT4 input/HOLD reset input/timer 0L capture input/ timer 0H capture input Interrupt acknowledge types <table border="1" style="margin-top: 5px;"> <thead> <tr> <th></th> <th>Rising</th> <th>Falling</th> <th>Rising & Falling</th> <th>H level</th> <th>L level</th> </tr> </thead> <tbody> <tr> <td>INT4</td> <td>enable</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>disable</td> </tr> </tbody> </table> | | Rising | Falling | Rising & Falling | H level | L level | INT4 | enable | enable | enable | disable | disable | Yes | | | | | | | | | | | | |
| | Rising | Falling | Rising & Falling | H level | L level | | | | | | | | | | | | | | | | | | | | | | |
| INT4 | enable | enable | enable | disable | disable | | | | | | | | | | | | | | | | | | | | | | |
| Port 7 P70 | I/O | <ul style="list-style-type: none"> • 1-bit I/O port • I/O specifiable in 1-bit units • Pull-up resistors can be turned on and off in 1-bit units. • Pin functions P70: INT0 input/HOLD reset input/timer 0L capture input/watchdog timer output P70(AN8): AD converter input Interrupt acknowledge types <table border="1" style="margin-top: 5px;"> <thead> <tr> <th></th> <th>Rising</th> <th>Falling</th> <th>Rising & Falling</th> <th>H level</th> <th>L level</th> </tr> </thead> <tbody> <tr> <td>INT0</td> <td>enable</td> <td>enable</td> <td>disable</td> <td>enable</td> <td>enable</td> </tr> </tbody> </table> | | Rising | Falling | Rising & Falling | H level | L level | INT0 | enable | enable | disable | enable | enable | No | | | | | | | | | | | | |
| | Rising | Falling | Rising & Falling | H level | L level | | | | | | | | | | | | | | | | | | | | | | |
| INT0 | enable | enable | disable | enable | enable | | | | | | | | | | | | | | | | | | | | | | |
| $\overline{\text{RES}}$ | I/O | External reset Input/internal reset output | No | | | | | | | | | | | | | | | | | | | | | | | | |
| CF1 | I | <ul style="list-style-type: none"> • Ceramic resonator oscillator input pin • Pin function General-purpose input port | No | | | | | | | | | | | | | | | | | | | | | | | | |
| CF2 | I/O | <ul style="list-style-type: none"> • Ceramic resonator oscillator output pin • Pin function General-purpose input port | No | | | | | | | | | | | | | | | | | | | | | | | | |

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Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor. Data can be read into any input port even if it is in the output mode.

| Port Name | Option selected in units of | Option type | Output type | Pull-up resistor |
|------------|-----------------------------|-------------|----------------|-----------------------|
| P00 to P07 | 1 bit | 1 | CMOS | Programmable (Note 1) |
| | | 2 | Nch-open drain | No |
| P10 to P17 | 1 bit | 1 | CMOS | Programmable |
| | | 2 | Nch-open drain | Programmable |
| P20 to P21 | 1 bit | 1 | CMOS | Programmable |
| | | 2 | Nch-open drain | Programmable |
| P70 | - | No | Nch-open drain | Programmable |

Note 1: The control of the presence or absence of the programmable pull-up resistors for port 0 and the switching between low-and high-impedance pull-up connection is exercised in nibble (4-bit) units (P00 to 03 or P04 to 07).

User Option Table

| Option Name | Option Type | Mask version *1 | Flash Version | Option Selected in Units of | Option Selection |
|--------------------------------------|----------------------|-----------------|---------------|-----------------------------|-------------------|
| Port output type | P00 to P07 | ○ | ○ | 1 bit | CMOS |
| | | | | | Nch-open drain |
| | P10 to P17 | ○ | ○ | 1 bit | CMOS |
| | | | | | Nch-open drain |
| | P20 to P21 | ○ | ○ | 1 bit | CMOS |
| | | | | | Nch-open drain |
| Program start address | - | x *2 | ○ | - | 00000h |
| | | | | | 01E00h |
| Low-voltage detection reset function | Detect function | ○ | ○ | - | Enable: Use |
| | | | | | Disable: Not Used |
| | Detect level | ○ | ○ | - | 7-level |
| Power-on reset function | Power-On reset level | ○ | ○ | - | 8-level |

*1: Mask option selection-No change possible after mask is completed.

*2: Program start address of the mask version is 00000h.

Recommended Unused Pin Connections

| Port Name | Recommended Unused Pin Connections | |
|------------|--|----------------------------|
| | Board | Software |
| P00 to P07 | Open | Output low |
| P10 to P17 | Open | Output low |
| P20 to P21 | Open | Output low |
| P70 | Open | Output low |
| CF1 | Pulled low with a 100kΩ resistor or less | General-purpose input port |
| CF2 | Pulled low with a 100kΩ resistor or less | General-purpose input port |

On-chip Debugger Pin Connection Requirements

For the treatment of the on-chip debugger pins, refer to the separately available documents entitled "RD87 on-chip debugger installation manual" and "LC872000 series on-chip debugger pin connection requirements"

Notes on CF1 and CF2 Pins

- When using as general-purpose input ports

Since the CF1 and CF2 pins are configured as CF oscillator pins at system reset time, it is necessary to add a current limiting resistor of 1kΩ or greater to the CF2 pin in series when using them as general-purpose input pins.

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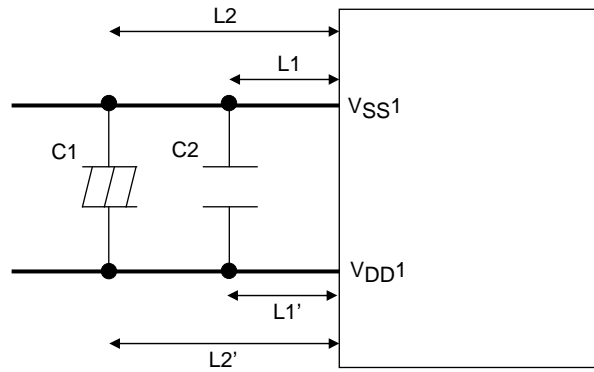
Differences between LC872G00 and LC872R00 Series.

| | | System Reset Time State | After System Reset is Released |
|--|---------|---------------------------------------|--------------------------------|
| Flash ROM version LC87F2G08A | CF1/XT1 | Set high via the internal Rf resistor | CF oscillation state |
| | CF2/XT2 | Set high | CF oscillation state |
| Mask ROM version LC872G08A | CF1/XT1 | Set low via the internal Rf resistor | CF oscillation state |
| | CF2/XT2 | Set low | CF oscillation state |
| Flash ROM version LC87F2R04A Mask ROM version LC872R04A | CF1 | Set low via the internal Rf resistor | CF oscillation state |
| | CF2 | High-impedance (OPEN) | CF oscillation state |

Power Pin Treatment Recommendations (V_{DD1}, V_{SS1})

Connect bypass capacitors that meet the following conditions between the V_{DD1} and V_{SS1} pins:

- Connect among the V_{DD1} and V_{SS1} pins and bypass capacitors C1 and C2 with the shortest possible heavy lead wires, making sure that the impedances between the both pins and the bypass capacitors are as possible ($L1=L1'$, $L2=L2'$).
- Connect a large-capacity capacitor C1 and a small-capacity capacitor C2 in parallel. The capacitance of C2 should be approximately 0.1μF.



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Absolute Maximum Ratings at Ta = 25°C, VSS1 = 0V

| Parameter | Symbol | Pin/Remarks | Conditions | Specification | | | | unit | |
|-------------------------------|--------------------------------|----------------------|---------------------------------|---|------|------|----------------------|------|-----|
| | | | | V _{DD} [V] | min | typ | max | | |
| Maximum supply voltage | V _{DD} max | V _{DD} 1 | | | -0.3 | | +6.5 | V | |
| Input voltage | V _I | CF1, CF2 | | | -0.3 | | V _{DD} +0.3 | | |
| Input/output voltage | V _{IO} | Ports 0, 1, 2 P70 | | | -0.3 | | V _{DD} +0.3 | | |
| High level output current | Peak output current | IOPH | Ports 0, 1, 2 | CMOS output select Per 1 applicable pin | | -10 | | mA | |
| | Mean output current (Note 1-1) | IOMH | Ports 0, 1, 2 | CMOS output select Per 1 applicable pin | | -7.5 | | | |
| | Total output current | ΣIOAH(1) | P10 to P14 | Total of all applicable pins | | -20 | | | |
| | | ΣIOAH(2) | P15 to P17 Ports 0, 2 | Total of all applicable pins | | -20 | | | |
| ΣIOAH(3) | | Ports 0, 1, 2 | Total of all applicable pins | | -25 | | | | |
| Low level output current | Peak output current | IOPL(1) | P02 to P07 Ports 1, 2 | Per 1 applicable pin | | | 20 | | |
| | | IOPL(2) | P00, P01 | Per 1 applicable pin | | | 30 | | |
| | | IOPL(3) | P70 | Per 1 applicable pin | | | 10 | | |
| | Mean output current (Note 1-1) | IOML(1) | P02 to P07 Ports 1, 2 | Per 1 applicable pin | | | | | 15 |
| | | IOML(2) | P00, P01 | Per 1 applicable pin | | | | | 20 |
| | | IOML(3) | P70 | Per 1 applicable pin | | | | 7.5 | |
| | Total output current | ΣIOAL(1) | P10 to P14 | Total of all applicable pins | | | | 50 | |
| | | ΣIOAL(2) | Ports 0, 2 P15 to P17 | Total of all applicable pins | | | | 60 | |
| ΣIOAL(3) | | Ports 0, 1, 2 | Total of all applicable pins | | | | 70 | | |
| ΣIOAL(4) | | P70 | Total of all applicable pins | | | | 7.5 | | |
| Power Dissipation | Pd max(1) | MFP24S(300mil)) | Ta=-40 to +85°C Package only | | | | 129 | mW | |
| | Pd max(2) | | | Ta=-40 to +85°C Package with thermal resistance board (Note 1-2) | | | | | 229 |
| | Pd max(3) | SSOP24(225mil) | Ta=-40 to +85°C Package only | | | | 111 | | |
| | Pd max(4) | | | Ta=-40 to +85°C Package with thermal resistance board (Note 1-2) | | | | | 334 |
| Operating ambient Temperature | T _{opr} | | | | -40 | | +85 | °C | |
| Storage ambient temperature | T _{stg} | | | | -55 | | +125 | | |

Note 1-1: The mean output current is a mean value measured over 100ms.

Note 1-2: SEMI standards thermal resistance board (size: 76.1×114.3×1.6mm, glass epoxy) is used.

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

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Allowable Operating Conditions at $T_a = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{SS1} = 0\text{V}$

| Parameter | Symbol | Pin/Remarks | Conditions | Specification | | | | unit |
|--|------------------------------|--|---|--------------------|-----------------|--------------|------------------|---------------|
| | | | | $V_{DD}[\text{V}]$ | min | typ | max | |
| Operating supply voltage (Note 2-1) | $V_{DD}(1)$ | V_{DD1} | $0.245\mu\text{s} \leq t_{CYC} \leq 200\mu\text{s}$ | | 2.7 | | 5.5 | V |
| | $V_{DD}(2)$ | | $0.294\mu\text{s} \leq t_{CYC} \leq 200\mu\text{s}$ | | 2.2 | | 5.5 | |
| Memory sustaining supply voltage | VHD | V_{DD1} | RAM and register contents sustained in HOLD mode. | | 1.6 | | | |
| High level input voltage | $V_{IH}(1)$ | Ports 1, 2 P70 port input/ interrupt side | | 2.2 to 5.5 | $0.3V_{DD}+0.7$ | | V_{DD} | |
| | $V_{IH}(2)$ | Port 0 | | 2.2 to 5.5 | $0.3V_{DD}+0.7$ | | V_{DD} | |
| | $V_{IH}(3)$ | Port 70 watchdog timer side | | 2.2 to 5.5 | $0.9V_{DD}$ | | V_{DD} | |
| | $V_{IH}(4)$ | CF1, $\overline{\text{RES}}$ | | 2.2 to 5.5 | $0.75V_{DD}$ | | V_{DD} | |
| Low level input voltage | $V_{IL}(1)$ | Ports 1, 2, P70 port input/ interrupt side | | 4.0 to 5.5 | V_{SS} | | $0.1V_{DD}+0.4$ | |
| | | | | 2.2 to 4.0 | V_{SS} | | $0.2V_{DD}$ | |
| | $V_{IL}(2)$ | Port 0 | | 4.0 to 5.5 | V_{SS} | | $0.15V_{DD}+0.4$ | |
| | | | | 2.2 to 4.0 | V_{SS} | | $0.2V_{DD}$ | |
| | $V_{IL}(3)$ | Port 70 watchdog timer side | | 2.2 to 5.5 | V_{SS} | | $0.8V_{DD}-1.0$ | |
| $V_{IL}(4)$ | CF1, $\overline{\text{RES}}$ | | 2.2 to 5.5 | V_{SS} | | $0.25V_{DD}$ | | |
| Instruction cycle time (Note 2-1) | tCYC (Note 2-2) | | | 2.7 to 5.5 | 0.245 | | 200 | μs |
| | | | | 2.2 to 5.5 | 0.294 | | 200 | |
| External system clock frequency | FEXCF | CF1 | <ul style="list-style-type: none"> • CF2 pin open • System clock frequency division ratio=1/1 • External system clock duty=50±5% | 2.7 to 5.5 | 0.1 | | 12 | MHz |
| | | | <ul style="list-style-type: none"> • CF2 pin open • System clock frequency division ratio=1/2 • External system clock duty=50±5% | 2.2 to 5.5 | 0.1 | | 10 | |
| | | | <ul style="list-style-type: none"> • CF2 pin open • System clock frequency division ratio=1/2 • External system clock duty=50±5% | 3.0 to 5.5 | 0.2 | | 24.4 | |
| Oscillation frequency range (Note 2-3) | FmCF(1) | CF1, CF2 | 12MHz ceramic oscillation See Fig. 1. | 2.7 to 5.5 | | 12 | | MHz |
| | FmCF(2) | CF1, CF2 | 10MHz ceramic oscillation See Fig. 1. | 2.2 to 5.5 | | 10 | | |
| | FmCF(3) | CF1, CF2 | 4MHz ceramic oscillation. CF oscillation normal amplifier size selected. (CFLAMP=0) See Fig. 1 | 2.2 to 5.5 | | 4 | | |
| | | | 4MHz ceramic oscillation. CF oscillation low amplifier size selected. (CFLAMP=1) See Fig. 1. | 2.2 to 5.5 | | 4 | | |
| | FmMRC | | Frequency variable RC oscillation. 1/2 frequency division ration. (RCCTD=0) (Note 2-4) | 2.7 to 5.5 | 7.6 | 8.0 | 8.4 | |
| | FmRC | | Internal medium-speed RC oscillation | 2.2 to 5.5 | 0.5 | 1.0 | 2.0 | |

Note 2-1: V_{DD} must be held greater than or equal to 2.2V in the flash ROM onboard programming mode.

Note 2-2: Relationship between tCYC and oscillation frequency is $3/\text{FmCF}$ at a division ratio of 1/1 and $6/\text{FmCF}$ at a division ratio of 1/2.

Note 2-3: See Tables 1 and 2 for the oscillation constants.

Note 2-4: When switching the system clock, allow an oscillation stabilization time of 100 μs or longer after the multifrequency RC oscillator circuit transmits from the "oscillation stopped" to "oscillation enabled" state.

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Electrical Characteristics at Ta = -40°C to +85°C, V_{SS1} = 0V

| Parameter | Symbol | Pin/Remarks | Conditions | Specification | | | | |
|---------------------------|----------------------|---|--|---------------------|----------------------|---------------------|-----|------|
| | | | | V _{DD} [V] | min | typ | max | unit |
| High level input current | I _{IH} (1) | Ports 0, 1, 2 P70 $\overline{\text{RES}}$ | Output disabled Pull-up resistor off V _{IN} =V _{DD} (Including output Tr's off leakage current) | 2.2 to 5.5 | | | 1 | μA |
| | I _{IH} (2) | CF1 | V _{IN} =V _{DD} | 2.2 to 5.5 | | | 15 | |
| Low level input current | I _{IL} (1) | Ports 0, 1, 2 P70 $\overline{\text{RES}}$ | Output disabled Pull-up resistor off V _{IN} =V _{SS} (Including output Tr's off leakage current) | 2.2 to 5.5 | -1 | | | μA |
| | I _{IL} (2) | CF1 | V _{IN} =V _{SS} | 2.2 to 5.5 | -15 | | | |
| High level output voltage | V _{OH} (1) | Ports 0, 1, 2 | I _{OH} =-1mA | 4.5 to 5.5 | V _{DD} -1 | | | V |
| | V _{OH} (2) | | I _{OH} =-0.35mA | 2.7 to 5.5 | V _{DD} -0.4 | | | |
| | V _{OH} (3) | | I _{OH} =-0.15mA | 2.2 to 5.5 | V _{DD} -0.4 | | | |
| Low level output voltage | V _{OL} (1) | Ports 0, 1, 2 | I _{OL} =10mA | 4.5 to 5.5 | | | 1.5 | |
| | V _{OL} (2) | | I _{OL} =1.4mA | 2.7 to 5.5 | | 0.4 | | |
| | V _{OL} (3) | | I _{OL} =0.8mA | 2.2 to 5.5 | | 0.4 | | |
| | V _{OL} (4) | P70 | I _{OL} =1.4mA | 2.7 to 5.5 | | 0.4 | | |
| | V _{OL} (5) | | I _{OL} =0.8mA | 2.2 to 5.5 | | 0.4 | | |
| | V _{OL} (6) | P00, P01 | I _{OL} =25mA | 4.5 to 5.5 | | 1.5 | | |
| | V _{OL} (7) | | I _{OL} =4mA | 2.7 to 5.5 | | 0.4 | | |
| | V _{OL} (8) | | I _{OL} =2mA | 2.2 to 5.5 | | 0.4 | | |
| Pull-up resistance | R _{pu} (1) | Ports 0, 1, 2 P70 | V _{OH} =0.9V _{DD} When Port 0 selected low-impedance pull-up. | 4.5 to 5.5 | 15 | 35 | 80 | kΩ |
| | R _{pu} (2) | | | 2.2 to 4.5 | 18 | 50 | 230 | |
| | R _{pu} (3) | Port 0 | V _{OH} =0.9V _{DD} When Port 0 selected high-impedance pull-up. | 2.2 to 5.5 | 100 | 210 | 400 | |
| Hysteresis voltage | V _{HYS} (1) | Ports 1, 2 P70 $\overline{\text{RES}}$ | | 2.7 to 5.5 | | 0.1V _{DD} | | V |
| | V _{HYS} (2) | | | 2.2 to 5.5 | | 0.07V _{DD} | | |
| Pin capacitance | CP | All pins | For pins other than that under test: V _{IN} =V _{SS} f=1MHz Ta=25°C | 2.2 to 5.5 | | 10 | | pF |

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Serial I/O Characteristics at Ta = -40°C to +85°C, VSS1 = 0V (Note 4)

| Parameter | Symbol | Pin/ Remarks | Conditions | Specification | | | | | | |
|---------------|-------------------|------------------------|-----------------------|--|---|--------------------|-----|--------------------|----|------|
| | | | | VDD[V] | min | typ | max | unit | | |
| Serial clock | Input clock | Frequency | tSCK(3) | SCK1(P15) | See Fig. 5. | 2.2 to 5.5 | 2 | | | tCYC |
| | | Low level pulse width | tSCKL(3) | | | | 1 | | | |
| | | High level pulse width | tSCKH(3) | | | | 1 | | | |
| | Output clock | Frequency | tSCK(4) | SCK1(P15) | <ul style="list-style-type: none"> • CMOS output selected • See Fig. 5. | 2.2 to 5.5 | 2 | | | tSCK |
| | | Low level pulse width | tSCKL(4) | | | | 1/2 | | | |
| | | High level pulse width | tSCKH(4) | | | | 1/2 | | | |
| Serial input | Data setup time | tsDI(2) | SB1(P14), S1(P14) | <ul style="list-style-type: none"> • Must be specified with respect to rising edge of SIOCLK. • See Fig. 5. | 2.2 to 5.5 | (1/3)tCYC +0.01 | | | μs | |
| | Data hold time | thDI(2) | | | | 0.01 | | | | |
| Serial output | Output delay time | tdD0(4) | SO1(P13), SB1(P14) | <ul style="list-style-type: none"> • Must be specified with respect to falling edge of SIOCLK. • Must be specified as the time to the beginning of output state change in open drain output mode. • See Fig. 5. | 2.2 to 5.5 | | | (1/2)tCYC +0.05 | μs | |

Note 4: These specifications are theoretical values. Add margin depending on its use.

Pulse Input Conditions at Ta = -40°C to +85°C, VSS1 = 0V

| Parameter | Symbol | Pin/Remarks | Conditions | Specification | | | | |
|----------------------------|--------------------|---|---|-------------------------|------------|-----|-----|------|
| | | | | VDD[V] | min | typ | max | unit |
| High/low level pulse width | tPIH(1) tPIL(1) | INT0(P70), INT1(P17), INT2(P16), INT4(P20 to P21), | <ul style="list-style-type: none"> • Interrupt source flag can be set. • Event inputs for timer 0 or 1 are enabled. | 2.2 to 5.5 | 1 | | | tCYC |
| | tPIH(2) tPIL(2) | INT3(P15) when noise filter time constant is 1/1 | <ul style="list-style-type: none"> • Interrupt source flag can be set. • Event inputs for timer 0 are enabled. | 2.2 to 5.5 | 2 | | | |
| | tPIH(3) tPIL(3) | INT3(P15) when noise filter time constant is 1/32 | <ul style="list-style-type: none"> • Interrupt source flag can be set. • Event inputs for timer 0 are enabled. | 2.2 to 5.5 | 64 | | | |
| | tPIH(4) tPIL(4) | INT3(P15) when noise filter time constant is 1/128 | <ul style="list-style-type: none"> • Interrupt source flag can be set. • Event inputs for timer 0 are enabled. | 2.2 to 5.5 | 256 | | | |
| | tPIL(5) | $\overline{\text{RES}}$ | | • Resetting is enabled. | 2.2 to 5.5 | 200 | | |

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AD Converter Characteristics at Ta = -40°C to +85°C, V_{SS1} = 0V

12bits AD Converter Mode

| Parameter | Symbol | Pin/Remarks | Conditions | Specification | | | | | |
|----------------------------|-------------------|--------------------------------------|---|---------------------|------------|-----------------|-----|-----------------|-----|
| | | | | V _{DD} [V] | min | typ | max | unit | |
| Resolution | N | AN0(P00) to AN6(P06), AN8(P70) | | 2.4 to 5.5 | | 12 | | bit | |
| Absolute accuracy | ET | | (Note 6-1) | | 2.7 to 5.5 | | | ±16 | LSB |
| | | | | | 2.4 to 5.5 | | | ±20 | |
| Conversion time | TCAD | | • See Conversion time calculation formulas. (Note 6-2) | | 4.0 to 5.5 | 32 | | 115 | μs |
| | | | | | 2.7 to 5.5 | 64 | | 115 | |
| | | | | | 2.4 to 5.5 | 410 | | 425 | |
| Analog input voltage range | VAIN | | | | 2.4 to 5.5 | V _{SS} | | V _{DD} | V |
| Analog port input current | I _{AINH} | | V _{AIN} =V _{DD} | 2.4 to 5.5 | | | 1 | μA | |
| | I _{AINL} | | V _{AIN} =V _{SS} | 2.4 to 5.5 | -1 | | | | |

8bits AD Converter Mode

| Parameter | Symbol | Pin/Remarks | Conditions | Specification | | | | | |
|----------------------------|-------------------|-------------------------------------|---|---------------------|------------|-----------------|-----|-----------------|-----|
| | | | | V _{DD} [V] | min | typ | max | unit | |
| Resolution | N | AN0(P00) to AN6(P06) AN8(P70) | | 2.4 to 5.5 | | 8 | | bit | |
| Absolute accuracy | ET | | (Note 6-1) | | 2.4 to 5.5 | | | ±1.5 | LSB |
| | | | | | | | | | |
| Conversion time | TCAD | | • See Conversion time calculation formulas. (Note 6-2) | | 4.0 to 5.5 | 20 | | 90 | μs |
| | | | | | 2.7 to 5.5 | 40 | | 90 | |
| | | | | | 2.4 to 5.5 | 250 | | 265 | |
| Analog input voltage range | VAIN | | | | 2.4 to 5.5 | V _{SS} | | V _{DD} | V |
| Analog port input current | I _{AINH} | | V _{AIN} =V _{DD} | 2.4 to 5.5 | | | 1 | μA | |
| | I _{AINL} | | V _{AIN} =V _{SS} | 2.4 to 5.5 | -1 | | | | |

Conversion time calculation formulas:

$$12\text{bits AD Converter Mode: TCAD(Conversion time)} = ((52/(\text{AD division ratio}))+2) \times (1/3) \times t\text{CYC}$$

$$8\text{bits AD Converter Mode: TCAD(Conversion time)} = ((32/(\text{AD division ratio}))+2) \times (1/3) \times t\text{CYC}$$

| External oscillation (F _{mCF}) | Operating supply voltage range (V _{DD}) | System division ratio (SYS _{SDIV}) | Cycle time (t _{CYC}) | AD division ratio (AD _{DIV}) | AD conversion time (TCAD) | |
|--|---|--|--------------------------------|--|---------------------------|---------|
| | | | | | 12bit AD | 8bit AD |
| CF-12MHz | 4.0V to 5.5V | 1/1 | 250ns | 1/8 | 34.8μs | 21.5μs |
| | 3.0V to 5.5V | 1/1 | 250ns | 1/16 | 69.5μs | 42.8μs |
| CF-10MHz | 4.0V to 5.5V | 1/1 | 300ns | 1/8 | 41.8μs | 25.8μs |
| | 3.0V to 5.5V | 1/1 | 300ns | 1/16 | 83.4μs | 51.4μs |
| CF-4MHz | 3.0V to 5.5V | 1/1 | 750ns | 1/8 | 104.5μs | 64.5μs |
| | 2.4V to 5.5V | 1/1 | 750ns | 1/32 | 416.5μs | 256.5μs |

Note 6-1: The quantization error (±1/2LSB) must be excluded from the absolute accuracy. The absolute accuracy must be measured in the microcontroller's state in which no I/O operations occur at the pins adjacent to the analog input channel.

Note 6-2: The conversion time refers to the period from the time an instruction for starting a conversion process till the time the conversion results register(s) are loaded with a complete digital conversion value corresponding to the analog input value.

The conversion time is 2 times the normal-time conversion time when:

- The first AD conversion is performed in the 12-bit AD conversion mode after a system reset.
- The first AD conversion is performed after the AD conversion mode is switched from 8-bit to 12-bit conversion mode.

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Power-on Reset (POR) Characteristics at Ta = -40°C to +85°C, VSS1 = 0V

| Parameter | Symbol | Pin/Remarks | Conditions | Specification | | | | |
|---------------------------------|--------|-------------|---|-------------------------|------|------|------|------|
| | | | | Option selected voltage | min | typ | max | unit |
| POR release voltage | PORRL | | <ul style="list-style-type: none"> Select from option. (Note 7-1) | 1.67V | 1.55 | 1.67 | 1.79 | V |
| | | | | 1.97V | 1.85 | 1.97 | 2.09 | |
| | | | | 2.07V | 1.95 | 2.07 | 2.19 | |
| | | | | 2.37V | 2.25 | 2.37 | 2.49 | |
| | | | | 2.57V | 2.45 | 2.57 | 2.69 | |
| | | | | 2.87V | 2.75 | 2.87 | 2.99 | |
| | | | | 3.86V | 3.73 | 3.86 | 3.99 | |
| | | | | 4.35V | 4.21 | 4.35 | 4.49 | |
| Detection voltage unknown state | POUKS | | <ul style="list-style-type: none"> See Fig. 7. (Note 7-2) | | | 0.7 | 0.95 | |
| Power supply rise time | PORIS | | <ul style="list-style-type: none"> Power supply rise time from 0V to 1.6V. | | | | 100 | ms |

Note7-1: The POR release level can be selected out of 4 levels only when the LVD reset function is disabled.

Note7-2: POR is in an unknown state before transistors start operation.

Low Voltage Detection Reset (LVD) Characteristics at Ta = -40°C to +85°C, VSS1 = 0V

| Parameter | Symbol | Pin/Remarks | Conditions | Specification | | | | |
|---|--------|-------------|--|-------------------------|-------|------|------|------|
| | | | | Option selected voltage | min | typ | max | unit |
| LVD reset Voltage (Note 8-2) | LVDET | | <ul style="list-style-type: none"> Select from option. (Note 8-1) (Note 8-3) See Fig. 8. | 1.91V | 1.81 | 1.91 | 2.01 | V |
| | | | | 2.01V | 1.91 | 2.01 | 2.11 | |
| | | | | 2.31V | 2.21 | 2.31 | 2.41 | |
| | | | | 2.51V | 2.41 | 2.51 | 2.61 | |
| | | | | 2.81V | 2.71 | 2.81 | 2.91 | |
| | | | | 3.79V | 3.69 | 3.79 | 3.89 | |
| | | | | 4.28V | 4.18 | 4.28 | 4.38 | |
| | | | | LVD hysteresis width | LVHYS | | | |
| 2.01V | | 55 | | | | | | |
| 2.31V | | 55 | | | | | | |
| 2.51V | | 55 | | | | | | |
| 2.81V | | 60 | | | | | | |
| 3.79V | | 65 | | | | | | |
| 4.28V | | 65 | | | | | | |
| Detection voltage unknown state | LVUKS | | <ul style="list-style-type: none"> See Fig. 8. (Note 8-4) | | | 0.7 | 0.95 | V |
| Low voltage detection minimum Width (Reply sensitivity) | TLVDW | | <ul style="list-style-type: none"> LVDET-0.5V See Fig. 9. | | 0.2 | | | ms |

Note8-1: The LVD reset level can be selected out of 3 levels only when the LVD reset function is enabled.

Note8-2: LVD reset voltage specification values do not include hysteresis voltage.

Note8-3: LVD reset voltage may exceed its specification values when port output state changes and/or when a large current flows through port.

Note8-4: LVD is in an unknown state before transistors start operation.

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Consumption Current Characteristics at Ta = -40°C to +85°C, VSS1 = 0V

| Parameter | Symbol | Pin/ Remarks | Conditions | Specification | | | | |
|---|----------|------------------|--|---------------------|-----|------|------|------|
| | | | | V _{DD} [V] | min | typ | max | unit |
| Normal mode consumption current (Note 9-1) (Note 9-2) | IDDOP(1) | V _{DD1} | <ul style="list-style-type: none"> FmCF=12MHz ceramic oscillation mode System clock set to 12MHz side Internal medium speed RC oscillation stopped. | 2.7 to 5.5 | | 6.1 | 10 | mA |
| | | | | 2.7 to 3.6 | | 3.7 | 6.4 | |
| | IDDOP(2) | | <ul style="list-style-type: none"> FmCF=10MHz ceramic oscillation mode System clock set to 10MHz side Internal medium speed RC oscillation stopped. | 2.2 to 5.5 | | 5.3 | 9.1 | |
| | | | | 2.2 to 3.6 | | 3.4 | 5.8 | |
| | IDDOP(3) | | <ul style="list-style-type: none"> FmCF=4MHz ceramic oscillation mode System clock set to 4MHz side Internal medium speed RC oscillation stopped. | 2.2 to 5.5 | | 2.6 | 5.5 | |
| | | | | 2.2 to 3.6 | | 1.9 | 3.4 | |
| | IDDOP(4) | | <ul style="list-style-type: none"> CF oscillation low amplifier size selected. (CFLAMP=1) FmCF=4MHz ceramic oscillation mode System clock set to 4MHz side Internal medium speed RC oscillation stopped. | 2.2 to 5.5 | | 1.1 | 2.1 | |
| | | | | 2.2 to 3.6 | | 0.56 | 1.1 | |
| | IDDOP(5) | | <ul style="list-style-type: none"> External FmCF oscillation stopped. System clock set to internal medium speed RC oscillation. | 2.2 to 5.5 | | 0.47 | 1.2 | |
| | | | | 2.2 to 3.6 | | 0.28 | 0.65 | |
| | IDDOP(6) | | <ul style="list-style-type: none"> External FmCF oscillation stopped. Internal medium speed RC oscillation stopped. | 2.7 to 5.5 | | 4.2 | 8.1 | |
| | | | | 2.7 to 3.6 | | 3.3 | 5.6 | |
| | | | <ul style="list-style-type: none"> System clock set to 8MHz with frequency variable RC oscillation.(RCCTD=0) 1/1 frequency division ratio. | | | | | |

Note9-1: Values of the consumption current do not include current that flows into the output transistors and internal pull-up resistors.

Note9-2: The consumption current values do not include operational current of LVD function if not specified.

Continued on next page.

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Continued from preceding page.

| Parameter | Symbol | Pin/ Remarks | Conditions | Specification | | | | unit |
|---|------------|-------------------|---|---------------------|-----|------|------|------|
| | | | | V _{DD} [V] | min | typ | max | |
| HALT mode consumption current (Note 9-1) (Note 9-2) | IDDHALT(1) | V _{DD} 1 | <ul style="list-style-type: none"> • HALT mode • FmCF=12MHz ceramic oscillation mode • System clock set to 12MHz side • Internal medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio | 2.7 to 5.5 | | 2.3 | 4.1 | mA |
| | | | | 2.7 to 3.6 | | 1.2 | 1.9 | |
| | IDDHALT(2) | | <ul style="list-style-type: none"> • HALT mode • FmCF=10MHz ceramic oscillation mode • System clock set to 10MHz side • Internal medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio | 2.2to 5.5 | | 1.9 | 3.4 | |
| | | | | 2.2 to 3.6 | | 1.0 | 1.6 | |
| | IDDHALT(3) | | <ul style="list-style-type: none"> • HALT mode • FmCF=4MHz ceramic oscillation mode • System clock set to 4MHz side • Internal medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio | 2.2 to 5.5 | | 1.3 | 2.5 | |
| | | | | 2.2 to 3.6 | | 0.53 | 1.0 | |
| | IDDHALT(4) | | <ul style="list-style-type: none"> • HALT mode • CF oscillation low amplifier size selected. (CFLAMP=1) • FmCF=4MHz ceramic oscillation mode • System clock set to 4MHz side • Internal medium speed RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/4 frequency division ratio | 2.2 to 5.5 | | 0.80 | 1.5 | |
| | | | | 2.2 to 3.6 | | 0.31 | 0.62 | |
| | IDDHALT(5) | | <ul style="list-style-type: none"> • HALT mode • External FmCF oscillation stopped. • System clock set to internal medium speed RC oscillation • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio | 2.2 to 5.5 | | 0.28 | 0.73 | |
| | | | | 2.2 to 3.6 | | 0.14 | 0.36 | |
| | IDDHALT(6) | | <ul style="list-style-type: none"> • HALT mode • External FmCF oscillation stopped. • Internal medium speed RC oscillation stopped. • System clock set to 8MHz with frequency variable RC oscillation. (RCCTD=0) • 1/1 frequency division ratio. | 2.7 to 5.5 | | 1.3 | 2.7 | |
| | | | | 2.7 to 3.6 | | 0.93 | 1.8 | |
| HOLD mode consumption current (Note 9-1) (Note 9-2) | IDDHOLD(1) | V _{DD} 1 | <ul style="list-style-type: none"> • HOLD mode • CF1=V_{DD} or open (External clock mode) | 2.2 to 5.5 | | 0.03 | 25 | μA |
| | | | | 2.2 to 3.6 | | 0.02 | 5.9 | |
| | IDDHOLD(2) | | <ul style="list-style-type: none"> • HOLD mode • CF1=V_{DD} or open (External clock mode) • Ta=-10 to +50°C | 5.0 | | 0.03 | 1.2 | |
| | | | | 3.3 | | 0.02 | 0.56 | |
| | | | | 2.5 | | 0.01 | 0.40 | |
| | IDDHOLD(3) | | <ul style="list-style-type: none"> • HOLD mode • CF1=V_{DD} or open (External clock mode) • LVD option selected | 2.2 to 5.5 | | 3.0 | 29 | |
| | | | | 2.2 to 3.6 | | 2.3 | 10 | |
| | IDDHOLD(4) | | <ul style="list-style-type: none"> • HOLD mode • CF1=V_{DD} or open (External clock mode) • Ta=-10 to +50°C • LVD option selected | 5.0 | | 3.0 | 7.3 | |
| 3.3 | | | | 2.3 | 3.4 | | | |
| 2.5 | | | | 2.0 | 2.9 | | | |

Note9-1: Values of the consumption current do not include current that flows into the output transistors and internal pull-up resistors.

Note9-2: The consumption current values do not include operational current of LVD function if not specified.

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F-ROM Programming Characteristics at Ta = +10°C to +55°C, VSS1 = 0V

| Parameter | Symbol | Pin/Remarks | Conditions | Specification | | | | |
|-----------------------------|----------|------------------|------------------------------------|---------------------|-----|-----|-----|------|
| | | | | V _{DD} [V] | min | typ | max | unit |
| Onboard programming current | IDDFW(1) | V _{DD1} | • Only current of the flash block. | 2.2 to 5.5 | | 5 | 10 | mA |
| Programming time | tFW(1) | | • Erasing time | 2.2 to 5.5 | | 20 | 30 | ms |
| | tFW(2) | | • Programming time | | | 40 | 60 | μs |

Characteristics of a Sample Main System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a Our designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Oscillator

- CF oscillation normal amplifier size selected (CFLAMP=0)

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| Nominal Frequency | Type | Oscillator Name | Circuit Constant | | | | Operating Voltage Range [V] | Oscillation Stabilization Time | | Remarks |
|-------------------|------|-----------------|------------------|---------|--------|--------|-----------------------------|--------------------------------|----------|----------------|
| | | | C1 [pF] | C2 [pF] | Rf [Ω] | Rd [Ω] | | typ [ms] | max [ms] | |
| 12MHz | SMD | CSTCE12M0G52-R0 | (10) | (10) | Open | 680 | 2.2 to 5.5 | 0.1 | 0.5 | Internal C1,C2 |
| | | | | | Open | 1.0k | 2.5 to 5.5 | 0.1 | 0.5 | |
| 10MHz | SMD | CSTCE10M0G52-R0 | (10) | (10) | Open | 680 | 2.0 to 5.5 | 0.1 | 0.5 | |
| | | | | | Open | 1.0k | 2.1 to 5.5 | 0.1 | 0.5 | |
| | LEAD | CSTLS10M0G53-B0 | (15) | (15) | Open | 680 | 2.2 to 5.5 | 0.1 | 0.5 | |
| | | | | | Open | 1.0k | 2.4 to 5.5 | 0.1 | 0.5 | |
| 8MHz | SMD | CSTCE8M00G52-R0 | (10) | (10) | Open | 1.0k | 1.9 to 5.5 | 0.1 | 0.5 | |
| | | | | | Open | 1.5k | 2.0 to 5.5 | 0.1 | 0.5 | |
| | LEAD | CSTLS8M00G53-B0 | (15) | (15) | Open | 1.0k | 2.0 to 5.5 | 0.1 | 0.5 | |
| | | | | | Open | 1.5k | 2.2 to 5.5 | 0.1 | 0.5 | |
| 6MHz | SMD | CSTCR6M00G53-R0 | (15) | (15) | Open | 1.5k | 1.9 to 5.5 | 0.1 | 0.5 | |
| | | | | | Open | 2.2k | 2.0 to 5.5 | 0.1 | 0.5 | |
| | LEAD | CSTLS6M00G53-B0 | (15) | (15) | Open | 1.5k | 2.0 to 5.5 | 0.1 | 0.5 | |
| | | | | | Open | 2.2k | 2.1 to 5.5 | 0.1 | 0.5 | |
| 4MHz | SMD | CSTCR4M00G53-R0 | (15) | (15) | Open | 1.5k | 1.8 to 5.5 | 0.2 | 0.6 | |
| | | | | | Open | 3.3k | 1.9 to 5.5 | 0.2 | 0.6 | |
| | LEAD | CSTLS4M00G53-B0 | (15) | (15) | Open | 1.5k | 1.8 to 5.5 | 0.2 | 0.6 | |
| | | | | | Open | 3.3k | 1.9 to 5.5 | 0.2 | 0.6 | |

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- CF oscillation low amplifier size selected (CFLAMP=1)

■ MURATA

| Nominal Frequency | Type | Oscillator Name | Circuit Constant | | | | Operating Voltage Range [V] | Oscillation Stabilization Time | | Remarks |
|-------------------|------|--------------------|------------------|---------|-----------------|-----------------|-----------------------------|--------------------------------|----------|----------------|
| | | | C1 [pF] | C2 [pF] | Rf [Ω] | Rd [Ω] | | typ [ms] | max [ms] | |
| 4MHz | SMD | CSTCR4M00G53-R0 | (15) | (15) | Open | 1.0k | 1.9 to 5.5 | 0.2 | 0.6 | Internal C1,C2 |
| | | | | | Open | 2.2k | 2.1 to 5.5 | 0.2 | 0.6 | |
| | | CSTCR4M00G53095-R0 | (15) | (15) | Open | 1.0k | 1.8 to 5.5 | 0.2 | 0.6 | |
| | | | | | Open | 2.2k | 1.9 to 5.5 | 0.2 | 0.6 | |
| | LEAD | CSTLS4M00G53-B0 | (15) | (15) | Open | 1.0k | 2.0 to 5.5 | 0.2 | 0.6 | |
| | | | | | Open | 2.2k | 2.1 to 5.5 | 0.2 | 0.6 | |
| | | CSTLS4M00G53095-B0 | (15) | (15) | Open | 1.0k | 1.8 to 5.5 | 0.2 | 0.6 | |
| | | | | | Open | 2.2k | 1.9 to 5.5 | 0.2 | 0.6 | |

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after VDD goes above the operating voltage lower limit (see Figure 3).

- Time till the oscillation gets stabilized after the CPU reset state is released.
- Till the oscillation gets stabilized after the instruction for starting the main clock oscillation circuit is executed.
- Till the oscillation gets stabilized after the HOLD mode is reset.

(Notes on the implementation of the oscillator circuit)

- Oscillation is influenced by the circuit pattern layout of printed circuit board. Place the oscillation-related components as close to the CPU chip and to each other as possible with the shortest possible pattern length.
- Keep the signal lines whose state changes suddenly or in which large current flows as far away from the oscillator circuit as possible and make sure that they do not cross one another.
- Be sure to insert a current limiting resistor (Rd) so that the oscillation amplitude never exceeds the input voltage level that is specified as the absolute maximum rating.
- The oscillator circuit constants shown above are sample characteristic values that are measured using the Our designated oscillation evaluation board. Since the accuracy of the oscillation frequency and other characteristics vary according to the board on which the IC is installed, it is recommended that the user consult the resonator vendor for oscillation evaluation of the IC on a user's production board when using the IC for applications that require high oscillation accuracy. For further information, contact your resonator vendor or Our company Semiconductor sales representative serving your locality.
- It must be noted, when replacing the flash ROM version of a microcontroller with a mask ROM version, that their operating voltage ranges may differ even when the oscillation constant of the external oscillator is the same.

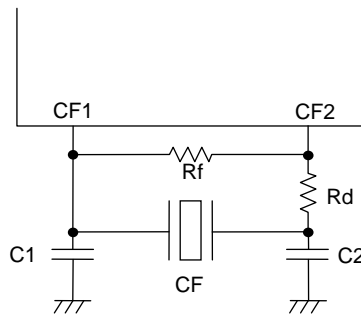


Figure 1 CF Oscillator Circuit

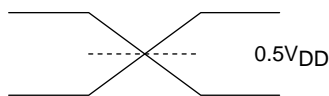
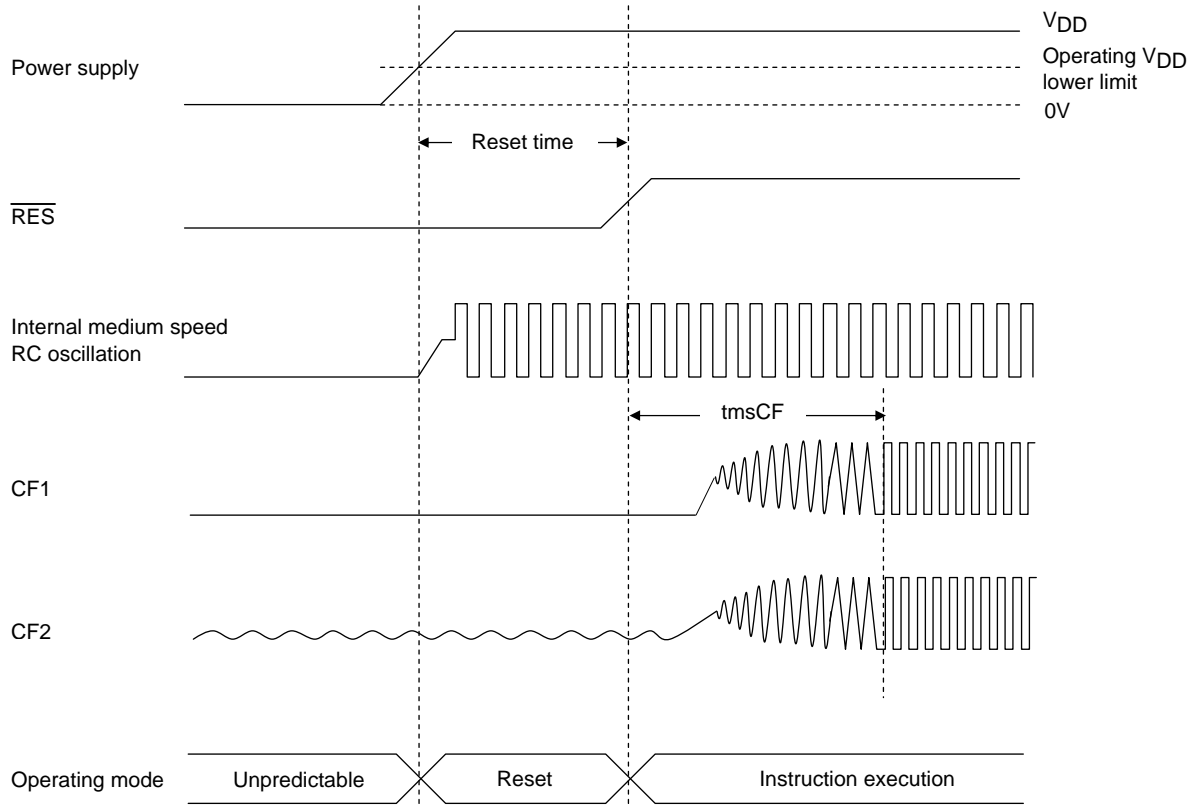
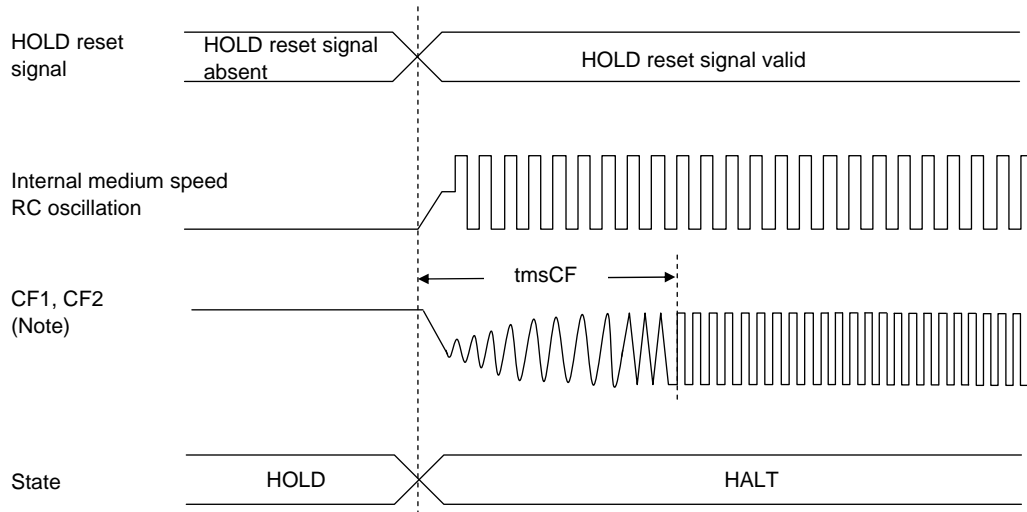


Figure 2 AC Timing Measurement Point

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Reset Time and Oscillation Stabilization Time

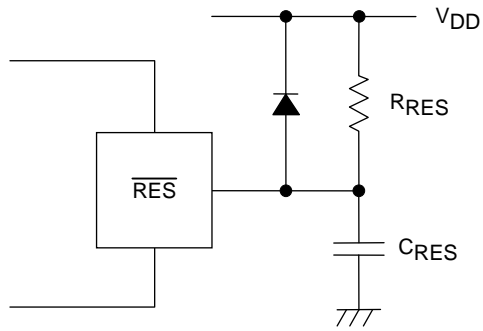


HOLD Reset Signal and Oscillation Stabilization Time

Note: External oscillation circuit is selected.

Figure 3 Oscillation Stabilization Times

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Note:
External circuits for reset may vary depending on the usage of POR and LVD. Please refer to the user's manual for more information..

Figure 4 Reset Circuit

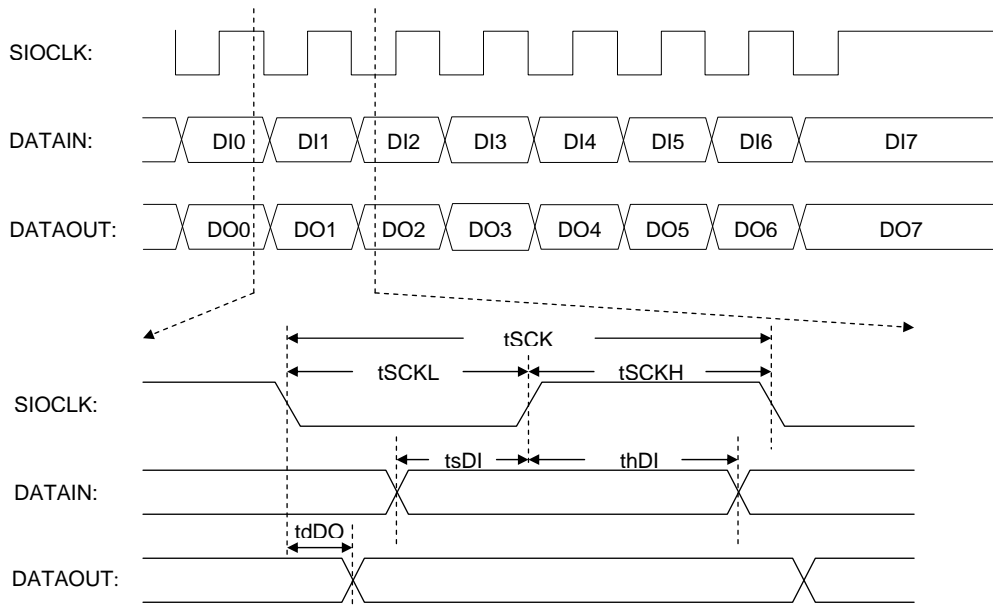


Figure 5 Serial I/O Output Waveforms

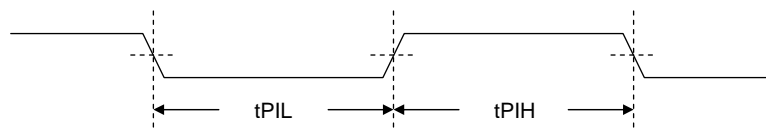


Figure 6 Pulse Input Timing Signal Waveform

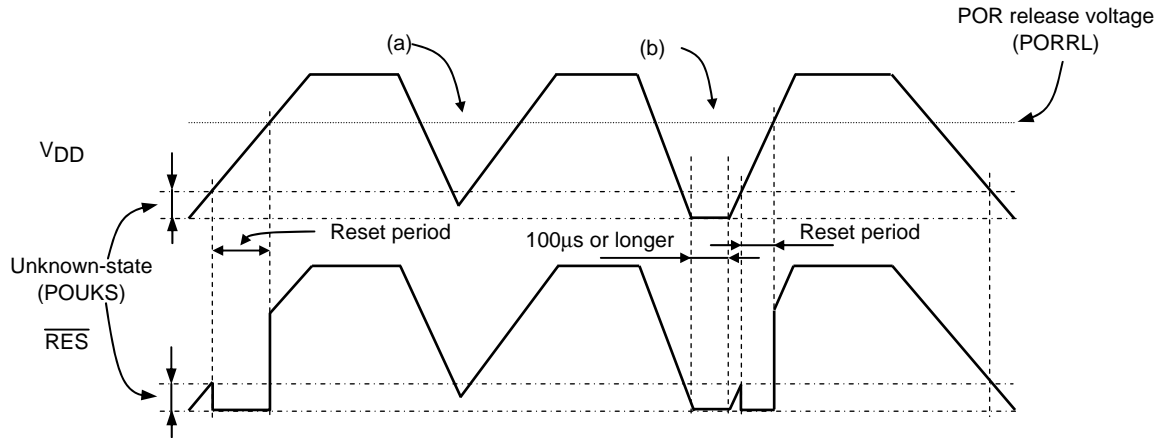


Figure 7 Waveform observed when only POR is used (LVD not used)
(RESET pin: Pull-up resistor RRES only)

- The POR function generates a reset only when power is turned on starting at the V_{SS} level.
- No stable reset will be generated if power is turned on again when the power level does not go down to the V_{SS} level as shown in (a). If such a case is anticipated, use the LVD function together with the POR function or implement an external reset circuit.
- A reset is generated only when the power level goes down to the V_{SS} level as shown in (b) and power is turned on again after this condition continues for $100\mu\text{s}$ or longer.

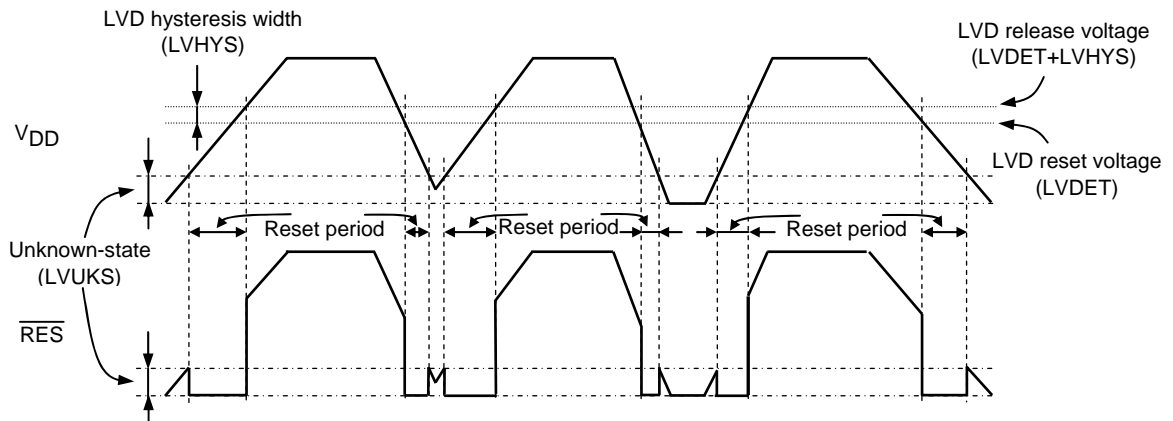


Figure 8 Waveform observed when both POR and LVD functions are used
(RESET pin: Pull-up resistor RRES only)

- Resets are generated both when power is turned on and when the power level lowers.
- A hysteresis width (LVHYS) is provided to prevent the repetitions of reset release and entry cycles near the detection level.

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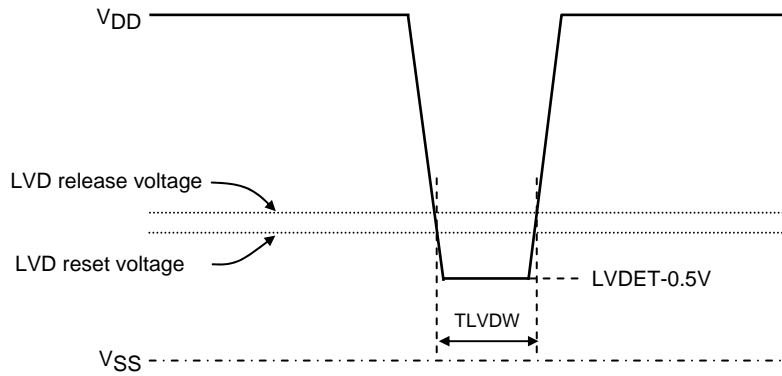


Figure 9 Low voltage detection minimum width
(Example of momentary power loss / Voltage variation waveform)

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