Low Voltage Dual D-Type Positive Edge-Triggered Flip-Flop with 5 V Tolerant Inputs

74LCX74

General Description

The LCX74 is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary (Q, $\overline{Q}$) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

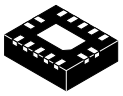
Asynchronous Inputs:

- LOW input to $\overline{S}_D$ (Set) sets Q to HIGH level
- LOW input to $\overline{C}_D$ (Clear) sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on $\overline{C}_D$ and $\overline{S}_D$ makes both Q and $\overline{Q}$ HIGH

Features

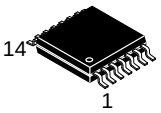
- 5 V Tolerant Inputs
- 1.65 V − 5.5 V V_{CC} Specifications Provided
- 7.0 ns t_{PD} Max. (V_{CC} = 3.3 V)
- 10 μA I_{CC} Max.
- Power Down High Impedance Inputs and Outputs
- ±24 mA Output Drive (V_{CC} = 3.0 V)
- Implements Proprietary Noise/EMI Reduction Circuitry
- Latch-up Performance Exceeds JEDEC 78 Conditions
- ESD Performance:
  - Human Body Model > 2000 V
- These Devices are Pb-Free, Halide Free and are RoHS Compliant

MARKING DIAGRAMS

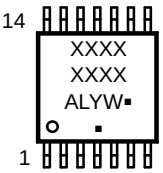


QFN14 3.0x2.5, 0.5P
CASE 510CB

XXXXXX = Specific Device Code
Z = Assembly Plant Code
XY = Date Code (Year & Week)
KK = Lot Run Traceability Code



TSSOP−14 WB
DT SUFFIX
CASE 948G



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

Connection Diagrams

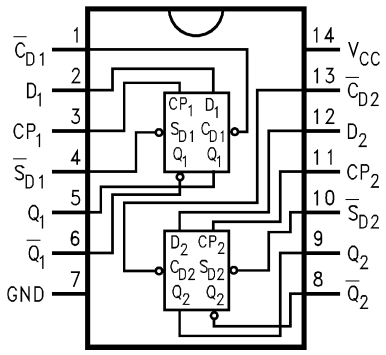
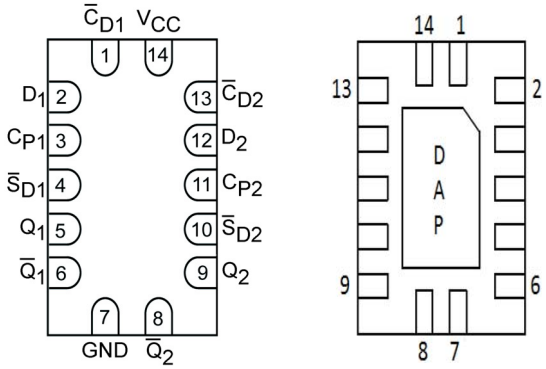


Figure 1. Pin Assignment for TSSOP



(Top View) (Bottom View)

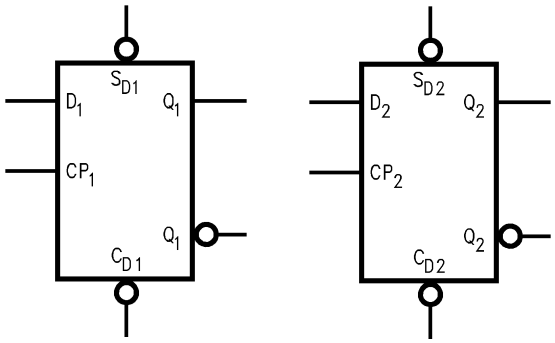
Figure 2. Pin Assignment for DQFN

PIN DESCRIPTION

Pin Names	Description
D_1, D_2	Data Inputs
CP_1, CP_2	Clock Pulse Inputs
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs
Q_1, $\overline{Q}_1$, Q_2, $\overline{Q}_2$	Outputs
DAP	No Connect

1. DAP (Die Attach Pad)

Logic Symbols



IEEE/IEC

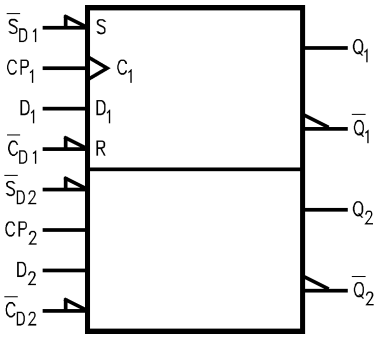


Figure 3. Logic Symbols

TRUTH TABLE (Each Half)

Input				Outputs	
$\overline{S}_D$	$\overline{C}_D$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	↗	H	H	L
H	H	↗	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↗ = LOW-to-HIGH Clock Transition
Q_0 ($\overline{Q}_0$) = Previous Q ($\overline{Q}$) before LOW-to-HIGH Transition of Clock

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +6.5	V
V_I	DC Input Voltage (Note 2)		−0.5 to +6.5	V
V_O	DC Output Voltage (Note 2)	Active-Mode (High or Low State)	−0.5 to V_{CC} + 0.5	V
		Tri-State Mode	−0.5 to +6.5	
		Power-Down Mode (V_{CC} = 0 V)	−0.5 to +6.5	
I_{IK}	DC Input Diode Current V_I < GND		−50	mA
I_{OK}	DC Output Diode Current V_O < GND		−50	mA
I_O	DC Output Source/Sink Current		±50	mA
I_{CC} or I_{GND}	DC Supply Current per Supply Pin or Ground Pin		±100	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 2)	QFN14	130	°C/W
		TSSOP−14	150	
P_D	Power Dissipation in Still Air at 125°C	QFN14	962	mW
		TSSOP−14	833	
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage (Note 4)	Human Body Model	2000	V
		Charged Device Model	N/A	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. I_O absolute maximum rating must be observed.
3. Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2-ounce copper trace no air flow per JESD51−7.
4. HBM tested to EIA / JESD22−A114−A. CDM tested to JESD22−C101−A. JEDEC recommends that ESD qualification to EIA/JESD22−A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	Operating	1.65	2.5, 3.3	5.5	V
		Data Retention Only	1.5	2.5, 3.3	5.5	
V_I	Digital Input Voltage		0	−	5.5	V
V_O	Output Voltage	Active Mode (High or Low State)	0	−	V_{CC}	V
		Tri-State Mode	0	−	5.5	
		Power Down Mode (V_{CC} = 0 V)	0	−	5.5	
T_A	Operating Free-Air Temperature		−40	−	+125	°C
t_r, t_f	Input Rise or Fall Rate	V_{CC} = 1.65 V to 1.95 V	0	−	20	nS/V
		V_{CC} = 2.3 V to 2.7 V	0	−	20	
		V_{IN} from 0.8 V to 2.0 V, V_{CC} = 3.0 V	0	−	10	
		V_{CC} = 4.5 V to 5.5 V	0	−	5	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

5. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		T_A = −40°C to +125°C		Unit
				Min	Max	Min	Max	
V_{IH}	HIGH Level Input Voltage		1.65 – 1.95	0.65 x V_{CC}	–	0.65 x V_{CC}	–	V
			2.3 – 2.7	1.7	–	1.7	–	
			3.0 – 3.6	2.0	–	2.0	–	
			4.5 – 5.5	0.70 x V_{CC}	–	0.70 x V_{CC}	–	
V_{IL}	LOW Level Input Voltage		1.65 – 1.95	–	0.35 x V_{CC}	–	0.35 x V_{CC}	V
			2.3 – 2.7	–	0.7	–	0.7	
			3.0 – 3.6	–	0.8	–	0.8	
			4.5 – 5.5	–	0.30 x V_{CC}	–	0.30 x V_{CC}	
V_{OH}	High-Level Output Voltage	V_I = V_{IH} or V_{IL}						V
		I_{OH} = −100 μA	1.65 to 5.5	V_{CC} – 0.1	–	V_{CC} – 0.1	–	
		I_{OH} = −4 mA	1.65	1.29	–	1.29	–	
		I_{OH} = −8 mA	2.3	1.8	–	1.8	–	
		I_{OH} = −12 mA	2.7	2.2	–	2.2	–	
		I_{OH} = −16 mA	3.0	2.4	–	2.4	–	
		I_{OH} = −24 mA	3.0	2.2	–	2.2	–	
		I_{OH} = −32 mA	4.5	3.7	–	3.7	–	
V_{OL}	Low-Level Output Voltage	V_I = V_{IH} or V_{IL}						V
		I_{OL} = 100 μA	1.65 to 5.5	–	0.1	–	0.1	
		I_{OL} = 4 mA	1.65	–	0.24	–	0.24	
		I_{OL} = 8 mA	2.3	–	0.3	–	0.3	
		I_{OL} = 12 mA	2.7	–	0.4	–	0.4	
		I_{OL} = 16 mA	3.0	–	0.4	–	0.4	
		I_{OL} = 24 mA	3.0	–	0.55	–	0.55	
		I_{OL} = 32 mA	4.5	–	0.6	–	0.6	
I_I	Input Leakage Current	V_I = 0 to 5.5 V	3.6	–	±5.0	–	±5.0	μA
I_{OFF}	Power Off Leakage Current	V_I = 5.5 V or V_O = 5.5 V	0	–	10	–	10	μA
I_{CC}	Quiescent Supply Current	V_I = 5.5 V or GND	3.6	–	10	–	10	μA
ΔI_{CC}	Increase in I_{CC} per Input	V_{IH} = V_{CC} – 0.6 V	2.3 to 3.6	–	500	–	500	μA

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	V_{CC} (V)	T_A = −40°C to +85°C		T_A = −40°C to +125°C		Unit
				Min	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay, CP_n to (Q_n or $\overline{Q}_n$)	Waveform 1	1.65 to 1.95	–	12.5	–	12.5	ns
			2.3 to 2.7	–	8.4	–	8.4	
			2.7	–	8.0	–	8.0	
			3.0 to 3.6	–	7.0	–	7.0	
			4.5 to 5.5	–	5.0	–	5.0	
t_{PLH}, t_{PHL}	Propagation Delay, ($\overline{S}_{Dn}$ or $\overline{C}_{Dn}$) to (Q_n or $\overline{Q}_n$)	Waveform 2	1.65 to 1.95	–	12.5	–	12.5	ns
			2.3 to 2.7	–	8.4	–	8.4	
			2.7	–	8.0	–	8.0	
			3.0 to 3.6	–	7.0	–	7.0	
			4.5 to 5.5	–	5.0	–	5.0	

AC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	V_{CC} (V)	T_A = −40°C to +85°C		T_A = −40°C to +125°C		Unit
				Min	Max	Min	Max	
f_{max}	Clock Pulse Frequency	Waveform 1	1.65 to 1.95	90	−	90	−	MHz
			2.3 to 2.7	150	−	150	−	
			2.7	150	−	150	−	
			3.0 to 3.6	150	−	150	−	
			4.5 to 5.5	150	−	150	−	
t_s	Setup Time	Waveform 1	1.65 to 1.95	4.0	−	4.0	−	ns
			2.3 to 2.7	4.0	−	4.0	−	
			2.7	2.5	−	2.5	−	
			3.0 to 3.6	2.5	−	2.5	−	
			4.5 to 5.5	2.5	−	2.5	−	
t_h	Hold Time	Waveform 1	1.65 to 1.95	2.0	−	2.0	−	ns
			2.3 to 2.7	2.0	−	2.0	−	
			2.7	1.5	−	1.5	−	
			3.0 to 3.6	1.5	−	1.5	−	
			4.5 to 5.5	1.5	−	1.5	−	
t_W	Pulse Width, CP_n	Waveform 4	1.65 to 1.95	4.0	−	4.0	−	ns
			2.3 to 2.7	4.0	−	4.0	−	
			2.7	3.3	−	3.3	−	
			3.0 to 3.6	3.3	−	3.3	−	
			4.5 to 5.5	3.3	−	3.3	−	
	Pulse Width, $\overline{S_{Dn}}$ or $\overline{C_{Dn}}$	Waveform 4	1.65 to 1.95	4.0	−	4.0	−	ns
			2.3 to 2.7	4.0	−	4.0	−	
			2.7	3.6	−	3.6	−	
			3.0 to 3.6	3.3	−	3.3	−	
			4.5 to 5.5	3.3	−	3.3	−	
t_{rec}	Recovery Time	Waveform 3	1.65 to 1.95	4.5	−	4.5	−	ns
			2.3 to 2.7	4.5	−	4.5	−	
			2.7	3.0	−	3.0	−	
			3.0 to 3.6	2.5	−	2.5	−	
			4.5 to 5.5	2.5	−	2.5	−	
t_{OSHL}, t_{OSLH}	Output to Output Skew		1.65 to 1.95	−	−	−	−	ns
			2.3 to 2.7	−	−	−	−	
			2.7	−	−	−	−	
			3.0 to 3.6	−	1.0	−	1.0	
			4.5 to 5.5	−	−	−	−	

6. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH−to−LOW (t_{OSHL}) or LOW−to−HIGH (t_{OSLH}).

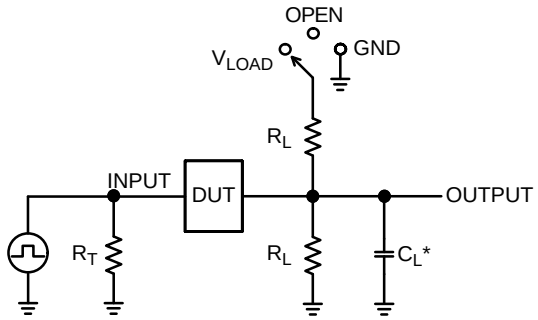
DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Parameter	Condition	V_{CC} (V)	T_A = +25°C Typ	Unit
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	C_L = 50 pF, V_{IH} = 3.3 V, V_{IL} = 0 V	3.3	0.8	V
		C_L = 30 pF, V_{IH} = 2.5 V, V_{IL} = 0 V	2.5	0.6	
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	C_L = 50 pF, V_{IH} = 3.3 V, V_{IL} = 0 V	3.3	–0.8	V
		C_L = 30 pF, V_{IH} = 2.5 V, V_{IL} = 0 V	2.5	–0.6	

CAPACITANCE

Symbol	Parameter	Condition	Typ	Unit
C_{IN}	Input Capacitance	V_{CC} = Open, V_I = 0 V or V_{CC}	7	pF
C_{OUT}	Output Capacitance	V_{CC} = 3.3 V, V_I = 0 V or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	V_{CC} = 3.3 V, V_I = 0 V or V_{CC}, f = 10 MHz	25	pF

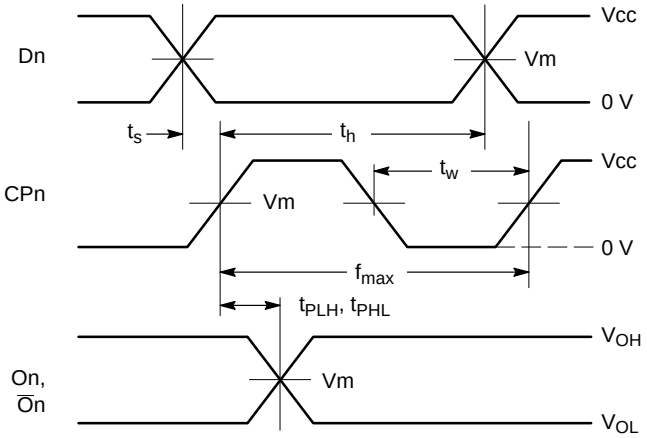
AC Loading and Waveforms (Generic for LCX Family)



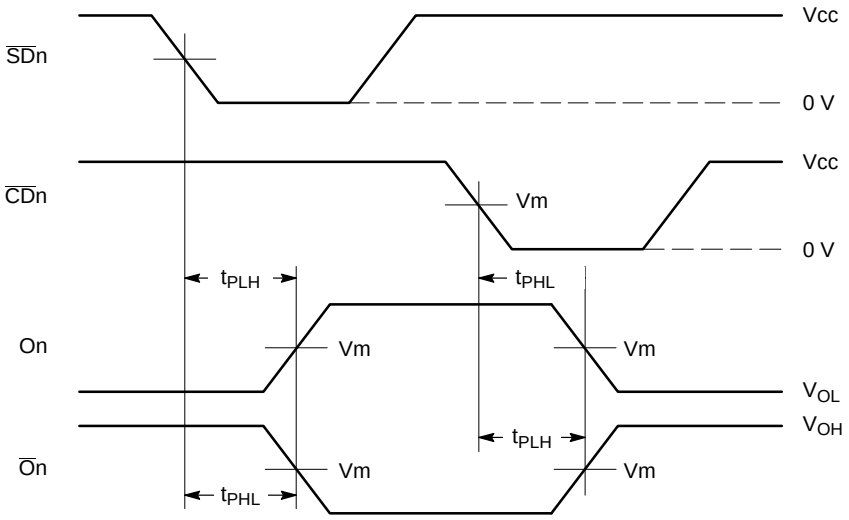
Test	Switch Position
t_{PLH} / t_{PHL}	Open
t_{PLZ} / t_{PZL}	V_{LOAD}
t_{PHZ} / t_{PZH}	GND

C_L includes probe and jig capacitance
R_T is Z_{OUT} of pulse generator (typically 50 Ω)
f = 1 MHz, t_W = 500 ns

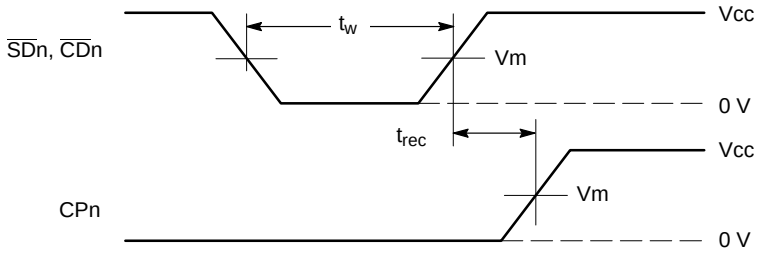
Figure 4. Test Circuit



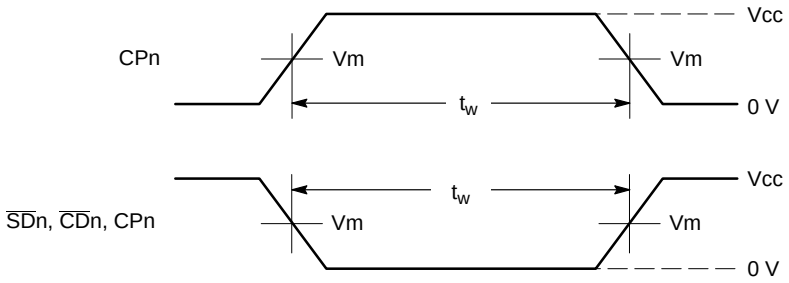
WAVEFORM 1 − PROPAGATION DELAYS, SETUP AND HOLD TIMES
t_R = t_F = 2.5 ns, 10% to 90%; f = 1 MHz; t_W = 500 ns



WAVEFORM 2 − PROPAGATION DELAYS
t_R = t_F = 2.5 ns, 10% to 90%; f = 1 MHz; t_W = 500 ns



WAVEFORM 3 − RECOVERY TIME
$t_R = t_F$ = 2.5 ns from 10% to 90%; f = 1 MHz; t_w = 500 ns



WAVEFORM 4 − PULSE WIDTH
$t_R = t_F$ = 2.5 ns (or fast as required) from 10% to 90%;
Output requirements: $V_{OL} \le 0.8$ V, $V_{OH} \ge 2.0$ V

V_{CC}, V	R_L, Ω	C_L, pF	V_{LOAD}	V_m, V	V_Y, V
1.65 to 1.95	500	30	2 x V_{CC}	V_{CC} / 2	0.15
2.3 to 2.7	500	30	2 x V_{CC}	V_{CC} / 2	0.15
2.7	500	50	6 V	1.5	0.3
3.0 to 3.6	500	50	6 V	1.5	0.3
4.5 to 5.5	500	50	2 x V_{CC}	V_{CC} / 2	0.3

Figure 5. Waveforms

Schematic Diagram (Generic for LCX Family)

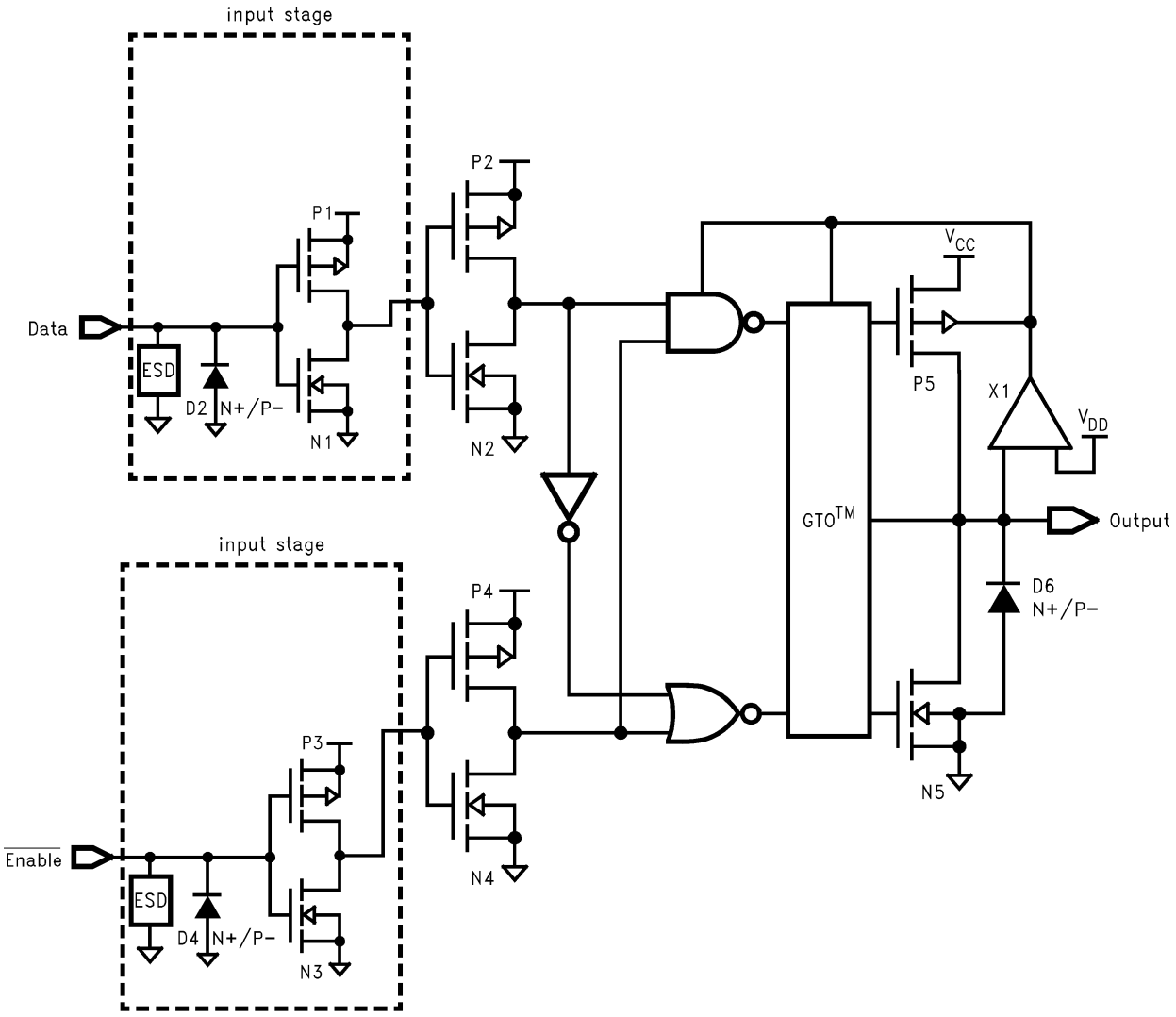


Figure 6. Schematic Diagram

ORDERING INFORMATION

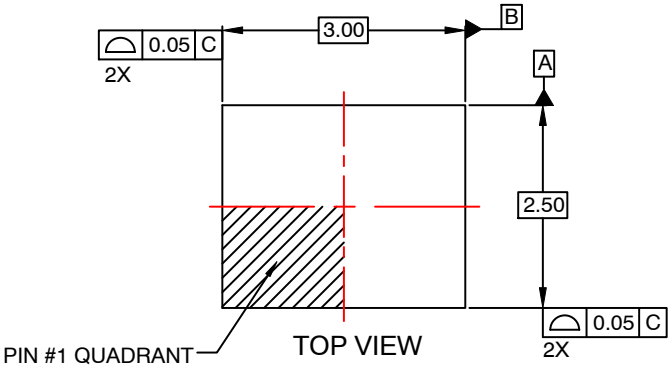
Device	Marking	Package	Shipping†
74LCX74MTCX	LCX 74	TSSOP−14 (Pb-Free, Halide Free)	2500 Units / Tape & Reel
74LCX74BQX	LCX74	QFN14 (Pb-Free, Halide Free)	3000 Units / Tape & Reel

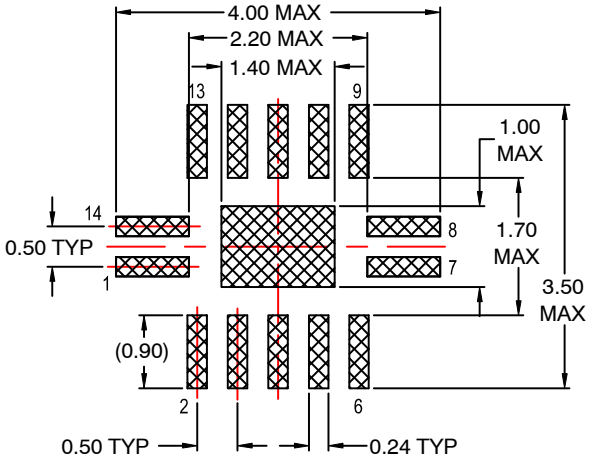
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*−Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

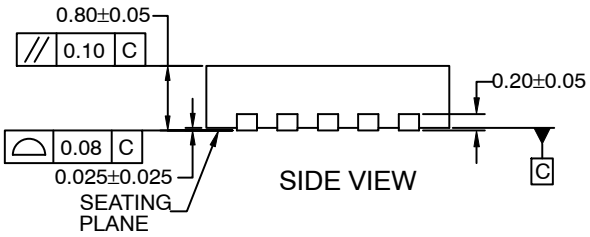
QFN14 3.0x2.5, 0.5P
CASE 510CB
ISSUE O

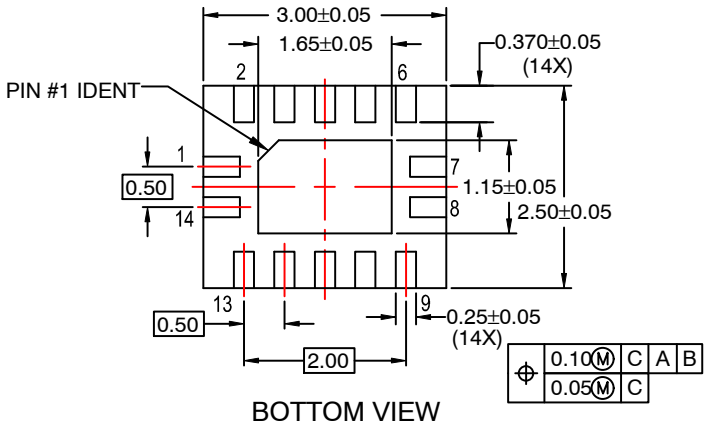
DATE 31 AUG 2016





RECOMMENDED LAND PATTERN





NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO−241, VARIATION AA

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

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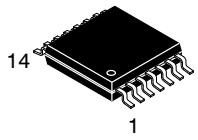
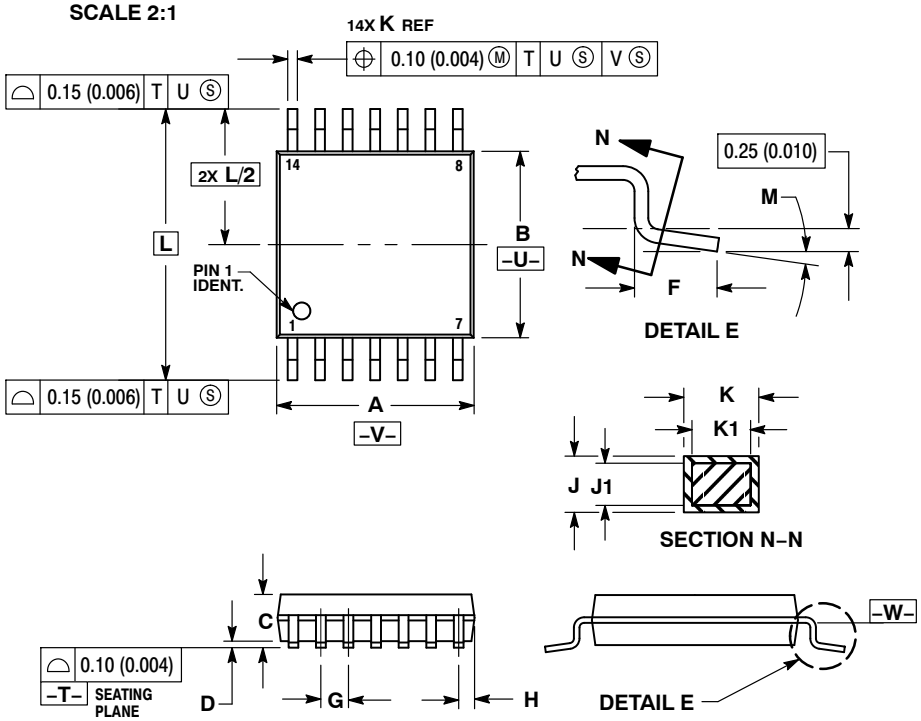


SCALE 2:1

TSSOP−14 WB
CASE 948G
ISSUE C

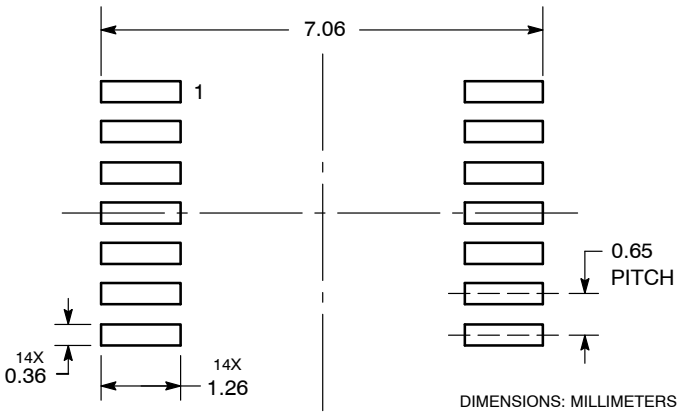
DATE 17 FEB 2016



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

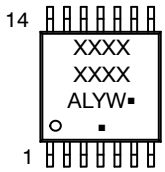
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**TSSOP−14 WB**	**PAGE 1 OF 1**

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