TFA9894_SDS

High Efficiency Class-D Audio Amplifier

Rev. 3.1 — 13 May 2019 Product data sheet

1 General description

The TFA9894 is a high efficiency 10 V boosted class-D audio amplifier with a sophisticated SpeakerBoost and Protection algorithm. It can deliver up to 5.6 W (AVG) output power into an 8 Ω speaker and up to 6.2 W (AVG) output power into 4 Ω speaker, at a battery supply voltage of 4.0 V. The internal adaptive DC-to-DC converter raises the power supply voltage up to 10 V, providing ample headroom for major improvements in sound quality.

A safe working environment is provided for the speaker under all operating conditions. The TFA9894 maximizes acoustic output while ensuring membrane displacement and voice coil temperature do not exceed their rated limits. This function is based on a speaker box model that operates in all speaker environments (e.g. free air, closed box or vented box). Furthermore, advanced signal processing ensures that the quality of the audio signal is never degraded by unwanted clipping or distortion in the amplifier or speaker.

The adaptive sound maximizer algorithm uses feedback to calculate both the temperature and the excursion accurately, allowing the TFA9894 to adapt to changes in the acoustic environment.

Internal adaptive DC-to-DC conversion boosts the supply rail to provide additional headroom and power output. The supply voltage is only raised when necessary. This maximizes the output power of the class-D audio amplifier while limiting quiescent power consumption.

The device can be configured to drive either a hands-free speaker for audio playback, or a receiver speaker, for handset playback, allowing it to be embedded in platforms supporting both a hands-free speaker and a handset speaker. The maximum output power, the gain, and the noise levels are lower in handset call use case than in hands-free call use case.

The TFA9894 also incorporates battery protection. By limiting the supply current when the battery voltage is low, it prevents the audio system from drawing excessive load currents from the battery, which could cause a system undervoltage. This circuitry minimizes the impact of a falling battery voltage by preventing unexpected device switch off due to excessive current drawn from the battery.

The device features a second order closed loop architecture, used in a class-D audio amplifier, providing excellent audio performance and high supply voltage ripple rejection. The audio input interface is TDM and the control settings are communicated via an I2C-bus interface.

The TFA9894 is available in a 48-bump Wafer Level Chip-Size Package (WLCSP) with a 400 µm pitch.

2 Features and benefits

- Sophisticated SpeakerBoost and Protection algorithm that maximizes speaker performance while protecting the speaker:
  - Fully embedded software, no additional license fee, or porting required
  - Fully integrated solution, including DSP, amplifier, DC-to-DC, thermal sensing
- Adaptive excursion control - guarantees that the speaker membrane excursion never exceeds its rated limit
- Real-time temperature protection - direct measurement ensures that voice coil temperature never exceeds its rated limit
- Environmentally aware - automatically adapts speaker parameters to acoustic and thermal changes including compensation for speaker-box leakage
- Clip avoidance - DSP algorithm prevents clipping even with sagging supply voltage
- Automatic bandwidth extension to increase low-frequency response
- TFA9894 high output power: 5.6 W (AVG) into 8 Ω at 4.0 V supply voltage (THD = 1 %, VBST = 10 V), 6.2 W (AVG) into 4 Ω at 4.0 V supply voltage (THD = 1 %, VBST = 9 V)
- Supports handset and hands-free (4 Ω to 32 Ω) speaker configurations
- High efficiency, low power dissipation, and low noise speaker driver (Dynamic Range > 110 dB).
- Adaptive DC-to-DC converter increases the supply voltage smoothly when switching between fixed boost and adaptive boost mode, preventing large battery supply spikes and limiting quiescent power consumption.
- Wide supply voltage range (fully operational from 2.7 V to 5.5 V)
- Very low noise output (typical 14 µV with null DATA input at Fs = 48 kHz)
- I^2C-bus control interface (400 kHz)
- Speaker current and voltage monitoring (via the TDM-bus), as well as DSP data output (with and without pilot tone) for Acoustic Echo Cancellation (AEC) at the Host.
- Various sample frequencies supported:
  - TFA9894/N1: 44.1 kHz, 48 kHz, and 96 kHz
  - TFA9894/N2: 16 kHz, 32 kHz, 44.1 kHz, 48 kHz, and 96 kHz
- Configurable full duplex 4-wires TDM input interface.
- Programmable interrupt control via a dedicated interrupt pin
- Thermal foldback and over temperature protection
- 15 kV system-level ESD protection without external components on amplifier output

3 Applications

- Mobile phones & Tablets
- Portable Gaming Devices
- Portable Navigation Devices (PND)

4 Quick reference data

Table 1. Quick reference data

All parameters are guaranteed for V_{BAT} = 4.0 V; V_{DDD} = V_{DDE} = 1.8 V; V_{DDP} = V_{BST} = 10 V, adaptive boost mode; L_{BST} = 1 µH[1]; R_L = 8 Ω[1]; L_L = 44 µH[1]; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C; default settings, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{BAT}	battery supply voltage	on pin V_{BAT}; in application, V_{BAT} must not be lower than V_{DDD} levels.		2.7	-	5.5	V
V_{DDE}	digital supply voltage	on pin VDDE		1.65	1.8	1.95	V
V_{DDD}	digital supply voltage	on pin V_{DDD}		1.65	1.8	1.95	V
V_{DDP}	power supply voltage	on pin V_{DDP}		2.7	-	10.2	V
R_L	Speaker Impedance			3.2	-	38.4	Ω
I_{BAT}	battery supply current	active state; on pin VBAT; operating mode with load R_L = 8 Ω; DC-to-DC in adaptive boost mode; V_{BAT} = 4.0 V; V_{DDP} = 10 V; −40 dBFs pink noise input signal		-	5.7	-	mA
		idle state; on pin VBAT; operating mode with load R_L = 8 Ω and no output signal; no output capacitance; DC-to-DC converter in adaptive boost mode; V_{BAT} = 4.0 V; low power mode enabled		-	2.7	-	mA
		power-down state; on pin VBAT; DC-to-DC in power-down mode; T_j = 25 °C; no clock.		-	1	-	µA
I_{DDD}	digital supply current	active state (DSP running); on pin VDDD; operating mode with load R_L = 8 Ω; DC-to-DC in adaptive boost mode; V_{BAT} = 4.0 V; V_{DDP} = 10 V; −40 dBFs pink noise input signal		-	15.5	-	mA
		Idle state (DSP disabled); on pin VDDD; operating mode with load R_L = 8 Ω; no output signal; no output capacitance; DC-to-DC converter in adaptive boost mode; V_{BAT} = 4.0 V; low power mode enabled		-	3.9	-	mA
		power-down state; on pin VDDD; DC-to-DC in power-down mode; T_j = 25 °C; no clock.		-	10	-	µA
$P_{o(AVG)}$	Average output power	THD+N = 1 %; (R_L = 8 Ω; L_L = 44 µH); V_{BST} = 10 V; V_{BAT} = 4.0 V; V_{DDD} = 1.8 V		5.3	5.6	-	W
		THD+N = 1 %; (R_L = 6 Ω; L_L = 30 µH); V_{BST} = 10 V; V_{BAT} = 4.0 V; V_{DDD} = 1.8 V		5.8	6.1	-	W
		THD+N = 1 %; (R_L = 4 Ω; L_L = 22 µH); V_{BST} = 10 V; V_{BAT} = 4.0 V; V_{DDD} = 1.8 V		6.0	6.2	-	W
THD+N	total harmonic distortion-plus-noise	P_o = 2.0 W; R_L = 4 Ω or 8 Ω		-	0.015	0.09	%

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
ΔG	Gain variation over freq.	BW = 20 Hz to 15 kHz; V_{BAT} = 3.4 V to 5 V		−0.1	-	0.7	dB
V_{POP}	Pop noise	at mode transition and gain change; with C_L < 200 pF[2]		-	-	2	mV
$V_{n(o)}$	output noise voltage	a-weighted; no input signal; low noise mode; f_s = 48 kHz	[3] [4]	-	14	18	µV
		a-weighted; no input signal; low noise mode; f_s = 44.1 kHz	[3] [4]	-	15	18	µV
		a-weighted; no input signal; low noise mode; f_s = 16 kHz, high performance or 32 kHz, high performance	[3] [4]	-	15	18	µV
DR	dynamic range	a-weighted; V_{BAT} = 3.4 V to 5 V; S/N = maximum signal (at THD = 1 %) − $V_{n(o)}$; no signal applied		110	114	-	dB
S/N	signal-to-noise ratio	a-weighted; V_{BAT} = 3.4 V to 5 V; S/N = maximum signal (at THD = 1 %) − $V_{n(o)}$; with signal applied		100	-	-	dB
η_{po}	output power efficiency	on pin V_{BAT}; Input: 100 Hz sinewave; R_L = 8 Ω; DC-to-DC in adaptive boost mode; V_{BAT} = 4.0 V; V_{DDP} = 10 V; P_o = 4 W		-	82	-	%

[1] L_{BST} = boost converter inductance; R_L = load resistance; L_L = load inductance (speaker).
[2] When C_L is above 200 pF, Low Power Mode must be disabled.
[3] This parameter is not tested during production; the value is guaranteed by design and checked during product validation.
[4] TFA9894/N1 supports 44.1 kHz, 48 kHz, and 96 kHz. TFA9894/N2 supports 16 kHz, 32 kHz, 44.1 kHz, 48 kHz, and 96 kHz.

5 Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TFA9894UK/N1	WLCSP48	wafer-level chip-scale package; 48 bumps; 0.4 mm pitch; 2.51 mm x 3.55 mm x 0.50 mm body; no backside coating	SOT1887-2
TFA9894BUK/N1	WLCSP48	wafer-level chip-scale package; 48 bumps; 0.4 mm pitch; 2.51 mm x 3.55 mm x 0.525 mm body; backside coating	SOT1887-3
TFA9894AUK/N1	WLCSP48	wafer-level chip-scale package; 48 bumps; 0.4 mm pitch; 2.51 mm x 3.55 mm x 0.50 mm body; RDL; no backside coating	SOT1887-4
TFA9894CUK/N1	WLCSP48	wafer-level chip-scale package; 48 bumps; 0.4 mm pitch; 2.51 mm x 3.55 mm x 0.525 mm body; RDL; backside coating	SOT1887-5
TFA9894UK/N2	WLCSP48	wafer-level chip-scale package; 48 bumps; 0.4 mm pitch; 2.51 mm x 3.55 mm x 0.50 mm body; no backside coating	SOT1887-2
TFA9894BUK/N2	WLCSP48	wafer-level chip-scale package; 48 bumps; 0.4 mm pitch; 2.51 mm x 3.55 mm x 0.525 mm body; backside coating	SOT1887-3
TFA9894AUK/N2	WLCSP48	wafer-level chip-scale package; 48 bumps; 0.4 mm pitch; 2.51 mm x 3.55 mm x 0.50 mm body; RDL; no backside coating	SOT1887-4
TFA9894CUK/N2	WLCSP48	wafer-level chip-scale package; 48 bumps; 0.4 mm pitch; 2.51 mm x 3.55 mm x 0.525 mm body; RDL; backside coating	SOT1887-5

6 Block diagram

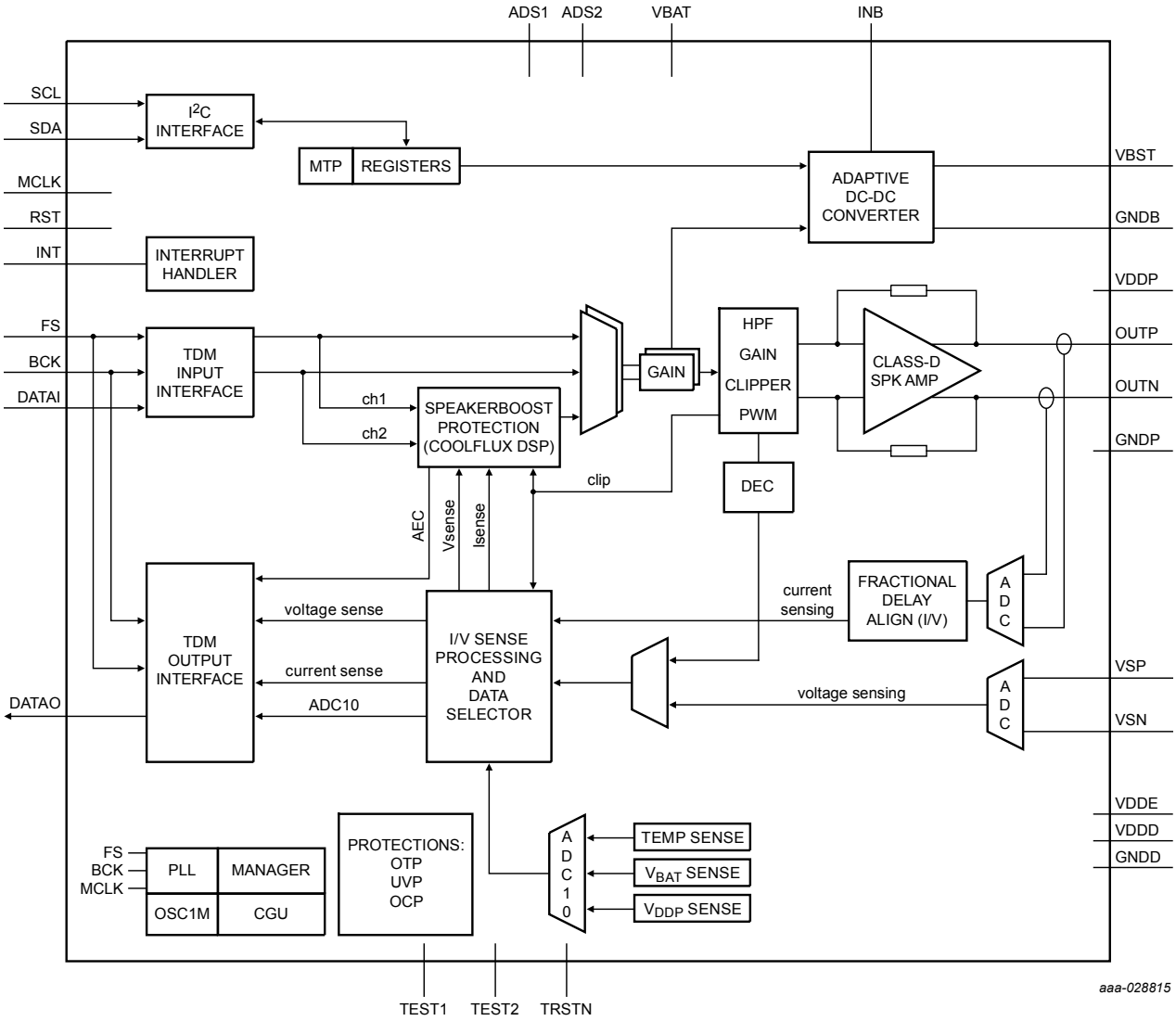
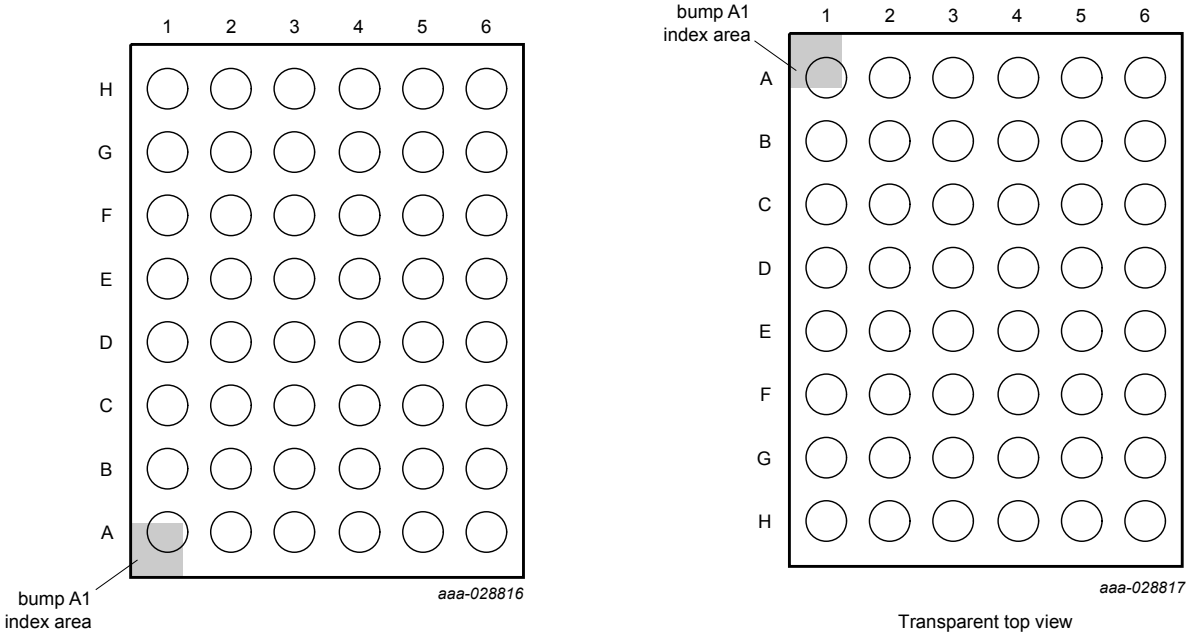


Figure 1. Block diagram

7 Pinning information

7.1 Pinning



a. Bottom view

b. Transparent top view

Figure 2. Bump configuration

	1	2	3	4	5	6
A	MCLK	VDDE	VDDD	GNDD	GNDD	GNDD
B	GNDD	FS	VDDD	SCL	GNDD	GNDD
C	BCK	FS	VDDD	SCL	SDA	TRSTN
D	DATAO	DATAI	ADS2	ADS1	INT	VBAT
E	RST	GNDD	VSN	TEST2	TEST1	VSP
F	GNDB	GNDB	GNDB	GNDD	GNDP	GNDD
G	INB	INB	INB	OUTP	GNDP	OUTN
H	VBST	VBST	VBST	VDDP	VDDP	VDDP

aaa-028818

Transparent top view

Figure 3. Bump mapping

Table 3. Pinning

Symbol	Pin	Type	Description
MCLK	A1	I	master clock input
VDDE	A2	P	pad digital supply voltage (to be connected to VDDD)
VDDD	A3	P	digital supply voltage
GNDD	A4	P	digital ground
GNDD	A5	P	digital ground
GNDD	A6	P	digital ground
GNDD	B1	P	digital ground
FS	B2	I	digital audio frame sync for TDM interface
VDDD	B3	P	digital supply voltage
SCL	B4	I	digital I^2C-bus clock input
GNDD	B5	P	digital ground
GNDD	B6	P	digital ground
BCK	C1	I	digital audio bit clock input for TDM interface
FS	C2	I	digital audio frame sync for TDM interface
VDDD	C3	P	digital supply voltage
SCL	C4	I	digital I^2C-bus clock input
SDA	C5	I/O	digital I^2C-bus data input/output
TRSTN	C6	I	test signal input TRSTN, connect to PCB ground
DATAO	D1	O	digital audio data output for TDM interface
DATAI	D2	I	digital audio data input for TDM interface
ADS2	D3	I	digital address select input 2
ADS1	D4	I	digital address select input 1
INT	D5	O	digital interrupt output
VBAT	D6	P	battery supply voltage
RST	E1	I	digital reset input
GNDD	E2	P	digital ground
VSN	E3	I/O	voltage sensing inverting / test signal IO 4
TEST2	E4	I/O	test signal IO 2; for test purposes only, connect to PCB ground
TEST1	E5	I/O	test signal IO 1; for test purposes only, connect to PCB ground
VSP	E6	I/O	voltage sensing non-inverting
GNDB	F1	P	booster ground
GNDB	F2	P	booster ground
GNDB	F3	P	booster ground
GNDD	F4	P	digital ground
GNDP	F5	P	power ground

Symbol	Pin	Type	Description
GNDD	F6	P	digital ground
INB	G1	P	DC-to-DC boost converter input
INB	G2	P	DC-to-DC boost converter input
INB	G3	P	DC-to-DC boost converter input
OUTP	G4	P	non-inverting output
GNDP	G5	P	power ground
OUTN	G6	P	inverting output
VBST	H1	O	boosted supply voltage output
VBST	H2	O	boosted supply voltage output
VBST	H3	O	boosted supply voltage output
VDDP	H4	P	power supply voltage
VDDP	H5	P	power supply voltage
VDDP	H6	P	power supply voltage

8 Functional description

The TFA9894 is a highly efficient Bridge Tied Load (BTL) class-D audio amplifier with a sophisticated SpeakerBoost and Protection algorithm, depicted in block diagram of Figure 1.

TFA9894 contains a TDM input/output interface for communicating with the audio host. The interface is compliant with standard TDM interfaces and supports a wide range of TDM configurations. It can also be configured to output current sense and voltage sense information. The audio host can use this information.

The SpeakerBoost and Protection algorithm, running on a CoolFlux Digital Signal Processor (DSP) core, maximizes the acoustical output of the speaker while limiting membrane excursion and voice coil temperature to safe levels. The mechanical protection implemented guarantees that speaker membrane excursion never exceeds its rated limit, to an accuracy of 10 %. Thermal protection guarantees that the voice coil temperature never exceeds its rated limit, to an accuracy of approximately ±10 °C during music playback. Furthermore, advanced signal processing ensures that the audio quality always remains acceptable.

The protection algorithm implements an adaptive speaker model that is used to predict the extent of membrane excursion. The model is continuously updated to ensure that the protection scheme remains effective even when speaker parameter values change or the acoustic enclosure is modified.

The SpeakerBoost and Protection algorithm boosts the output sound pressure level within given mechanical, thermal, and quality limits. An optional Bandwidth extension mode extends the low frequency response up to a predefined limit before maximizing the output level. This mode is suitable for listening to high quality in quiet environments.

The frequency response of the TFA9894 can be modified via ten fully programmable cascaded second-order biquad filters. The first two biquads are processed with 48-bit double precision; biquads 3 to 10 are processed with 24-bit single precision.

At low battery voltage levels, the gain (from TDM interface to speaker output) is automatically reduced to limit battery current (when battery safeguard is enabled).

The SpeakerBoost and Protection algorithm or the host application (external) can control the output volume. In the latter case, the boost features of the SpeakerBoost and Protection algorithm must be disabled to avoid neutralizing external volume control.

The digital audio stream is converted into two pulse width modulated (PWM) signals which are then injected into the class-D audio amplifier. The 3-level PWM scheme supports filterless speaker drive.

When the audio stream crosses a programmable voltage threshold, an adaptive DC-to-DC converter boosts the battery supply voltage. When boosting, the DC-to-DC provides a boosted supply in line with the audio signal. In this mode, two configurations are available (two-levels mode or tracking mode (default)).

9 I²C-bus interface and register settings

The TFA9894 supports the 400 kHz I²C-bus microcontroller interface mode standard. The I²C-bus is used to control theTFA9894 and to transmit and receive data. The TFA9894 can only operate in I²C slave mode, as a slave receiver or as a slave transmitter.

9.1 TFA9894 addressing

The TFA9894 is accessed via an 8-bit code. Bits 1 to 7 contain the device address. Bit 0 (R/W) indicates whether a read (1) or a write (0) operation has been requested. Four separate addresses are supported for stereo applications. Address selection is via pins ADS1 and ADS2. The levels on pins ADS1 and ADS2 determine the values of bits 1 and 2, respectively, of the device address. The generic address is independent of pins ADS1 and ADS2.

Table 4. Address selection via pins ADS1 and ADS2

ADS2 pin voltage (V)	ADS1 pin voltage (V)	Address	Function
0	0	01101000	for write mode
		01101001	for read mode
0	V_{DDD}	01101010	for write mode
		01101011	for read mode
V_{DDD}	0	01101100	for write mode
		01101101	for read mode
V_{DDD}	V_{DDD}	01101110	for write mode
		01101111	for read mode
don't care	don't care	00011100 (generic address)	for write mode
		00011101 (generic address)	for read mode

9.2 I²C-bus write cycle

The sequence of events that must be followed when writing data to the I2C-bus registers of the TFA9894 is detailed in Table 5. One byte is transmitted at a time. Each register stores two bytes of data. Data is always written in byte pairs. Data transfer is always MSB first.

The write cycle sequence using SDA is as follows:

1. The microcontroller asserts a start condition (S).
2. The microcontroller transmits the 7-bit device address of the TFA9894, followed by the R/W bit set to 0.
3. The TFA9894 asserts an acknowledge (A).
4. The microcontroller transmits the 8-bit TFA9894 register address to which the first data byte is written.
5. The TFA9894 asserts an acknowledge.
6. The microcontroller transmits the first byte (the most significant byte).
7. The TFA9894 asserts an acknowledge.

8. The microcontroller transmits the second byte (the least significant byte).
9. The TFA9894 asserts an acknowledge.
10. The microcontroller can either assert the stop condition (P) or continue transmitting data by sending another pair of data bytes, repeating the sequence from step 6. In the latter case, the targeted register address has been auto-incremented by the TFA9894.

Table 5. I^2C bus write cycle

Start	TFA9894 address	R/$\overline{W}$		TFA9894 first register address		MSB		LSB		More data...	Stop
S	01101A_2A_1	0	A	ADDR	A	MS1	A	LS1	A	<..>	P

9.3 I^2C-bus read cycle

The sequence of events that must be followed when reading data from the I^2C-bus registers of the TFA9894 detailed in Table 6. One byte is transmitted at a time. Each of the registers stores two bytes of data. Data is always written in byte pairs. Data transfer is always MSB first.

The read cycle sequence using SDA is as follows:

1. The microcontroller asserts a start condition (S).
2. The microcontroller transmits the 7-bit device address of the TFA9894, followed by the R/W bit set to 0.
3. The TFA9894 asserts an acknowledge (A).
4. The microcontroller transmits the 8-bit TFA9894 register address from which the first data byte is read.
5. The TFA9894 asserts an acknowledge.
6. The microcontroller asserts a repeated start (Sr).
7. The microcontroller retransmits the device address followed by the R/W bit set to 1.
8. The TFA9894 asserts an acknowledge.
9. The TFA9894 transmits the first byte (the MSB).
10. The microcontroller asserts an acknowledge.
11. The TFA9894 transmits the second byte (the LSB).
12. The microcontroller asserts either an acknowledge or a negative acknowledge (NA).
    - If the microcontroller asserts an acknowledge, the target register address is auto-increased by the TFA9894 and steps 9 to 12 are repeated.
    - If the microcontroller asserts a negative acknowledge, the TFA9894 frees the I^2C-bus and the microcontroller generates a stop condition (P).

Table 6. I^2C-bus read cycle

Start	TFA9894 address	R/$\overline{W}$		First register address			TFA9894 address	R/$\overline{W}$		MSB		LSB		More data...		Stop
S	01101A_2A_1	0	A	ADDR	A	Sr	01101A_2A_1	1	A	MS1	A	LS1	A	<....>	NA	P

10 Limiting values

Table 7. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT}	battery supply voltage	on pin VBAT	−0.3	-	+6	V
V_{BST}	booster output voltage	on pin VBST	−0.3	-	+12	V
V_{INB}	booster input voltage	on pin INB	−0.3	-	+12[1]	V
V_{DDP}	power supply voltage	on pin VDDP	−0.3	-	+12	V
V_{OUTx}	voltage on speaker connections	on pin OUTN, OUTP	−0.3	-	+12[1]	V
V_{DDD}	digital supply voltage	on pin VDDD	−0.3	-	+2.5	V
V_{DDE}	digital supply voltage	on pin VDDE	−0.3	-	+2.5	V
V_{LTESTx}	low-voltage test pins	on pin TEST1/TEST2	−0.3	-	+6	V
V_{HVSx}	high-voltage pins	on pin VSP, VSN	−0.3	-	+12[1]	V
T_j	junction temperature		-	-	+125	°C
T_{stg}	storage temperature		−55	-	+150	°C
T_{amb}	ambient temperature		−40	-	+85	°C
V_{ESD}	electrostatic discharge voltage	according to Human Body Model (HBM)	−2	-	+2	kV
		according to Charge Device Model (CDM)	−500	-	+500	V

[1] Using NXP demo board, with a 1 mm wire/PCB track lengths, AC pulse from −6 V to +15 V can be observed on INB, OUTP, OUTN, VSP, VSN without damaging the device as these spikes do not end up inside the actual device.

11 Thermal characteristics

Table 8. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	4-layer application board	37	K/W

12 Characteristics

12.1 DC characteristics

Table 9. DC characteristics

All parameters are guaranteed for V_{BAT} = 4.0 V; V_{DDD} = V_{DDE} = 1.8 V; V_{DDP} = V_{BST} = 10 V, adaptive boost mode; L_{BST} = 1 µH[1]; R_L = 8 Ω[1]; L_L = 44 µH[1]; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C; default settings, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{BAT}	battery supply voltage	on pin VBAT; V_{BAT} must not be lower than V_{DDD}		2.7	-	5.5	V
I_{BAT}	battery supply current	active state; on pin VBAT; operating mode with load R_L = 8 Ω; DC-to-DC in adaptive boost mode; V_{BAT} = 4.0 V; V_{DDP} = 10 V; −40 dBFs pink noise input signal		-	5.7	-	mA
		idle state; on pin VBAT; operating mode with load R_L = 8 Ω; no output signal; no output capacitance; DC-to-DC converter in adaptive boost mode; V_{BAT} = 4.0 V; low power mode enabled		-	2.7	-	mA
		idle state; on pin VBAT; operating mode with load R_L = 8 Ω; no output signal; no output capacitance; DC-to-DC converter in adaptive boost mode; V_{BAT} = 4.0 V; low power mode disabled		-	5.7	-	mA
		power-down state; on pin VBAT; DC-to-DC in power-down mode; T_j = 25 °C; no clock.		-	1	-	µA
V_{DDP}	power supply voltage	on pin VDDP		2.7	-	10.2	V
V_{DDE}	digital supply voltage	on pin VDDE		1.65	1.8	1.95	V
V_{DDD}	digital supply voltage	on pin VDDD		1.65	1.8	1.95	V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{DDD}	digital supply current	active state (DSP running); on pin VDDD; operating mode with load R_L = 8 Ω; DC-to-DC in daptive boost mode; V_{BAT} = 4.0 V; V_{DDP} = 10 V; −40 dBFS pink noise input signal		-	15.5	-	mA
		idle state (DSP disabled); on pin VDDD; operating mode with load R_L = 8 Ω; no output signal; no output capacitance; DC-to-DC converter in adaptive boost mode; V_{BAT} = 4.0 V; low power mode enabled		-	3.9	-	mA
		idle state (DSP disabled); on pin VDDD; operating mode with load R_L = 8 Ω; no output signal; no output capacitance; DC-to-DC converter in adaptive boost mode; V_{BAT} = 4.0 V; low power mode disabled		-	5.2	-	mA
		power-down state; on pin VDDD; DC-to-DC in power-down mode; T_j = 25 °C; no clock		-	10	-	µA
Pins FS, BCK, DATAI, ADS1, ADS2, SCL, SDA, RST, TRST, MCLK (input)							
V_{IH}	HIGH-level input voltage			$0.7V_{DDD}$	-	V_{DDD}	V
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DDD}$	V
C_{in}	input capacitance		[2]	-	-	3	pF
I_{LI}	input leakage current	1.8 V on input pin		-	-	0.1	µA
		1.8 V on input pin RST		-	90	120	µA
		1.8 V on input pin TRST		-	20	30	µA
Pins DATAO, INT push-pull output stages (output)							
V_{OH}	HIGH-level output voltage	I_{OH} = 4 mA		V_{DDD} − 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA		-	-	400	mV
Pins SDA, open-drain outputs, external 10 kΩ resistor to V_{DDD}							
V_{OH}	HIGH-level output voltage	I_{OH} = 4 mA		V_{DDD} − 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA		-	-	400	mV
Pins OUTP, OUTN							
R_{DSon}	total drain-source on-state resistance	(PMOS + NMOS transistors)		-	430	520	mΩ
Protection							
$T_{act(th\_prot)}$	thermal protection activation temperature			130	-	-	°C
$V_{uvp(VBAT)}$	undervoltage protection on pin VBAT			2.3	-	2.7	V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{O(ocp)}$	overcurrent protection output current			2.5	-	-	A
DC-to-DC converter							
V_{BST}	voltage on pin V_{BST}	DCVOS = 111111; fixed boost mode and switching amplifier		9.8	10	10.2	V

[1] L_{BST} = boost converter inductance; R_L = load resistance; L_L = load inductance (speaker).
[2] This parameter is not tested during production; the value is guaranteed by design and checked during product validation.

12.2 AC characteristics

Table 10. AC characteristics

All parameters are guaranteed for V_{BAT} = 4.0 V; V_{DDD} = V_{DDE} = 1.8 V; V_{DDP} = V_{BST} = 10 V, adaptive boost mode; L_{BST} = 1 µH[1]; R_L = 8 Ω[1]; L_L = 44 µH[1]; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C; default settings, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Amplifier output power							
$P_{o(AVG)}$	average output power	hands-free speaker, THD+N = 1 %					
		R_L = 8 Ω; L_L = 44 µH; V_{BST} = 10 V; V_{BAT} = 4.0 V; V_{DDD} = 1.8 V		5.3	5.6	-	W
		R_L = 6 Ω; L_L = 32 µH; V_{BST} = 10 V; V_{BAT} = 4.0 V; V_{DDD} = 1.8 V		5.8	6.1	-	W
		R_L = 4 Ω; L_L = 22 µH; V_{BST} = 9 V; V_{BAT} = 4.0 V; V_{DDD} = 1.8 V		6.0	6.2	-	W
		receiver speaker; THD+N = 1 %; V_{BST} = 10 V					
		R_L = 32 Ω; handset call; V_{BAT} = 4.0 V		0.15	0.2	-	W
		R_L = 32 Ω; multimedia playback; V_{BAT} = 4.0 V		1.10	1.5	-	W
Amplifier output pins (OUTP and OUTN)							
$\|V_O(offset)\|$	output offset voltage after trimming	absolute value; after trimming; V_{DDP} = 3.4 V to 10 V; V_{BAT} = 3.4 V to 5 V		-	-	1.0	mV
Amplifier performances							
η_{po}	output power efficiency	on pin V_{BAT}; operating mode with load R_L = 8 Ω; DC-to-DC in adaptive boost mode; V_{BAT} = 4.0 V; V_{DDP} = 10 V, P_o = 380mW (average music playback output power)	[2]	-	81	-	%
		on pin V_{BAT}; Input: 100 Hz sinewave; R_L = 8 Ω; DC-to-DC in adaptive boost mode; V_{BAT} = 4.0 V; V_{DDP} = 10 V; P_o = 600 mW	[2]	-	91	-	%
		on pin V_{BAT}; Input: 100 Hz sinewave; R_L = 8 Ω; DC-to-DC in adaptive boost mode; V_{BAT} = 4.0 V; V_{DDP} = 10 V; P_o = 4 W	[2]	-	82	-	%
THD+N	total harmonic distortion-plus-noise	P_o = 2.0 W; R_L = 4 Ω or 8 Ω	[1]	-	0.015	0.09	%
		P_o = 0.1 W; R_L = 32 Ω	[1]	-	0.04	0.09	%

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{n(o)}$	output noise voltage	a-weighted; no input signal; low noise mode; f_s = 48 kHz	[2] [3]	-	14	18	µV
		a-weighted; no input signal; low noise mode; f_s = 44.1 kHz.	[2] [3]	-	15	18	µV
		a-weighted; no input signal; low noise mode; f_s = 16 kHz, high performance or f_s = 32kHz, high performance	[2] [3]	-	15	18	µV
		a-weighted; no input signal; low-noise mode; f_s = 16 kHz, or f_s = 32 kHz	[2] [3]	-	-	50	µV
DR	dynamic range	a-weighted; V_{BAT} = 3.4 V to 5 V; S/N = maximum signal (at THD = 1 %) − $V_{n(o)}$; no signal applied	[2]	110	114	-	dB
S/N	signal-to-noise ratio	a-weighted; V_{BAT} = 3.4 V to 5 V; S/N = maximum signal (at THD = 1 %) − $V_{n(o)}$; with signal applied	[2]	100	-	-	dB
PSRR	power supply rejection ratio (from V_{BAT})	booster in follower mode (V_{DDP} = V_{BAT}); f_{ripple} = 217 Hz square wave; V_{ripple} = 50 mV_{pp}; V_{BAT} = 4.0 V		70	80	-	dB
		booster in follower; f_{ripple} = 20 Hz to 1 kHz sinewave; V_{ripple} = 200 mV_{RMS}; V_{BAT} = 3.4 V to 5.0 V		70	80	-	dB
		booster in follower mode (V_{DDP} = V_{BAT}); f_{ripple} = 1 kHz to 20 kHz sinewave; V_{ripple} = 200 mV_{RMS}; V_{BAT} = 3.4 V to 5.0 V		55	64	-	dB
ΔG	gain variation over frequency	BW = 20 Hz to 15 kHz; V_{BAT} = 3.4 V to 5 V; P_o = 2.0 W; R_L = 8 Ω		−0.1	-	0.7	dB
V_{POP}	pop noise	At mode transition and gain change, with C_L < 200 pF[4]		-	-	2	mV
R_L	load Impedance			3.2	8	38.4	Ω
C_L	load capacitance	[5]		-	200	1000	pF
L_L	load inductance			30	-	-	µH

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{sw}	switching frequency	directly coupled to the TDM input frequency		256	-	384	kHz
$G_{(TDM-VO)}$	TDM to V_O gain	INPLEV = 0 dB		6	-	21	dBV
		INPLEV = −6 dB		0	-	15	dBV
Amplifier power-up, power-down and propagation delays							
$t_{d(on)PLL}$	PLL turn-on delay time	PLL locked on BCK		-	1.3	-	ms
		PLL locked on FS		-	$(2^5 \times 1 / f_s) + 0.3$	-	ms
		PLL locked on MCLK; MCLK = 13 MHz and AUDFS = 11 or 12 AND DIRECTPLL = 0		-	6.5	-	ms
		PLL locked on MCLK; MCLK = 13 MHz and AUDFS is not 11 or 12		-	1.3	-	ms
		PLL locked on MCLK; MCLK = 13 MHz and AUDFS = 11 or 12 AND DIRECTPLL = 1		-	1.3	-	ms
		PLL locked on MCLK; MCLK is not 13 MHz		-	1.3	-	ms
$t_{d(on)amp}$	amplifier turn-on delay time	f_s = 48 kHz[6]		-	55	-	µs
$t_{d(pd)}$	turn-off delay time			-	115	-	µs
$t_{d(alarm)}$	alarm delay time			-	300	-	ms
t_{PD}	propagation delay	f_s = 96 kHz	[3]	-	330	600	µs
		f_s = 44.1 kHz/48 kHz	[3]	-	650	700	µs
		f_s = 32 kHz/32 kHz HP	[3]	-	700	750	µs
		f_s = 16 kHz/16 kHz HP	[3]	-	890	940	µs
Booster inductance							
L	inductance			0.33	1.0	2.2	µH
f_b	booster switching frequency	fixed boost; V_{DDP} = 10 V; I_{load} = 1 A; f_s = 48 kHz		-	2.05	-	MHz
Sensing performance							
$\Delta V_{sense}/I_{sense}$	V_{sense}/I_{sense} ratio mismatch	pilot tone 100 mVpk	[7]	-	2	-	%
THD+N	total harmonic distortion-plus-noise on current sensing	V_i = −12 dBFs		-	-	0.75	%
S/N	signal-to-noise ratio on current sensing	I_O = 1 A (peak); a-weighted		62	65	-	dB
BrownOut Detection (BOD)							
$V_{th(BOD)}$	BOD threshold voltage	BODTHLVL = 10[8]		1.55	1.575	1.6	V
$V_{hys(BOD)}$	BOD hysteresis	BODHYS = 1		-	20	-	mV
$t_{t(BOD)}$	BOD delay time	BODFILT = 10		-	10	-	µs

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Clocks							
$t_{jit(p-p)}$	input clock jitter time	MCLK		-	0.5	1.0	ns
		BCK (3.072 MHz)		-	1.0	2.0	ns
		FS[9]		-	-	20	ns
$\delta_{i(clk)}$	clock input cuty cycle	MCLK		40	-	60	%

[1] L_{BST} = boost converter inductance; R_L = load resistance; L_L = load inductance (speaker).
[2] This parameter is not tested during production; the value is guaranteed by design and checked during product validation.
[3] TFA9894/N1 supports 44.1 kHz, 48 kHz, and 96 kHz. TFA9894/N2 supports 16 kHz, 32 kHz, 44.1 kHz, 48 kHz, and 96 kHz..
[4] When C_L exceeds 200 pF, Low Power Mode must be disabled.
[5] When C_L is above 200pF, Low Power Mode must be disabled.
[6] At power up, audio is output on OUTP/OUTN after $t_{d(on)amp}$ + $t_{d(on)PLL}$.
[7] Intended for Speaker protection. In combination with NXP Speaker protection a speaker temperature accuracy of ±10 °C can be realized.
[8] Recommended setting.
[9] When the PLL is locked on FS on TFA9894N2 devices, the system is less sensitive to jitter.

12.3 TDM timing characteristics

Table 11. TDM bus interface characteristics

All parameters are guaranteed for V_{BAT} = 4.0 V; V_{DDD} = V_{DDE} = 1.8 V; V_{DDP} = V_{BST} = 10 V, adaptive boost mode; L_{BST} = 1 µH[1]; R_L = 8 Ω[1]; L_L = 44 µH[1]; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C; default settings, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_s	sampling frequency	pin FS; audio mode[2]					
		TFA9894/N2		16	-	48	kHz
		TFA9894/N1		44.1	-	48	kHz
		on pin FS; 96 kHz mode		-	96	-	kHz
f_{clk}	clock frequency	on pin BCK; audio mode	[2]	$32f_s$	-	$384f_s$	kHz
		on pin BCK; 96 kHz mode		-	-	$96f_s$	kHz
t_{su}	set-up time	FS edge to BCK HIGH	[3]	10	-	-	ns
		DATA edge to BCK HIGH		10	-	-	ns
t_h	hold time	BCK HIGH to FS edge	[3]	10	-	-	ns
		BCK HIGH to DATA edge		10	-	-	ns

[1] L_{BST} = boost converter inductance; R_L = load resistance; L_L = load inductance.
[2] The TDM bit clock input (BCK) is used as a clock input for the amplifier and the DC-to-DC converter. Note that both the BCK and FS signals need to be present for the clock to operate correctly.
[3] This parameter is not tested during production; the value is guaranteed by design and checked during product validation.

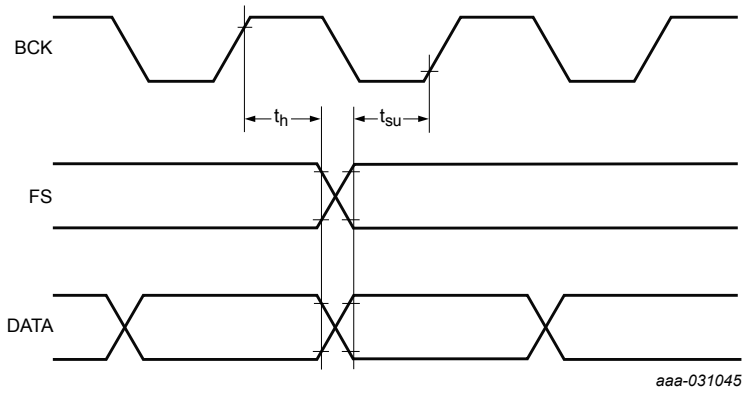


Figure 4. TDM timing

12.4 I²C timing characteristics

Table 12. I²C-bus interface characteristics

All parameters are guaranteed for V_{BAT} = 4.0 V; V_{DDD} = V_{DDE} = 1.8 V; V_{DDP} = V_{BST} = 0 V, adaptive boost mode; L_{BST} = 1 µH[1]; R_L = 8 Ω[1]; L_L = 44 µH[1]; f_i = 1 kHz; f_s = 48 kHz; T_{amb} = 25 °C; default settings, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency			-	-	400	kHz
t_{LOW}	LOW period of the SCL clock			1.3	-	-	µs
t_{HIGH}	HIGH period of the SCL clock			0.6	-	-	µs
t_r	rise time	SDA and SCL signals	[2]	20 + 0.1 C_b	-	-	ns
t_f	fall time	SDA and SCL signals	[2]	20 + 0.1 C_b	-	-	ns
$t_{HD;STA}$	hold time (repeated) START condition		[3]	0.6	-	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition			0.6	-	-	µs
$t_{SU;STO}$	set-up time for STOP condition			0.6	-	-	µs
t_{BUF}	bus free time between a STOP and START condition			1.3	-	-	µs
$t_{SU;DAT}$	data set-up time			100	-	-	ns
$t_{HD;DAT}$	data hold time			0	-	-	µs
t_{SP}	pulse width of spikes that must be suppressed by the input filter		[4]	0	-	50	ns
C_b	capacitive load for each bus line			-	-	400	pF

[1] L_{BST} = boost converter inductance; R_L = load resistance; L_L = load inductance (speaker).
[2] C_b is the total capacitance of one bus line in pF. The maximum capacitive load for each bus line is 400 pF.
[3] After this period, the first clock pulse is generated.
[4] To be suppressed by the input filter.

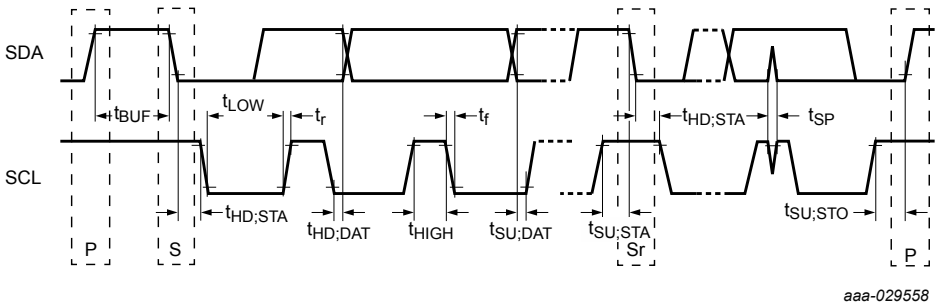


Figure 5. I2C timing

13 Application information

13.1 External components

The DC-to-DC converter needs a battery supply voltage capacitor (C_{VBAT}), an output capacitor (C_{VDDP}), and an inductor (L_{BST}) to work properly. The nominal values of these components are 22 µF, 33 µF, and 1 µH, respectively. If a larger coil is used, the capacitance must also be increased. A 1 µF decoupling capacitor (C_{VDDD}) must be connected close to the VDDD pin. The VDDE pin must be connected externally to the VDDD pin. One 4.7 kΩ resistor (RVS) must be connected between each voltage sensing input and its corresponding amplifier output (VSP/OUTP and VSN/OUTN).

13.1.1 DC-to-DC converter output capacitor

A ceramic capacitor is required at the output of the DC-to-DC converter (C_{VDDP}).

Capacitors constructed using X5R (−55 °C to +85 °C) or X7R (−55 °C to +125 °C) dielectric materials are preferred because they are compact, feature low ESR, and are sufficiently stable over a wide temperature range. The capacitance value decreases over the DC biasing voltage range (50 % to 85 % decrease). Consequently, the selected capacitor must have a nominal value three to four times higher than the required minimum effective capacitance.

Note: *The DC-to-DC converter capacitor connected to pin VBST (C_{VDDP}) is critical for stability. The recommended effective value (the capacitance value at the maximum boost voltage) of C_{VDDP} depends on the coil inductance, and is given in Table 13. The position of the capacitor and the layout of the board are also critical. It is recommended to connect C_{VDDP} as close as possible to the BST and GNDB pins without vias in the PCB tracks.*

In many applications, it is desirable to limit the height of components as much as possible. This can be achieved for C_{VDDP} by placing two smaller capacitors in parallel. The rated voltage should be 10 V or higher.

Table 13. DC-to-DC minimum output capacitor

Effective coil value (at maximum current)	Minimum effective capacitance (at the boost voltage)
0.47 µH	3.4 µF
1 µH[1]	4 µF
1.5 µH	12 µF
2.2 µH	20 µF

[1] Recommended value; larger values are not preferred because of the cost of and space needed for the coil (L_{BST}) and the capacitor (C_{VDDP}).

The values in the Table 14 and Table 15 are guaranteed for capacitors rated X5R or higher.

Table 14. DC-to-DC recommended output capacitor

Specification	Conditions	Min	Typ	Max	Unit
nominal capacitance; 20 % tolerance	6 Ω or 8 Ω speaker; 1 µH inductor (L_{BST})	-	33	-	µF
minimum effective capacitance	6 Ω or 8 Ω speaker; 1 µH inductor (L_{BST})	4	-	-	µF
rated voltage		10	-	-	V

13.1.2 Battery capacitor

C_{VBAT} must be at least half the value of C_{VDDP}.

Table 15. Battery Recommended capacitor

Specification	Min	Typ	Max	Unit
nominal capacitance; 20 % tolerance	-	22	-	µF
rated voltage	10	-	-	V

13.1.3 DC-to-DC converter inductor

An inductor is required at the output of the DC-to-DC converter (L_{BST}). For stability, the inductance of the coil should remain above 0.33 µH and below 2.2 µH under all conditions. The most commonly available values are 1 µH and 1.5 µH. A nominal value 1 µH provides the optimum balance between current capability, component size and efficiency.

The choice of inductor is configured using DCCV bit. It is strongly influenced by the impedance of the speaker used in the application. The speaker impedance determines the output current of the DC-to-DC converter. The coil current contains a ripple around the average current resulting in a peak inductor current, $I_{L(peak)}$. The value of the peak inductor current is determined by the minimum required battery voltage, the boost voltage and the inductor value.

Recommend specifications for the DC-to-DC convertor inductor are given in Table 16.

Table 16. DC-to_DC Recommended inductor

Specification	Min	Typ	Max	Unit
nominal inductance; 20 % tolerance	0.47[1]	-	2.2	µH
DC resistance	-	-	100	mΩ
saturation current	-	4.2	-	A

[1] 0.33 µH (min) at $I_{L(peak)}$.

13.2 PCB layout considerations

Great care should be taken when designing the PCB layout for a class-D amplifier and booster circuit since the layout can affect the audio performance, the booster performance, the Electromagnetic Compatibility (EMC) performance and/or the thermal performance.

13.2.1 DC-to-DC converter stability

To avoid stability problems, the DC-to-DC converter output capacitor must to be connected as close as possible to GNDB/GNDP via thick tracks as well as to V_{BST}/V_{DDP} in the top layer.

13.2.2 EMC considerations

EMC standards define to what degree a (sub)system is susceptible to externally imposed electromagnetic influences and to what degree a (sub)system is responsible for emitting electromagnetic signals in standby and in normal operating modes.

EMC immunity and emission values are normally measured over a frequency range from 180 kHz up to 3 GHz.

The coupling capacitors on pins V_{DDD}, V_{DDP}, and V_{BAT} and the booster inductor L_{BST} should be placed close to the TFA9894, referenced to a solid ground plane. The design should include a solid ground plane below the IC.

Long speaker cables (or traces) should be avoided when designing a filterless class-D amplifier. Long speaker cables have a negative effect on electromagnetic emissions. Speaker traces/cables of less than 10 cm are recommended.

13.3 Application diagrams

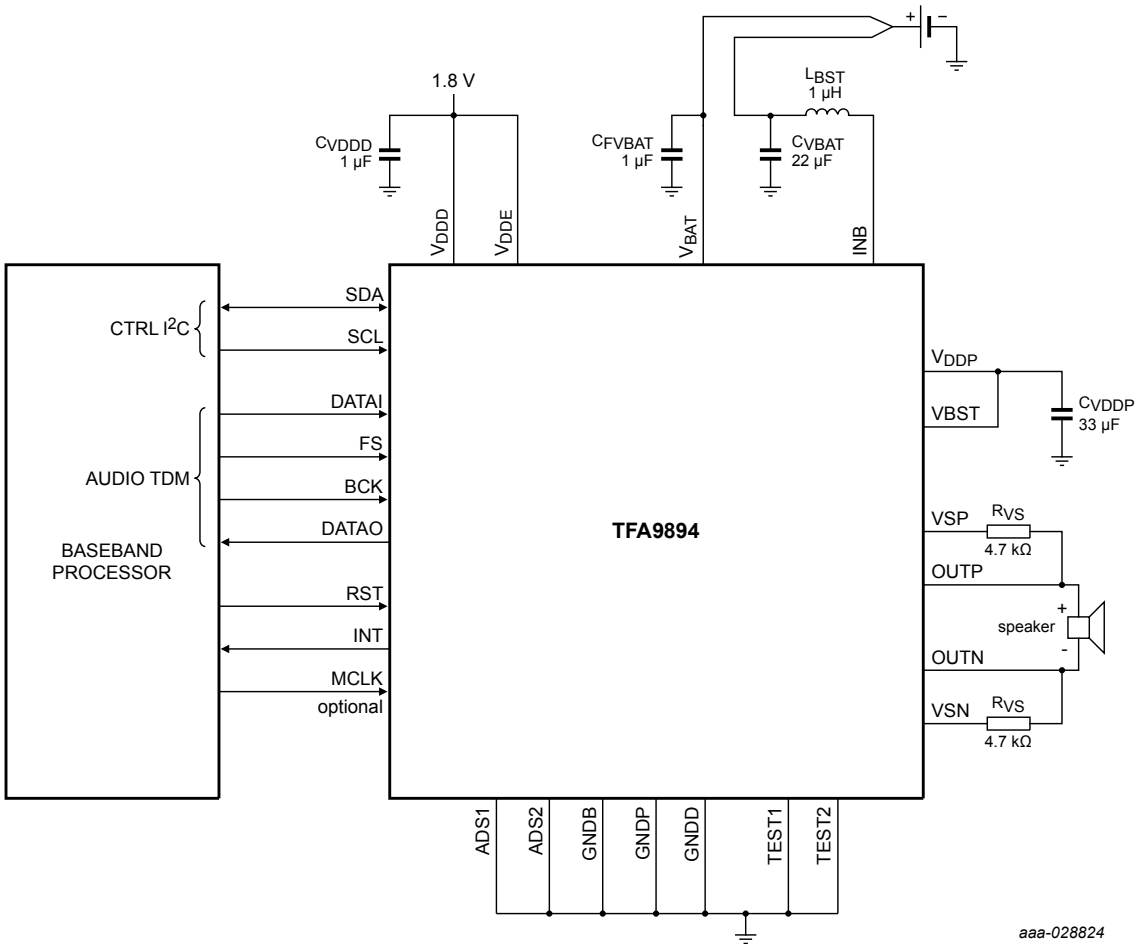


Figure 6. Typical mono application

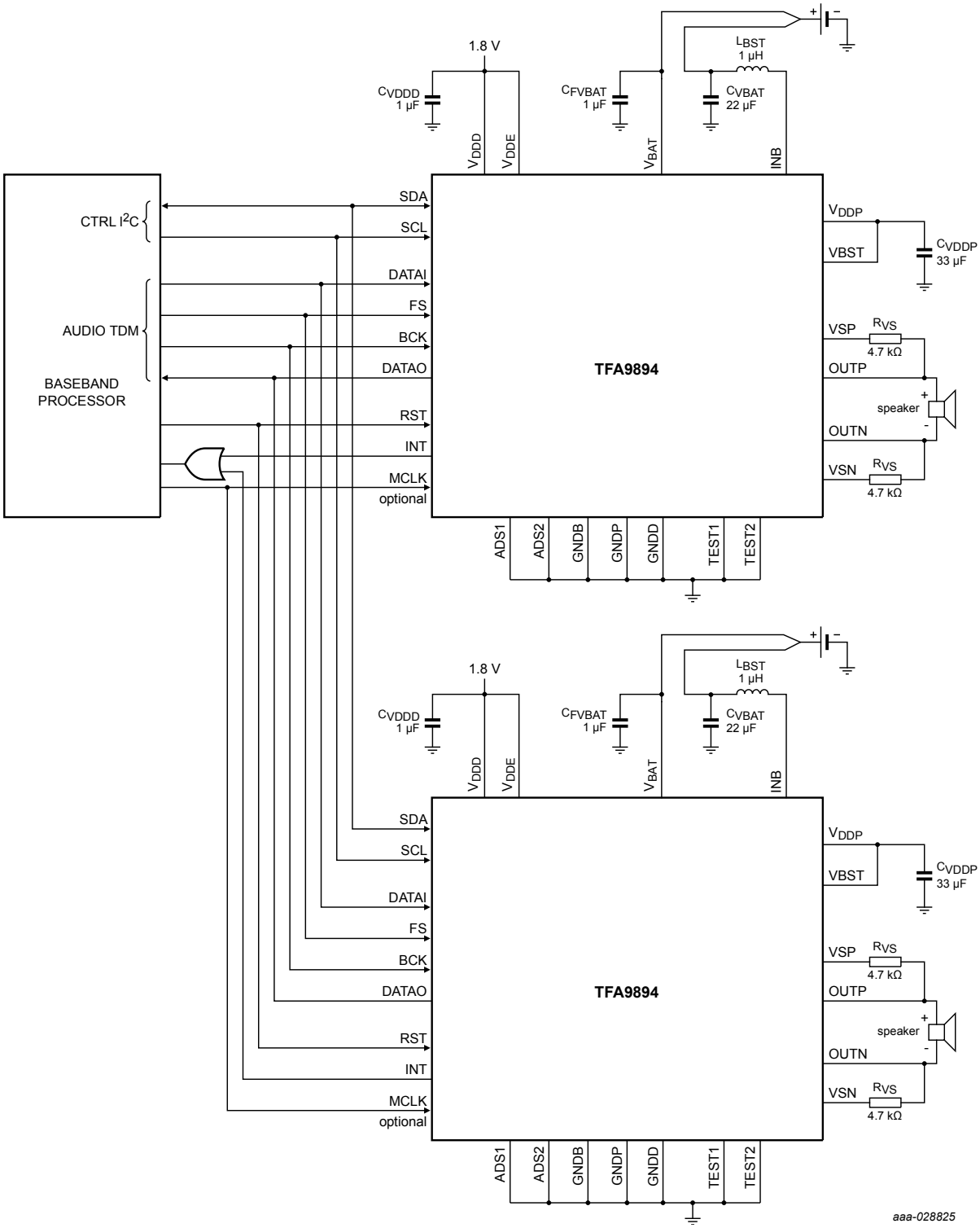


Figure 7. Typical stereo application

14 Package outline

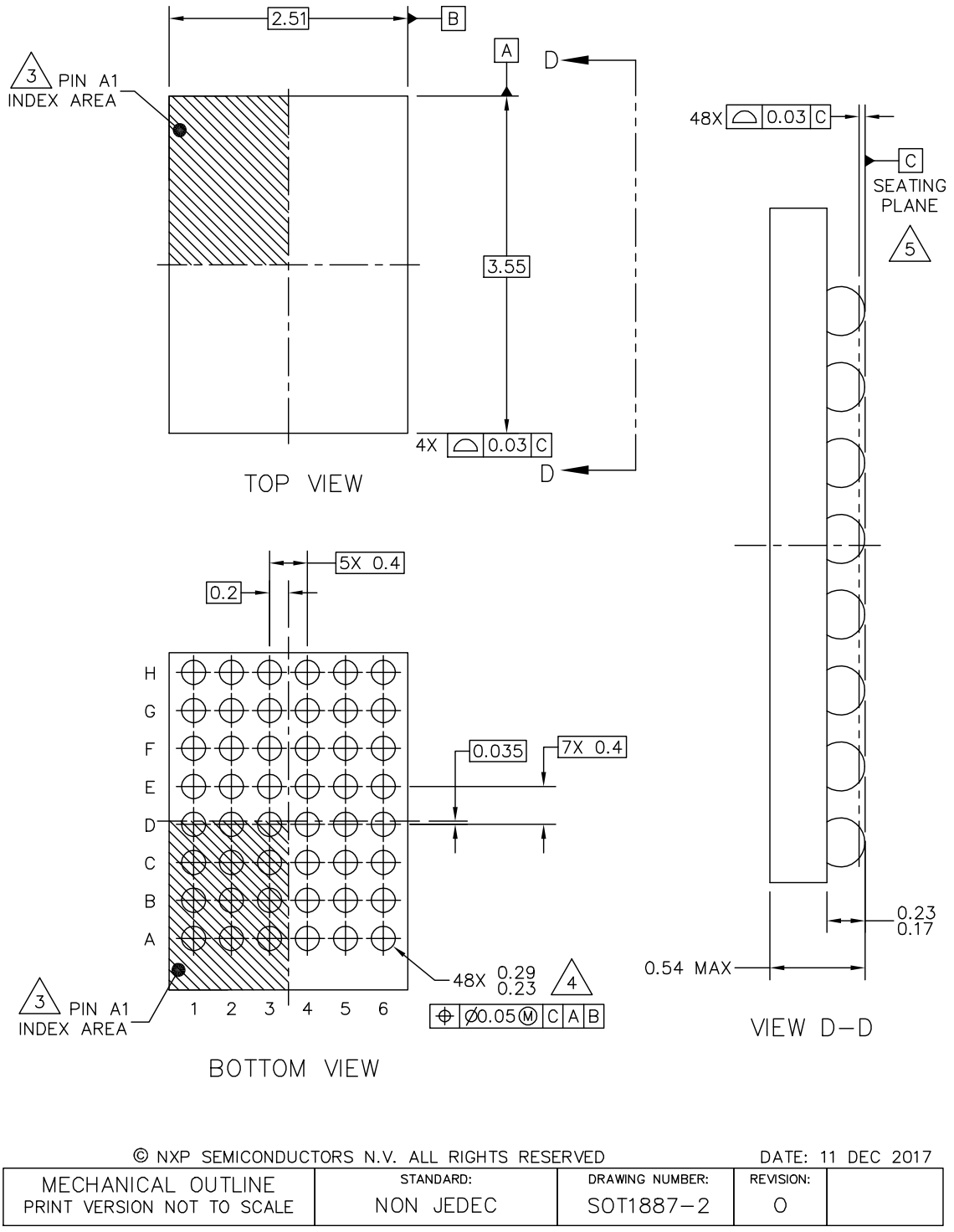


Figure 8. TFA9894UK package outline SOT1887-2 (WLCSP48)

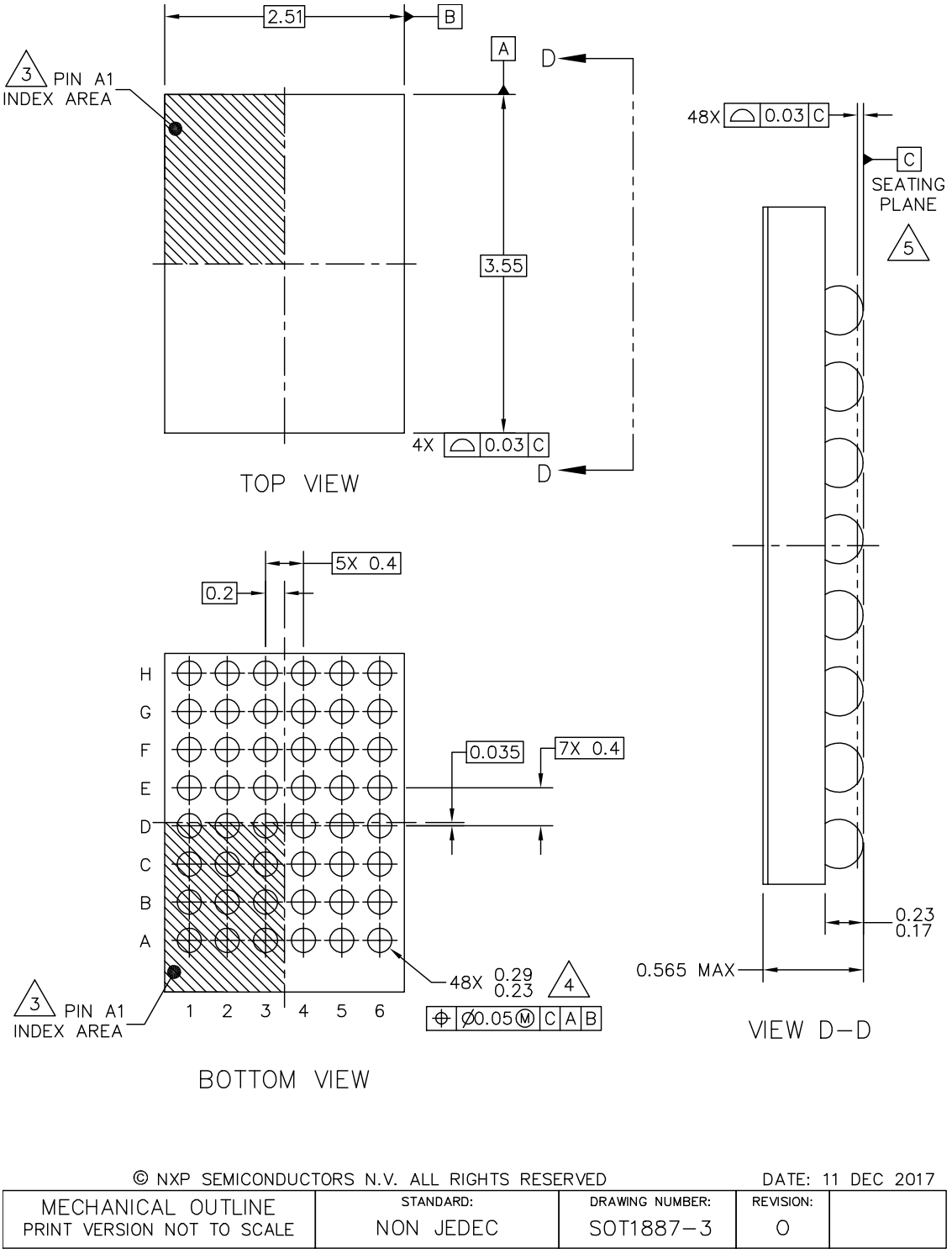


Figure 9. TFA9894BUK package outline SOT1887-3 (WLCSP48)

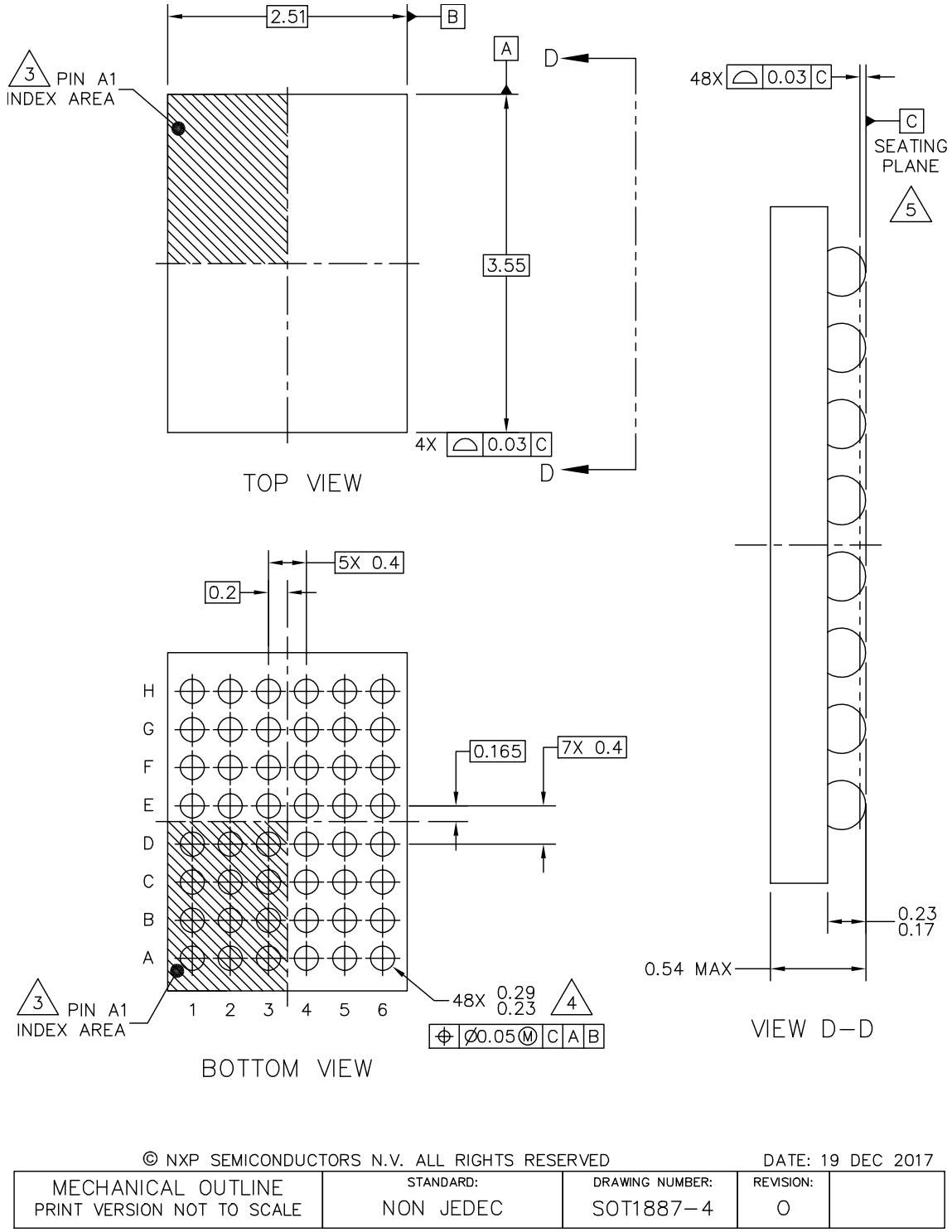


Figure 10. TFA9894AUK package outline SOT1887-4 (WLCSP48)

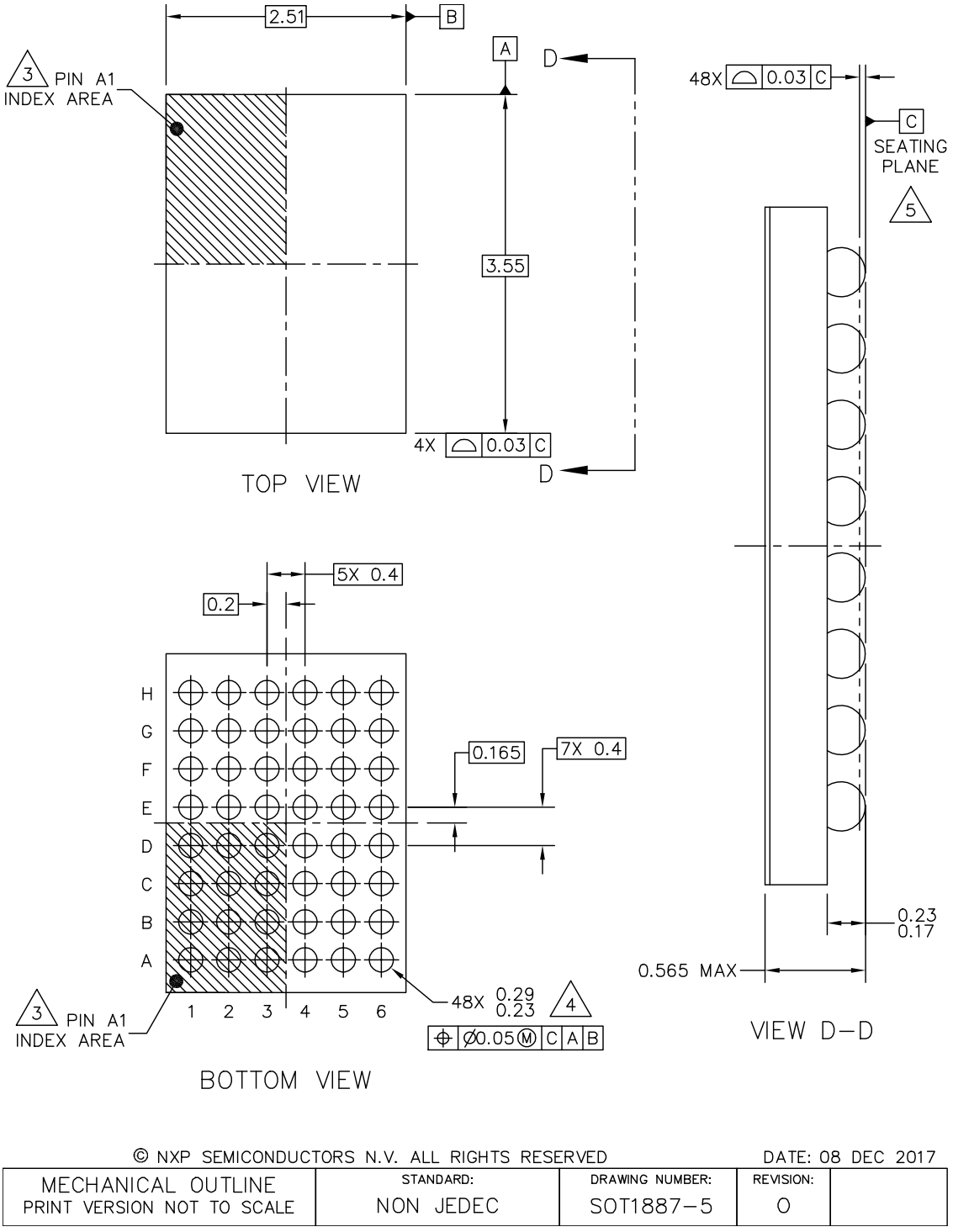


Figure 11. TFA9894CUK package outline SOT1887-5 (WLCSP48)

15 Soldering of WLCSP packages

15.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering WLCSP (Wafer Level Chip-Scale Packages) can be found in application note *AN10439 "Wafer Level Chip Scale Package"* and in application note *AN10365 "Surface mount reflow soldering description"*.

Wave soldering is not suitable for this package.

All NXP WLCSP packages are lead-free.

15.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

15.3 Reflow soldering

Key characteristics in reflow soldering are:

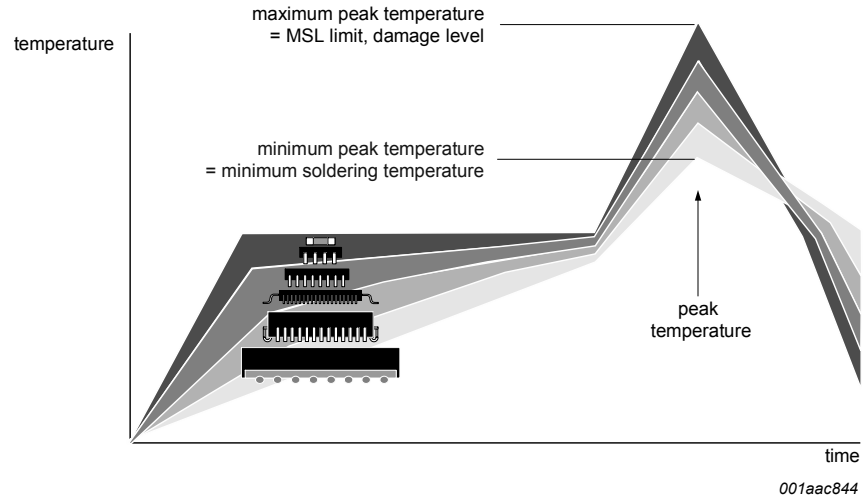
- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 12) than a SnPb process, thus reducing the process window.
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board.
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 17.

Table 17. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2 000	> 2 000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must always be respected.

Studies have shown that small packages reach higher temperatures during reflow soldering (see Figure 12).



MSL: Moisture Sensitivity Level

Figure 12. Temperature profiles

For further information on temperature profiles, refer to application note *AN10365 "Surface mount reflow soldering description"*.

15.3.1 Stand off

The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate
- The bump height on the chip

The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

15.3.2 Quality of solder joint

A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

15.3.3 Rework

In general, rework is not recommended. By rework, we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip are damaged. In that case it is recommended not to reuse the chip again.

Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The

surface of the substrate should be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in application note *AN10365 "Surface mount reflow soldering description"*.

15.3.4 Cleaning

Cleaning can be done after reflow soldering.

16 Revision history

Table 18. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TFA9894_SDS v.3.1	20190513	Product data sheet	-	TFA9894_SDS v.3
Modifications:	• Section 7.1 "Pinning" has been updated.			
TFA9894_SDS v.3	20181218	Product data sheet		TFA9894_SDS v.2
Modifications:	• Text and graphics have been updated throughout this document.			
TFA9894_SDS v.2	20180719	Product data sheet	-	TFA9894_SDS v.1
Modifications:	• POD versions corrected in Table 2. • POD names corrected in Figure 8, Figure 9, Figure 10, and Figure 11. • List of Figures has been updated.			
TFA9894_SDS v.1	20180529	Product data sheet	-	-

17 Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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