UM12044

MCIMX93-QSB Board User Manual

Rev. 1 — 12 February 2024 User manual

Document information

Information	Content
Keywords	MCIMX93-QSB, i.MX93, UM12044
Abstract	The i.MX 93 QSB (MCIMX93-QSB) is a platform designed to show the most commonly used features of the i.MX 93 Applications Processor in a small and low-cost package.

1 MCIMX93-QSB overview

The i.MX 93 QSB (MCIMX93-QSB) is a platform designed to show the most commonly used features of the i.MX 93 Applications Processor in a small and low-cost package. The MCIMX93-QSB board is an entry-level development board, which helps developers to get familiar with the processor before investing a large amount of resources in more specific designs. The board is lead-free and RoHS-compliant.

This document includes system setup and configurations, and provides detailed information on the overall design and usage of the QSB from a hardware system perspective.

1.1 Block diagram

Figure 1 shows the MCIMX93-QSB block diagram.

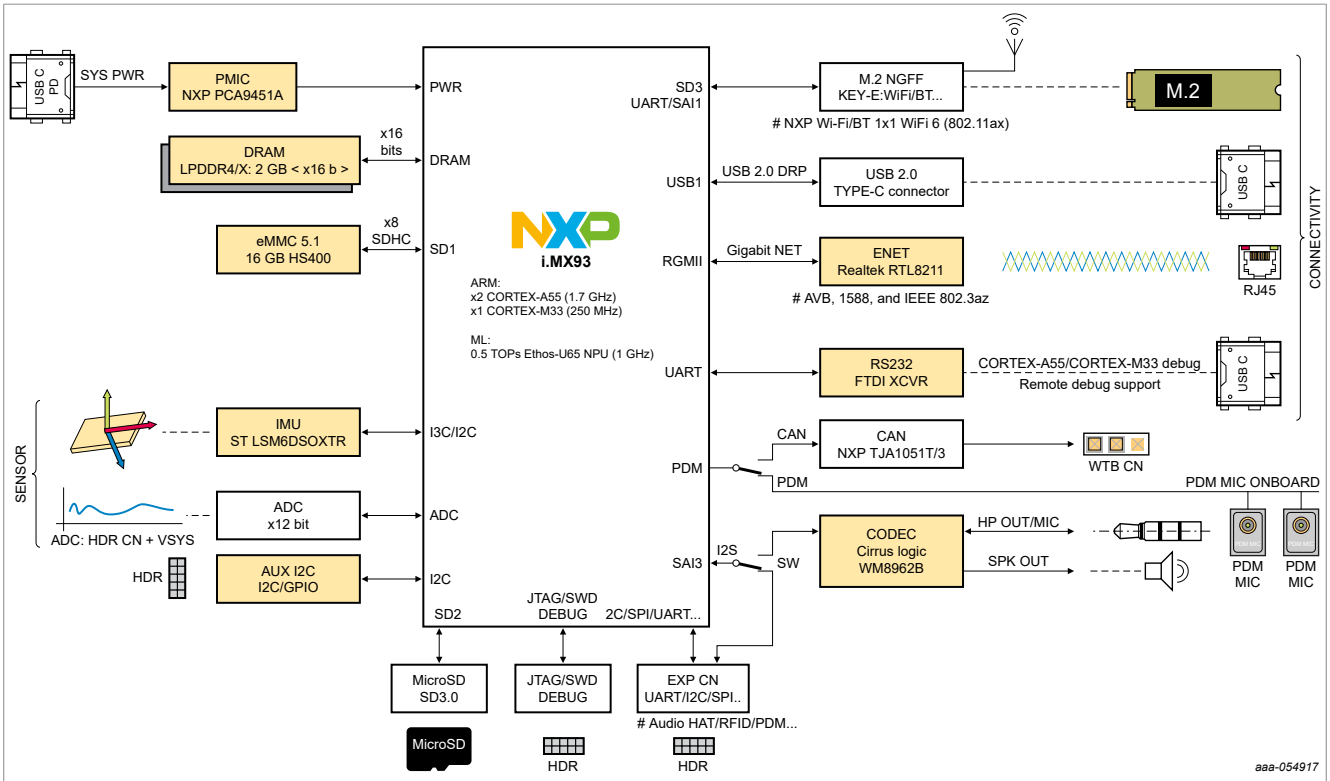

Figure 1. MCIMX93-QSB block diagram

1.2 Board features

Table 1 lists the features of MCIMX93-QSB.

Table 1. MCIMX93-QSB features

Board feature	Target processor feature used	Description
Applications processor		Applications processor features dual Arm Cortex-A55 cores of up to 1.7 GHz clock speed with an NPU that accelerates machine learning inference. A general-purpose Arm Cortex-M33 up to 250 MHz clock speed is for real-time and low-power processing. ***Note:*** *For more details on the i.MX 93 processor, see the i.MX 93 Applications Processor Reference Manual.*

Table 1. MCIMX93-QSB features*...continued*

Board feature	Target processor feature used	Description
USB interface	USB 2.0 high-speed host and device controller	One USB 2.0 Type C connector
DRAM memory	DRAM controller and PHY	2 GB LPDDR4X (Micron MT53E1G16D1FW-046 AAT:A)
Mass storage	Ultra secure digital host controller (uSDHC)	• One 16 GB eMMC5.1 (SanDisk SDINBDA6-16G-I (2D MLC)) • One MicroSD card connector (SD3.0 supported) • One M.2 / NGFF module
Boot configuration	Four boot mode BOOT_ MODE[3:0] pins	• One 4-bit DIP switch for boot configuration • The default boot mode is single boot from the eMMC device • Supports two other boot devices, one QSPI NOR flash (M.2 QSPI card) and the other is SD card (microSD connector)
Ethernet interface	ENET controller	• 10/100/1000 Mbit/s RGMII Ethernet with one RJ45 connector with TSN support (J501) connected with external PHY, RTL8211
CAN interface	CAN	One high-speed CAN transceiver TJA1057GT/3 connected with a 4-pin CAN FD connector
Wi-Fi / Bluetooth / IEEE 802.15.4 interface	USB, SDIO, I2S, UART, I2C, and GPIO	• One M.2/NGFF Key E mini card 75-pin connector, J1707, supporting SDIO, I2S, UART, I2C, and Vendor-defined SPI interfaces • Murata Type-2EL (SDIO+UART+SPI) module. It is based on the NXP IW612 SoC, which supports dual-band (2.4 GHz / 5 GHz) 1x1 Wi-Fi 6, Bluetooth 5.2, and IEEE 802.15.4
Audio	SAI/I2S	• 3.5 mm audio jack (J1201) for headset, microphone, and headphone output support • Audio codec WM8962B can support 24-bit I2S data and a 48 kHz sampling rate
	PDM	• PDM CLK and data signals are multiplexed with CAN transmit and receive signals • One 2:1 demux (TMUX1574RSVR) for PDM and CAN signals; it is configured through IO expander (PCAL6524HEAZ) port2[1] • Four-lane PDM microphone support
Sensors	I2C/I3C	• LSM6DSO iNEMO Inertial module, a 3D digital accelerometer, and a 3D digital gyroscope • Temperature sensor (P3T1085UK)
ADC interface	ADC	Two-channel ADC support
TAMPER	Battery backed secure module (BBSM)	x2 Tamper function support
External RTC	I2C	One real-time clock (PCF2131) for the M.2 interface through the R959 zero-ohm resistor (DNP by default)
Debug interface		• One USB-to-UART/MPSSE device, FT4232H • One USB 2.0 Type-C connector (J1708) for the FT4232H device provides quad serial ports with various configurations: – Two channels are configured as UART ports, which are used for Cortex A55 and Cortex M33 system debug – Two channels are used for remote debug of JTAG, boot mode, ONOFF, and SYS_nRST
Expansion port		40-pin dual-row pin header for GPIO expansion
I2C connector	I2C	8-pin dual-row pin header for I2C expansion

Table 1. MCIMX93-QSB features*...continued*

Board feature	Target processor feature used	Description
I/O expanders		• One I/O expander to provide remote I/O expansion for the target processor via the I2C-bus interface • One IO expander to provide IO expansion for FT4232H device for boot config, ONOFF, POR_B, and SYS_nRST
Power		• One USB 2.0 Type-C connector for power delivery only • PCA9451AHNY PMIC • Discrete DCDC/LDO
PCB		• MCIMX93-QSB: 3.4 inch × 5.5 inch, 4-layer
Orderable part number		MCIMX93-QSB

1.3 Board kit contents

Table 2 lists the items included in the MCIMX93-QSB board kit.

Table 2. Board kit contents

Item description	Quantity
MCIMX93-QSB board assembly	1
USB Type-C 45 W Power Delivery Supply, 5 V / 3 A, 9 V / 3 A, 15 V / 3 A, 20 V / 2.25 A supported	1
USB 2.0 Type-C Male to USB 2.0 Type-A Male cable	1
M.2 module (PN: LBES5PL2EL; Wi-Fi 6 / BT5.2 / 802.15.4 support)	1
MCIMX93-QSB Quick Start Guide	1

1.4 Board pictures

Figure 2 shows the top-side view of the MCIMX93-QSB board.

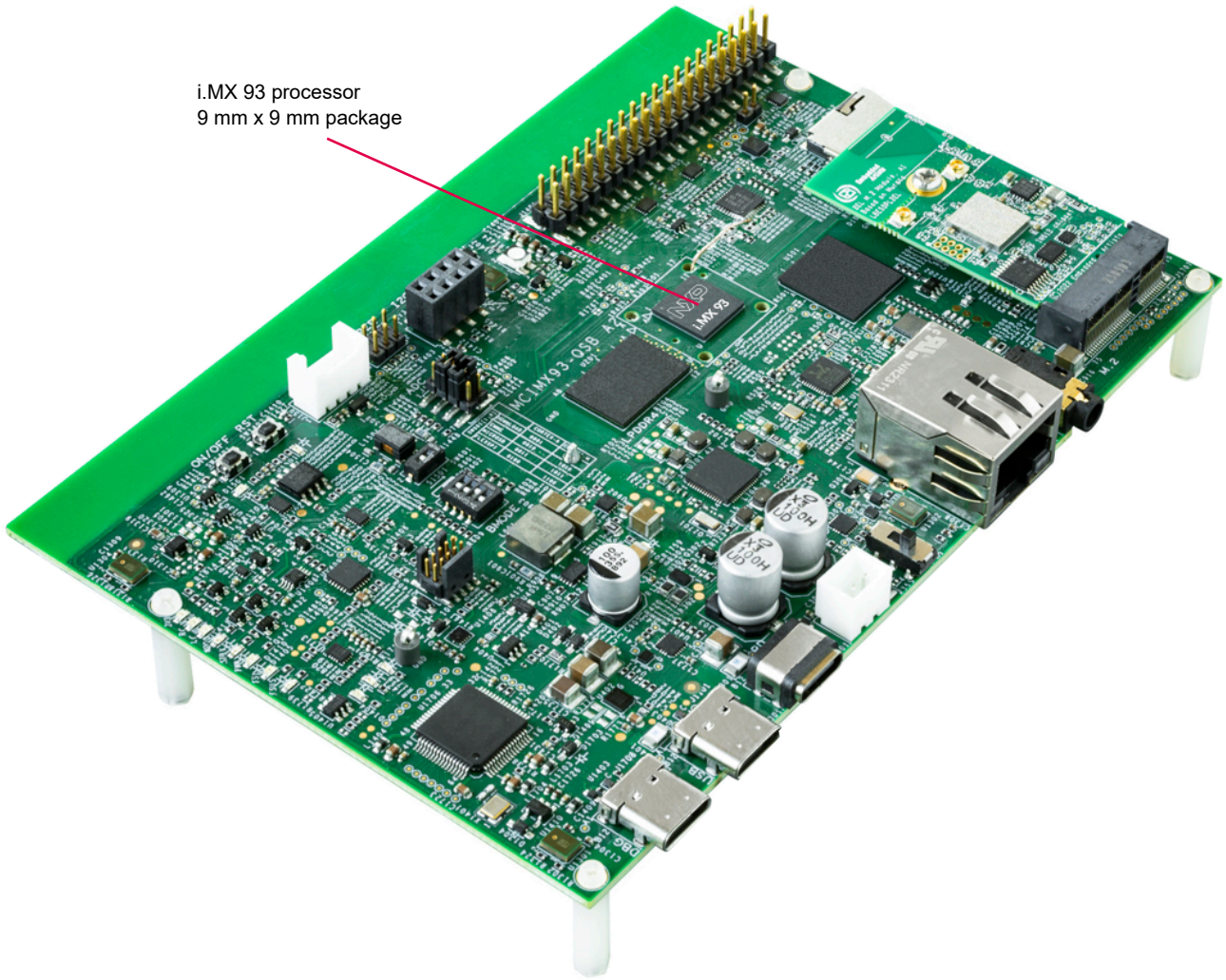

Figure 2. MCIMX93-QSB top-side view

Figure 3 shows the onboard connectors on the MCIMX93-QSB board.

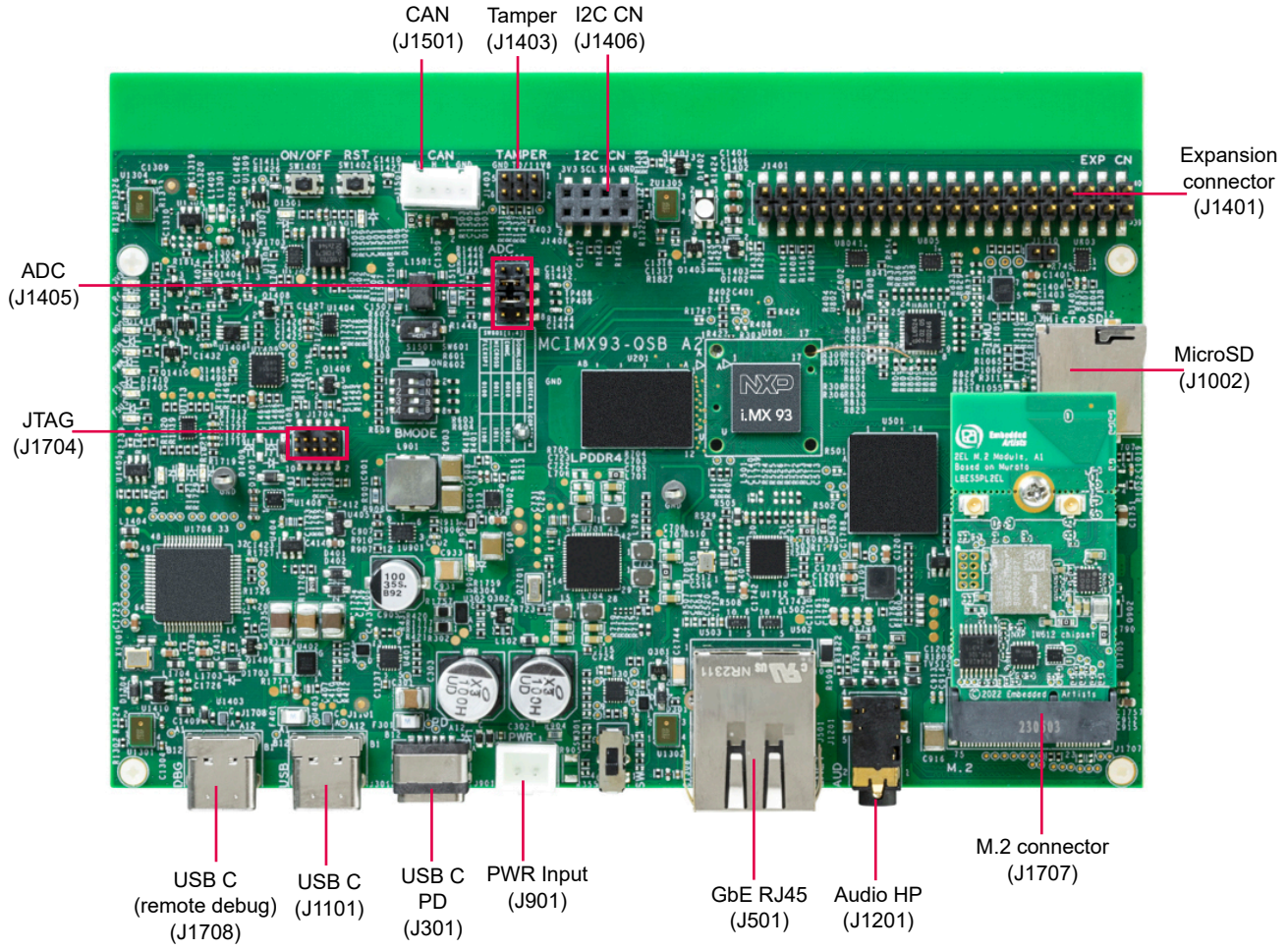

Figure 3. MCIMX93-QSB connectors

Figure 4 shows the onboard switches, buttons, and LEDs available on the MCIMX93-QSB board.

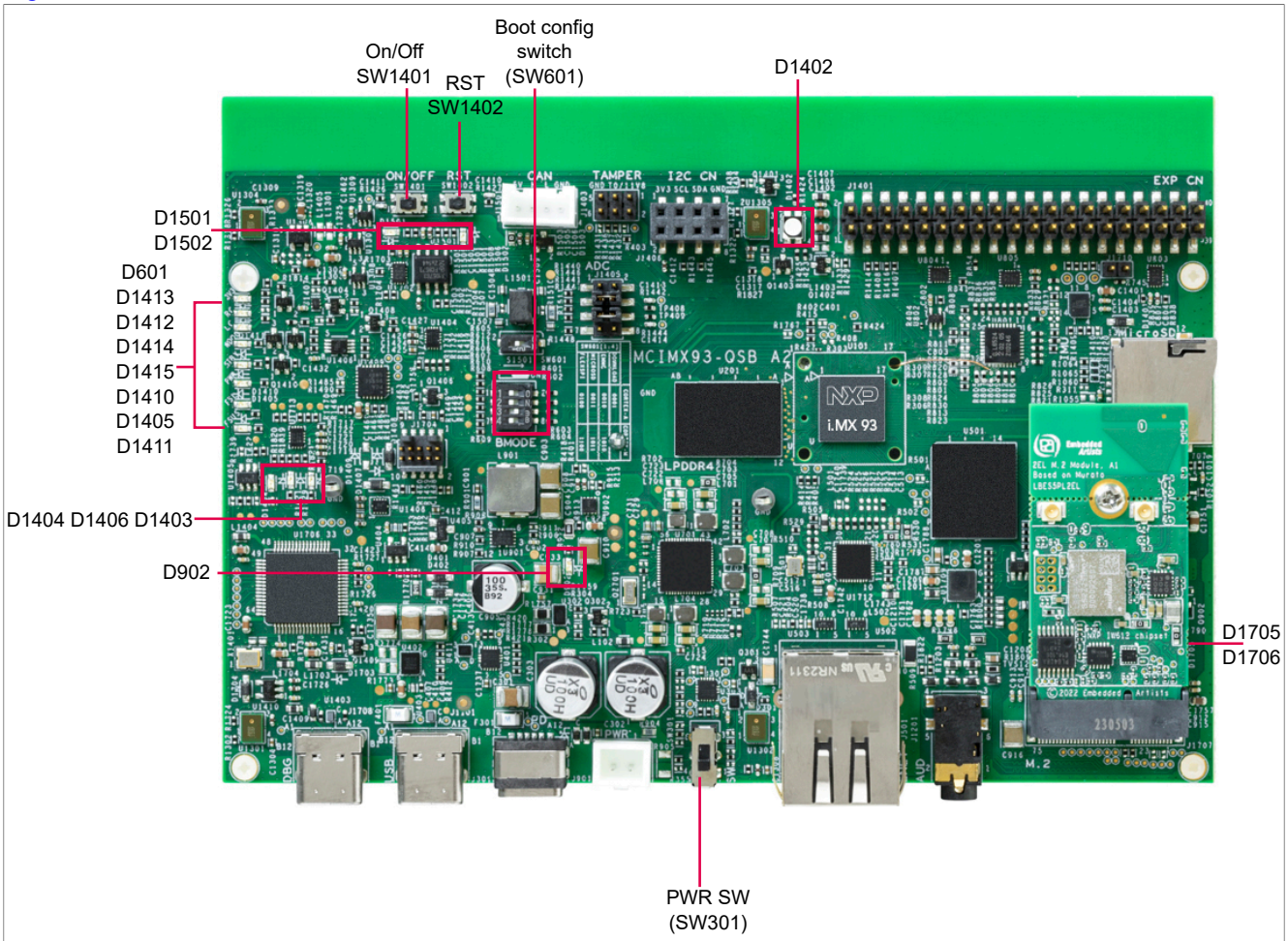

Figure 4. MCIMX93-QSB switches, buttons, and LEDs

Figure 5 shows the bottom-side view of the MCIMX93-QSB board.

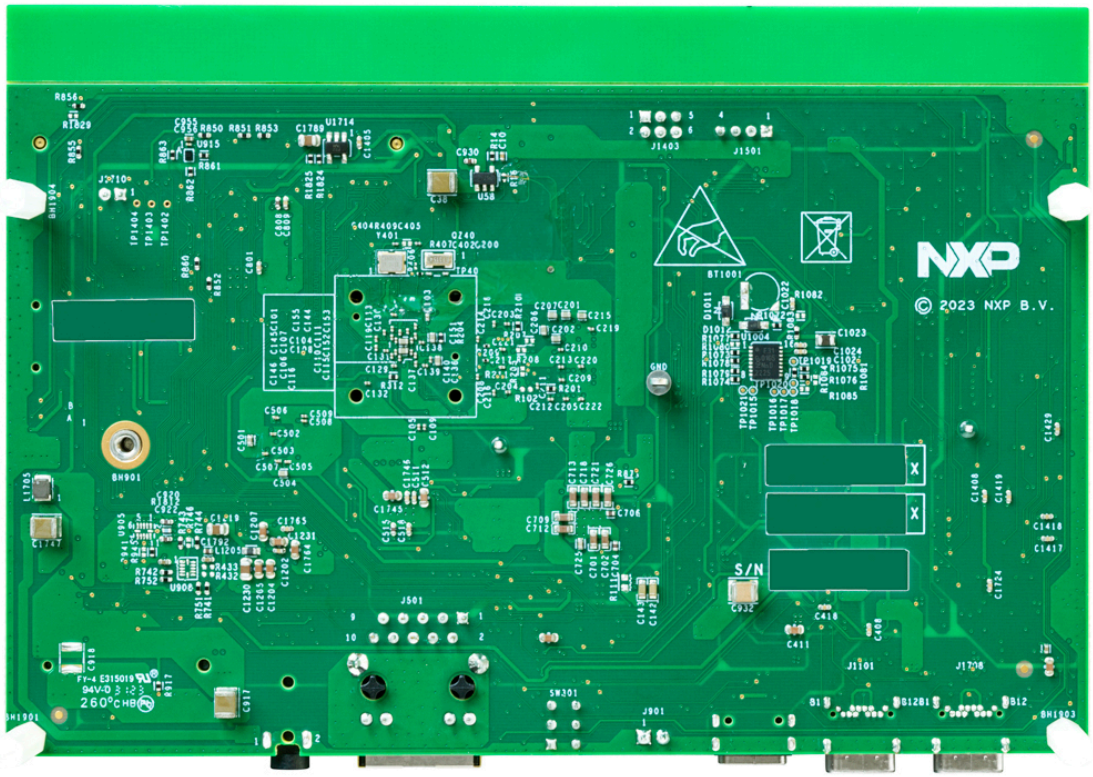

Figure 5. MCIMX93-QSB bottom-side view

1.5 Connectors

See Figure 3 for connectors position on the board.

Table 3 describes the MCIMX93-QSB board connectors.

Table 3. MCIMX93-QSB board connectors

Part identifier	Connector type	Description	Reference section
J901	2-pin connector	15 V input power supply	Section 2.2
J301, J1101	USB 2.0 Type C	USB connectors	Section 2.15
J501	RJ45 jack	Ethernet connector	Section 2.16
J1707	75-pin connector	M.2 socket Key E	Section 2.10
J1401	40-pin connector	GPIO expansion	Section 2.17
J1002	Micro SD push-push connector	MicroSD 3.0	Section 2.8
J1405	2x4-pin connector	ADC x2 channel	Section 2.13
J1406	2x4-pin connector	I2C connector	Section 2.4
J1403	2x3-pin connector	BBSM Tamper	The header can be used for tamper (different mode test).
J1501	4-pin connector	CAN bus	Section 2.12

Table 3. MCIMX93-QSB board connectors*...continued*

Part identifier	Connector type	Description	Reference section
J1201	3.5 mm audio jack	KJ366EYS audio jack for onboard audio codec	Section 2.6
J1708	USB Type-C connector	Remote Debug connector	USB debug interface
J1704	2x5-pin connector	FTSH-105-01-L-DV-K JTAG header	Section 2.19.2

1.6 Jumpers

No jumpers are available on the board.

1.7 Push buttons

Figure 4 shows the push buttons available on the board.

Table 4 describes the MCIMX93-QSB push buttons.

Table 4. MCIMX93-QSB push buttons

Part identifier	Switch name	Description
SW1401	Power button	The i.MX 93 applications processor supports the use of a button input signal to request main SoC power state changes (that is, ON or OFF) from the power management unit. The ON/OFF button is connected to the ONOFF pin of the i.MX 93 processor. • In the ON state: – If the ON/OFF button is held longer than the debounce time, the power off interrupt is generated – If the button is held longer than the defined max timeout, the state transits from ON to OFF, and sends the PMIC_ON_REQ signal to turn off the powers of the PMIC and load switch • In the OFF state: – If the ON/OFF button is held longer than the OFF-to-ON time, the state transits from OFF to ON, and sends the PMIC_ON_REQ signal to turn on the powers of the PMIC and load switch
SW1402	Reset button (RESET)	The button is directly connected to the PMIC PCA9451AHNY. Holding the RESET button forces a reset of the PMIC power outputs on the board. The i.MX 93 applications processor is immediately turned off and reinitiates a boot cycle from the OFF state.

1.8 LEDs

The MCIMX93-QSB board has light-emitting diodes (LEDs) to monitor system functions, such as power-on, reset, board faults. The information collected from LEDs can be used for debugging purposes.

Figure 4 shows the LEDs available on the board.

Table 5 describes the MCIMX93-QSB LEDs.

Table 5. MCIMX93-QSB LEDs

Part identifier	LED color	LED name	Description (When LED in ON)
D601	GREEN	3V3 LED	LED for 3V3 power supply.

Table 5. MCIMX93-QSB LEDs*...continued*

Part identifier	LED color	LED name	Description (When LED in ON)
D902	Red	PWR LED	LED for main power supply. When On, indicates VDD_5V power supply is ON, and the board is powered on.
D1402	Red-Green-Blue	RGB LED with PWM	LEDs are used to show system status, no special function by default.
D1403	ORANGE	Cortex A55 UART	• D1403 ON – The UART data received from the host computer. • D1404 ON – The UART data transmitted to the host computer.
D1404	GREEN		
D1405	GREEN	Cortex M33 UART	• D1405 ON – The UART data transmitted to the host computer. • D1406 ON – The UART data received from the host computer.
D1406	ORANGE		
D1410	RED	System LED	• ON: FT4232H IC power is ON • OFF: FT4232H IC power is OFF
D1411	ORANGE		• ON: FT4232H function is suspended • OFF: FT4232H function is running
D1412	RED		• ON: Local JTAG for debug • OFF: Remote JTAG for debug
D1413	GREEN		• ON: Remote JTAG for debug • OFF: Local JTAG for debug
D1414	ORANGE		• ON: WDOG_B trigger to PCA9451AHNY PMIC • OFF: Normal operation
D1415	ORANGE		• ON: PMIC_STBY_REQ trigger to PCA9451AHNY PMIC • OFF: Normal operation
D1705	GREEN	M2_LED1	M.2 module LED1
D1706	ORANGE	M2_LED2	M.2 module LED2
D1501	GREEN	CAN LED	CAN receive LED
D1502	ORANGE	CAN LED	CAN transmit LED

2 MCIMX93-QSB functional description

This chapter describes the features and functions of the MCIMX93-QSB board.

Note: *For details of the i.MX93 MPU features, see i.MX93 Applications Processor Reference Manual.*

2.1 Processor

The i.MX93 processor represents NXP Semiconductor latest achievement in the machine learning, vision system, advanced multimedia, and industrial automation focused products that offer high-performance processing with a high degree of functional integration, targeted toward the growing market of Smart Home, Building, City, Industry 4.0, and Consumer applications.

For more detailed information about the processor, see the *i.MX 93 Application Processors Data Sheet* and *i.MX 93 Applications Processor Reference Manual* at https://www.nxp.com/imx93.

2.2 Power supply

The primary power supply to the MCIMX93-QSB board is VBUS_IN (12 V - 20 V) through the USB Type-C PD connector (J301).

The DC buck switching regulator MP8759GD (U901) is used that switches the VBUS_IN supply to the VSYS_5V (5 V) power supply, which is an input power supply for the PCA9451AHNY PMIC (U701) and other discrete devices on the board.

Note: *The J901 connector is reserved for power input test. When the USB PD charger is not in use, you can provide 15 V power on J901 and short R905 to power up the system (For test purpose only).*

Figure 6 shows the MCIMX93-QSB power supply block diagram.

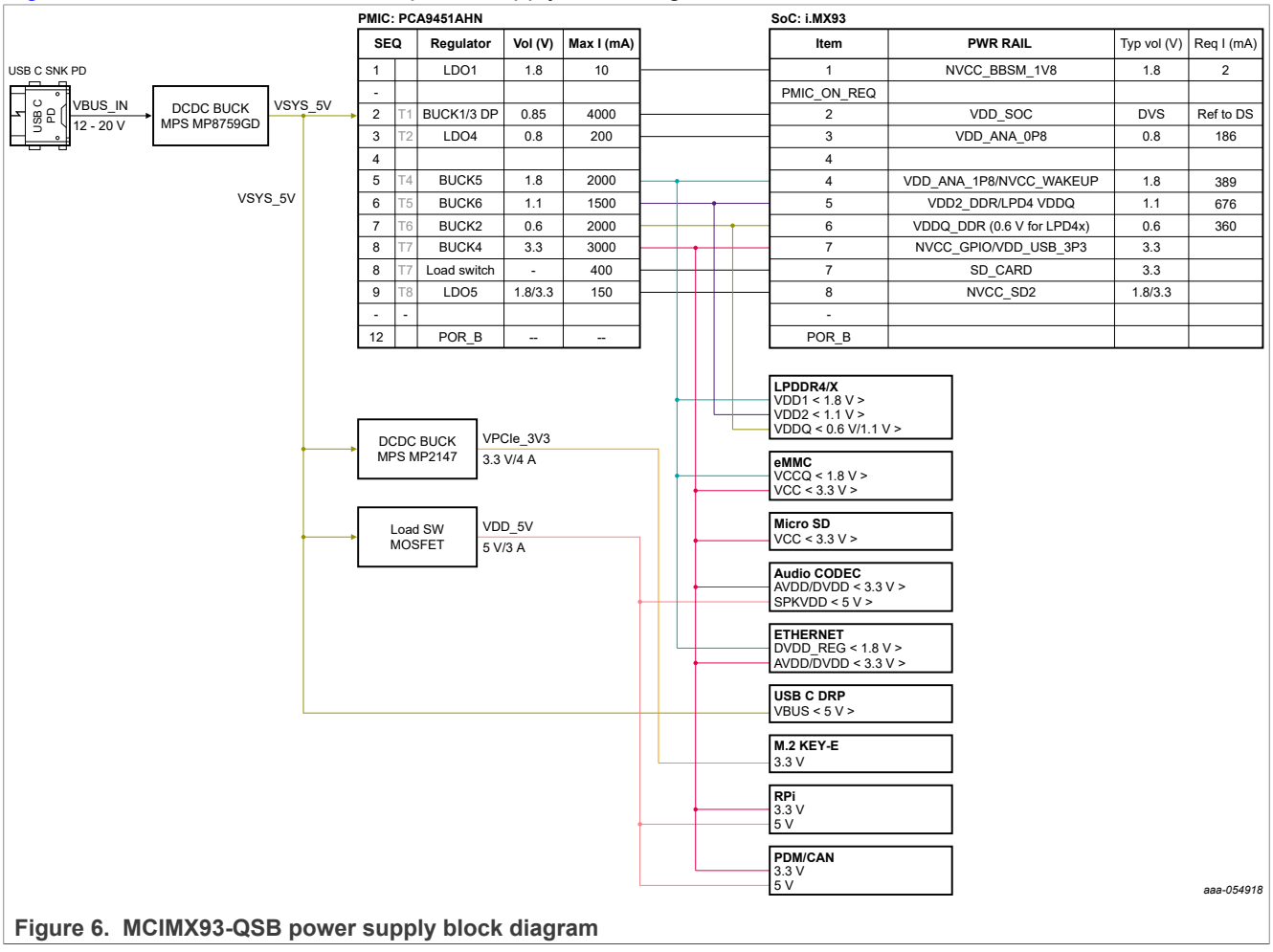

Figure 6. MCIMX93-QSB power supply block diagram

Table 6 describes the MCIMX93-QSB board power supplies.

Table 6. MCIMX93-QSB power supply

Part identifier designator	Manufacturing part number	Part manufacturer	Power supply	Voltage	Description
U901	MP8759GD	Monolithic Power Systems Inc.	VSYS_5V	5 V	Supplies power to: • PMIC PCA9451AHNY (U701) • Step-down switcher MP2147GD (U1710) • NX20P3483UK USB PD and Type-C switch (U402)

Table 6. MCIMX93-QSB power supply*...continued*

Part identifier designator	Manufacturing part number	Part manufacturer	Power supply	Voltage	Description
					• LDO for load switch (U902)
U1710	MP2147	Monolithic Power Systems Inc.	VPCIe_3V3	3.3 V	Supplies power to M.2 / NGFF interface
U701	PCA9451AHNY	NXP Semiconductors	BUCK2: LPD4/x_ VDDQ_0V6	0.6 V ***Note:*** • *0.6 V for LPDDR4X* • *1.1 V for LPDDR4*	Power source for VDDQ_DDR (supply for CPU DRAM PHY I/O (LPDDR4/X))
			BUCK1/3: VDD_ SOC_0V85[1][2]	0.85 V	Power source for VDD_SOC (supply for SoC logic and Arm core)
			BUCK4: VDD_3V3	3.3 V	• Input power supply for PMIC load switch • Supplies to I2C IO expander (U801), 2:1 switch (TMUX1574RSVR), USB power delivery (PD) PHY IC (PTN5110NHQZ), Ethernet PHY, dual-supply buffer (74AVC4 T3144), I2C connector (J1406), Accelerometer and Gyroscope device (U1401), CAN PHY, temperature sensor, Audio codec, DMIC LDO and switch, eMMC 5.1 device • Power source for: – NVCC_GPIO, power supply for GPIO when it is in 3.3 V mode – VDD_USB_3P3
			BUCK5: VDD_1V8	1.8 V	Supplies to: • AVDD, DCVDD, CPVDD, PL VDD supplies of codec WM8962 • eMMC 5.1 device • NVCC_WAKEUP, digital IO supply
			BUCK6: LPD4/x_ VDD2_1V1	1.1 V	Supplies to: • VDD2_DDR, DDR PHY supply voltage
			LDO1: NVCC_ BBSM_1V8	1.8 V	NVCC BBSM IO supply
			LDO4: VDD_ANA_ 0P8	0.8 V	Analog core supply voltage
			LDO5: NVCC_SD2	1.8 V / 3.3 V	microSD card
			Switch: VSD_3V3 (input from Buck 4)	-	microSD card
U902	DML3006LFDS-7 (Load switch)	Diodes Incorporated	VDD_5V	5 V	• PDM/CAN interface • RPi interface
U1202	AP22818AKBWT (Power switch)	Diodes Incorporated	AUD_5V	5 V	Supplies to audio codec (SPKVDD1 and SPKVDD2)
U405	TLV76033DBZR (linear voltage regulator)	Texas Instruments	VLDO_3V3	3.3 V	Always On LDO is used for preventing the NX20P3483UK load switch (for USB Type-C) to enter into Dead Battery mode

Table 6. MCIMX93-QSB power supply*...continued*

Part identifier designator	Manufacturing part number	Part manufacturer	Power supply	Voltage	Description
U1710	MP2147GD (Step-Down Switcher)	MPS	VPCIe_3V3	3.3 V	Supplies to M.2 module
U1306	NCP161ASN180 T1G (LDO regulator)	ON Semiconductor	VMIC_1V8	1.8 V	Supplies to DMICs
U58	AP22814AW5 (Power switch)	Diodes Incorporated	EXP_5V	5.5 V	Supplies to the 40-pin GPIO connector (J1401)
U1714	AP22818AKBWT (Load switch)	Diodes Incorporated	EXP_3V3	3.3 V	Supplies to the 40-pin GPIO connector (J1401)

[1] BUCK 1 and BUCK 3 are configured as dual phase mode.
[2] PCA9451AHNY BUCK1/3 dual phase default output voltage is 0.85 V. The software changes it to 0.9 V for overdrive mode.

For further details on the power sequence needed by the i.MX 93, refer to section "Power sequence" in the *i.MX 93 Applications Processor Reference Manual*.

2.3 Clocks

MCIMX93-QSB provides all the clocks required for the processor and peripheral interfaces.

Table 7 summarizes the specifications of each clock and the component that provides it.

Table 7. MCIMX93-QSB clocks

Part identifier	Clock generator	Clock	Specifications	Destination
Y401	Crystal oscillator	• XTALI_24M • XTALO_24M	Frequency: 24 MHz	Target processor
QZ401	Crystal oscillator	• XTALI_32K • XTALO_32K	Frequency: 32.768 kHz	NVCC_BBSM block of target processor
QZ701	Crystal oscillator	• XIN_32K • XOUT_32K	Frequency: 32.768 kHz	PCA9451AHNY PMIC
X1401	Crystal oscillator	• FT_OSCI • FT_OSCO	Frequency: 12 MHz	FT4232H
Y501	Crystal oscillator	• ETH1_XTALI • ETH1_XTALO	Frequency: 25 MHz	Ethernet RMII PHY1

2.4 I2C interface

The i.MX 93 processor supports a low-power inter-integrated circuit (I2C) module that supports an efficient interface to an I2C-bus as a master. The I2C interface provides a method of communication between a number of devices available on MCIMX93-QSB board.

One 8-pin dual-row pin header connector (J1406) is provided on the MCIMX93-QSB board to support I2C connection. The developers can use the port for some specific application development.

Table 8 explains the I2C header, J1406, pinout.

Table 8. I2C header (J1406) pinout

Pin	Signal name	Description
1, 2	VDD_3V3	Power output, 3.3 V
3, 4	I2C_SCL	I2C clock signal, 3.3 V
5, 6	I2C_SDA	I2C data signal, 3.3 V
7, 8	GND	Ground

Table 9 describes the I2C devices and their I2C addresses (7-bit) on the board.

Table 9. I2C devices on board

Part identifier	Device	I2C address (7-bit)	Port	Speed	Voltage	Description
U801	PCAL6524HEAZ	0x22 (0b'01000[10]x)	MX-I2C2	1 MHz Fm+	3.3 V	IO expander for IRQ/ OUTPUT
U301	PTN5110NHQZ	0x52 (0b'10100[10]x)	MX-I2C1	400 kHz	3.3 V	USB Type-C Power Delivery PHY
U401	PTN5110NHQZ	0x50 (0b'10100[00]x)	MX-I2C1	400 kHz	3.3 V	USB Type-C Power Delivery PHY
U402	NX20P3483UK	0x71 (0b'11100[01]x)	MX-I2C1	400 kHz	3.3 V	USB load switch
U1401	LSM6DSOXTR	0x6A (0b'110101[0]x)	MX-I2C1	I3C/I2C- 400 kHz	3.3 V	IMU (I3C support)
U1709	WM8962B	0x1A (0b'0011010x)	MX-I2C1	526 kHz	3.3 V	Audio codec
U701	PCA9451AHNY	0x25 (0b'0100101x)	MX-I2C2	1 MHz Fm+	3.3 V	PMIC
U1409	PCA9655 EMTTXG	0x21 (0b'0100001)	FTDI-I2C	1 MHz Fm+	3.3 V	Remote debug and power measurement (RDPM) interface IO expander
U915	P3T1085UK	0x48 (0b'1001000x)	MX-I2C1	I3C/I2C-400 kHz	3.3 V	Temperature sensor (I3C support)
U1004	PCF2131TF	0x53 (0b'1010011x)	MX-I2C1	400 kHz	3.3 V	External RTC

2.5 Boot mode and boot device configuration

The i.MX 93 processor offers multiple boot configurations, which can be selected by the SW601 switch on the board or from the boot configuration stored on the internal eFUSE of the processor. In addition, the i.MX 93 can download a program image from a USB connection when configured in serial download mode. The four dedicated BOOT MODE pins are used to select the various boot modes.

Figure 7 shows the boot mode selection switch.

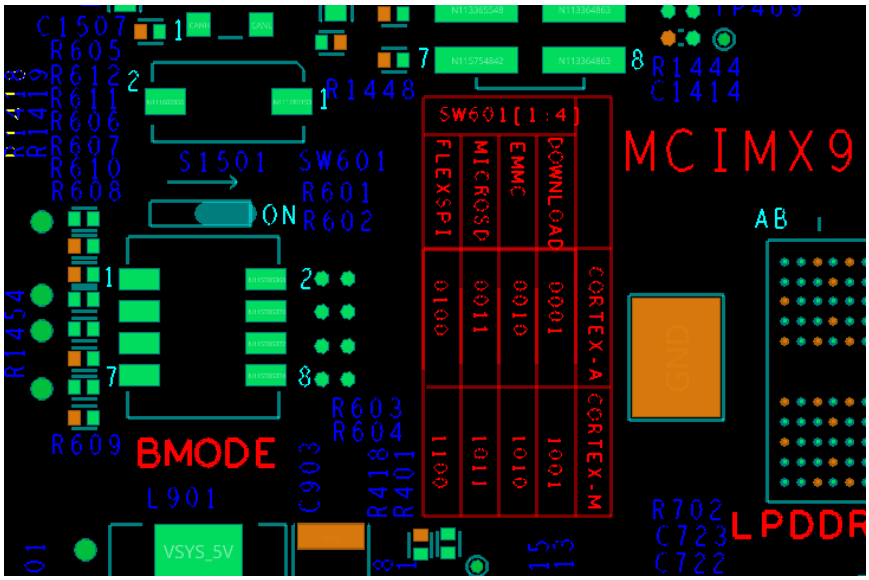

Figure 7. Boot mode selection switch

Table 10 describes the values used in different boot modes.

Table 10. Boot mode settings

SW601[1:4]	BOOT_MODE[3:0]	Boot core	Boot device
0000	0000	Cortex-A55 (Single boot)	From internal fuses
0001	0001		Serial downloader (USB1)
0010	0010		uSDHC1 8-bit eMMC 5.1
0011	0011		uSDHC2 4-bit SD3.0
0100	0100		FlexSPI Serial NOR
0101	0101		FlexSPI Serial NAND 2K
0110	0110		Infinite loop
0111	0111		Test mode (A55)
1000	1000	Cortex-M33 (Low-power boot)	Low-power boot (LPB): Boot from fuses
1001	1001		LPB: Serial downloader (USB1)
1010	1010		LPB: uSDHC1 8-bit 1.8 V eMMC 5.1
1011	1011		LPB: uSDHC2 4-bit SD 3.0
1100	1100		LPB: FlexSPI Serial NOR
1101	1101		LPB: FlexSPI Serial NAND 2K
1110	1110		Infinite loop
1111	1111		Test mode (for DFT ATE test)

On the MCIMX93-QSB board, the default boot mode is from the eMMC device. The other two boot devices on the board are QSPI NOR flash (M.2 QSPI card is required) and the microSD connector. Set SW601[3:0] as 0010 to choose uSDHC1 (eMMC) as boot device, set 0011 to choose uSDHC2 (SD), and set 0101 to choose QSPI NOR. Set 0001 to enter USB Serial Download.

Note:

For more information about the boot modes and boot device configuration, see chapter "System Boot" in the i.MX 93 Applications Processor Reference Manual.

Figure 8 shows the connection of SW601 and i.MX 93 boot mode signals.

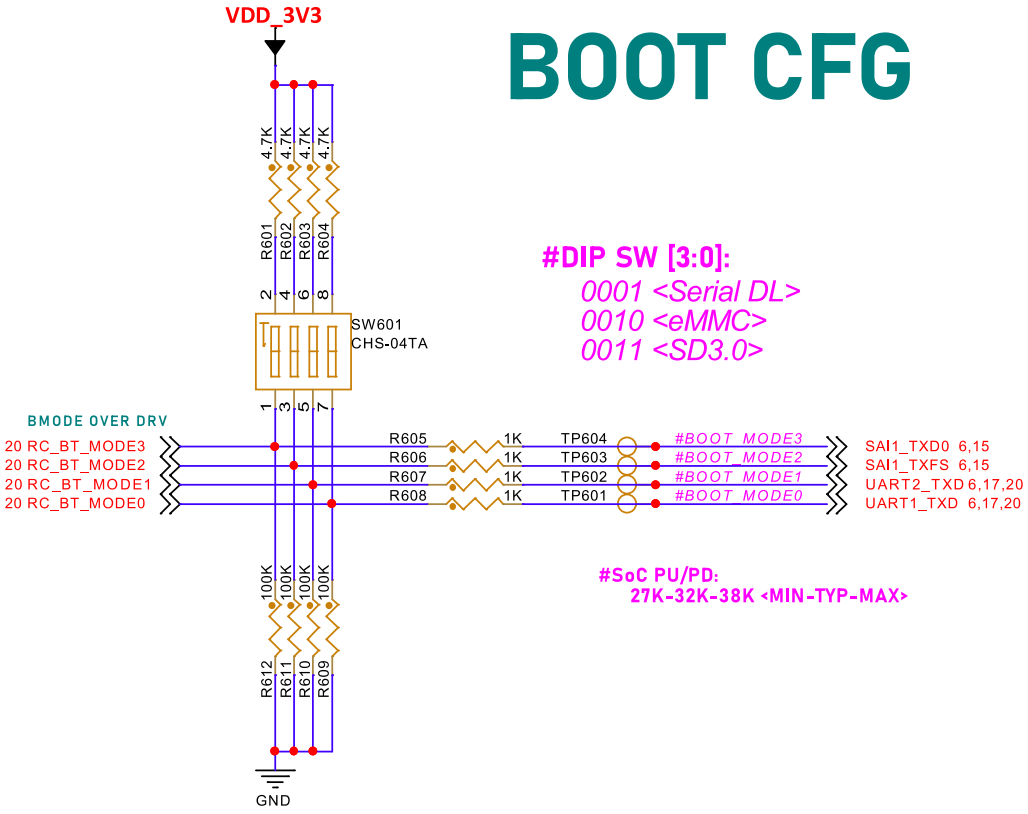

Figure 8. Boot configuration schematic

2.6 Audio interface

The audio module of the i.MX93 processor includes three synchronous audio interface (SAI) controllers and one pulse-density modulated (PDM) microphone controller. The SAI interface is a synchronous serial interface that is used to transfer audio data. PDM is used to receive audio from a microphone.

On MCIMX93-QSB, the SAI3 controller is connected to an audio codec (WM8962B). The audio codec used for encoding/decoding of audio data can support 24-bit I2S data and 48 kHz sampling rate. The audio codec is connected to the audio jack (J1201) for audio input/output. The J1201 connector is a 3.5 mm 4-pole CTIA standard audio jack.

The PDM microphone interface of the processor provides PDM support on the MCIMX93-QSB board. The PDM clock and data signals received on the board are multiplexed with CAN transmit and receive signals. One four-channel switch TMUX1574RSVR (U1702) is used on the board to output either PDM CLK/Data or CAN transmit/receive data depending upon the configuration done through the MIC/CAN_SEL signal from the IO expander (PCAL6524HEAZ, I2C Address 0x34).

Two pairs of microphones (U1301/2 and U1304/5) are used on the board for the PDM interface.

Table 11 describes the audio codec, audio jacks, and PDM microphones.

Table 11. Audio codec, audio jacks, and PDM microphones

Part identifier	Manufacturing part number	Description
J1201	KJ366EYS	3.5 mm audio jack for onboard audio codec
U1709	Cirrus Logic WM8962B	Stereo audio codec. It receives analog audio from an input audio jack, encodes it as digital signals, decodes digital signals back to analog audio, and sends it to the output audio jack
U1301/U1302/ U1304/ U1305	SPK0641HT4H-1	Digital microphone with a single-bit PDM output

2.7 LPDDR4x DRAM memory

The MCIMX93-QSB board features one 1 Gig × 16 (1 channel ×16 I/O × 1 rank) LPDDR4x SDRAM chip (MT53E1G16D1FW-046 AAT:A) for a total of 2 GB of RAM memory. The LPDDR4x DRAM memory is connected to the i.MX 93 DRAM controller.

The ZQ calibration resistors used by the LPDDR4x chip and the processor are 120 Ohm 1 % resistors.

In the physical layout, the LPDDR4x chip is placed at the TOP side of the board. The data traces are not necessarily connected to the LPDDR4x chips in sequential order. Instead, the data traces are connected as best determined by the layout and other critical traces for the ease of routing.

2.7.1 LPDDR4x to LPDDR4 migration

The MCIMX93-QSB DRAM part is MT53E1G16D1FW-046 AAT:A that supports both LPDDR4x and LPDDR4 modes, however, LPDDR4X has been selected as the default option on the board.

There are two ways to verify the LPDDR4 operation:

- Rework DRAM VDDQ power to 1.1 V to support LPDDR4 by performing the following steps:
  1. Remove R704
  2. Install R702
  3. Make sure that the DRAM parameters meet the LPDDR4 requirement

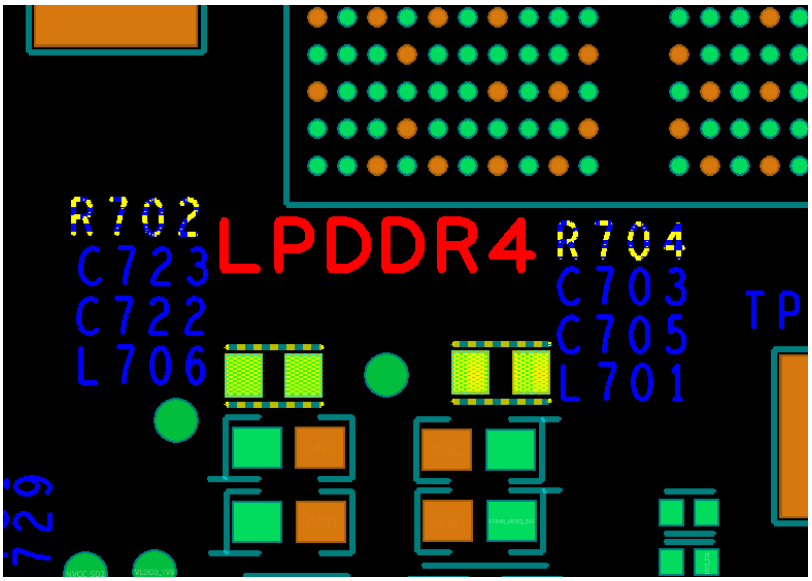

Figure 9. Board configuration for migration from LPDDR4X to LPDDR4 mode

- No hardware rework is required. Change the DRAM VDDQ power to 1.1 V by software to configure the PMIC by I2C after system power on.

2.8 SD card interface

The target processor has three ultra secure digital host controller (uSDHC) modules for SD/eMMC interface support. The uSDHC2 interface of the i.MX 93 processor connects to the microSD card slot (J1002) on the MCIMX93-QSB board. This connector supports one 4-bit SD3.0 microSD card. To select it as the boot device of the board, see Section 2.5.

2.9 eMMC memory

The eMMC memory is connected to the uSDHC1 interface of the i.MX 93 processor, which can support eMMC 5.1 devices. It is the default boot device of the board. Table 10 shows the boot settings.

Table 12 describes the eMMC memory device that is supported by the uSDHC1 interface.

Table 12. Supported eMMC device

Part identifier	Part number	Configuration	FBGA	Manufacturer	Memory size
U501	SDINBDA6-16G-I	3D TLC	TFBGA-153	SanDisk	16 GB

2.10 M.2 connector and Wi-Fi/Bluetooth module

The MCIMX93-QSB board supports the M.2/NGFF Key E mini card 75-pin connector, J1707. The M.2 mini card connector supports USB, SDIO, I2S, UART, I2C, SPI, and GPIO connection. The connector can be used for Wi-Fi/Bluetooth cards, 802.15.4 Radio, or 3G/4G cards.

On the board, the Murata Type-2EL M.2 module is assembled by default. It is based on an NXP IW612 chipset supporting dual-band (2.4 GHz / 5 GHz) 1x1 Wi-Fi 6, Bluetooth 5.2, and 802.15.4.

Table 13 describes the pinout of the M.2 mini card connector (J1707).

Table 13. M.2 mini card connector (J1707) pinout

Pin number	M.2 mini card connector pin	Connection details
2, 4, 72, 74	3V3_1, 3V3_2, 3V3_3, 3V3_4	Connects to VPCIe_3V3 power supply
6	LED1	Connects to M.2 Green LED, D1705
8	I2S_SCK	Connects to the SAI1_TXC pin of the processor
10	I2S_WS	Connects to the SAI1_TXFS pin of the processor
12	I2S_SD_IN	Connects to the SAI1_RXD pin of the processor
14	I2S_SD_OUT	Connects to the SAI1_TXD pin of the processor
16	LED2	Connects to M.2 Orange LED, D1706
20	UART_WAKE	M2_UART_nWAKE input for IO expander (PCAL6524HEAZ, P0_3, I2C address: 0x22)
22	UART_RXD	Connects to UART5_RXD, which is routed through resistor R417 to the processor pin DAP_TDI and processor interface DAP
32	UART_TXD	Connects to UART5_TXD, which is routed through resistor R414 to the processor pin DAP_TDO_TRACESWO and processor interface DAP

Table 13. M.2 mini card connector (J1707) pinout*...continued*

Pin number	M.2 mini card connector pin	Connection details
34	UART_CTS	Connects to UART5_CTSI, which is routed through resistor R416 to the processor pin DAP_TCLK_SWCLK and processor interface DAP
36	UART_RTS	Connects to UART5_RTSO, which is routed through resistor R419 to the processor pin DAP_TMS_SWDIO and processor interface DAP
38	VEN_DEF1	Connects to multiplexed SPI and UART signal, VEN_SPI_TXD/UART_SOUT
40	VEN_DEF2	Connects to multiplexed SPI and UART signal, VEN_SPI_RXD/UART_SIN
42	VEN_DEF3	Connects to multiplexed SPI and UART signal, VEN_SPI_CLK/UART_RTSO
50	SUSCLK	Connects to PMIC_32K_OUT, generated by PCA9451AHNY PMIC
52	PERST0	M2_nRST input for IO expander (PCAL6524HEAZ, P2_2, I2C address: 0x22)
54	W_DISABLE2	M2_nDIS2 input for IO expander (PCAL6524HEAZ, P2_3, I2C address: 0x22)
56	W_DISABLE1	M2_nDIS1 input for IO expander (PCAL6524HEAZ, P2_4, I2C address: 0x22)
58	I2C_DATA	Connects to the SDAL pin of PCA9451AHNY PMIC
60	I2C_CLK	Connects to the SCLL pin of PCA9451AHNY PMIC
62	ALERT	M2_nALERT input for IO expander (PCAL6524HEAZ, P1_2, I2C address: 0x22)
64	RESERVED	Connects to multiplexed SPI and UART signal, VEN_SPI_FRM/UART_CTSI
9	SDIO_CLK	Connects to the processor pin SD3_CLK and processor interface SDHC3
11	SDIO_CMD	Connects to the processor pin SD3_CMD and processor interface SDHC3
13	SDIO_DATA0	Connects to the processor pin SD3_DATA0 and processor interface SDHC3
15	SDIO_DATA1	Connects to the processor pin SD3_DATA1 and processor interface SDHC3
17	SDIO_DATA2	Connects to the processor pin SD3_DATA2 and processor interface SDHC3
19	SDIO_DATA3	Connects to the processor pin SD3_DATA3 and processor interface SDHC3
21	SDIO_WAKE	SD3_nWAKE input for IO expander (PCAL6524HEAZ, P0_5, I2C address: 0x22)
23	SDIO_RST	SD3_nRST output from IO expander (PCAL6524HEAZ, P1_4, I2C address: 0x22)
55	PEWAKE0	PCIE_nWAKE (not used on the board)
1, 7, 18, 33, 39, 45, 51, 57, 63, 69, 75	GND	Connected to the ground

For further details about i.MX 93 interfaces, see the *i.MX 93 Applications Processor Reference Manual*.

2.11 QSPI NOR Flash

The QSPI memory is connected to the FlexSPI interface of i.MX 93, which can support up to 166 MHz DDR mode device. The M.2 slot (J1707) is used on the board to insert the QSPI memory card. It can support 166 MHz SDR and 90 MHz DDR operation. To select it as the boot device of the EVK board, see the boot settings in Table 10.

2.12 CAN interface

The flexible controller area network (FlexCAN) is a full implementation of the CAN protocol specification, the CAN with flexible data rate (CAN FD) protocol, and the CAN 2.0 version B protocol, which supports both standard and extended message frames and long payloads. The i.MX93 processor supports two CAN FD controllers.

On the MCIMX93-QSB board, CAN transmit and receive signals are multiplexed with PDM clock and data signals. One four-channel switch TMUX1574RSVR (U1702) is used on the board to output either PDM CLK/Data or CAN transmit/receive data depending upon the configuration done through the IO expander (PCAL6524HEAZ, I2C Address 0x34).

On the board, one high-speed CAN transceiver TJA1057GT/3 supports the CAN interface. The high-speed CAN transceiver drives CAN signals (multiplexed with PDM data signals) between the target processor and a 4-pin header connected to its physical two-wire CAN bus.

Table 14 describes the HS CAN transceiver and header.

Table 14. High-speed CAN transceiver and header

Part identifier	Manufacturing part number	Description
U1501	TJA1057GT/3	High-speed CAN transceiver. It provides an interface between a CAN protocol controller and the physical two-wire CAN bus.
J1501	Not applicable	1x4 CAN header. It is connected to the CAN bus and allows external connection with the bus.

Note: *For details about TJA1057, see TJA1057 data sheet at nxp.com.*

Table 15 explains pinout for CAN header, J1501.

Table 15. CAN header - pinout

Pin	Signal name	Description
1	VDD_5V	5V power supply
2	CAN_H	CAN transceiver high signal
3	CAN_L	CAN transceiver low signal
4	GND	Ground

2.13 ADC interface

The i.MX93 processor supports one 12-bit 4-channel analog-to-digital converter (ADC).

On the MCIMX93-QSB board, two-channel ADC support is provided through one 8-pin ADC connector (J1405). The two channels connect to the ADC_IN0 and ADC_AN1 pins of the processor.

2.14 I3C interface

The MIPI Alliance Improved Inter-Integrated Circuit (MIPI I3C) brings major improvements in use and power over I2C, and provides an alternative to SPI for mid-speed applications. The i.MX93 processor supports two I3C modules: I3C1 and I3C2.

On MCIMX93-QSB, the I3C1 module is used as an I3C master for an Accelerometer/Gyroscope device (LSM6DSOXTR) and a Temperature sensor (P3T1085UK) connected to the I3C bus.

2.15 USB interface

The i.MX 93 processor features two USB 2.0 controllers (USB1 and USB2) with two integrated USB PHYs. On the MCIMX93-QSB board, the USB1 controller is used and is connected to the USB2.0 Type-C Port (J1101).

The 6-pin USB Type-C port is also available on the board for the power supply.

Table 16 describes the USB Type-C PD port and the associated peripheral devices.

Table 16. USB Type-C PD device connections

Part identifier	Device part type / part number	Description
J301	USB Type-C PD	It is used for power only. It does not support USB data transfer. It is the only power supply port therefore it must always be supplied for system power.
U303	NX20P0407	It is a single-chip USB Type-C port protection device that provides 28 V short-to-VBUS overvoltage protection to CC1/CC2 and SBU1/SBU2 pins.
U302	NX20P5090	It is an advanced 5 A unidirectional power switch for USB PD. It includes under voltage lockout, over voltage lockout, Reverse Current Protection, and overtemperature protection circuits. It is designed to isolate the power switch terminals automatically when a fault condition occurs.
U301	PTN5110	It is a single-port TCPC-compliant USB power delivery (PD) PHY IC that implements the Type-C configuration channel (CC) interface and USB PD Physical layer functions to a Type-C port manager (TCPM) that handles PD policy management.
SW301	M096H-A020RT21A	Switch to control CC for Type-C PD power on/off control. • SW301: 1-2/4-5 → PD adapter off (default setting) • SW301: 3-2/6-5 → PD adapter ON

Table 17 describes the peripherals used for connection between USB controller 1 and USB2.0 Type-C connector.

Table 17. Devices used for connection between USB controller 1 and USB2.0 Type-C connector

Part identifier	USB Port Type	Description
J1101	USB2.0 Type-C	Connects to full-speed USB host and device controller (USB 1) of the target processor. It can operate as a device or host. The USBC_VBUS signal controls the VBUS drive for the USB port.
U411	NX20P0407	It is a single-chip USB Type-C port protection device that provides 28 V short-to-VBUS overvoltage protection to CC1/CC2 and SBU1/SBU2 pins.
U402	NX20P3483UK	USB PD and Type-C high-voltage sink/source combo switch with protection
U401	PTN5110	It is a single-port TCPC-compliant USB power delivery (PD) PHY IC that implements the Type-C configuration channel (CC) interface and USB PD physical layer functions to a Type-C port manager (TCPM) that handles PD Policy management.
U405	TLV76033DBZR	This LDO is used for preventing the load SW NX20P3483UK enter into dead battery mode.

2.16 Ethernet

The i.MX 93 processor supports two Gigabit Ethernet controllers (capable of simultaneous operation) with support for energy efficient Ethernet (EEE), Ethernet AVB, and IEEE 1588.

On the MCIMX93-QSB board, one RTL8211FDI-VD-CG Ethernet transceiver is used that complies with 10Base-T, 100Base-TX, and 1000Base-T IEEE 802.3 standards. The data transferred between the Ethernet controller (ENET1) and PHY (U1712) is via the reduced gigabit media-independent interface (RGMII) for 1000Base-T, 10Base-T, and 100Base-TX.

The transceiver connects to one 10 / 100 / 1000 Mbit/s Link/Active RJ45 connector. The RJ45 connector integrates a Magnetic transformer inside, so it can be directly connected to an Ethernet transceiver (or PHY).

The ENET1_nRST signal from the I2C IO expander (U801, PCAL6524HEAZ) is used to reset the Ethernet transceiver.

Table 18 describes the peripheral devices between the processor and Gigabit Ethernet connector.

Table 18. Ethernet connections

Processor controller	Part identifier	Manufacturer and Part number	Description
ENET1	U1712	Realtek RTL8211FDI-VD-CG	The transceiver provides the physical layer functions to transmit and receive Ethernet packets with transmission and reception capabilities at 10 Mb/s, 100 Mb/s, or 1000 Mb/s.
	J501	-	RJ45 Gigabit Ethernet (10/100/1000 Mbit/s) connector for connecting an Ethernet cable
	U502	Nexperia PUSB3FR4	The device protects a high-speed Ethernet interface against electrostatic discharge (ESD).
	U503		

2.17 GPIO expansion

One 40-pin dual-row Raspberry Pi GPIO connector (J1401) is available on the MCIMX93-QSB board to support I2S, UART, I2C, and GPIO connections. The header can be used to access various pins or to plug in accessory cards, such as the 8MIC-RPI-MX8 card.

The connector is as shown in Figure 3.

Table 19 describes the GPIO connector (J1401) pinout.

Table 19. J1401 pin definition

Pin number	Signal
1	VRPi_3V3
2	EXP_5V
3	GPIO_IO02
4	EXP_5V
5	GPIO_IO03
6	GND
7	GPIO_IO04
8	GPIO_IO14
9	GND

Table 19. J1401 pin definition*...continued*

Pin number	Signal
10	GPIO_IO15
11	EXP_GPIO_IO17
12	EXP_GPIO_IO18
13	IOEXP_IO27
14	GND
15	IOEXP_IO22
16	EXP_GPIO_IO23
17	VRPi_3V3
18	EXP_GPIO_IO24
19	EXP_GPIO_IO10
20	GND
21	EXP_GPIO_IO09
22	EXP_GPIO_IO25
23	EXP_GPIO_IO11
24	EXP_GPIO_IO08
25	GND
26	GPIO_IO07
27	GPIO_IO00
28	GPIO_IO01
29	GPIO_IO05
30	GND
31	GPIO_IO06
32	EXP_GPIO_IO12
33	GPIO_IO13
34	GND
35	EXP_GPIO_IO19
36	EXP_GPIO_IO16
37	-
38	EXP_GPIO_IO20
39	GND
40	EXP_GPIO_IO21

2.17.1 GPIO Mux

On MCIMX93-QSB, three 2:1 (SPDT) 4-channel switches (TMUX1574RSVR) are provided 2:1 mapping of SPI, SAI, Ethernet, and expander GPIO signals on processor GPIO signals. The selection is done using the EXP_SEL configuration signal from the PCAL6524HEAZ IO expander.

Table 20, Table 21, and Table 22 describe the mapping of different signals on GPIO signals with the configuration detail.

Table 20. GPIO signals mapping using the four-channel TMUX1574RSVR switch (U803)

Source A signal	Source B signal	Output (Drain) signal	Configuration
SAI3_RXFS	EXP_GPIO_IO12	GPIO_IO12	EXP_SEL signal from PCAL6524HEAZ IO expander (U801) • SEL = Low: Source A signals are output as a drain • SEL = High: Source B signals are output as a drain
SAI3_RXC	EXP_GPIO_IO18	GPIO_IO18	
SAI3_TXD	EXP_GPIO_IO19	GPIO_IO19	
SAI3_RXD	EXP_GPIO_IO20	GPIO_IO20	

Table 21. GPIO signals mapping using the four-channel TMUX1574RSVR switch (U805)

Source A signal	Source B signal	Output (Drain) signal	Configuration
SPI3_CS0	EXP_GPIO_IO08	GPIO_IO08	EXP_SEL signal from PCAL6524HEAZ IO expander (U801) • SEL = Low: Source A signals are output as a drain • SEL = High: Source B signals are output as a drain
SPI3_MISO	EXP_GPIO_IO09	GPIO_IO09	
SPI3_MOSI	EXP_GPIO_IO10	GPIO_IO10	
SPI3_CLK	EXP_GPIO_IO11	GPIO_IO11	

Table 22. GPIO signals mapping using the four-channel TMUX1574RSVR switch (U804)

Source A signal	Source B signal	Output (Drain) signal	Configuration
ENET1_nINT	EXP_GPIO_IO16	GPIO_IO16	EXP_SEL signal from PCAL6524HEAZ IO expander (U801) • SEL = Low: Source A signals are output as a drain • SEL = High: Source B signals are output as a drain
SAI3_MCLK	EXP_GPIO_IO17	GPIO_IO17	
IMU_INT1	EXP_GPIO_IO21	GPIO_IO21	
-	-	-	

2.18 I2C IO expander

One MCIMX93-QSB, one 24-bit IO expander is provided to support I/O expansion through the I2C bus interface.

The detail of the IO expander is as below:

- Part number: U801
- Manufacturer and Part number: ON Semiconductor, PCAL6524HEAZ
- I2C address: 0x22 (0b'01000[10]x)

Table 23 describes IO Expander pin description.

Table 23. IO expander pinout

IO expander pin	Direction	Signal	Description
P0_0	I	TCPC_nINT	Interrupt from USB PHY PTN5110 (U301)
P0_1	I	RTC_nINTA	Interrupt from External RTC PCF2131 (U1004)
P0_2	O	EXP5V_EN	Enable signal for power switch AP22814AW5 (U58)
P0_3	I	M2_UART_nWAKE	UART wake signal from M.2 module
P0_4	I	HP_DET	Signal for audio jack (J1201) detection ***Note:*** *A low on HP_DET indicates that the audio jack is unplugged and a high indicates that the audio jack is plugged.*
P0_5	I	SD3_nWAKE	SD wake-up signal from M.2 module
P0_6	O	IOEXP_IO25	Signal for GPIO expander (J1401)
P0_7	O	IOEXP_IO24	Signal for GPIO expander (J1401)
P1_0	I	IOEXP_IO27	Signal for GPIO expander (J1401)
P1_1	I	AUD_nINT	Interrupt from audio codec
P1_2	I	M2_nALERT	I2C alert signal from M.2 module
P1_3	I	PMIC_nINT	Interrupt from PMIC PCA9451AHNY
P1_4	O	SD3_nRST	M.2 SD reset signal
P1_5	O	EXT1_PWREN	Controls power enable signal for MP2147GD (U1710) switch
P1_6	I	I3C_TEMP_nINT	Reserved for level shifter (default) and Temperature sensor (P3T1085UK)
P1_7	O	ENET1_nRST	Controls Ethernet PHY RTL8211 reset
P2_0	O	AUD_PWREN	Enables speaker power AUD_5V for the audio codec
P2_1	O	MIC/CAN_SEL	Configures the four-channel switch TMUX1574RSVR (U1702) to output either PDM CLK/Data or CAN transmit/receive data
P2_2	O	M2_nRST	Controls PCI reset (PERST0) pin of M.2 module
P2_3	O	M2_nDIS2	Controls output enable for 74AVC4T3144 (U904) translator
P2_4	O	M2_nDIS1	Controls power enable signal for MP2147GD (U1710) switch
P2_5	O	EXP3V3_EN	Enable signal for load switch AP22818AKBWT (U1714)
P2_6	O	EXP_SEL	Selection signal for three GPIO mux (TMUX1574RSVR): U803, U805, and U804 • EXP_SEL=0: SxA pin signals are output at Dx pins • EXP_SEL=1: SxB pin signals are output at Dx pins
P2_7	O	CAN_STBY	Control input for CAN transceiver TJA1057GT (U1501)

2.19 Control and debug interface

On the MCIMX93-QSB board, the control and debug interface is supported using the high-speed USB2.0 to UART device, FT4232H (U1706).

The FT4232H device features four UART ports. The first two ports are configured in multiprotocol synchronous serial engine (MPSSE) mode. These ports are used to emulate JTAG and I2C synchronous serial mode. The other two ports are configured in asynchronous serial mode and are used as UART ports for debugging Arm Cortex-A55 and Cortex-M33 cores.

Table 24 provides the connection detail of four 8-bit channels of the FT4232H device.

Table 24. FT4232H channel configuration

FT4232H channel	Configuration	Description
Channel A	JTAG interface	Used for remote JTAG debug interface ***Note:*** *Local JTAG - Standard 10-pin JTAG header (J1704) on board is used for local debug, paralleled with JTAG from the FTDI chip.*
Channel A/B	System test/control	• System automated test - The GPIOs on the A-bus of FT4232 are used to detect assertion of [POR_B, PMIC_ON_REQ, STBY_REQ, WDOG_B] from Q1407~Q1410, enabling the system automated tests. • System control - I2C from the B-bus of FT4232 and I2C IO expander (U1409) is used to control POR_B, SYS_nRST, and ONOFF for remote cold/warm reset and suspend/resume.
Channel B	Remote boot mode read/write	Used for general-purpose input / output (GPIO) expansion through the I2C−bus and interrupt
Channel C	UART → USB bridge	Used as an UART debug port for debugging the Arm Cortex-A55 core of the i.MX93 processor
Channel D	UART → USB bridge	Used as an UART debug port for debugging the Arm Cortex-M33 core of the i.MX93 processor

2.19.1 USB debug interface

On the MCIMX93-QSB board, a debug USB connector (J1708) is available that allows connection with the host computer for debugging the board. The USB connector connects with the FT4232H device through the USBDM/USBDP pins of the device.

Note: *The FT4232H device requires installing the USB drivers that can be downloaded from http://www.ftdichip.com. After the driver for FT4232H is installed, the host computer will enumerate four COM ports when the USB cable is plugged into the J1708 connector. This makes the device appear as a virtual COM port (VCP). You can use these ports to communicate with or debug the processor with the USB interface via a standard PC serial emulation port (for example, Putty and Tera Term). Table 25 describes the required parameter settings.*

Table 25. Terminal setting parameters

Data rate	*115,200 Baud*
Data bits	*8*
Parity	*None*
Stop bits	*1*

2.19.2 JTAG interface

The i.MX 93 Applications Processor has four JTAG signals on dedicated pins, and one HW reset input signal POR_B. The four JTAG signals used by the processor are:

- **JTAG_TCK (TAP Clock)**
- **JTAG_TMS (TAP Machine State)**
- **JTAG_TDI (TAP Data In)**
- **JTAG_TDO (TAP Data Out)**

These signals are connected on the MCIMX93-QSB board either to the FT4232H JTAG signals or to the 10-pin JTAG connector (J1704). To avoid the FT4232H JTAG conflict with external JTAG, the following configuration is used.

- RC_SEL = H, VTREF = OFF, remote JTAG is enabled
- RC_SEL = L, VTREF = OFF, local JTAG is enabled (default setting)

The MCIMX93-QSB board provides a 2x5-pin Samtec FTSH-105-01-L-DV-K header (J1704) for connecting a remote JTAG debugger for the board debugging. Table 26 describes the JTAG header pins.

Table 26. JTAG header (J1704) pinout

Pin number	Signal Name	Description
1	VTREF	Power supply
2	CON_JTAG_TMS	Test access point (TAP) machine state
3	GND	Ground
4	CON_JTAG_TCK	TAP clock
5	GND	Ground
6	CON_JTAG_TDO	TAP data out
7	GND	Ground
8	CON_JTAG_TDI	TAP data in
9	GND	Ground
10	SYS_nRST	System reset

The JTAG connector (J1704) is shown in Figure 3.

2.19.3 System ID

The MCIMX93-QSB board has a 2-kbit serial-I2C electrically erasable programmable read-only memory (EEPROM). The system ID memory detail is as below:

- Part identifier: U1405
- Manufacturer and part number: Microchip 93LC56BT

The 93LC56BT EEPROM connects with the FT4232H device through the following device pins:

- EECS - EEPROM – Chip Select, Type - I/O
- EECLK - Clock signal to EEPROM, Type - O
- EEDATA - EEPROM – Data, Type I/O

The system ID memory can be programmed over USB using FT_PROG. The memory is used to customize the USB VID, PID, serial number, product description strings, and power descriptor value of the FT4232H.

2.19.4 FTDI IO expansion

On MCIMX93-QSB, the 16-bit IO expander is connected with the FTDI-I2C port through SCL/SDA pins. The detail of the IO expander is as below:

- Part number: U1409
- Manufacturer and Part number: ON Semiconductor, PCA9655EMTTXG
- I2C address: 0b'0100001x (0x21)

Table 27 describes IO expander.

Table 27. FTDI IO expander (U1409) pinout

IO expander pin	Direction	Signal	Description
IO0_0	I/O	FT_BOOT_MODE0	Boot mode configuration pins. ON the board, boot mode configuration can be selected either by the SW601 DIP switch or in software through the IO expander. For details on boot mode and boot device configuration, see Section 2.5.
IO0_1	I/O	FT_BOOT_MODE1	
IO0_2	I/O	FT_BOOT_MODE2	
IO0_3	I/O	FT_BOOT_MODE3	
IO0_[7:4]	-	-	Not connected
IO1_0	O	FT_POR_B	Active-low power-on reset for battery-backed nonsecure module (BBNSM) of the processor
IO1_1	O	FT_SYS_nRST	System reset. On the board, system reset can either be done using the reset button SW1402 or in software through the IO expander.
IO1_2	O	FT_ONOFF	ON/OFF for the NVCC_BBSM module of the processor. On the board, ON/OFF functionality can be provided either using the ONOFF button SW1401 or in software through the IO expander.
IO1_3	O	FT_RC_SEL	-
IO1_4	O	FT_BMODE_DIR	Direction control input for dual supply translating transceiver (74AVC4T245GU)
IO1_5	O	FT_SD_PWREN	Power enable for SD card connector (J1002)
IO1_6	O	FT_SD_CD	Enable SD card detect signal
IO1_7	-	-	Not connected

2.20 PCB information

Table 1 lists the dimensions of the MCIMX93-QSB. The board is made with standard 4-layer technology and the material used is FR4. Table 28 describes the PCB stack-up information.

Table 28. MCIMX93-QSB stack up information

Layer	Description	Copper (Oz.)	Generic	Er	Dielectric thickness (mil)
1	Signal	0.5+Plating	-	-	-
-	Dielectric	-	106 H	3.52	2.072
2	GND	1	-	-	-
-	Dielectric		Core 1.4 MM	3.76	55.12
3	Power	1	-	-	-
-	Dielectric	-	106 H	3.52	2.072
4	Signal	0.5+Plating	-	-	-

Table 28. MCIMX93-QSB stack up information...*continued*

Layer	Description	Copper (Oz.)	Generic	Er	Dielectric thickness (mil)
Finished:	62.992 (+6.299/-6.299) mil			1.6 (+0.16/-0.16) MM	
Designed:	63 mil			1.57 MM	
Material:	185 HR				

3 Board errata

Not applicable for the current board revision.

4 Related documentation

Table 29 lists and explains the additional documents and resources that you can refer to for more information on the MCIMX93-QSB board. Some of the documents listed below may be available only under a non-disclosure agreement (NDA). To request access to these documents, contact your local field applications engineer (FAE) or sales representative.

Table 29. Related documentation

Document	Description	Link / how to access
i.MX 93 Applications Processor Reference Manual	Intended for system software and hardware developers and application programmers who want to develop products with i.MX 93 MPU	IMX93RM
i.MX 93 Application Processors Data Sheet for Industrial Products	Provides information about electrical characteristics, hardware design considerations, and ordering information	IMX93IEC
i.MX93 Hardware Design Guide	This document aims to help hardware engineers design and to test their i.MX 93 processor-based designs. It provides information about board layout recommendations and design checklists to ensure first-pass success and avoidance of board bring-up problems.	IMX93HDG

5 Acronyms

Table 30 lists and explains the acronyms used in this document.

Table 30. Acronyms

Term	Description
BGA	Ball grid array
CAN	Controller area network
Codec	A combination of a coder and decoder operating in different directions of transmission in the same equipment
DMIC	Digital PDM microphone
FD	Flexible data-rate
GPIO	General-purpose input/output

Table 30. Acronyms...*continued*

Term	Description
HS	High-speed
I2C	Inter-integrated circuit
I2S	Inter-IC sound
I3C	Improved inter-integrated circuit
IDE	Integrated development environment
LDO	Low dropout regulator
LED	Light-emitting diode
MCU	Microcontroller unit
MIPI	Mobile industry processor interface
NGFF	Next generation form factor
PDM	Pulse-density modulation
PMIC	Power management integrated circuit
POR	Power-on reset
PWM	Pulse width modulation
QSPI	Quad serial peripheral interface
RGMII	Reduced gigabit media independent Interface
SMT	Surface-mount technology
UART	Universal asynchronous receiver/transmitter
USB	Universal serial bus
uSDHC	Ultra secure digital host controller

6 Revision history

Table 31 summarizes the revisions to this document.

Table 31. Revision history

Document ID	Release date	Description
UM12044 v.1	12 February 2024	Initial public release

Legal information

Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at https://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Suitability for use in non-automotive qualified products — Unless this document expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

NXP B.V. — NXP B.V. is not an operating company and it does not distribute or sell products.

Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

Contents

For more information, please visit: https://www.nxp.com

Date of release: 12 February 2024
Document identifier: UM12044

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

NXP:

MCIMX93-QSB