# UM11734

## Hardware user manual for FRDM665SPIEVB

Rev. 1 — 25 July 2022 User manual

**Document information**

| Information | Content |
|---|---|
| Keywords | MC33665A, SPI, BMS gateway IC |
| Abstract | User manual for starting work with MC33665A SPI EVB. |

**Revision history**

| Rev | Date | Description |
|---|---|---|
| 1 | 20220725 | initial version |

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# 1 Introduction

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This page guides the user through the process of setting up and using the MC33665A serial peripheral interface (SPI) evaluation board (EVB).

# 2 Finding kit resources and information on the NXP web site

NXP Semiconductors provides online resources for this evaluation board and its supported device(s) on http://www.nxp.com.

The information page for the FRDM665SPIEVB evaluation board is at http://www.nxp.com/FRDM665SPIEVB. The information page provides overview information, documentation, software and tools, parametrics, ordering information and a Getting Started tab. The Getting Started tab provides quick-reference information applicable to using the FRDM665SPIEVB evaluation board, including the downloadable assets referenced in this document.

# 3 Getting ready

Working with the FRDM665SPIEVB requires the kit contents, additional hardware, and a Windows PC workstation with installed software.

## 3.1 Kit contents

The FRDM665SPIEVB kit includes:

- MC33665A SPI EVB, SPI to four transformer physical layer (TPL) interface EVB
- One TPL daisy chain cable; two-wire twisted-pair daisy chain interface cable
- One power cable, 4-pin socket
- Quick Start Guide

## 3.2 Additional hardware

In addition to the kit contents, the following hardware is necessary or beneficial:

- External dual power supply 8 V to 16 V/2 A (optional)
- EVBs of battery cell controller (BCC) devices from NXP
- S32K344EVB-Q172 evaluation and development board for S32K344 from NXP
- 14-cell battery pack or a battery emulator, such as BATT-14CEMULATOR

# 4 Getting to know the hardware

## 4.1 Kit overview

The FRDM665SPIEVB serves as a hardware evaluation tool in support of the MC33665A device of NXP. The MC33665A is a gateway router that can route TPL messages from a microcontroller to four different TPL ports. It is designed for use in both automotive and industrial applications. The device can route both TPL2 and TPL3 messages. FRDM665SPIEVB is an ideal board for rapid prototyping of MC33665A for SPI interface to MCU.

FRDM665SPIEVB supports an SPI for both requests (REQ) and responses (RSP). Differential communication to daisy chain devices can be established with four different ports.

## 4.2 Board features

The main features of FRDM665SPIEVB are:

- Request SPI
- Response SPI
- Onboard transformer isolation for TPL communication to BCC devices
- Configurable VIO voltage
- Configurable VDD5V from internal and external supply
- DIP switch for configuring the SPI of MC33665A to operate with or without crystals
- Reset switch for the device and board
- LED display for the status of power
- Connectors to interface directly with S32K344EVB launchpad
- Connectors for external interface to general-purpose input/output (GPIO) and $I^2C$-bus

## 4.3 Block diagram

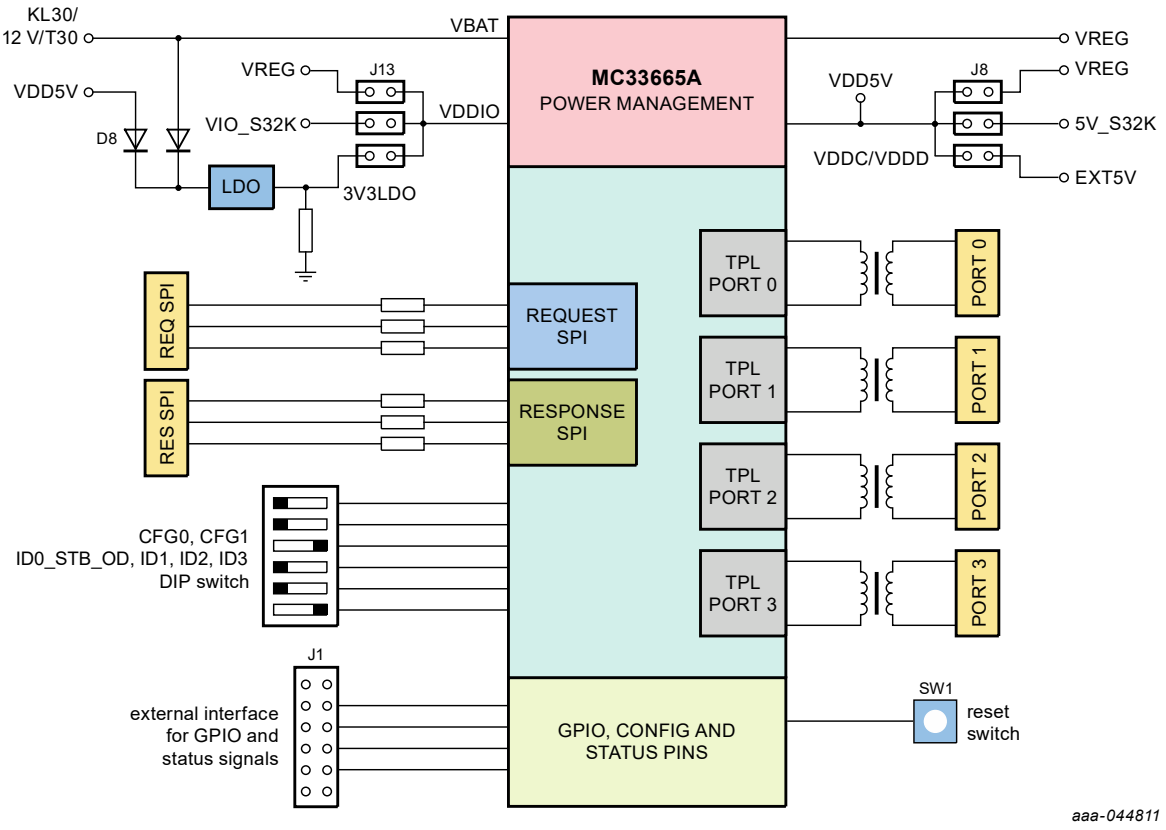


**Figure 1. FRDM665SPIEVB block diagram**

## 4.4 Board description

The FRDM665SPIEVB allows the user to prototype and test all functions of the MC33665A gateway router.

It can be stacked directly on the S32K344EVB. Different modes of SPI communication can be established with MC33665A from K1 to K6 connectors. The FRDM665SPIEVB can be supplied with 12 V at J6 connector or it can be powered directly from S32K344EVB or EXT5V at J11. VDDC and VDDD can be selected by bridging one of the positons in jumper J8 (Table 7) to select the 5 V. Bridging options jumper at J13 (Table 8) makes it possible to select the VIO voltage of 3.3 V or 5 V or VIO of S32K344EVB. S32K344EVB can be supplied with USB connection when connected to a PC.

SPI interface to external controller boards can be done with J7 for REQ SPI and J16 for RSP SPI. Ensure the VIO of external controller board is the same as the VIO selected with jumper J13. Single SPI or dual SPI modes can be selected by using jumpers at J14. Populating all jumpers at J14 enables single SPI mode and depopulates jumpers at J14 for dual SPI mode. SW2 DIP switch can be used to select the CFG and ID configuration for MC33665A. BCC devices can be connected to daisy chain ports 0 to 3 via connectors J5, J12, J17, and J18.

Connector J1 gives the option to access the GPIO and $I^2C$-bus pins of MC33665A.

Contact the NXP engineering team for using TPL autowake function in FRDM665SPIEVB.

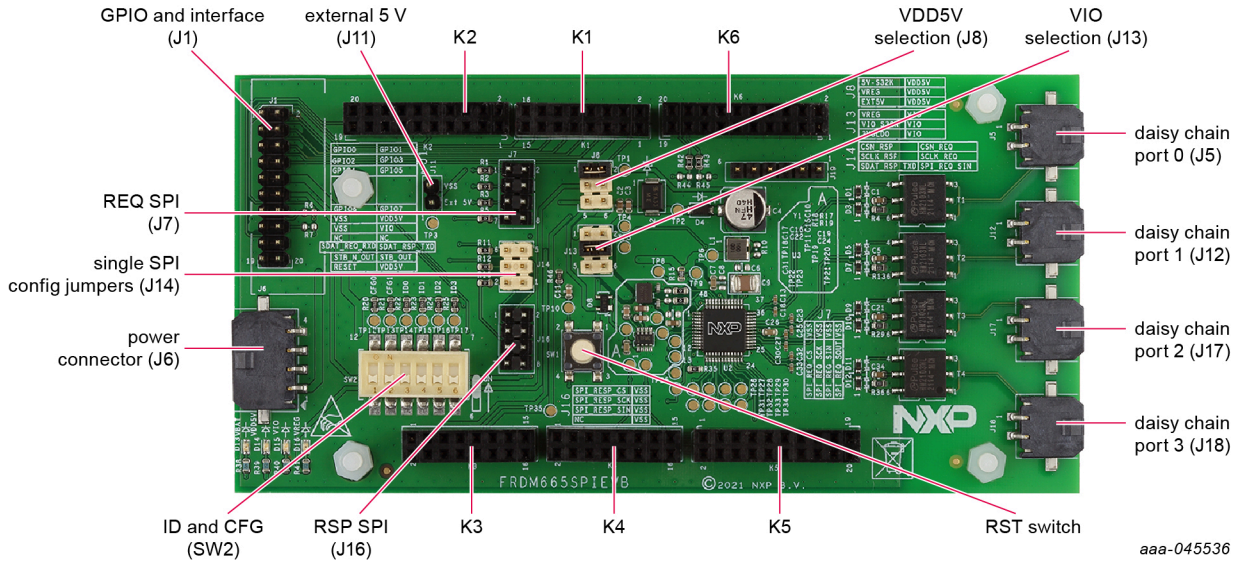


**Figure 2. SPI EVB description**

Power configuration of the board can be reflected by LEDs populated on board. LEDs glow on board reflects the right power interface connected to FRDM665SPIEVB.

**Table 1. Power status LEDs**

| LED | VBAT 12 V | External 5 V | S32K344EVB |
|---|---|---|---|
| D13 - red | X | - | - |
| D14 - green | X | X | X |
| D15 - green | X | X | X |
| D16 - red | X | - | - |

## 4.5 Connectors

FRDM665SPIEVB has multiple connectors for interfacing to MCU, internal GPIO, and external BCC devices.

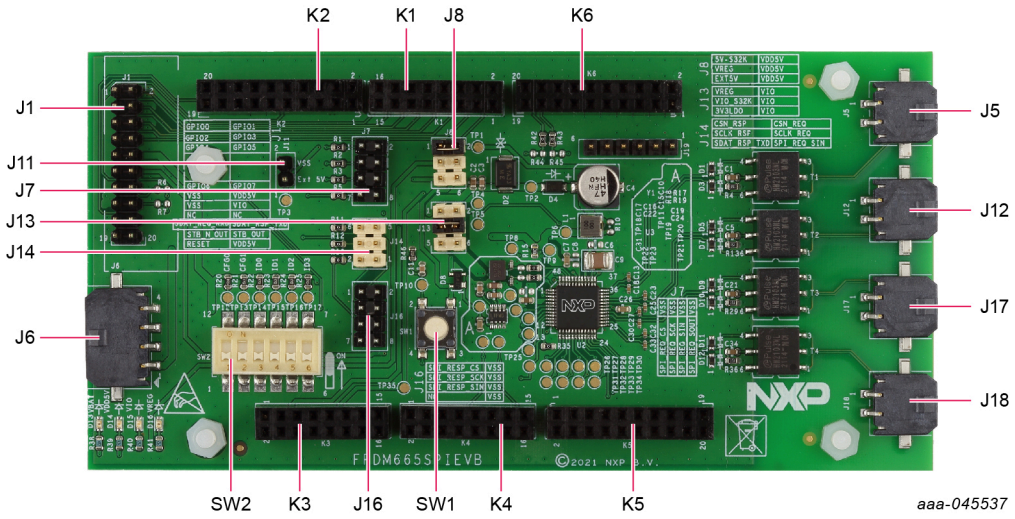


**Figure 3. FRDM665SPIEVB connectors**

Pin configuration of connectors is shown in Table 2 to Table 15.

**Table 2. Power connector - J6**

| Pin number | Connection | Description |
|---|---|---|
| 1 | VBAT | connection to 12 V |
| 2 | - | not connected |
| 3 | - | not connected |
| 4 | GND | ground connection for MC33665A and interface boards |

**Table 3. GPIO and interface - J1**

| Pin number | Connection | Description |
|---|---|---|
| 1 | GPIO0 | interface to GPIO0 or INT0 for MC33665A |
| 2 | GPIO1 | interface to GPIO1 or INT1 for MC33665A |
| 3 | GPIO2 | interface to GPIO2 or INT2 for MC33665A |
| 4 | GPIO3 | interface to GPIO3 or INT3 for MC33665A |
| 5 | GPIO4 | interface to GPIO4 or $I^2C$-bus in MC33665A |
| 6 | GPIO5 | interface to GPIO5 or $I^2C$-bus in MC33665A |
| 7 | GPIO6 | interface to GPIO6 or SYNC in MC33665A |
| 8 | GPIO7 | interface to GPIO7 or HOLD in MC33665A |
| 9 | VSS/GND | ground |
| 10 | VDD5V | 5 V supply line |
| 11 | VSS/GND | ground |
| 12 | VIO | VIO interface for MC33665A |
| 13 | - | not connected |
| 14 | - | not connected |

**Table 3. GPIO and interface - J1*...continued***

| Pin number | Connection | Description |
|---|---|---|
| 15 | NC-SDAT_RSP_TXD | connect R6 to interface SDAT_RSP_TXD of MC33665A |
| 16 | NC-SDAT_REQ_RXD | connect R7 to interface SDAT_REQ_RXD of MC33665A |
| 17 | STB_N_OUT | inverted standby signal from MC33665A |
| 18 | STB_OUT | standby signal from MC33665A |
| 19 | RESET | reset signal for MC33665A |
| 20 | VDD5V | 5 V supply line |

**Table 4. Response SPI - J16**

| Pin number | Connection | Description |
|---|---|---|
| 1 | SPI_RESP_CS | chip select for response SPI |
| 2 | GND | ground |
| 3 | SPI_RESP_CLK | clock interface for response SPI |
| 4 | GND | ground |
| 5 | SPI_RESP_SIN | response TXD of MC33665A |
| 6 | GND | ground |
| 7 | - | not connected |
| 8 | GND | ground |

**Table 5. Request SPI - J7**

| Pin number | Connection | Description |
|---|---|---|
| 1 | SPI_REQ_CS | chip select for request SPI |
| 2 | GND | ground |
| 3 | SPI_REQ_SCK | clock interface for request SPI |
| 4 | GND | ground |
| 5 | SPI_REQ_SIN | response TXD of MC33665A; interfaced to MC33665A by shorting jumper pin 1 and pin 2 in J14 |
| 6 | GND | ground |
| 7 | SPI_REQ_SOUT | request RXD of MC33665A |
| 8 | GND | ground |

**Table 6. External 5 V - J11**

| Pin number | Connection | Description |
|---|---|---|
| 1 | EXT5V | external 5 V supply |
| 2 | VSS/GND | ground |

**Table 7. VDD5V jumper - J8**

| Pin number | Connection | Description |
|---|---|---|
| 1-2 | 5V-S32K344EVB | connection of 5 V from S32K344EVB to MC33665A SPI EVB; functional only when FRDM665SPIEVB is used with S32K344 stackable EVB. Note: Default connection. |
| 3-4 | VREG | 5 V generated by VREG is connected to VDD5V. Note: It needs an external 12 V connection to VBAT with J6. |
| 5-6 | EXT5V | external 5 V supply connected to J11 is selected for EXT5V |

**Table 8. VIO jumper - J13**

| Pin number | Connection | Description |
|---|---|---|
| 1-2 | VREG | connects constant 5 V generated by VREG to VDDIO/VIO of MC33665A |
| 3-4 | VIO-S32K | connects VIO preselected in S32K344EVB to MC33665A. Note: Default connection. |
| 5-6 | 3V3LDO | connects constant 3.3 V generated by low dropout (LDO) to VDDIO/VIO of MC33665A |

**Table 9. Single SPI jumper - J14**

| Pin number | Connection | Description |
|---|---|---|
| 1-2 | SDAT_RSP_TXD | bridge SDAT_RSP_TXD for single SPI mode |
| 3-4 | SCLK_RSP | bridge SCLK_RSP with SCLK_REQ for single SPI mode |
| 5-6 | CSN_RSP | bridge CSN_RSP with CSN_REQ for single SPI mode |

**Table 10. S32K344EVB connector - K1**

| Pin number | Connection | Description |
|---|---|---|
| 1 | HOLD | interface to MC33665A GPIO7 |
| 3 | SYNC | interface to MC33665A GPIO6 |
| 5 | GPIO5 | interface to MC33665A GPIO5 |
| 7 | GPIO4 | interface to MC33665A GPIO4 |
| 9 | GPIO3 | interface to MC33665A GPIO3 |
| 11 | GPIO2 | interface to MC33665A GPIO2 |
| 13 | GPIO1 | interface to MC33665A GPIO1 |
| 15 | GPIO0 | interface to MC33665A GPIO0 |
| Other | - | not connected |

**Table 11. S32K344EVB connector - K2**

| Pin number | Connection | Description |
|---|---|---|
| 1 | STB_OUT | interface to MC33665A standby signal STB_OUT |

**Table 11. S32K344EVB connector - K2***...continued*

| Pin number | Connection | Description |
|---|---|---|
| 5 | CSN_RSP | interface to MC33665A CSN_RSP |
| 7 | SDAT_REQ_RXD | interface to MC33665A request RXD |
| 9 | SDAT_RSP_TXD | interface to MC33665A response TXD |
| 11 | SCLK_RSP | interface to MC33665A response clock |
| 17 | RESET | interface to MC33665A RESET signal |
| 19 | WAKE_IN | interface to MC33665A WAKE_IN signal |
| Other | - | not connected |

**Table 12. S32K344EVB connector - K3**

| Pin number | Connection | Description |
|---|---|---|
| 3 | VIO-S32K | preselected VIO from S32K344EVB |
| 9 | 5V-S32K | 5 V power rail from S32K344EVB |
| 11 | VSS | ground |
| 13 | VSS | ground |
| Other | - | not connected |

**Table 13. S32K344EVB connector - K4**

| Pin number | Connection | Description |
|---|---|---|
| 7 | SCLK_REQ | request clock signal to MC33665A |
| 13 | SDAT_REQ_RXD | request RXD signal to MC33665A |
| 15 | CSN_REQ | request CSN to MC33665A |
| Other | - | not connected |

**Table 14. S32K344EVB connector - K5**

| Pin number | Connection | Description |
|---|---|---|
| 12 | VSS | ground |
| Other | - | not connected |

**Table 15. S32K344EVB connector - K6**

| Pin number | Connection | Description |
|---|---|---|
| 5 | SDAT_RSP_TXD | response signal from MC33665A<br>• Must disable pin of S32K344 |
| 7 | SDAT_REQ_RXD | request signal to MC33665A<br>• Must disable pin of S32K344 |
| 12 | VSS | ground |

Table 15. S32K344EVB connector - K6...*continued*

| Pin number | Connection | Description |
|---|---|---|
| Other | - | not connected |

# 5 Configuring the hardware

FRDM665SPIEVB can be configured as stacked board to S32K344EVB.

## 5.1 Stacked board configuration

As shown in Figure 4, FRDM665SPIEVB and S32K344EVB can be connected together and stacked for communication (dual SPI) and power interface. Power can be supplied to FRDM665SPIEVB with K3 connector from S32K344EVB. External power supply to FRDM665SPIEVB with J6 connector is optional. Check the power LEDs D15 and D14 during this setup or configuration. In case it is not glowing, check the jumper settings at J8 and J13. Jumpers J8 and J13 must be connected appropriately to have VDD5V and VIO to MC33665A from S32K344EVB. For stacked board configuration, remove the four plastic holders placed on four corners of FRDM665SPIEVB.

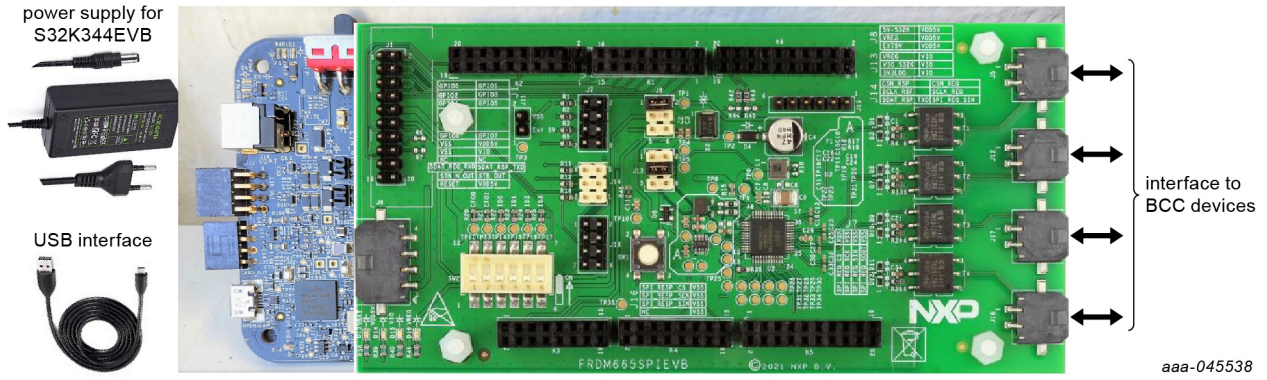


**Figure 4. Board interface connections**

## 5.2 External board configuration

FRDM665SPIEVB can be interfaced with external microcontroller boards for SPI and GPIO interface of MC33665A. Connect 12 V at J6 or external 5 V to J11 interface. Select the 5 V to MC33665A with jumper J8. Care should be taken in selecting the right VIO for both external microcontroller board and FRDM665SPIEVB. Jumper J13 can be used to select the right VIO for MC33665A. Before powering up the boards, crosscheck the VIO selection for microcontroller board and FRDM665SPIEVB. Care must be taken for interconnection wires of request SPI and response SPI from external microcontroller board to FRDM665SPIEVB. It must be twisted pair with short GND wires interconnecting the boards (FRDM665SPIEVB and microcontroller).

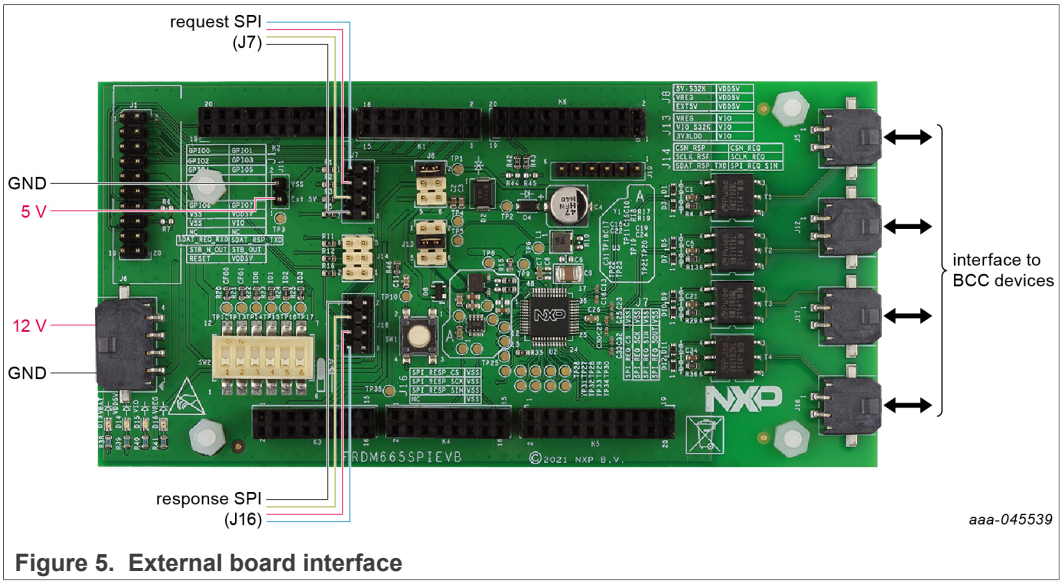


**Figure 5. External board interface**

Communication can be established by MCU to BCC devices connected on different ports with SPI interface on MC33665A.

# 6 Available accessories

**Table 16. Accessories**

| Part number | Description |
|---|---|
| FRDM33772CSPEVB | evaluation board for MC33772C with SPI communication |
| RD33771CDSTEVB | evaluation board for MC33771C BCC with isolated daisy chain communication |
| BATT-14EXTENDER | battery emulator extender |
| BATT-14CEMULATOR | 14-cell battery pack to supply MC33771C EVBs |
| S32K3X4EVB-Q172 | evaluation and development board for general-purpose MCU (S32K344) |
| BATT-TPLCABLE20 | TPL, two-wire, twisted, 20 cm long cable |
| BATT-TPLCABLE50 | TPL, two-wire, twisted, 50 cm long cable |
| BATT-14CTCABLE25 | cell terminal (CT) cable, 14 cells, 25 cm long |

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