TJA1466

CAN SIC transceiver with partial networking and advanced system monitoring

Rev. 1.0 — 16 October 2024 Product data sheet

1 General description

The TJA1466 is a high-speed CAN transceiver that provides an interface between a controller area network (CAN) or flexible data rate CAN (CAN FD) protocol controller and the physical two-wire CAN bus. TJA1466 transceivers implement the CAN physical layer as defined in ISO 11898-2:2024 and SAE J2284-1 to SAE J2284-5, making them fully interoperable with high-speed classical CAN and CAN FD transceivers. The TJA1466 was developed in compliance with ISO 26262, achieving ASIL B.

The TJA1466 features very low power consumption in Standby and Sleep modes. It supports CAN partial networking by means of selective wake-up functionality as specified in ISO 11898-2:2024, making the TJA1466 the ideal choice for CAN system implementations where only nodes that are needed are to be activated. Nodes that are not needed for the function being performed can be powered down to minimize system power consumption, even when CAN bus traffic is running.

The TJA1466 includes a comprehensive set of features including two configurable general-purpose I/O pins (GPIO), an SPI for configuration, mode control and diagnostics, a question & answer (Q&A) watchdog with dedicated reset and failsafe/limp home pins and accurate V_{IO} undervoltage and overvoltage monitoring.

The TJA1466 can be configured to ignore CAN FD and CAN XL frames while waiting for a valid wake-up frame. This additional feature of partial networking, called CAN FD/XL passive, is the perfect fit for networks that support a mix of classical CAN, CAN FD and CAN XL communication.

In Normal mode, the TJA1466 supports external CAN protocol controllers that communicate according to classical CAN, CAN FD, or CAN XL in SIC mode without switching to FAST mode (according to ISO 11898-2:2024 Annex A).

The TJA1466 features CAN signal improvement capability (SIC), as defined in ISO 11898-2:2024. SIC significantly reduces signal ringing on a network, allowing reliable 2 Mbit/s and 5 Mbit/s CAN FD communication in larger and more complex topologies. Tight bit timing symmetry enables CAN FD communication up to 8 Mbit/s.

The TJA1466 comes in three variants:

- TJA1466A supporting 1.8 V V_{IO} supply and monitoring
- TJA1466B supporting 3.3 V V_{IO} supply and monitoring
- TJA1466C supporting 5 V V_{IO} supply and monitoring

2 Features and benefits

2.1 General

- ISO 11898-2:2024 parameter sets A-C, SAE J2284-1 to SAE J2284-5 and SAE J1939-14 compliant

- ISO 26262, ASIL B compliant
- Partial networking capability through selective wake-up functionality
- Q&A watchdog with window and timeout modes
- Configurable general-purpose I/O (GPIO) pins
- Second RXD and/or TXD pins (RXD2/TXD2), configurable via GPIO
- Direct transmitter on/off control input (TXEN_N) via GPIO
- CAN signal improvement capability as defined in ISO 11898-2:2024 parameter set C to significantly reduce signal ringing effects on a network
- Autonomous bus biasing
- Low electromagnetic emission (EME) and high electromagnetic immunity (EMI)
- Qualified according to AEC-Q100 Grade 1
- VIO input for interfacing with 1.8 V, 3.3 V to 5 V microcontrollers
- ListenOnly mode for node diagnosis and failure containment
- DHVQFN18 package (3.0 mm × 4.5 mm) with automatic optical inspection (AOI) capabilities
- Option to disable Sleep mode
- Software Development mode
- Dark green product (halogen free and restriction of hazardous substances (RoHS) compliant)
- Selectable interrupts on RXD; option to signal only wake-up and power-on related interrupts or all interrupts
- 4-byte general-purpose memory
- SPI system reset
- End-of-line microcontroller flashing support through CAN pins
- Selectable WAKE pin filter time

2.2 Predictable and fail-safe behavior

- Undervoltage detection on all supply pins with defined behavior below the undervoltage thresholds
- Functionality guaranteed from the undervoltage detection thresholds up to the maximum limiting voltage values
- Transceiver disengages from the bus (high-ohmic) when the battery voltage drops below the Off mode threshold
- Internal biasing of TXD to enable defined fail-safe behavior
- Dedicated failsafe pin, configurable for limp-home or failsafe output functionality
- Dedicated reset pin for triggering and detecting reset events

2.3 Low-power management

- Very low-current Standby and Sleep modes, with local and remote wake-up capability
- Local wake-up via the WAKE pin
- Remote wake-up via a wake-up pattern (WUP) or wake-up frame (WUF)
- Configurable CAN wake-up pattern (dom-rec-dom or dom-rec-dom-rec) according to ISO 11898-2:2024.
- Selective wake-up according to ISO 11898-2:2024
- Entire node containing the TJA1466 can be powered down via INH while still supporting local and remote wake-up
- Only V_{BAT} is needed to support local and remote wake-up
- Support for pretended networking through low-power ListenOnly mode

2.4 Diagnosis and Protection

- Overtemperature diagnosis and protection

- Overvoltage detection with defined behavior on VIO supply pin
- Transmit data (TXD) dominant time-out diagnosis and protection
- Bus dominant failure diagnosis
- Cold start diagnosis (first battery connection)
- High ESD handling capability on the bus pins
- Bus pins and VBAT protected against automotive transients

3 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT}	battery supply voltage		4.75	-	40	V
I_{BAT}	battery supply current	Normal mode or (ListenOnly mode; VBATVCC = 1 or LPL = 0); $V_{BAT} \leq 28$ V	-	-	400	µA
		ListenOnly mode; VBATVCC = 0 and LPL = 1; $V_{BAT} \leq 28$ V	-	-	525	µA
		Sleep or Standby mode; CAN Offline Bias mode; partial networking enabled; $T_{vj} < 85$ °C; VBATVCC = 0	-	-	450	µA
		Sleep mode; CAN Offline mode; $T_{vj} < 85$ °C; $V_{IO} = 0$ V	-	12	20	µA
		Standby mode; CAN Offline mode; $T_{vj} < 85$ °C	-	-	50	µA
$V_{uvd(VBAT)}$	undervoltage detection voltage on pin VBAT		4.25	-	4.75	V
V_{CC}	supply voltage		4.5	-	5.5	V
I_{CC}	supply current	Normal mode; transmitter dominant	-	42	60	mA
		Normal or (ListenOnly mode and LPL = 0); transmitter recessive	-	7	10	mA
		ListenOnly mode; LPL = 1; VBATVCC = 1; $T_{vj} < 150$ °C	-	90	165	µA
		ListenOnly mode; LPL = 1; VBATVCC = 0; $T_{vj} < 150$ °C	-	-	40	µA
		Sleep or Standby mode; $T_{vj} < 85$ °C	-	-	3	µA
$V_{uvd(VCC)}$	undervoltage detection voltage on pin VCC		4	-	4.5	V
V_{IO}	supply voltage		1.71	-	5.5	V
I_{IO}	supply current	Normal or ListenOnly mode (excluding pull-up currents on V_{IO}-related pins)	-	-	5	µA
		Standby or Sleep mode; $T_{vj} < 85$ °C	-	-	2	µA
$V_{uvd(VIO)}$	undervoltage detection voltage on pin VIO	Sleep mode	1.5	-	1.71	V
$V_{uvd(VIO)}$[1]	undervoltage detection voltage on pin VIO	TJA1466A	1.62	-	1.692	V
		TJA1466B, TJA1466C	2.97	-	3.102	V
$V_{uvr(VIO)}$[1]	undervoltage recovery voltage on pin VIO	TJA1466A	1.638	-	1.71	V
		TJA1466B, TJA1466C	3.003	-	3.135	V
$V_{ovd(VIO)}$[1]	overvoltage detection voltage on pin VIO	TJA1466A	1.89	-	1.98	V
		TJA1466B	3.465	-	3.63	V
		TJA1466C	5.25	-	5.5	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 on pins CANH, CANL	-8	-	+8	kV

Table 1. Quick reference data*...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CANH}	voltage on pin CANH	limiting value	-36	-	+40	V
V_{CANL}	voltage on pin CANL	limiting value	-36	-	+40	V
T_{vj}	virtual junction temperature		-40	-	+150	°C

[1] In all modes except Sleep and Off.

4 Ordering information

Table 2. Ordering information

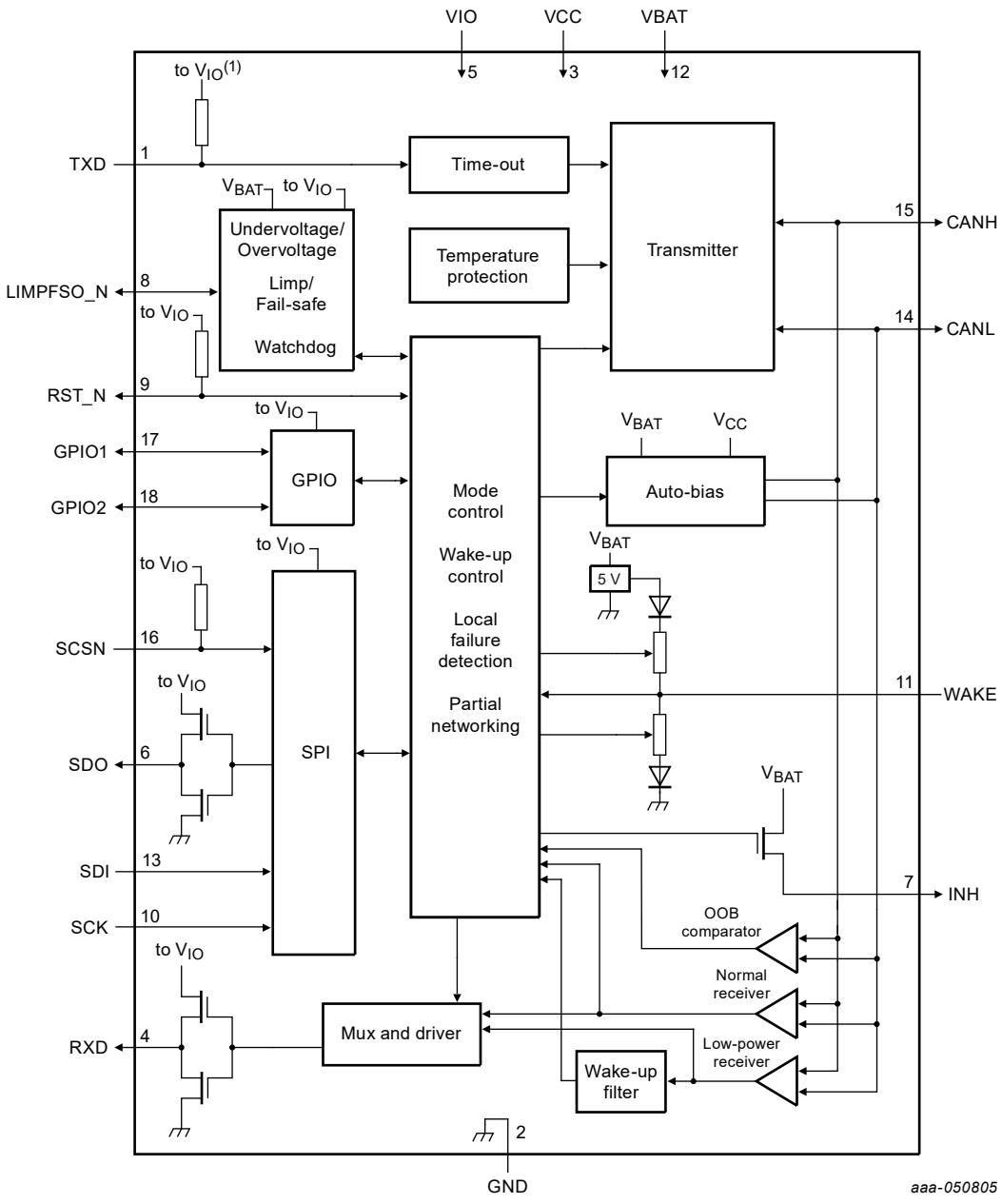
Type number	Package		
	Name	Description	Version
TJA1466AHG	DHVQFN18	plastic thermal enhanced very thin small outline package; no leads; 18 terminals; body 3 × 4.5 × 0.85 mm	SOT2163-1
TJA1466BHG			
TJA1466CHG			

Table 3. Feature overview of the complete TJA1466 family

See Section 18 for a feature overview of the complete TJA1445x/TJA1446x/TJA1465x/TJA1466x family.

	Partial Networking			V_{IO} supply			Data rate		Special features							
Device	Selective wake-up	CAN FD passive	CAN XL passive	1.8 V V_{IO}	3.3 V V_{IO}	5.0 V V_{IO}	Up to 5 Mbit/s CAN FD	Up to 8 Mbit/s CAN SIC	ISO 26262 ASIL B compliance	GPIO pins	TXEN_N pin	RST_N pin	FSO/LIMP pin	V_{IO} undervoltage monitoring	V_{IO} overvoltage monitoring	Q&A watchdog
TJA1466A	●	●	●	●			●	●	●	2		●	●	●	●	●
TJA1466B	●	●	●		●		●	●	●	2		●	●	●	●	●
TJA1466C	●	●	●			●	●	●	●	2		●	●	●	●	●

5 Block diagram



(1) See Table 8.

Figure 1. Block diagram

6 Pinning information

6.1 Pinning

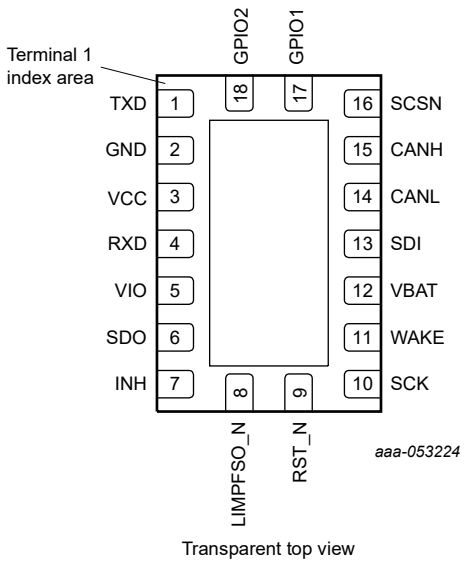


Figure 2. Pin configuration diagram

6.2 Pin description

Table 4. Pin description

Symbol	Pin	Type[1]	Description
TXD	1	I	transmit data input
GND[2]	2	G	ground
VCC	3	P	supply voltage for CAN transmitter
RXD	4	O	receive data output
VIO	5	P	supply voltage for I/O level adapter
SDO	6	O	SPI data output
INH	7	AO	inhibit output for switching external voltage supplies or indicating wake-up from Sleep mode (active-HIGH)
LIMPFSO_N	8	AIO	limp home fail-safe output (active-LOW)
RST_N	9	I/O	reset input/output (active-LOW)
SCK	10	I	SPI clock input
WAKE	11	AI	local wake-up input
VBAT	12	P	battery supply voltage
SDI	13	I	SPI data input
CANL	14	AIO	LOW-level CAN bus line
CANH	15	AIO	HIGH-level CAN bus line
SCSN	16	I	SPI chip select input (active-LOW)

Table 4. Pin description...*continued*

Symbol	Pin	Type[1]	Description
GPIO1	17	I/O	general purpose input/output 1
GPIO2	18	I/O	general purpose input/output 2

[1] I: digital input; O: digital output; I/O: digital input/output; AI: analog input; AO: analog output; AIO: analog input/output; P: power supply; G: ground.
[2] DHVQFN18 package die supply ground is connected to both the GND pin and the exposed center pad. The GND pin must be soldered to board ground. For enhanced thermal and electrical performance, it is also recommended to solder the exposed center pad to board ground.

7 Functional description

7.1 Supply

Table 5. Supply description

Supply pin	Supply	Description
VBAT	V_{BAT}	Main supply for the device, needed for all internal processes; supplies the CAN receivers
VCC	V_{CC}	Supply for the CAN transmitter and for bus biasing
VIO	V_{IO}	Supply and reference level for the digital interface pins TXD and RXD, the SPI interface, RST_N, LIMPFSO_N and the GPIO pins

7.2 System operating modes

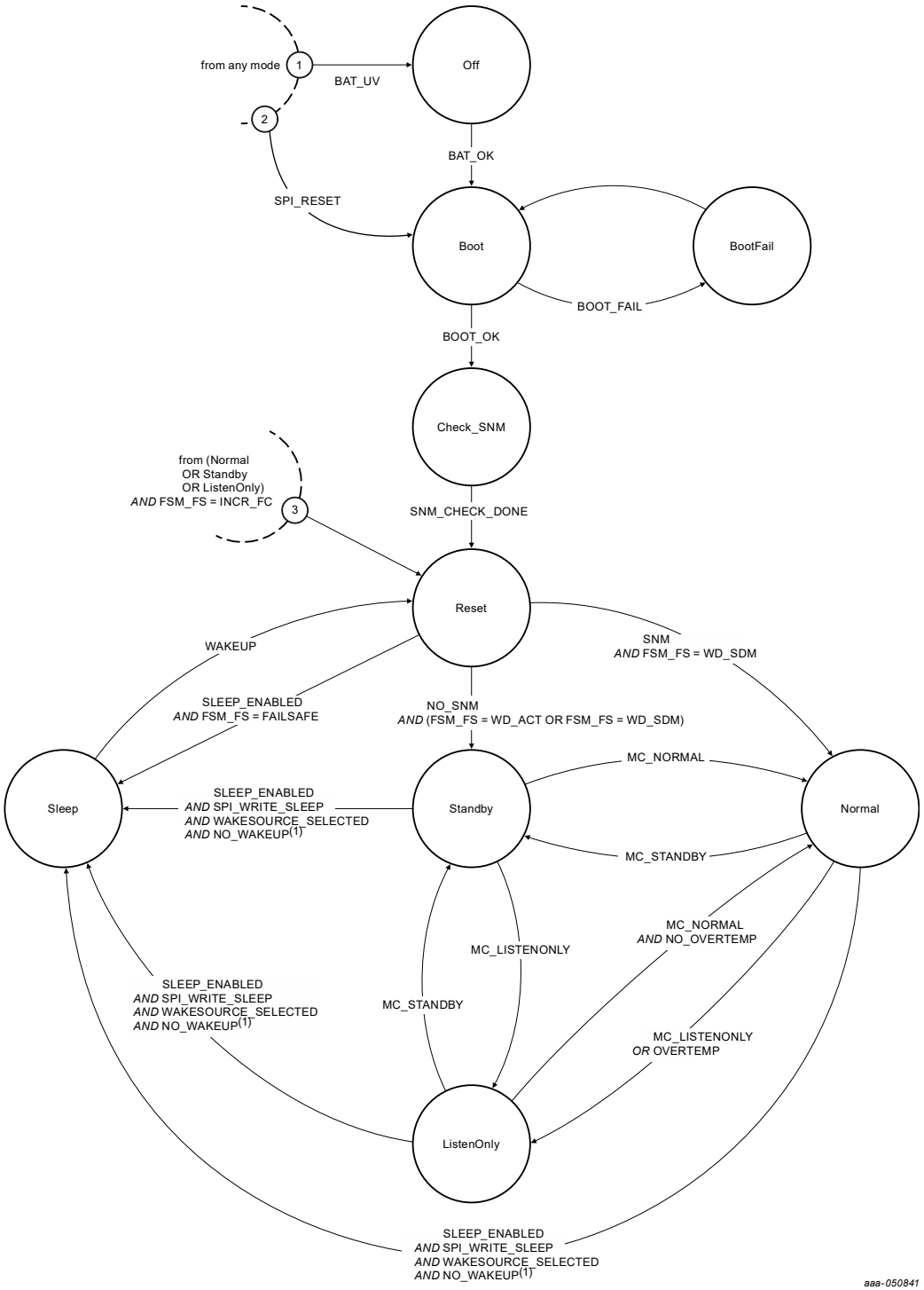
Table 6 contains a summary of the system finite state machine (FSM_MAIN) operating modes. A mode transition diagram is shown in Figure 3. Mode changes are completed after transition time $t_{t(moch)}$. Abbreviations used in the mode transition diagram are defined in Table 7.

Table 6. FSM_MAIN operating modes

Operating mode	Description
Off	Device is deactivated
Boot	Device loads the configuration
BootFail	Device switches to BootFail mode when booting was unsuccessful
Check_SNM	Device checks the CAN bus status
Reset	Device resets the host via the RST_N pin
Standby	Device is in the first-level low-power mode with INH active
Sleep	Device is in the second-level low-power mode with INH inactive
ListenOnly	Device is able to receive CAN data from the bus
Normal	Device is able to transmit and receive CAN bus traffic

Table 7. State diagram legend

Category	Abbreviation	Definition
VBAT pin status	BAT_UV	$V_{BAT} < V_{uvd(VBAT)}$ for $t > t_{det(uv)VBAT}$
	BAT_OK	$V_{BAT} > V_{uvd(VBAT)}$ for $t > t_{rec(uv)VBAT}$
Memory check during boot phase	BOOT_OK	passed internal memory consistency check (takes up to $t_{startup}$)
	BOOT_FAIL	failed internal memory consistency check
Start-to-Normal mode check	SNM	CAN bus must remain dominant for $t > t_{t(snm)}$ in Check_SNM mode
	SNM_CHECK_DONE	$t > t_{t(snm)}$ or CAN bus recessive
	NO_SNM	CAN bus detected recessive in CHECK_SNM mode or valid SPI message detected since Boot mode
Wake-up request status	WAKEUP	valid local or remote wake-up trigger received
	NO_WAKEUP	no valid local or remote wake-up trigger received
Wake-up source selection	WAKESOURCE_SELECTED	local (WAKE) and/or remote wake-up source selected
Temperature status	NO_OVERTEMP	$T_j < T_{j(sd)rel}$
	OVERTEMP	$T_j > T_{j(sd)}$
Sleep mode control	SLEEP_ENABLED	SLEEPDIS = 0
Mode select	MC_NORMAL	Normal mode (MC = 1111)
	MC_STANDBY	Standby mode (MC = 0110)
	SPI_WRITE_SLEEP (see Section 7.12.1)	Sleep mode command (SPI write MC = 0001)
	MC_LISTENONLY	ListenOnly mode (MC = 1000)
SPI system reset	SPI_RESET	SPI forces system reset (see Section 7.12.2)



(1) Conditions need to be met before MC = 0001 is issued, else the device will not switch to Sleep mode.

Figure 3. System state diagram (FSM_MAIN)

Transitions that take priority over all others are indicated with priority 1-3 (encircled number at state exit). All other transitions are mutually exclusive.

The device can enter Normal mode directly (SNM) via a boot sequence after power on or a system reset. To pass the SNM check, the CAN bus must be in dominant state before the main state machine enters

Check_SNM mode and must remain dominant for at least t > $t_{t(snm)}$. When Normal mode was entered directly after booting, bit SNMS in the system status register is set to 1.

7.2.1 Pin and functional block states per operating mode

Table 8. Pin state per System operating mode

All supplies within operating range.

Pin	Off	Boot/ Check_SNM	BootFail	Reset	Sleep	Standby	Listen Only	Normal
TXD	high-Z	high-Z	high-Z	pulled HIGH[1]	pulled HIGH[1]	pulled HIGH[1]	pulled HIGH[1]	pulled HIGH[1]
RXD	high-Z	high-Z	high-Z	HIGH or LOW when interrupt pending[2]	HIGH or LOW when interrupt pending[2].	HIGH or LOW when interrupt pending[2]	CAN bus status	CAN bus status
SDO	high-Z	high-Z	high-Z	high-Z	high-Z	high-Z when SCSN HIGH	high-Z when SCSN HIGH	high-Z when SCSN HIGH
INH	high-Z	high-Z	high-Z	HIGH[3]	high-Z	HIGH[3]	HIGH[3]	HIGH[3]
LIMPFSO_N	high-Z	LIMPSOC	LOW	LIMPSOC	LIMPSOC	LIMPSOC	LIMPSOC	LIMPSOC
RST_N	LOW	LOW	LOW	LOW	LOW	pulled HIGH[1]	pulled HIGH[1]	pulled HIGH[1]
SCK	high-Z	high-Z	high-Z	repeater	repeater	repeater	repeater	repeater
SDI	high-Z	high-Z	high-Z	repeater	repeater	repeater	repeater	repeater
SCSN	high-Z	high-Z	high-Z	pulled HIGH[1]	pulled HIGH[1]	pulled HIGH[1]	pulled HIGH[1]	pulled HIGH[1]
GPIO1	high-Z	high-Z	high-Z	GPIO	GPIO	GPIO	GPIO	GPIO
GPIO2	high-Z	high-Z	high-Z	GPIO	GPIO	GPIO	GPIO	GPIO

[1] HIGH = driven to V_{IO} level, as defined in Table 57.
[2] Interrupt pending: at least one bit set in one or more interrupt status registers (see Section 7.12.12).
[3] HIGH = driven to V_{BAT} level, as defined in Table 57

Table 9. Functional state per System operating mode

All supplies within operating range with no error condition present.

Function	SPI configuration	Off/Boot/Boot Fail/Check_ SNM	Reset	Sleep	Standby	ListenOnly	Normal
SPI		off	off	off	on	on	on
CAN		high-Z	GND or 2.5 V bias (autobias)	GND or 2.5 V bias (autobias)	GND or 2.5 V bias (autobias)	$V_{CC}/2$[1] bias and receiver active	$V_{CC}/2$ bias and transmitter and receiver active
Local wake-up		off	on	on	on	on	on

Table 9. Functional state per System operating mode...*continued*

All supplies within operating range with no error condition present.

Function	SPI configuration	Off/Boot/Boot Fail/Check_ SNM	Reset	Sleep	Standby	ListenOnly	Normal
CAN wake-up	PNCOK = 0	off	on	on	on	off	off
	PNCOK = 1	off	off	off	off	off	off
Partial networking	PNCOK = 0	off	off	off	off	off	off
	PNCOK = 1	off	on	on	on	on	on
Watchdog	SDM = 1	off	off	off	off	off	off
	SDM = 0 WDOFF = 1[2]	off	off	off	stopped	window	window
	SDM = 0 WDOFF = 0	off	off	off	timeout	window	window
Overtemp		off	off	off	off	off[3]	on

[1] 2.5 V when LPL = 1.
[2] WDOFF is set to 0 when an interrupt is pending on RXD in Standby mode.
[3] Overtemperature detection remains active after a transition from Normal mode to ListenOnly mode due to an overtemperature condition.

7.2.2 Local wake-up via the WAKE pin

The device monitors the WAKE pin and can be configured to respond on a rising and/or falling edge:

- A WPR interrupt is generated on a rising edge if WPRE = 1 (see Table 45)
- A WPF interrupt is generated on a falling edge if WPFE = 1 (see Table 45)

A local wake-up request is registered when the logic level on pin WAKE changes and the new level remains stable for at least t_{wake}. t_{wake} is configured via bit WFC in Table 44. The WAKE pin status can be read via bit WPS in the System status register (Table 19). The GPIO pins can also be configured as V_{IO} level wake pins (see Section 7.10).

7.3 Fail-safe operating modes

Depending on the configuration, a single or continuous violation of one or more monitored functions will trigger the device to enter FSM_FS Fail-safe mode from FSM_MAIN Reset mode. The following functions are monitored:

- V_{IO} undervoltage or overvoltage
- Incorrect serving of the watchdog
- Reset pin (RST_N) clamped HIGH during the reset process or clamped LOW at any time
- Reset process timeout (> $t_{to(rst)}$)
- Fail-safe counter overflows

Table 10. FSM_FS operating modes

Operating mode	Description
Reset_IDLE	Reset pin (RST_N) is pulled LOW; waiting for FSM_MAIN to enter Reset mode
Reset_INIT	Reset pin (RST_N) is pulled LOW when the reset process is initiated; reset timeout timer started ($t_{to(rst)}$)
Reset_TIM	Reset pin (RST_N) held low for $t_{d(rst)}$

Table 10. FSM_FS operating modes...*continued*

Operating mode	Description
Reset_REL	Reset process completed and RST_N pin released (set HIGH)
WD_SDM	The watchdog is off because the device is in Software Development mode
WD_ACT	The watchdog is active
WD_RES	The watchdog timer is reset
WD_RES_F	The watchdog timer is reset after an invalid watchdog trigger or due to a watchdog timer overflow. In this mode, the watchdog fail counter (WDFC) is incremented.
Fail-safe	LIMPFSO_N output enabled and FSCC reset to 0
INCR_FC	Increment failure counter

Table 11. State diagram legend

Category	Abbreviation	Definition
V_{IO} monitoring	VIO_OV_LONG	$V_{IO} > V_{ovd(VIO)}$ for $t > t_{det(ov)long}$
	VIO_OK	($V_{IO} < V_{ovd(VIO)}$ for $t > t_{rec(ov)}$) AND ($V_{IO} > V_{uvd(VIO)}$ for $t > t_{rec(uv)}$)
	VIO_NOK	($V_{IO} < V_{uvd(VIO)}$ for $t > t_{det(uv)}$) OR ($V_{IO} > V_{ovd(VIO)}$ for $t > t_{det(ov)}$)
Interrupt handling	INTERRUPT_PENDING	interrupt pending on RXD
	NO_INTERRUPT_PENDING	no interrupt pending on RXD
RST_N monitoring	RSTN_HIGH	$V_{RST\_N} > V_{IH(RST\_N)}$ for $t > t_{fltr(rst)}$
	RSTN_TIMEOUT	$t > t_{to(rst)}$
	RSTN_DELAY	$t > t_{d(rst)}$
	EXT_RSTN_TRIG	$V_{RST\_N} < V_{IL(RST\_N)}$ for $t > t_{fltr(rst)}$
	RSTN_CHECK_OK	RST_N HIGH within $t_{rel(rst)}$
	RSTN_CHECK_NOK	RST_N LOW after $t_{rel(rst)}$
Sleep mode control	SLEEP_DISABLED	SLEEPDIS = 1
	SLEEP_ENABLED	SLEEPDIS = 0

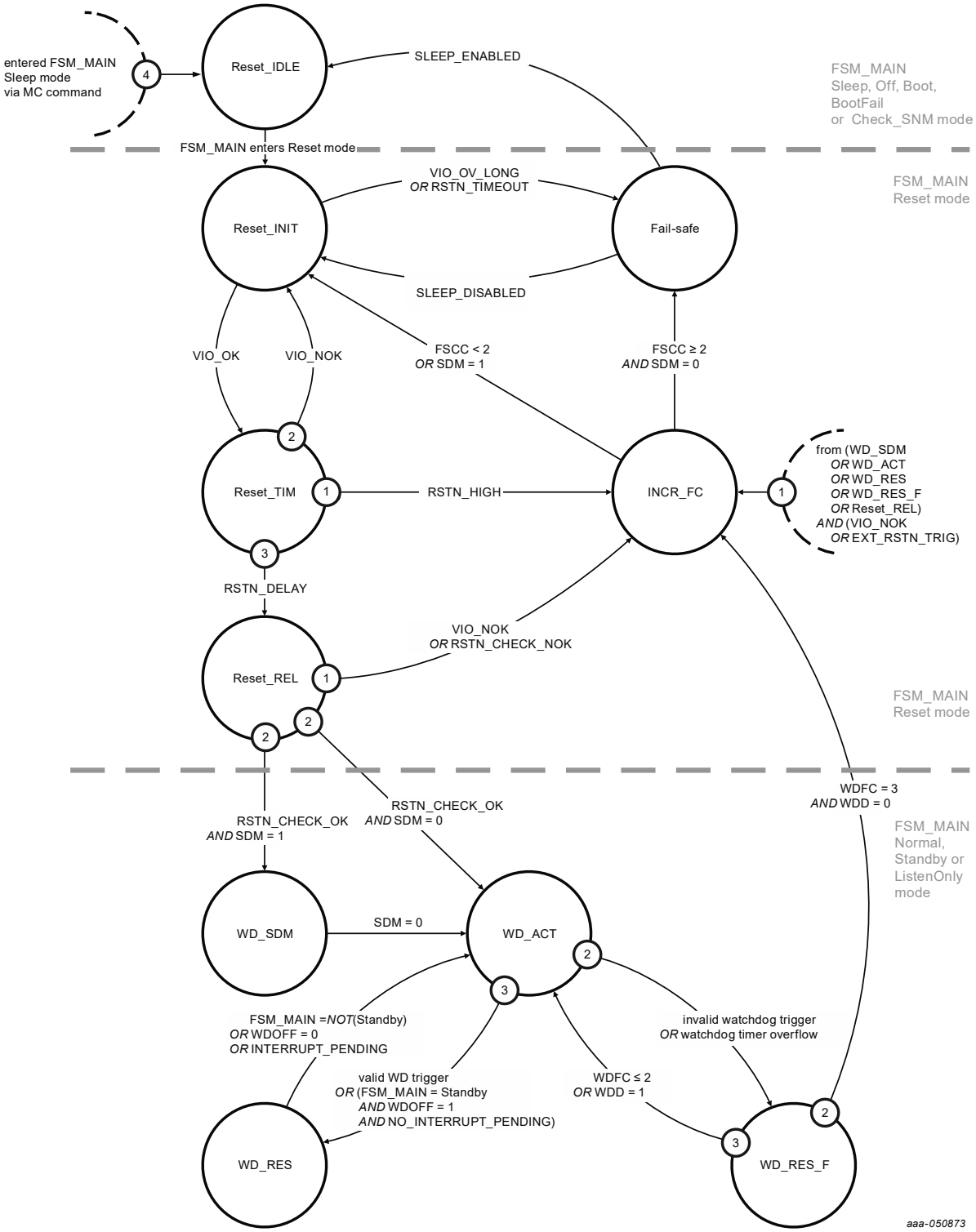


Figure 4. Fail-safe state diagram (FSM_FS)

Transitions that take priority over all others are indicated with priority 1-4 (encircled number at state exit). All other transitions are mutually exclusive.

When the device enter Normal mode directly (SNM; see Table 7) via a boot sequence after power on or a system reset (see Section 7.2), it also enters Software Development mode (SDM; see Section 7.5.1).

If a valid SPI message was detected after entering SNM and SDM, the transceiver will switch from Reset mode to Standby mode when a reset loop is triggered.

If no valid SPI message was detected after entering SNM and SDM, the transceiver will return from Reset mode to Normal mode when a reset loop is triggered.

7.4 CAN operating modes

Table 12 contains a summary of the CAN finite state machine (FSM_CAN) operating modes. A mode transition diagram is shown in Figure 5. Abbreviations used in the mode transition diagram are defined in Table 13.

Table 12. CAN operating modes

Operating mode	Description
CAN Off	The CAN transceiver is off.
CAN Offline	The CAN transceiver is in a low-power mode, able to react to a wake-up pattern (WUP) on the bus.
CAN OfflineBias	The CAN transceiver is in a low-power mode, able to react to a wake-up pattern (WUP) or wake-up frame (WUF) on the bus.
CAN ListenOnly	Only the CAN receiver is active and able to capture a wake-up frame (WUF); the RXD pin reflects the CAN bus status.
CAN Active	The CAN transceiver is active and able to capture a wake-up frame (WUF).

Table 13. State diagram legend

Category	Abbreviation	Definition
CAN bus events	BUSSILENCE	CAN bus idle for $t > t_{to(silence)}$
	WUP	valid CAN wake-up pattern detected
VCC pin status	VCC_OK	$V_{CC} > V_{uvd(VCC)}$ for $t > t_{rec(uv)}$
	VCC_UV	$V_{CC} < V_{uvd(VCC)}$ for $t > t_{det(uv)}$

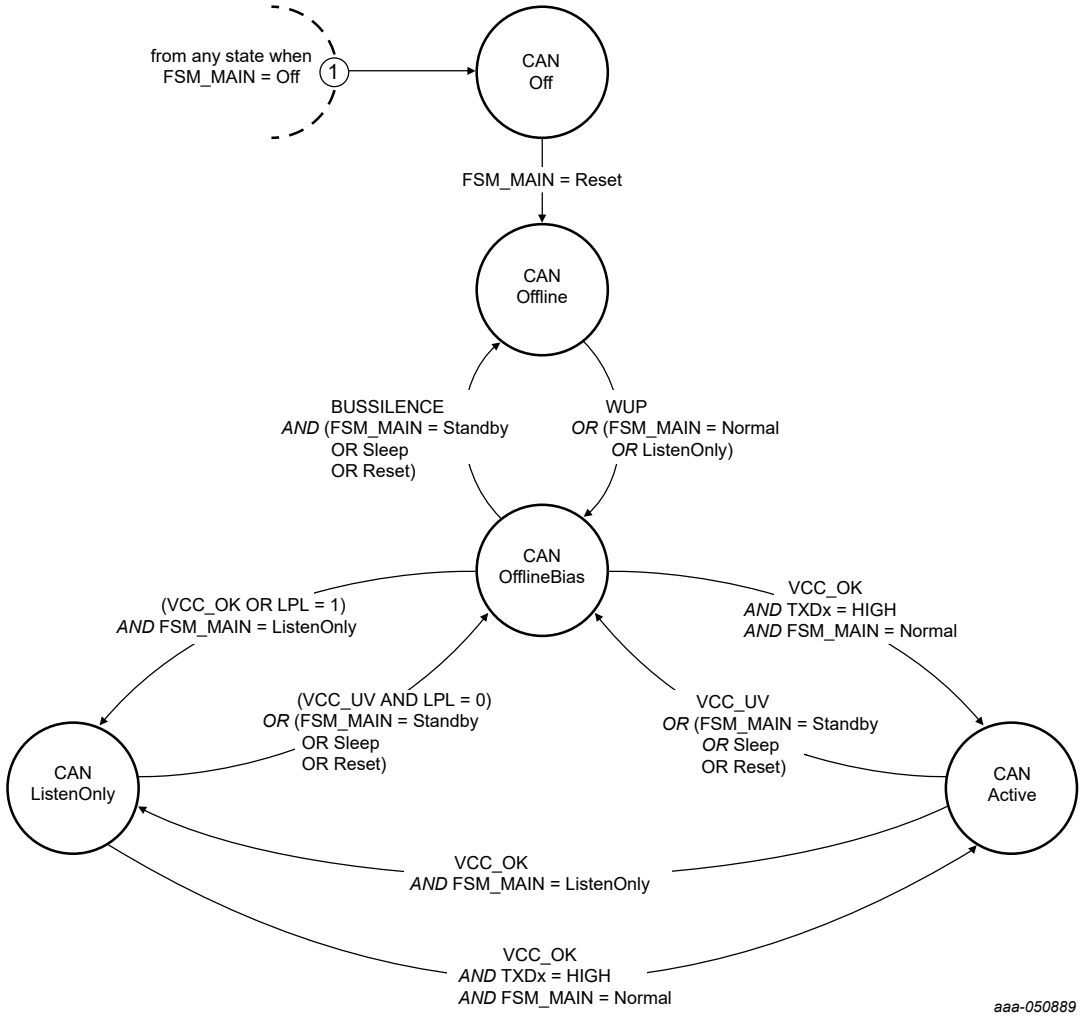


Figure 5. CAN state diagram (FSM_CAN)

State transitions are mutually exclusive. FSM_MAIN = Off condition overrides any transition triggered at the same time, indicated by '1' (priority 1) in Figure 5.

Low-power ListenOnly mode (LPL = 1; see Figure 5 and Table 21) is intended for Pretended Networking use cases and provides CAN listen-only behavior without a V_{CC} supply. In this mode, the CAN transmitter is switched off to minimize quiescent current and CAN bus biasing is derived from V_{BAT} (see Table 14). The receiver operates normally.

7.4.1 Functional block state per CAN operating mode

Table 14. Functional block state per CAN operating mode

Block	SPI configuration	CAN Off	CAN Offline	CAN Offline Bias	CAN Listen Only	CAN Active
CAN transmitter	LPL = 0	off	off	off	recessive	active [1]
	LPL = 1	off	off	off	off	active [1]
CAN receiver		off	off	off	active	active

Table 14. Functional block state per CAN operating mode*...continued*

Block	SPI configuration	CAN Off	CAN Offline	CAN Offline Bias	CAN Listen Only	CAN Active
CAN bias	VBATVCC = 1	high-Z	GND	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
	LPL = 0 and VBATVCC = 0	high-Z	GND	2.5 V derived from V_{BAT}	$V_{CC}/2$	$V_{CC}/2$
	LPL = 1 and VBATVCC = 0	high-Z	GND	2.5 V derived from V_{BAT}	2.5 V derived from V_{BAT}	$V_{CC}/2$

[1] If GPIOx is configured as TXEN_N and HIGH, status will be recessive.

7.4.2 CAN wake-up

The TJA1466 supports remote wake-up via a CAN wake-up pattern (WUP) or selective wake-up via a CAN wake-up frame (WUF).

7.4.2.1 CAN wake-up pattern (WUP)

The CAN wake-up pattern (WUP) is used for two purposes:

- To activate CAN biasing in CAN Offline mode (transition from CAN offline to CAN OfflineBias)
- To trigger a CAN wake-up event

The following conditions must be met to trigger a wake-up event via a CAN WUP:

- The CAN transceiver is in CAN Offline or CAN OfflineBias mode
- CAN wake-up enabled (CWE = 1)
- CAN wake-up frame detection (WUF) deactivated (CPNC = 0 or PNCOK = 0)

The TJA1466 supports both the standard (ISO 11898-2:2024, section 5.5.4) and the extended (ISO 11898-2:2024, section A.4.1) wake-up patterns (see Figure 6 and Figure 7). The WUP is selected via bit CWC in the CAN configuration register (Table 21).

The wake-up pattern consists of:

ISO 11898-2:2024, section 5.5.4, standard WUP

- a dominant phase of at least $t_{wake(busdom)}$ followed by
- a recessive phase of at least $t_{wake(busrec)}$ followed by
- a dominant phase of at least $t_{wake(busdom)}$

ISO 11898-2:2024, section A.4.1, WUP extension

- standard WUP followed by a recessive phase of at least $t_{wake(busrec)}$

Dominant or recessive bits between the phases shorter than $t_{wake(busdom)}$ or $t_{wake(busrec)}$, respectively, are ignored.

The complete wake-up pattern must be received within $t_{to(wake)bus}$ to be recognized as a valid wake-up pattern (see Figure 6 and Figure 7). Otherwise, the internal wake-up logic is reset. The complete wake-up pattern then needs to be retransmitted to trigger a wake-up event.

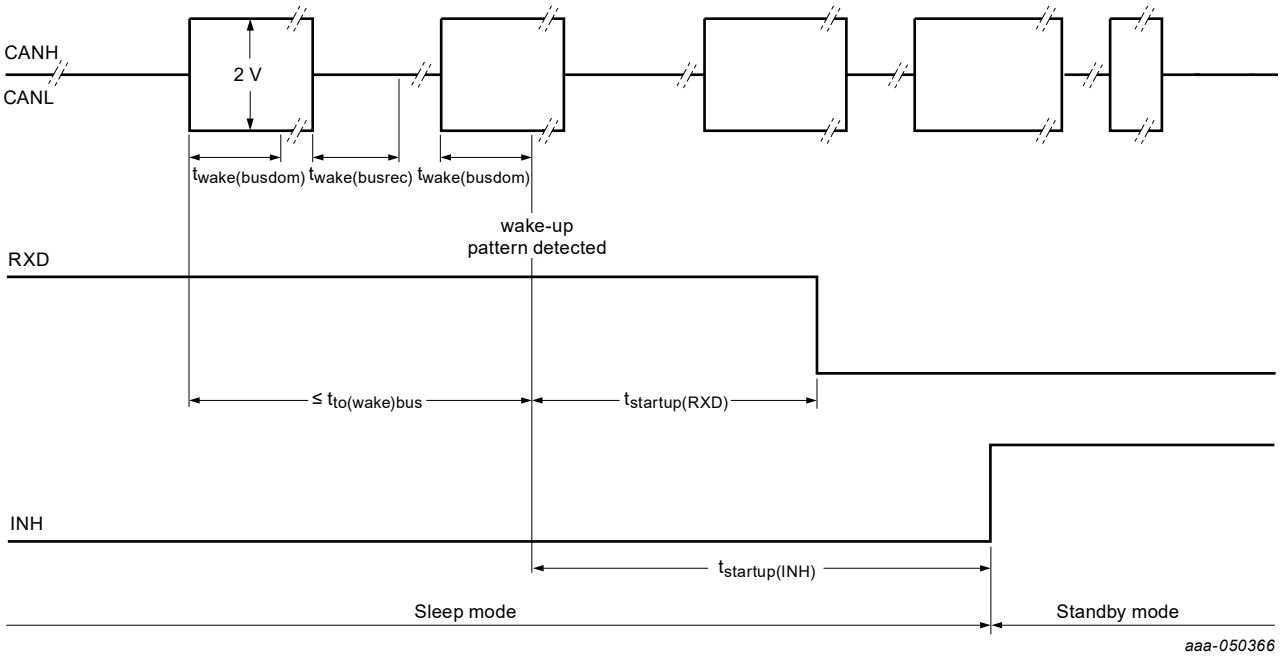


Figure 6. Standard wake-up pattern in Sleep mode with CWE = 1, PNCOK = 0 and CWC = 0

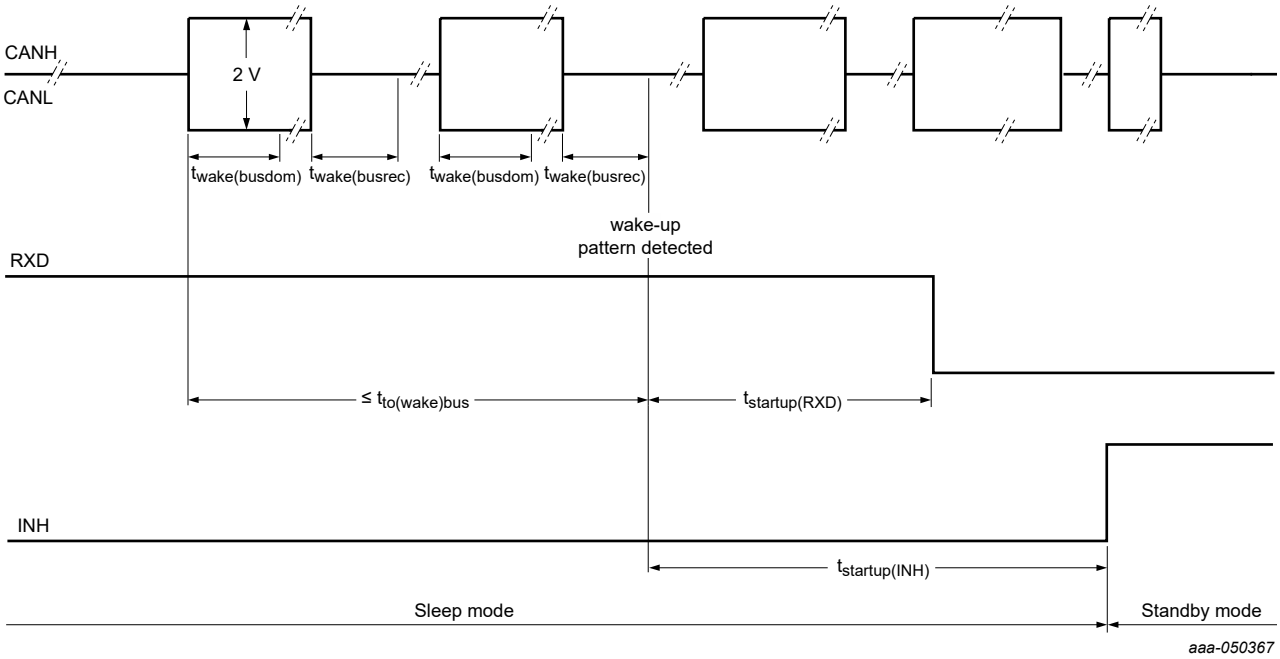


Figure 7. Extended wake-up pattern in Sleep mode with CWE = 1, PNCOK = 0 and CWC = 1

7.4.2.2 CAN wake-up frame (WUF)

CAN partial networking through selective wake-up detection allows a device in a CAN network to be selectively woken up in response to a wake-up frame (WUF) on the CAN bus.

Selective wake-up detection uses one of two filtering methods:

- Identifier-only filtering (PNDM = 0)
- Identifier + data length code + data mask filtering (PNDM = 1)

The following conditions must be met to enable CAN WUF functionality:

- CAN biasing needs to be activated (CAN OfflineBias, CAN ListenOnly or CAN Active mode)
- CAN wake-up enabled (CWE = 1)
- CAN partial networking configuration completed (PNCOK = 1)
- CAN partial networking enabled (CPNC = 1)
- No CAN partial networking error detected (CPNERRS = 0)

The PN configuration is defined in the following registers:

- ID registers (Table 34)
- ID mask registers (Table 35)
- Data mask registers (Table 36)
- Frame control register (Table 37)
- Data rate and filter configuration register (Table 38)

Bit PNCOK in the partial networking and CAN configuration register (Table 39) must be set (to 1) to activate the contents of the PN registers. PNCOK is cleared automatically when the contents of any PN register is changed and needs to be set again to load and activate the new configuration.

The arbitration bit rate is selected via bits CDR (see Table 38). CAN bit rates of 50 kbit/s, 100 kbit/s, 125 kbit/s, 250 kbit/s, 500 kbit/s, 667 kbit/s and 1000 kbit/s are supported during selective wake-up.

7.4.2.2.1 Identifier matching

The wake-up frame format, standard (11-bit) or extended (29-bit) identifier, is selected via bit IDE in the frame control register (Table 37).

- IDE = 0: standard CBFF (classical base frame format, 11-bit)
- IDE = 1: extended CEFF (classical extended frame format, 29-bit)

A valid WUF identifier is defined and stored in the ID registers (Table 34). An ID mask can be defined to exclude selected bits from being evaluated during WUF detection. The ID mask is defined in the mask registers (Table 35), where a 1 means ‘don’t care’.

When PNDM = 0, a valid wake-up frame is detected and a wake-up event is captured (CAN wake-up interrupt generated; see Table 48) when:

- the identifier field in the received wake-up frame matches the pattern in the PN ID registers (excluding the masked bits)
- the frame is a valid CBFF or CEFF frame according to the ISO 11898-1:2024 (including CRC and CRC delimiter)

7.4.2.2.2 Data field matching

In addition to the identifier field, the data field in the CAN frame is also evaluated during WUF detection when PNDM = 1.

The data field indicates the nodes to be woken up. Within the data field, groups of nodes can be pre-defined and associated with bits in a data mask. By comparing the incoming data field with the data mask, multiple groups of nodes can be woken up simultaneously with a single wake-up message.

The data length code (bits DLC in the frame control register; Table 37) determines the number of data bytes expected (between 0 and 8) in the data field of a CAN wake-up frame. If one or more data bytes are expected (DLC ≠ 0000), at least one bit in the data field of the received wake-up frame must be set to 1 and at least one equivalent bit in the associated data mask register in the transceiver (see Table 36) must also be set to 1 for a successful wake-up. Each matching pair of 1s indicates a group of nodes to be activated (since the data field is up to 8 bytes long, up to 64 groups of nodes can be defined).

The relationship between the data mask registers and the data bytes in the CAN message is illustrated in Figure 8. DM7 represents the mask for the last transmitted byte, DM6 for the last-but-one byte and so on.

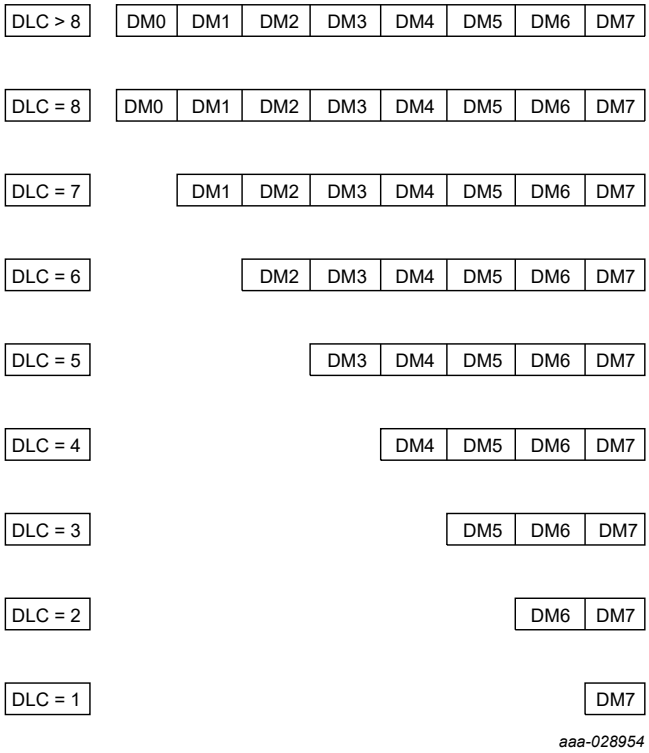


Figure 8. Data mask register usage for different values of DLC

If DLC = 0000, a node will wake up if the WUF contains a valid identifier and the received data length code is 0000, regardless of the values stored in the data mask (the data field is not evaluated when DLC = 0000). If DLC ≠ 0000 and all data mask bits are set to 0, the device cannot be woken up via the CAN bus (note that all data mask bits are set to 1 by default; see Table 36). If a WUF contains a valid ID but the DLCs (in the Frame control register and in the WUF) don't match, the data field is ignored and no nodes are woken up.

Remote frames do not contain data, but request data and can have a DLC ≠ 0000; so remote frames are not supported when PNDM = 1. If remote frames need to trigger a wake-up, identifier-only filtering should be selected (PNDM = 0).

When PNDM = 1, a WUF is detected when all the following conditions are met:

- The identifier field in the received wake-up frame matches the pattern and format in the ID registers (Table 34), excluding masked bits.
- The received CAN frame is not a Remote frame.
- The received data length code matches the DLC setting in the frame control register (Table 37).
- DLC:
  - DLC = 0000 or
  - DLC ≠ 0000 and at least one bit in the data field of the received frame is set with the corresponding bit in the associated data mask register (Table 36) also set.
- The frame is a valid CBFF or CEFF frame according to the ISO 11898-1:2024 (including CRC and CRC delimiter).

7.4.2.2.3 WUF error processing

If the TJA1466 receives a CAN message containing a protocol error (e.g. a 'stuffing error') transmitted in advance of the ACK field, an internal error counter is incremented. If a classical CAN message (CBFF or CEFF) is received without any errors appearing in front of the ACK field, the counter is decremented. Data received after the CRC delimiter and before the next SOF is ignored by the CAN wake-up frame detector module. If the counter overflows (counter > 31), a frame detect error is captured (PNFDER = 1) and the device wakes up.

The error counter value can be read via bits PN_ERR_ERROR_COUNT (Table 33). The counter is reset to zero when no activity is detected on the CAN bus for $t_{to(silence)}$ or selective wake-up detection is disabled (CPNC = 0 OR PNCOK = 0). The status, whether the last frame was decoded successfully, can be determined via bit LFDS in the partial networking status register (Table 32).

If selective wake-up is disabled (CPNC = 0) or partial networking is not configured (PNCOK = 0), wake-up will be performed as described in Section 7.4.2.1.

7.4.2.2.4 CAN FD passive and CAN XL passive

CAN frames in the ISO 11898-1:2024 compliant FD base frame format (FBFF) or FD extended frame format (FEFF), or the upcoming CAN XL frame format (XLFF), are not supported for selective wake-up. The device can be configured to tolerate these frames or treat them as invalid frames via bit PNECC in the partial networking control register (Table 39).

With PNECC = 0, the error counter is incremented when an FBFF, FEFF or XLFF frame is received. With PNECC = 1, the error counter is not affected because FBFF, FEFF and XLFF frames are ignored.

CAN FD tolerance as described in the ISO 11898-2 standard is supported for bitfilter 1 and bitfilter 2. The TJA1466 also supports additional bit filter settings for higher arbitration rates up to 1 Mbit/s and data bit rates up to 8 Mbit/s (see bits CDR and IDFS in Table 38 and $t_{fltr(bit)dom}$ in Table 58).

For CAN XL FAST mode (ISO 11898-2:2024) tolerance, CAN XL level-scheme detection must be enabled to prevent the new CAN XL voltage scheme being misinterpreted as bus idle. CAN XL FAST mode tolerance is enabled by setting CXLDE to 1.

7.5 Watchdog

A Q&A watchdog is provided to supervise the host controller.

The watchdog operates in Window or Timeout mode, or can be turned off/disabled:

- The watchdog will be in Timeout mode while the device is in Standby mode. In Timeout mode, the watchdog can be (re-)triggered at any time within a defined watchdog period (t_{wd}) by a correct answer to the watchdog question. The watchdog period is set via bits WDP in the Watchdog configuration register (Table 27).

- The watchdog will be in Window mode while the device is in Normal or ListenOnly mode. In Window mode, the watchdog can be (re-)triggered at any time during the second half of the watchdog period by a correct answer to the watchdog question.
- In Standby mode, the watchdog can be disabled by setting WDOFF = 1 if no interrupts are pending. Any new interrupt or write attempt to WDA will re-activate the watchdog and clear the WDOFF bit.

A valid watchdog trigger needs a watchdog question to be answered via the SPI meeting the following conditions:

- The answer (WDA) is the bitwise inverse of the question (WDQ)
- The SPI transfer is valid (no SPIF)
- The answer is scheduled in the correct time frame as dictated by the watchdog

The watchdog question can be read via bits WDQ and the reply needs to be written to WDA (see Table 29 and Table 30).

An invalid watchdog trigger is detected when:

- an incorrect answer is written to bits WDA
- the watchdog is not triggered within the defined time window (watchdog timer overflow)
- the watchdog is triggered in the first half of the watchdog period while the watchdog is running in window mode

Both valid and invalid watchdog triggers reset the watchdog timer and generate a new watchdog question.

The watchdog fail counter (WDFC) in the watchdog trigger count register (Table 31) is initialized to 2 when the device leaves Reset mode. When an invalid watchdog trigger is detected, WDFC is incremented (unless it is already 3). If WDFC = 3 after the counter has been incremented, and watchdog debugging has not been enabled (by setting WDD = 1; see Section 7.5.1), the device enters FSM_FS INCR_FC mode (see Section 7.11.9).

7.5.1 Software Development mode

Software Development mode (SDM) is provided for test purposes and is typically used during the software development phase. It can only be entered via the SNM boot sequence (see Section 7.2). The watchdog is inactive in Software Development mode. The SDM status, active or inactive, can be read via bit SDM in the system status register (Table 19).

In Software Development mode, reset generation via the watchdog can be disabled via bit WDD in the Watchdog configuration register (Table 27). When SDM = 0 (watchdog active), bit WDD can be cleared (watchdog debug disable) but not set (remains 0). When data is written to the WDA register, bit SDM is cleared and normal operation resumes. When WDD = 1, an incorrect serving of the watchdog does not trigger the reset process.

7.6 Interrupt processing

A number of events can be captured and reported to the host via the interrupt mechanism. Pin RXD is used to signal an interrupt event in Standby or Sleep mode. Two options are supported:

- RXDINTC = 0: RXD goes LOW when a wake-up or power-on interrupt is pending
- RXDINTC = 1: RXD goes LOW when any interrupt is pending

Interrupts are enabled individually via dedicated bits in the interrupt enable registers (see Section 7.12.12). When an interrupt is generated, pin RXD goes LOW to alert the host. The host can then determine which event triggered the interrupt by polling the interrupt status registers. PO and PNFDER interrupts are always enabled; so they do not have associated interrupt enable bits.

Interrupts are cleared by writing 1 (W1C) to the relevant interrupt status bits. Clearing an interrupt does not necessarily mean the event that triggered the interrupt has been resolved. If there is a collision, setting the interrupt takes precedence over clearing the interrupt.

7.7 Device ID

A byte is reserved in the register map for the unique device identification code; see bit IDS in Table 54.

7.8 Lock control

Sections of the register address area can be write-protected to prevent unintended modifications. Note that this facility only protects locked bits from being modified via the SPI and will not prevent the TJA1466 updating registers. Sections that can be locked are detailed in Section 7.12.13.

7.9 General-purpose memory

The TJA1466 allocates 4 bytes of memory to store user information. The general-purpose registers can be accessed via the SPI at address 0xFF0 to 0xFF3 (see Section 7.12.14). The general-purpose registers are only cleared when the battery is first connected.

7.10 GPIO pins

The TJA1466 contains two general-purpose I/O pins (GPIO) that can be assigned to a number of functions (see Table 15, Table 25 and Table 26).

Table 15. Configurable GPIO functions

GPIO function	Description
Digital input	pin status can be read via GPIOxS
Digital output	output polarity defined via GPPx
TXEN_N input	CAN transmitter disabled when GPIO pin driven HIGH
INT_N interrupt output	active state signals an interrupt is pending
Additional RXD output (RXD2)	GPIO1 only, two options: • CAN bus forwarded to both RXD and RXD2 (via GPIO1) outputs • CAN bus forwarded to RXD2 only; RXD forced HIGH in Listen Only and Normal modes; pin RXD behavior in all other modes as in Table 8
Additional TXD input (TXD2)	GPIO2 only, two options: • TXD and TXD2 (via GPIO2) data fed to the CAN bus - the CAN bus will be recessive only when both TXD and TXD2 are HIGH • only TXD2 enabled (TXD input ignored) - the CAN bus is driven dominant when TXD2 is LOW
V_{CC} undervoltage status output	active state indicates V_{CC} undervoltage detected (UVCCS)
TXD dominant status output	active state indicates TXD clamped dominant (TXDDOMS)
TXD2 dominant status output	active state indicates TXD2 clamped dominant (TXD2DOMS) - GPIO1 only
CAN WUP detect status output	active state indicates WUP detected
CAN WUF detect status output	active state indicates WUF detected
CAN bus biasing status output	active state indicates bus biasing is active
WAKE pin rising edge detect output	active state indicates rising edge detected on WAKE pin

Table 15. Configurable GPIO functions *...continued*

GPIO function	Description
WAKE pin falling edge detect output	active state indicates falling edge detected on WAKE pin
CAN in Active mode and ready to transmit status output (CTS)	active state if CAN in Active mode
CAN in ListenOnly mode status output	active state if CAN in ListenOnly mode
Local low-voltage wake-up input	wake-up on rising, falling or both edges on GPIO pin
INH2: low-voltage inhibit output	active state if INH2 activated

The status of the GPIO pins, HIGH or LOW, can be read (after $t_{fltr(GPIO)}$) via bits GPIOxS in the GPIO status register (Table 24), independently of the selected function.

When an input function is selected, the pin behavior can be configured as:

- floating
- pull-up
- pull-down
- repeater

When an output function is selected, the pin output driver can be configured as:

- push-pull
- open-drain high-side driver
- high-side driver plus weak pull-down
- open-drain low-side driver
- low-side driver plus weak pull-up

For selected output functions, the GPIO pins can be configured as active-HIGH or active-LOW (see Table 23). The minimum pulse width when GPIO is configured as output is greater than $t_{w(min)}$.

7.11 Failure handling

The TJA1466 incorporates a number of safety features used for error detection and processing.

7.11.1 TXD dominant timeout

A LOW level on pin TXD (or on GPIO2 in TJA1466B when configured as a second TXD input, see Section 7.10) persisting longer than $t_{to(dom)TXD}$ releases the bus lines to recessive state. This feature prevents the CAN bus being blocked by continuous dominant clamping. A CAN failure interrupt is generated (TXDDOM/TXD2DOM = 1), if enabled (TXDDOME/TXD2DOME = 1), when a TXD dominant timeout is detected. The TXD dominant status can be read via bit TXDDOMS/TXD2DOMS in the CAN status register (Table 22).

7.11.2 CAN transmitter enable/disable (TXEN_N)

Pins GPIO1 and GPIO2 can be configured as enable/disable signals (TXEN_N) for the CAN transmitter (see Section 7.10). A HIGH level on a GPIO pin configured as a TXEN_N input signal disables the transmitter, releasing the bus lines to recessive state independent of the level on pin TXD and/or TXD2 (if configured on GPIO2). The TXEN_N status can be read via bit GP1S or GP2S in the GPIO status register (Table 24).

7.11.3 Bus dominant timeout

A dominant state on the CAN bus lasting longer than $t_{to(dom)bus}$ generates a CAN bus failure interrupt (BUSDOM = 1), if enabled (BUSDOME = 1; Table 46). The status of the bus can be read via bit BUSDOMS in the CAN status register (Table 22). Note that this feature is only available in Normal mode and in Listen Only modes when LPL = 0.

7.11.4 V_{CC} undervoltage

The TJA1466 monitors the supply voltage on pin VCC. When V_{CC} drops below the undervoltage detection threshold $V_{uvd(VCC)}$ for longer than $t_{det(uv)}$, a V_{CC} undervoltage interrupt is generated (UVCC = 1), if enabled (UVCCE = 1; Table 45). The V_{CC} undervoltage status can be read via bit UVCCS in the system status register (Table 19).

7.11.5 V_{IO} undervoltage and overvoltage

The TJA1466 monitors the supply voltage on pin VIO. If an undervoltage or overvoltage is detected, a reset process is initiated (see Section 7.3) and pin RST_N is forced LOW. The reset process continues until the device recovers from the undervoltage or overvoltage. The V_{IO} undervoltage and overvoltage thresholds are defined in Table 11.

7.11.6 V_{BAT} undervoltage

The TJA1466 monitors the supply voltage on pin VBAT. It switches directly to Off mode when V_{BAT} drops below the undervoltage detection threshold, $V_{uvd(VBAT)}$ for $t_{det(uv)}$. As a consequence, bit PO is set (see Table 48).

7.11.7 Overtemperature

The TJA1466 only monitors the junction temperature when MC = Normal. When the junction temperature exceeds $T_{j(sd)}$, the device switches from Normal mode to ListenOnly mode (see Section 7.2). An overtemperature interrupt is generated (OT = 1), if enabled (OTE = 1; see Table 48). The device recovers and switches back to Normal mode when the junction temperature falls below the shutdown release threshold, $T_{j(sd)rel}$. The overtemperature status can be read via bit OTS in the system status register (Table 19) when the device is in Normal or ListenOnly mode.

7.11.8 RST_N monitoring

Pin RST_N is a bidirectional open-drain low-side driver with integrated pull-up resistance. The TJA1466 monitors pin RST_N for an externally triggered reset. A reset process is initiated when RST_N is held LOW for $t_{fltr(rst)}$.

7.11.9 Fail-safe handling

The TJA1466 contains a fail-safe counter that is incremented (up to 3) each time the device enters FSM_FS INCR_FC mode (see Figure 4). The value of the fail-safe counter can be read and modified via bits FSCC (Table 40). If the device exits INCR_FC mode while FSCC ≥ 2, pin LIMPFSO_N is forced LOW (after $t_{d(fdet-LF\_NL)}$), the device switches to FSM_FS Fail-safe mode and enters FSM_MAIN Sleep mode (by default: SLEEPDIS = 0). The device will not enter FSM_MAIN Sleep mode if SLEEPDIS = 1. CAN and WAKE pin interrupts are enabled automatically (bits CWE, WPRE and WPFE set; see Table 45) when the device enters Fail-safe mode.

7.11.10 Fail-safe output

The LIMPFSO_N pin can be configured as a fail-safe output or for limp home functionality (see NXP application notes AN14452).

It can be used to signal a failure condition to the application via a LOW or floating level, depending on how the pin is configured. The status of the pin can be read via bits LIMPFSOS.

LIMPFSO_N is configured via bits LIMPFSOC in the Fail-safe output control register (Table 40). However:

- LIMPFSOC is always set to 01 (LOW) when the device enters Fail-safe mode
- if LIMPFSOC = 10 or 11 when the device enters INCR_FC mode, it is automatically set to 00 (high-Z)
- if LIMPFSOC = 00 or 01 when the device enters INCR_FC mode, it remains unchanged
- SPI system reset: no change to LIMPFSOC if it was 01 before SPI reset; set to 00 if it was 10 or 11.

7.12 SPI interface

The serial peripheral interface (SPI) provides the communication link with the microcontroller. The SPI is configured for full duplex data transfer, so status information is returned when new control data is shifted in. The interface also offers a read-only access option, allowing registers to be read back by the application without changing the register content.

The SPI uses four interface signals for synchronization and data transfer:

- SCSN: SPI chip select; active LOW
- SCK: SPI clock
- SDI: SPI data input
- SDO: SPI data output; floating when pin SCSN is HIGH (may need external pull-up or pull-down if not available in the host controller)

Bit sampling is performed on the falling edge of the clock and data is shifted in/out on the rising edge, as illustrated in Figure 9.

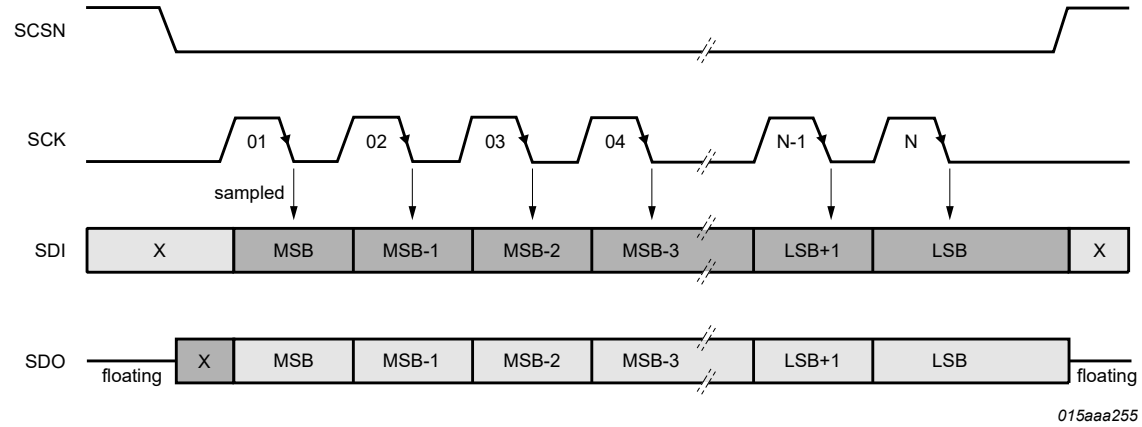


Figure 9. SPI timing protocol

The SPI data in the TJA1466 is stored in a number of dedicated 8-bit registers. Each register is assigned a unique 12-bit address. A minimum of three bytes (24 bits) must be transmitted to the TJA1466 for a single register read or write operation (see Figure 9). Six bytes (48 bits) are needed to transmit the maximum of 4 data bytes (see Figure 10).

The first byte contains the 8 most significant bits of the address; the second byte contains the 4 least significant bits of the address, a ‘read-only’ bit, a 2-bit payload size (PLS) and a parity bit. The read-only bit must be 0

to indicate a write operation and 1 to indicate a read operation. PLS indicates the number of data bytes being transmitted:

- 00 - 1 data byte
- 01 - 2 data bytes
- 10 - 3 data bytes
- 11 - 4 data bytes

The parity bit covers the address bits, read-only bit and PLS bits. It must be calculated in the user application as part of the SPI command indicating even parity, creating an even number of 1s in the first 2 bytes including the parity bit.

The third and subsequent bytes contain the data to be written. For two or more data bytes (PLS ≠ 00), the register address is incremented automatically after each data byte, see Figure 10.

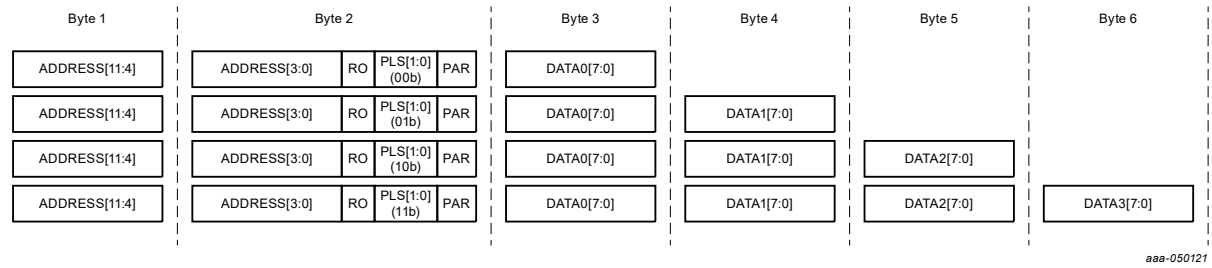


Figure 10. SPI addressing

During the SPI data, read or write operation, the first 15 bits received on pin SDI are returned via pin SDO; bit 16 returns the parity calculated for these 15 bits. During the data phase of the SPI protocol, the contents of the addressed register is returned via the SDO pin.

The devices tolerates write attempts to registers that do not exist.

7.12.1 SPI error handling

The TJA1466 can detect a number of SPI transmission failures:

- an incorrect parity bit was received
- the number of clock cycles is less than 24 or does not match the expected value based on the PLS
- an address rollover (> FFFh) was detected
- an undefined MC code was received
- a write access was attempted to a locked register
- the SPI message was not completed (SCSN HIGH) within the timeout time, $t_{to(SPI)}$

In all cases, an SPI fail interrupt is generated (provided SPIFE = 1) and the entire message is ignored.

When the necessary conditions for a Sleep mode transition (no wake-up source enabled, SLEEPDIS = 1 or pending wake-up interrupt) are not met, the device will not switch to sleep mode, even though MC = 0001.

In the case of an incorrect parity or too many clock cycles, pin SDO goes LOW until the next rising edge on SCSN. When the duration of the SPI message exceeds $t_{to(SPI)}$, the SDO pin goes high-Z.

7.12.2 SPI system reset

A system reset can be forced via the SPI, causing the device to restart via Boot mode and setting bit PO. To trigger a system reset, enable SPI write access to the System reset register by setting LKRST to 0 in the Lock control register; then write consecutively 0x01 followed 0x80 to bits SFR in the System reset register (see

Table 43). Both SPI accesses to the System reset register should be 24-bit. Any deviation from this sequence will abort the system reset.

Information that was in the general-purpose memory (Table 53) when the reset was initiated will still be available after the reset sequence has been completed.

7.12.3 SPI register map

Table 16. SPI register map overview

Register type	Address	Register name
Mode control	0x000	Mode control register
Interrupt enable (LKIE)	0x010	System interrupt enable register
	0x011	CAN interrupt enable register
	0x012	GPIO interrupt enable register
Partial networking (LKPNC)	0x020	Partial networking ID register 0
	0x021	Partial networking ID register 1
	0x022	Partial networking ID register 2
	0x023	Partial networking ID register 3
	0x024	Partial networking ID mask register 0
	0x025	Partial networking ID mask register 1
	0x026	Partial networking ID mask register 2
	0x027	Partial networking ID mask register 3
	0x028	Partial networking data mask register 0
	0x029	Partial networking data mask register 1
	0x02A	Partial networking data mask register 2
	0x02B	Partial networking data mask register 3
	0x02C	Partial networking data mask register 4
	0x02D	Partial networking data mask register 5
	0x02E	Partial networking data mask register 6
	0x02F	Partial networking data mask register 7
	0x030	Partial networking frame control register
	0x031	Partial networking data rate and filter configuration register
	0x032	Partial networking and CAN configuration register
Configuration (LKCFG)	0x040	Wake-up pulse configuration register
	0x041	CAN configuration register
	0x042	GPIO1 configuration register
	0x043	GPIO2 configuration register
	0x045	GPIO polarity configuration register
	0x046	System configuration register
	0x047	Watchdog configuration register
Lock	0x050	Lock control register
Interrupt status	0x060	System interrupt status register
	0x061	CAN interrupt status register
	0x062	Partial networking interrupt status register
	0x063	GPIO interrupt status register

Table 16. SPI register map overview*...continued*

Register type	Address	Register name
General status	0x070	Mode status register
	0x071	System status register
	0x072	CAN status register
	0x073	Partial networking status register
	0x074	GPIO status register
	0x075	Partial networking error count status register
	0x076	Fail-safe output status register
	0x077	Watchdog status register
Watchdog	0x080	Watchdog question register
	0x081	Watchdog answer register
	0x082	Watchdog trigger count register
FSO	0x090	Fail-safe counter register
	0x091	Fail-safe output control register
Reset (LKRST)	0xFE0	System reset register
General-purpose memory (LKGPM)	0xFF0	General-purpose memory register 0
	0xFF1	General-purpose memory register 1
	0xFF2	General-purpose memory register 2
	0xFF3	General-purpose memory register 3
ID	0xFFF	Device identification

7.12.4 System control and status registers

Reset values after system startup (BOOT_OK; see Figure 3) are indicated by '*'.

Table 17. Mode control register (address 000h)

Bit	Symbol	Access	Value	Description
7:4	reserved	R	-	always write 0000; ignore on read
3:0	MC	R/W	0001[1]	Sleep mode
			0110*	Standby mode
			1000	ListenOnly mode
			1111[2]	Normal mode

[1] Value after Reset-to-Sleep mode transition.
[2] Value after Reset-to-Normal mode transition

Table 18. Mode status register (address 070h)

Bit	Symbol	Access	Value	Description
7:4	reserved	R	-	ignore on read
3:0	MCS	R	0001	Sleep mode

Table 18. Mode status register (address 070h)*...continued*

Bit	Symbol	Access	Value	Description
			0110	Standby mode
			1000	ListenOnly mode
			1111	Normal mode

Table 19. System status register (address 071h)

Bit	Symbol	Access	Value	Description
7:6	reserved	R	-	ignore on read
5	OTS	R		overtemperature status available when MC = Normal and MCS = Normal/Listen Only
			0	no overtemperature or MC ≠ Normal
			1	overtemperature detected
4	SDM	R		software development mode
			0	watchdog active
			1	watchdog disabled
3	UVCCS	R		V_{CC} undervoltage status
			0	no undervoltage on VCC
			1	V_{CC} undervoltage detected
2	NMS	R		Normal mode status
			0	device entered Normal mode after power up
			1	device did not enter Normal mode power up
1	SNMS	R		Start-to-Normal mode status
			0	device did not enter Normal mode after power up
			1	device entered Normal mode directly from Reset mode
0	WPS	R		WAKE pin status
			0	WAKE pin LOW
			1	WAKE pin HIGH

Table 20. System configuration register (address 046h)

Bit	Symbol	Access	Value	Description
7:5	reserved	R	-	always write 000; ignore on read
4	SLEEPDIS	R/W		Sleep mode enable:
			0*	enable Sleep mode
			1	disable Sleep mode
3	BCCTRL	R/W		VBAT clamp control:
			0*	enable VBAT clamp
			1	disable VBAT clamp

Table 20. System configuration register (address 046h)*...continued*

Bit	Symbol	Access	Value	Description
2	RXDINTC	R/W		interrupt signaling at RXD in Sleep/Standby modes
			0*	wake-up and power-on interrupts detected
			1	all enabled interrupts detected
1	reserved	R	-	always write 0; ignore on read
0	VBATVCC	R/W		VBAT/VCC configuration
			0*	separate V_{BAT} and V_{CC} supplies; typical application; autobiasing supplied from V_{BAT}
			1	common V_{BAT} and V_{CC} supplies; applications with permanently active regulator; autobiasing is supplied from V_{CC}

7.12.5 CAN configuration and status registers

Reset values after system startup (BOOT_OK; see Figure 3) are indicated by '*'.

Table 21. CAN configuration register (address 041h)

Bit	Symbol	Access	Value	Description
7:6	reserved	R	-	always write 00; ignore on read
5	TXRXLP	R/W		TXD-to-RXD loopback:
			0*	normal TXD and RXD behavior
			1	TXD is forwarded to RXD and CAN bus remains recessive in CAN Active mode
4	TX2RX2LP[1]	R/W		TXD2-to-RXD2 loopback:
			0*	normal TXD2 and RXD2 behavior
			1	TXD2 is forwarded to RXD2 and CAN bus remains recessive in CAN Active mode
3:2	reserved	R	-	always write 00; ignore on read
1	LPL	R/W		low-power ListenOnly mode enable:
			0*	low-power ListenOnly mode disabled
			1	low-power ListenOnly mode enabled
0	CWC	R/W		CAN wake-up pattern selection:
			0*	ISO 11898-2:2024 wake pattern (dom-rec-dom)
			1	ISO 11898-2:2024 wake pattern (dom-rec-dom-rec)

[1] GPIO1 configured as second RXD output (RXD2) and GPIO2 configured as second TXD input (TXD2).

Table 22. CAN status register (address 072h)

Bit	Symbol	Access	Value	Description
7	CTS	R		CAN transceiver status:
			0	CAN transceiver not in Active mode or not ready to transmit
			1	CAN transceiver in Active mode and ready to transmit

Table 22. CAN status register (address 072h) *...continued*

Bit	Symbol	Access	Value	Description
6:4	reserved	R	-	ignore on read
3	CBSS	R		CAN bus silence status:
			0	no bus silence longer than $t_{to(silence)}$ detected
			1	bus silence detected for longer than $t_{to(silence)}$
2	BUSDOMS	R		BUS clamped dominant status:
			0	CAN bus not clamped dominant
			1	CAN bus clamped dominant
1	TXD2DOMS	R		TXD2 clamped dominant status:
			0	TXD2 not clamped dominant
			1	TXD2 clamped dominant
0	TXDDOMS	R		TXD clamped dominant status:
			0	TXD not clamped dominant
			1	TXD clamped dominant

7.12.6 GPIO configuration and status registers

Reset values after system startup (BOOT_OK; see Figure 3) are indicated by '*'.

Table 23. GPIO output polarity configuration register (address 045h)

Bit	Symbol	Access	Value	Description
7:2	reserved	R	-	always write 000000; ignore on read
1	GPP2	R/W		GPIO2 polarity:
			0*	default polarity
			1	inverted polarity
0	GPP1	R/W		GPIO1 polarity:[1]
			0*	default polarity
			1	inverted polarity

[1] n.a when when GPIO1 is configured as RXD2.

Table 24. GPIO status register (address 074h)

Bit	Symbol	Access	Value	Description
7:2	reserved	R	-	ignore on read
1	GPIO2S	R		GPIO2 pin status:
			0	GPIO2 LOW
			1	GPIO2 HIGH
0	GPIO1S	R		GPIO1 pin status:
			0	GPIO1 LOW
			1	GPIO1 HIGH

Table 25. GPIO1 configuration register (address 042h)

Bit	Symbol	Access	Value	Description
7:5	GPIO1C	R/W		GPIO1 pin configuration:
			000	input: floating output: push-pull
			001	input: pull-up output: open-drain high-side driver
			010	input: pull-down output: high-side driver plus weak pull-down
			011*	input: repeater output: open-drain low-side driver
			100	input: repeater output: low-side driver plus weak pull-up
			101 - 111	reserved
4:0	GPIO1FS	R/W		GPIO1 function select:
			0x00*	repeater function active, independent of GPIO1C
			0x01	digital input
			0x02	digital output: LOW when GPP1 = 0; HIGH when GPP1 = 1
			0x03	TXEN_N input; CAN transmitter disabled when GPIO pin driven HIGH
			0x04	INT_N interrupt output; active-LOW when GPP1 = 0 (default); active-HIGH when GPP1 = 1
			0x05	reserved
			0x06	GPIO1 configured as second RXD output (RXD2); CAN bus forwarded to both GPIO1 (RXD2) and RXD
			0x07	reserved
			0x08	GPIO1 configured as second RXD output (RXD2); CAN bus only forwarded to GPIO1 (RXD2)
			0x09	V_{CC} undervoltage status output (UVCCS)[1]
			0x0A	TXD dominant status output (TXDDOMS)[1]
			0x0B	TXD2 dominant status output (TXD2DOMS; available when GPIO2 configured as TXD2)[1]
			0x0C	wake-up pattern detect output[1]
			0x0D	wake-up frame detect output[1]
			0x0E	CAN bus biasing status output (HIGH, by default, indicates that CAN bus biasing is active)[1]
			0x0F	WAKE pin rising edge detect output[1]
			0x10	WAKE pin falling edge detect output[1]
			0x11	CAN Active mode ready-to-transmit status output (CTS)[1]
			0x12	CAN ListenOnly mode status output[1]
			0x13	digital input, rising edge qualified for wake-up interrupt if enabled via GPIO1E
			0x14	digital input, falling edge qualified for wake-up interrupt if enabled via GPIO1E

Table 25. GPIO1 configuration register (address 042h)*...continued*

Bit	Symbol	Access	Value	Description
			0x15	digital input, rising and falling edge qualified for wake-up interrupt if enabled via GPIO1E
			0x16	INH2 output[1]
			0x17 to 0x1F	reserved

[1] Active-HIGH when GPP1 = 0; active-LOW when GPP1 = 1

Table 26. GPIO2 configuration register (address 043h)

Bit	Symbol	Access	Value	Description
7:5	GPIO2C	R/W		GPIO2 pin configuration:
			000	input: floating output: push-pull
			001	input: pull-up output: open-drain high-side driver
			010	input: pull-down output: high-side driver plus weak pull-down
			011*	input: repeater output: open-drain low-side driver
			100	input: repeater output: low-side driver plus weak pull-up
			101 - 111	reserved
4:0	GPIO2FS	R/W		GPIO2 function select:
			0x00*	repeater function active, independent of GPIO2C
			0x01	digital input
			0x02	digital output: LOW when GPP2 = 0; HIGH when GPP2 = 1
			0x03	TXEN_N input; CAN transmitter disabled when GPIO pin driven HIGH
			0x04	INT_N interrupt output; active-LOW when GPP2 = 0 (default); active-HIGH when GPP2 = 1
			0x05	GPIO2 configured as second TXD input (TXD2); TXD and TXD2 (via GPIO2) data fed to the CAN bus
			0x06	reserved
			0x07	GPIO2 configured as second TXD input (TXD2); only TXD2 (via GPIO2) data fed to the CAN bus; TXD input ignored
			0x08	reserved
			0x09	V_{CC} undervoltage status output (UVCCS)[1]
			0x0A	TXD dominant status output (TXDDOMS)[1]
			0x0B	reserved
			0x0C	wake-up pattern detect output[1]

Table 26. GPIO2 configuration register (address 043h)*...continued*

Bit	Symbol	Access	Value	Description
			0x0D	wake-up frame detect output[1]
			0x0E	CAN bus biasing status (HIGH, by default, indicates that CAN bus biasing is active)[1]
			0x0F	WAKE pin rising edge detect output[1]
			0x10	WAKE pin falling edge detect output[1]
			0x11	CAN Active mode ready-to-transmit status output (CTS)[1]
			0x12	CAN ListenOnly mode status[1]
			0x13	digital input, rising edge qualified for wake-up interrupt if enabled via GPIO2E
			0x14	digital input, falling edge qualified for wake-up interrupt if enabled via GPIO2E
			0x15	digital input, rising and falling edge qualified for wake-up interrupt if enabled via GPIO2E
			0x16	INH2 output[1]
			0x17 to 0x1F	reserved

[1] Active-HIGH when GPP2 = 0; active-LOW when GPP2 = 1

7.12.7 Watchdog configuration and status registers

Reset values after system startup (BOOT_OK; see Figure 3) are indicated by '*'.

Table 27. Watchdog configuration register (address 047h)

Bit	Symbol	Access	Value	Description
7	WDD	R/W		watchdog debug:
			0*	watchdog debug disabled
			1	watchdog debug enabled[1]
6	WDOFF	R/W		watchdog on/off control:
			0*[2]	watchdog running in Standby mode
			1	watchdog in WD_RES state in Standby mode when no interrupt pending/wake-up is signaled on RXD
5:3	reserved	R	-	always write 000; ignore on read
2:0	WDP	R/W		watchdog period:
			000	10 ms
			001	20 ms
			010	50 ms
			011	100 ms
			100*[3]	200 ms
			101	500 ms
			110	1000 ms
			111	2000 ms

[1] WDD can be set to 1 only in software development mode (SDM = 1).
[2] Value after INCR_FC, a transition from Normal, ListenOnly or Standby to Sleep mode or when an interrupt is pending on RXD in Standby mode.
[3] Value after INCR_FC or a transition from Normal, ListenOnly or Standby to Sleep mode.

Table 28. Watchdog status register (address 077h)

Bit	Symbol	Access	Value	Description
7:5	WDRS	R		watchdog reset status:
			000	first battery connection
			001	watchdog counter overflow
			010	V_{IO} undervoltage
			011	V_{IO} overvoltage
			100	external reset trigger via RST_N pin
			101	reserved
			110	Fail-safe counter reached value 2
			111	MC = Sleep
4:2	WDPS	R		most recent watchdog trigger time:
			000	watchdog trigger time: < 12.5 %
			001	watchdog trigger time: ≥ 12.5 % and < 25 %
			010	watchdog trigger time: ≥ 25 % and < 37.5 %
			011	watchdog trigger time: ≥ 37.5 % and < 50 %
			100	watchdog trigger time: ≥ 50 % and < 62.5 %
			101	watchdog trigger time: ≥ 62.5 % and < 75 %
			110	watchdog trigger time: ≥ 75 % and < 87.5 %
			111	watchdog trigger time: ≥ 87.5 %
1	WDNTS	R		watchdog trigger detection:
			0	watchdog trigger detected
			1	watchdog trigger not detected
0	WDETS	R		early watchdog trigger detection:
			0	no early watchdog trigger detected
			1	early watchdog trigger detected

Table 29. Watchdog question register (address 080h)

Bit	Symbol	Access	Value	Description
7:0	WDQ	R		watchdog question

Table 30. Watchdog answer register (address 081h)

Bit	Symbol	Access	Value	Description
7:0	WDA	W		watchdog answer; always returns 0x00 on read

Table 31. Watchdog trigger count register (address 082h)

Bit	Symbol	Access	Value	Description
7:2	reserved	R	-	always write 000000; ignore on read
1:0	WDFC	R/W		watchdog fail counter value
			00	0
			01	1
			10*[1]	2
			11	3

[1] Value after INCR_FC or a transition from Normal, ListenOnly or Standby to Sleep mode.

7.12.8 Partial networking registers

Reset values after system startup (BOOT_OK; see Figure 3) and watchdog failure counter incremented (INCR_FC) are indicated by '#'.

Table 32. Partial networking status register (address 073h)

Bit	Symbol	Access	Value	Description
7	SYNCS	R		CAN partial networking sync status:
			0	CAN partial networking core not ready to decode frame
			1	CAN partial networking core ready to decode frame
6	CPNERRS	R		CAN partial networking error status:
			0	no CAN partial networking error detected; PNFDER = 0 and PNCOK = 1
			1	CAN partial networking error detected; PNFDER =1 or PNCOK = 0; wake-up via WUP only
5	CPNS	R		CAN partial networking status:
			0	CAN partial networking configuration error detected; PNCOK = 0
			1	CAN partial networking configuration OK; PNCOK = 1
4	LFDS	R		last frame decode status:
			0	most recent CAN frame not decoded successfully
			1	most recent CAN frame decoded successfully
3:0	reserved	R	-	ignore on read

Table 33. Partial networking error count status register (address 075h)

Bit	Symbol	Access	Value	Description
7:5	reserved	R	-	ignore on read
4:0	PNERRCNT	R		CAN partial networking error count status:
			00000	0
			00001	1
			00010	2
			00011	3
			...	...
			11111	31

Table 34. Partial networking ID registers 0 to 3 (addresses 020h to 023h)

Addr.	Bit	Symbol	Access	Value	Description
020h	7:0	ID7:ID0	R/W	00h#	bits ID7 to ID0 of the extended frame format
021h	7:0	ID15:ID8	R/W	00h#	bits ID15 to ID8 of the extended frame format
022h	7:2	ID23:ID18	R/W	00h#	bits ID23 to ID18 of the extended frame format bits ID5 to ID0 of the standard frame format

Table 34. Partial networking ID registers 0 to 3 (addresses 020h to 023h)*...continued*

Addr.	Bit	Symbol	Access	Value	Description
	1:0	ID17:ID16	R/W	00h#	bits ID17 to ID16 of the extended frame format
023h	7:5	reserved	R	-	always write 000; ignore on read
	4:0	ID28:ID24	R/W	00h#	bits ID28 to ID24 of the extended frame format bits ID10 to ID6 of the standard frame format

Table 35. Partial networking ID mask registers 0 to 3 (addresses 024h to 027h)

Addr.	Bit	Symbol	Access	Value	Description
024h	7:0	M7:M0	R/W	00h#	ID mask bits 7 to 0 of extended frame format
025h	7:0	M15:M8	R/W	00h#	ID mask bits 15 to 8 of extended frame format
026h	7:2	M23:M18	R/W	00h#	ID mask bits 23 to 18 of extended frame format ID mask bits 5 to 0 of standard frame format
	1:0	M17:M16	R/W	00h#	ID mask bits 17 to 16 of extended frame format
027h	7:5	reserved	R/W	00h#	always write 000; ignore on read
	4:0	M28:M24	R/W	00h#	ID mask bits 28 to 24 of extended frame format ID mask. bits 10 to 6 of standard frame format

Table 36. Partial networking data mask registers 0 to 7 (addresses 028h to 02Fh)

Addr.	Bit	Symbol	Access	Value	Description
028h	7:0	DM0	R/W	FFh#	data mask 0 configuration
029h	7:0	DM1	R/W	FFh#	data mask 1 configuration
02Ah	7:0	DM2	R/W	FFh#	data mask 2 configuration
02Bh	7:0	DM3	R/W	FFh#	data mask 3 configuration
02Ch	7:0	DM4	R/W	FFh#	data mask 4 configuration
02Dh	7:0	DM5	R/W	FFh#	data mask 5 configuration
02Eh	7:0	DM6	R/W	FFh#	data mask 6 configuration
02Fh	7:0	DM7	R/W	FFh#	data mask 7 configuration

Table 37. Partial networking frame control register (address 030h)

Bit	Symbol	Access	Value	Description
7	IDE	R/W		identifier format:
			0#	standard frame format (11-bit)
			1	extended frame format (29-bit)
6	PNDM	R/W		partial networking data mask:
			0	data length code and data field are ‘don’t care’ for wake-up
			1#	data length code and data field are evaluated at wake-up
5:4	reserved	R	-	always write 00; ignore on read

Table 37. Partial networking frame control register (address 030h)*...continued*

Bit	Symbol	Access	Value	Description
3:0	DLC	R/W		number of data bytes expected in a CAN frame (DLC):
			0000#	0
			0001	1
			0010	2
			0011	3
			0100	4
			0101	5
			0110	6
			0111	7
			1000	8
			1001 to 1111	8

Table 38. Partial networking data rate and filter configuration register (address 031h)

Bit	Symbol	Access	Value	Description
7:4	IDFS	R/W		idle detection filter select:
			0000#	bitfilter 0: ignore < 5.0 % of arbitration bit time; detect > 17.5 % of arbitration bit time (500 kbit/s max)
			0001	ISO bitfilter 1: ignore < 5.0 % of arbitration bit time; detect > 17.5 % of arbitration bit time (500 kbit/s max)
			0010	ISO bitfilter 2: ignore < 2.5 % of arbitration bit time; detect > 8.75 % of arbitration bit time (500 kbit/s max)
			0011	bitfilter 3: ignore < 18 ns; detect > 93 ns
			0100	bitfilter 4: ignore < 42 ns; detect > 119 ns
			0101	bitfilter 5: ignore < 67 ns; detect > 145 ns
			0110	bitfilter 6: ignore < 91 ns; detect > 170 ns
			0111 to 1111	reserved
3	reserved	R	-	always write 0; ignore on read
2:0	CDR	R/W		CAN arbitration bit rate selection:
			000	50 kbit/s
			001	100 kbit/s
			010	125 kbit/s
			011	250 kbit/s
			100#	500 kbit/s
			101	667 kbit/s
			110	reserved (PNCORE disabled)
			111	1 Mbit/s

Table 39. Partial networking and CAN configuration register (address 032h)

Bit	Symbol	Access	Value	Description
7:4	reserved	R	-	always write 0000; ignore on read
3	CXLDE	R/W		CAN XL FAST mode tolerance enable (used for bus integration):
			0#	CAN XL FAST mode tolerance disabled
			1	CAN XL FAST mode tolerance enabled
2	PNECC	R/W		partial networking error counter control:
			0#	CAN XL and CAN FD frames will increment error counter
			1	CAN XL and CAN FD frames will not increment error counter
1	PNCOK	R/W		CAN partial networking configuration:
			0#	partial networking register configuration invalid (wake-up via standard wake-up pattern only)
			1	partial networking register configuration valid
0	CPNC	R/W		CAN selective wake-up enable:
			0#	disable CAN selective wake-up
			1	enable CAN selective wake-up

7.12.9 Fail-safe configuration and status registers

Reset values after system startup (BOOT_OK; see Figure 3) are indicated by '*'.

Table 40. Fail-safe counter register (address 090h)

Bit	Symbol	Access	Value	Description
7:6	FSCC	R/W		fail-safe counter value:
			00*[1]	0
			01	1
			10	2
			11	3
5:0	reserved	R	-	always write 000000; ignore on read

[1] Value after entering Fail-safe mode.

Table 41. Fail-safe output control register (address 091h)

Bit	Symbol	Access	Value	Description
7:2	reserved	R	-	always write 000000; ignore on read
1:0	LIMPFSOC	R/W		LIMPFSO_N output control:
			00[1]	LIMPFSO_N high-Z
			01[2]	LIMPFSO_N driven LOW
			10[3]	LIMPFSO_N driven to V_{IO} level
			11[3]	LIMPFSO_N driven to V_{IO} level

[1] Value after entering Off mode.

[2] Value after entering FSM_FS Fail-safe or FSM_MAIN BootFail mode.
[3] Reset to 00 after boot, INCR_FC or Reset.

Table 42. Fail-safe output status register (address 076h)

Bit	Symbol	Access	Value	Description
7:1	reserved	R	-	ignore on read
0	LIMPFSOS	R		LIMPFSO_N pin status:
			0	$V_{LIMPFSO\_N} < V_{th(limp)min}$
			1	$V_{LIMPFSO\_N} > V_{th(limp)max}$

7.12.10 System reset register

Table 43. System reset register (address FE0h)

Bit	Symbol	Access	Value	Description
7:0	SFR	W		software-forced system reset:
			01h	set up system reset
			80h	confirm system reset

7.12.11 Wake-up pulse configuration register

Reset values after system startup (BOOT_OK; see Figure 3) are indicated by '*'.

Table 44. Wake-up pulse configuration register (address 040h)

Bit	Symbol	Access	Value	Description
7:1	reserved	R	-	always write 00h; ignore on read
0	WFC	R/W		wake-up pulse width (t_{wake}) on WAKE pin
			0*	short wake-up time
			1	long wake-up time

7.12.12 Interrupt registers

Reset values after system startup (BOOT_OK; see Figure 3) are indicated by '*'.

Write 1 to clear (W1C) interrupt status bit after interrupt detected.

Table 45. System interrupt enable register (address 010h)

Bit	Symbol	Access	Value	Description
7	reserved	R	-	always write 0; ignore on read
6	CWE	R/W		CAN wake-up interrupt enable:
			0*	disable CAN wake-up interrupt
			1[1]	enable CAN wake-up interrupt
5	OTE	R/W		overtemperature shutdown interrupt enable:
			0*	disable overtemperature shutdown interrupt
			1	enable overtemperature shutdown interrupt
4	SPIFE	R/W		SPI failure interrupt enable:
			0*	disable SPI failure interrupt
			1	enable SPI failure interrupt
3	UVCCE	R/W		V_{CC} undervoltage interrupt enable:
			0	disable V_{CC} undervoltage interrupt
			1*	enable V_{CC} undervoltage interrupt
2	reserved	R	-	always write 0; ignore on read
1	WPRE	R/W		WAKE pin rising-edge interrupt enable:
			0*	disable WAKE pin rising-edge interrupt
			1[1]	enable WAKE pin rising-edge interrupt
0	WPFE	R/W		WAKE pin falling-edge interrupt enable:
			0*	disable WAKE pin falling-edge interrupt
			1[1]	enable WAKE pin falling-edge interrupt

[1] Value after entering FSM_FS Fail-safe mode.

Table 46. CAN interrupt enable register (address 011h)

Bit	Symbol	Access	Value	Description
7:4	reserved	R	-	always write 0000; ignore on read
3	CBSE	R/W		CAN bus silence interrupt enable:
			0*	disable CAN bus silence interrupt
			1	enable CAN bus silence interrupt
2	BUSDOME	R/W		CAN bus dominant interrupt enable:
			0*	disable CAN bus dominant interrupt
			1	enable CAN bus dominant interrupt
1	TXD2DOME	R/W		TXD2 dominant timeout interrupt enable:

Table 46. CAN interrupt enable register (address 011h)*...continued*

Bit	Symbol	Access	Value	Description
			0*	disable TXD2 dominant timeout interrupt
			1	enable TXD2 dominant timeout interrupt
0	TXDDOME	R/W		TXD dominant timeout interrupt enable:
			0*	disable TXD dominant timeout interrupt
			1	enable TXD dominant timeout interrupt

Table 47. GPIO interrupt enable register (address 012h)

For GPIOx wake-up detection, bits GPIOxFS must be set to 0x13, 0x14 or 0x15 (see Table 25 and Table 26).

Bit	Symbol	Access	Value	Description
7:2	reserved	R	-	always write 000000; ignore on read
1	GPIO2E	R/W		GPIO2 interrupt enable:
			0*	disable GPIO2 interrupt
			1	enable GPIO2 interrupt
0	GPIO1E	R/W		GPIO1 interrupt enable:
			0*	disable GPIO1 interrupt
			1	enable GPIO1 interrupt

Table 48. System interrupt status register (address 060h)

Bit	Symbol	Access	Value	Description
7	PO[1]	R/W1C		power-on/system reset interrupt:
			0	no power-on/system reset interrupt detected
			1*	power-on/system reset interrupt detected
6	CW[2]	R/W1C		CAN wake-up interrupt:
			0*	no CAN wake-up interrupt detected
			1	CAN wake-up interrupt detected
5	OT	R/W1C		overtemperature warning interrupt:
			0*	no overtemperature warning interrupt detected
			1	overtemperature warning interrupt detected
4	SPIF	R/W1C		SPI failure interrupt:
			0*	no SPI failure interrupt detected
			1	SPI failure interrupt detected
3	UVCC	R/W1C		V_{CC} undervoltage interrupt:
			0*	no V_{CC} undervoltage interrupt detected
			1	V_{CC} undervoltage interrupt detected
2	reserved	R	-	always write 1; ignore on read

Table 48. System interrupt status register (address 060h)*...continued*

Bit	Symbol	Access	Value	Description
1	WPR[2]	R/W1C		WAKE pin rising-edge interrupt:
			0*	no WAKE pin rising-edge interrupt detected
			1	WAKE pin rising-edge interrupt detected
0	WPF[2]	R/W1C		WAKE pin falling-edge interrupt:
			0*	no WAKE pin falling-edge interrupt detected
			1	WAKE pin falling-edge interrupt detected

[1] PO interrupt is always enabled.
[2] This interrupt is also a wake-up source.

Table 49. CAN interrupt status register (address 061h)

Bit	Symbol	Access	Value	Description
7:4	reserved	R	-	always write 1111; ignore on read
3	CBS	R/W1C		CAN bus silence interrupt:
			0*	no CAN bus silence interrupt detected
			1	CAN bus silence interrupt detected
2	BUSDOM	R/W1C		CAN bus dominant interrupt:
			0*	no CAN bus dominant interrupt detected
			1	CAN bus dominant interrupt detected
1	TXD2DOM	R/W1C		TXD2 dominant timeout interrupt:
			0*	no TXD2 dominant timeout interrupt detected
			1	TXD2 dominant timeout interrupt detected
0	TXDDOM	R/W1C		TXD dominant timeout interrupt:
			0*	no TXD dominant timeout interrupt detected
			1	TXD dominant timeout interrupt detected

Table 50. Partial networking interrupt status register (address 062h)

Bit	Symbol	Access	Value	Description
7:3	reserved	R	-	always write 11111; ignore on read
2	PNFDER[1]	R/W1C		partial networking frame detection error interrupt:
			0*	no partial networking frame detection error interrupt detected
			1	partial networking frame detection error interrupt detected
1:0	reserved	R	-	always write 11; ignore on read

[1] PNFDER interrupt is always enabled.

Table 51. GPIO interrupt status register (address 063h)>

Bit	Symbol	Access	Value	Description
7:2	reserved	R	-	always write 111111; ignore on read
1	GPIO2	R/W1C		GPIO2 interrupt:
			0*	no GPIO2 interrupt detected
			1	GPIO2 interrupt detected
0	GPIO1	R/W1C		GPIO1 interrupt:
			0*	no GPIO1 interrupt detected
			1	GPIO1 interrupt detected

7.12.13 Lock control register

Reset values after system startup (BOOT_OK; see Figure 3) are indicated by '*'.

Table 52. Lock control register (address 050h)

Bit	Symbol	Access	Value	Description
7:5	reserved	R	-	always write 000; ignore on read
4	LKGPM	R/W		Lock control: general-purpose memory registers (0xFF0 to 0xFF3):
			0*	SPI write access enabled
			1	SPI write access disabled
3	LKRST	R/W		Lock control: system reset register (0xFE0):
			0	SPI write access enabled
			1*	SPI write access disabled
2	LKCFG	R/W		Lock control: System/Wake/CAN configuration registers (0x40 to 0x47):
			0*	SPI write access enabled
			1	SPI write access disabled
1	LKPNC	R/W		Lock control: partial networking configuration registers (0x020 to 0x032):
			0*	SPI write access enabled
			1	SPI write access disabled
0	LKIE	R/W		Lock control: interrupt enable registers (0x010, 0x011, 0x012):
			0*	SPI write access enabled
			1	SPI write access disabled

7.12.14 General-purpose memory registers

The TJA1466 allocates 4 bytes of memory for general-purpose registers used to store user information. Note that these registers are not cleared during an SPI system reset. They are cleared when the device enters Off mode.

Table 53. General-purpose memory registers 0 to 3 (addresses FF0h to FF3h)

Addr.	Bit	Symbol	Access	Value	Description
FF0h	7:0	GPM[7:0]	R/W	00h	general-purpose memory 0
FF1h	7:0	GPM[15:8]	R/W	00h	general-purpose memory 1

Table 53. General-purpose memory registers 0 to 3 (addresses FF0h to FF3h)*...continued*

Addr.	Bit	Symbol	Access	Value	Description
FF2h	7:0	GPM[23:16]	R/W	00h	general-purpose memory 2
FF3h	7:0	GPM[31:24]	R/W	00h	general-purpose memory 3

7.12.15 Device identification register

Table 54. Device identification register (address FFFh)

Bit	Symbol	Access	Value	Description
7:5	IDS	R		device identification number:
			30h	TJA1466A
			40h	TJA1466B
			50h	TJA1466C

8 Limiting values

Table 55. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134); all voltages are referenced to pin GND, unless otherwise specified; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Max	Unit
V_x	Voltage on pin x[1]	pins VCC, VIO	-0.3	+6	V
			-	+7[2]	V
		pins VBAT	-	+40	V
		LIMPFSO_N	-0.3	+40	V
		pin INH	-0.3	V_{BAT}+0.3[3]	V
		pins CANH, CANL, WAKE	-36	+40	V
		pins RXD, TXD, SCSN, SCK, SDI, SDO, RST_N, GPIOx	-0.3	V_{IO}+0.3[4]	V
$I_{r(VBAT)}$	reverse current on pin VBAT		-10	-	mA
$I_{O(INH)}$	output current on pin INH		-2	-	mA
$I_{O(LIMPFSO\_N)}$	output current on pin LIMPFSO_N		-	2	mA
$I_{O(RST\_N)}$	output current on pin RST_N		-	18	mA
$V_{(CANH-CANL)}$	voltage between pin CANH and pin CANL		-40	+40	V
V_{trt}	transient voltage	on pin VBAT; on pins CANH, CANL and WAKE via 1 nF capacitor; pin WAKE with 3 kΩ resistor [5]			
		pulse 1	-100	-	V
		pulse 2a	-	+75	V
		pulse 3a	-150	-	V
		pulse 3b	-	+100	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (150 pF, 330 Ω discharge circuit) [6]			
		on pins CANH, CANL; on pin VBAT with 100 nF capacitor; on pin WAKE with ≥3 kΩ resistor	-8	+8	kV
		Human Body Model (HBM)			
		on any pin [7]	-4	+4	kV
		on pins CANH, CANL [8]	-8	+8	kV
		Charged Device Model (CDM) [9]			
		on any pin	-500	+500	V
T_{vj}	virtual junction temperature	[10]	-40	+150	°C
T_{stg}	storage temperature	[11]	-55	+150	°C

[1] The device can sustain voltages up to the specified values over the product lifetime, provided applied voltages (including transients) never exceed these values.

[2] The device can withstand voltages between 6 V and 7 V for a total of 20 s over the product lifetime.

[3] Absolute maximum of 40 V.
[4] Subject to the qualifications detailed in Table notes 1 and 2 above for pin VIO, and for VIO-related input pins.
[5] Verified by an external test house according to IEC TS 62228, Section 4.2.4; parameters for standard pulses defined in ISO 7637, part 2.
[6] Verified by an external test house according to IEC TS 62228, Section 4.3.
[7] According to AEC-Q100-002.
[8] Pins stressed to reference group containing all ground and supply pins, emulating the application circuit (Figure 15). HBM pulse as specified in AEC-Q100-002 used.
[9] According to AEC-Q100-011.
[10] In accordance with IEC 60747-1. An alternative definition of virtual junction temperature is: $T_{vj} = T_{amb} + P \times R_{th(j-a)}$, where $R_{th(j-a)}$ is a fixed value used in the calculation of T_{vj}. The rating for T_{vj} limits the allowable combinations of power dissipation (P) and ambient temperature (T_{amb}).
[11] T_{stg} in application according to IEC61360-4. For component transport and storage conditions, see instead IEC61760-2.

9 Thermal characteristics

Table 56. Thermal characteristics

Value determined for free convection conditions on a JEDEC 2S2P board.

Symbol	Parameter	Conditions[1]	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	DHVQFN18	68	K/W
$R_{th(j-c)}$	thermal resistance from junction to case[2]	DHVQFN18	28	K/W
Ψ_{j-top}	thermal characterization parameter from junction to top of package	DHVQFN18	9	K/W

[1] According to JEDEC JESD51-2, JESD51-5 and JESD51-7 at natural convection on 2s2p board. Board with two inner copper layers (thickness: 35 µm) and thermal via array under the exposed pad connected to the first inner copper layer (thickness: 70 µm).
[2] Case temperature refers to the center of the heatsink at the bottom of the package.

10 Static characteristics

Table 57. Static characteristics

T_{vj} = -40 °C to +150°C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 1.71 V to 5.5 V; V_{BAT} = 4.75 V to 40 V; R_L = 60 Ω unless specified otherwise; all voltages are defined with respect to ground; positive currents flow into the IC.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply; pin VCC						
V_{CC}	supply voltage		4.5	-	5.5	V
V_{uvd}	undervoltage detection voltage	[2]	4	-	4.5	V
V_{uvhys}	undervoltage hysteresis voltage		50	-	-	mV
I_{CC}	supply current	Normal mode; transmitter dominant	-	42	60	mA
		Normal mode; short circuit on bus lines; -3 V < (V_{CANH} = V_{CANL}) < +40 V	-	-	125	mA
		Normal mode, transmitter recessive	-	7	10	mA
		ListenOnly mode, LPL = 0	-	7	10	mA
		ListenOnly mode; LPL = 1; VBATVCC = 0; T_{vj} < 150 °C	-	-	40	µA
		ListenOnly mode; LPL = 1; VBATVCC = 1; T_{vj} < 150 °C	-	90	165	µA
		Standby or Sleep mode; T_{vj} < 85 °C	-	-	3	µA
		Standby or Sleep mode; T_{vj} < 150 °C	-	-	40	µA
I/O level adapter supply; pin VIO						
V_{IO}	supply voltage		1.71	-	5.5	V
V_{uvd}	undervoltage detection voltage	Sleep mode [2]	1.5	-	1.71	V
		all modes except Sleep and Off [2]				
		TJA1466A	1.62	-	1.692	V
		TJA1466B, TJA1466C	2.97	-	3.102	V
V_{uvr}	undervoltage release voltage	all modes except Sleep and Off				
		TJA1466A	1.638	-	1.71	V
		TJA1466B, TJA1466C	3.003	-	3.135	V
V_{uvhys}	undervoltage hysteresis voltage	Sleep mode	33	-	-	mV
		all modes except Sleep and Off				
		TJA1466A	14	-	-	mV
		TJA1466B, TJA1466C	26	-	-	mV
V_{ovd}	overvoltage detection voltage	all modes except Sleep and Off				
		TJA1466A	1.89	-	1.98	V
		TJA1466B	3.465	-	3.63	V
		TJA1466C	5.25	-	5.5	V

Table 57. Static characteristics...*continued*

T_{vj} = -40 °C to +150°C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 1.71 V to 5.5 V; V_{BAT} = 4.75 V to 40 V; R_L = 60 Ω unless specified otherwise; all voltages are defined with respect to ground; positive currents flow into the IC.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{IO}	supply current	Normal or ListenOnly mode (excluding pull-up currents on V_{IO}-related pins); $V_{TXD} = V_{IO}$	-	-	5	µA
		Standby or Sleep mode; T_{vj} < 85 °C	-	-	2	µA
		Standby or Sleep mode; T_{vj} < 150 °C	-	-	4	µA
Supply; pin VBAT						
V_{BAT}	battery supply voltage		4.75	-	40	V
V_{uvd}	undervoltage detection voltage	all modes [2]	4.25	-	4.75	V
I_{BAT}	battery supply current	Normal mode or (ListenOnly mode; VBATVCC = 1 or LPL = 0); pin INH left open; CXLDE = 0; $V_{BAT} \leq 28$ V [3]	-	-	400	µA
		ListenOnly mode; VBATVCC = 0 and LPL = 1; pin INH left open; CXLDE = 0; $V_{BAT} \leq 28$ V [3]	-	-	525	µA
		Sleep or Standby mode; CAN Offline Bias mode; pin INH left open; CXLDE = 0; CWE = 1; CPNC = 1; PNCOK = 1; $V_{WAKE} = V_{BAT}$; $V_{BAT} \leq 28$ V [3]				
		VBATVCC = 0; Tvj < 85 °C	-	-	450	µA
		VBATVCC = 0; Tvj < 150 °C	-	-	500	µA
		VBATVCC = 1; Tvj < 85 °C	-	-	350	µA
		VBATVCC = 1; Tvj < 150 °C	-	-	375	µA
		CXLDE = 1; additional battery current when CXLDE changes from 0 to 1 with CPNC = 1 and PNCOK = 1; all modes except Off and CAN Offline	-	55	110	µA
		Standby mode; CAN Offline mode; pin INH left open; $V_{WAKE} = V_{BAT}$ or GND; $V_{BAT} \leq 28$ V				
		Tvj < 85 °C	-	22	50	µA
		Tvj < 150 °C	-	22	60	µA
		Sleep mode; CAN Offline mode; $V_{WAKE} = V_{BAT}$ or GND; $V_{BAT} \leq 28$ V; $V_{IO} = 0$ V				
		Tvj < 85 °C	-	12	20	µA
		Tvj < 150 °C	-	12	33	µA
		V_{BAT} = 32 V; BCCTRL = 0; additional current due to V_{BAT} being increased to 32 V	-	0.15	0.5	mA
		V_{BAT} = 40 V; BCCTRL = 0; additional current due to V_{BAT} being increased to 40 V	-	1.2	1.8	mA

Table 57. Static characteristics...*continued*

T_{vj} = -40 °C to +150°C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 1.71 V to 5.5 V; V_{BAT} = 4.75 V to 40 V; R_L = 60 Ω unless specified otherwise; all voltages are defined with respect to ground; positive currents flow into the IC.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CAN transmit data input; pin TXD						
V_{IH}	HIGH-level input voltage		$0.7V_{IO}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{IO}$	V
$V_{hys(TXD)}$	hysteresis voltage on pin TXD		50	-	-	mV
R_{pu}	pull-up resistance		20	-	80	kΩ
$I_{IL(off)}$	Off state input leakage current	TXD = high-Z or $V_{IO} < V_{uvd(VIO)}$; $0 V < V_{TXD} < V_{IO}$	-5	-	+5	µA
C_i	input capacitance	[3]	-	-	10	pF
CAN receive data output; pin RXD						
I_{OH}	HIGH-level output current	$V_{RXD} = V_{IO} - 0.4 V$	-10	-	-1	mA
I_{OL}	LOW-level output current	$V_{RXD} = 0.4 V$	1	-	10	mA
$I_{IL(off)}$	Off state input leakage current	RXD = high-Z or $V_{IO} < V_{uvd(VIO)}$; $0 V < V_{RXD} < V_{IO}$	-5	-	+5	µA
Serial peripheral interface						
input pins SDI, SCK and SCSN						
V_{IH}	HIGH-level input voltage		$0.7V_{IO}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{IO}$	V
V_{hys}	hysteresis voltage		50	-	-	mV
R_{pd}	pull-down resistance	on pins SCK and SDI in Repeater mode; $V_{SCK} = V_{IL}$; $V_{SDI} = V_{IL}$	20	-	80	kΩ
R_{pu}	pull-up resistance	on pins SCK and SDI in Repeater mode; $V_{SCK} = V_{IH}$; $V_{SDI} = V_{IH}$	20	-	80	kΩ
		on pin SCSN [4]	20	-	80	kΩ
$I_{IL(off)}$	Off state input leakage current	pins SDI and SCK; high-Z or $V_{IO} < V_{uvd(VIO)}$; $0 V < V_{SDI} < V_{IO}$; $0 V < V_{SCK} < V_{IO}$	-5	-	+5	µA
C_i	input capacitance	[3]	-	-	10	pF
output pin SDO						
I_{OH}	HIGH-level output current	V_{SDO} = VIO - 0.4 V	-10	-	-1	mA
I_{OL}	LOW-level output current	$V_{SDO} = 0.4 V$	1	-	10	mA
$I_{OL(off)}$	Off state output leakage current	$V_{SCSN} = V_{IO}$ or high-Z or $V_{IO} < V_{uvd(VIO)}$; $0 V < V_{SDO} < V_{IO}$	-5	-	+5	µA
General purpose I/Os; pins GPIOx						
I_{OH}	HIGH-level output current	V_{GPIOx} = VIO - 0.4 V; depending on GPIO configuration	-10	-	-1	mA
I_{OL}	LOW-level output current	$V_{GPIOx} = 0.4 V$; depending on GPIO configuration	1	-	10	mA

Table 57. Static characteristics...*continued*

T_{vj} = -40 °C to +150°C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 1.71 V to 5.5 V; V_{BAT} = 4.75 V to 40 V; R_L = 60 Ω unless specified otherwise; all voltages are defined with respect to ground; positive currents flow into the IC.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage	depending on GPIO configuration	$0.7V_{IO}$	-	-	V
V_{IL}	LOW-level input voltage	depending on GPIO configuration	-	-	$0.3V_{IO}$	V
V_{hys}	hysteresis voltage	depending on GPIO configuration	50	-	-	mV
R_{pu}	pull-up resistance	depending on GPIO configuration	20	-	80	kΩ
R_{pd}	pull-down resistance	depending on GPIO configuration	20	-	80	kΩ
$I_{OL(off)}$	Off state output leakage current	high-Z or $V_{IO} < V_{uvd(VIO)}$; 0 V < $V_{GPIOx} < V_{IO}$	-5	-	5	µA
C_i	input capacitance	[3]	-	-	10	pF
Reset input/output; pin RST_N						
V_{IH}	HIGH-level input voltage		$0.7V_{IO}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{IO}$	V
V_{hys}	hysteresis voltage		50	-	-	mV
V_{OL}	LOW-level output voltage	I_{RST_N} = 1 mA; ((0 V ≤ V_{BAT} ≤ $V_{uvd(VBAT)}$) and V_{VIO} ≥ 1.2 V) or (($V_{BAT} > V_{uvd(VBAT)}$) and (0 V ≤ V_{VIO} ≤ 5.5 V))	0	-	0.4	V
		I_{RST_N} = 10 mA; $V_{BAT} > V_{uvd(VBAT)}$ and 0 V ≤ V_{VIO} ≤ 5.5 V [3]	0	-	$0.25V_{IO}$	V
R_{pu}	pull-up resistance	to V_{IO}	20	-	80	kΩ
C_i	input capacitance	[3]	-	-	10	pF
Local wake-up input; pin WAKE						
R_{pu}	pull-up resistance	$V_{WAKE} > V_{th(wake)(max)}$ for t > $t_{wake(max)}$	100	-	400	kΩ
R_{pd}	pull-down resistance	$V_{WAKE} < V_{th(wake)(min)}$ for t > $t_{wake(max)}$	100	-	400	kΩ
$V_{th(wake)}$	wake-up threshold voltage	Sleep or Standby mode	1.8	-	2.6	V
V_{hys}	hysteresis voltage		90	-	-	mV
Limp/fail-safe ouput; pin LIMPFSO_N						
V_{OL}	LOW-level output voltage	$I_{LIMPFSO\_N}$ = 2 mA; LIMPFSO_N pin LOW (bit LIMPFSOC = 01)	0	-	0.5	V
I_L	leakage current	$V_{LIMPFSO\_N}$ = 40 V; LIMPFSO_N pin HIGH (V_{IO}) or high-Z (bit LIMPFSOC = 00, 10 or 11)	-2	-	2	µA
ΔV_H	HIGH-level voltage drop	$I_{LIMPFSO\_N}$ = -100 µA; LIMPFSO_N pin HIGH (V_{IO}; bit LIMPFSOC = 10 or 11)				
		TJA1466A	0	-	0.45	V
		TJA1466B, TJA1466C	0	-	1	V
$I_{O(sc)}$	short-circuit output current	$V_{LIMPFSO\_N}$ = 40 V; LIMPFSO_N pin LOW (bit LIMPFSOC = 01)	2	-	18	mA
$V_{th(limp)}$	limp threshold voltage	for read back	0.5	-	1.3	V

Table 57. Static characteristics...*continued*

T_{vj} = -40 °C to +150°C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 1.71 V to 5.5 V; V_{BAT} = 4.75 V to 40 V; R_L = 60 Ω unless specified otherwise; all voltages are defined with respect to ground; positive currents flow into the IC.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Inhibit output pin; pin INH						
ΔV_H	HIGH-level voltage drop	$\Delta V_H = V_{BAT} - V_{INH}$; I_{INH} = -1 mA	0	-	1	V
		$\Delta V_H = V_{BAT} - V_{INH}$; I_{INH} = -2 mA	0	-	2	V
I_L	leakage current	Sleep mode; high-Z	-2	-	2	µA
$I_{O(sc)}$	short-circuit output current	V_{INH} = 0 V	-15	-	-2	mA
Bus lines; pins CANH and CANL						
$V_{O(dom)}$	dominant output voltage	CAN Active mode; V_{TXD} = 0 V; $t < t_{to(dom)TXD}$; 4.75 V ≤ V_{CC} ≤ 5.25 V				
		pin CANH; R_L = 45 Ω to 65 Ω	3	3.5	4.26	V
		pin CANL; R_L = 45 Ω to 65 Ω	0.75	1.5	2.01	V
V_{TXsym}	transmitter voltage symmetry	$V_{TXsym} = V_{CANH} + V_{CANL}$; C_{SPLIT} = 4.7 nF; f_{TXD} = 250 kHz, 1 MHz or 2.5 MHz [3] [5]	$0.9V_{CC}$	-	$1.1V_{CC}$	V
$V_{cm(step)}$	common mode voltage step	[3] [5] [6]	-150	-	+150	mV
$V_{cm(p-p)}$	peak-to-peak common mode voltage	[3] [5] [6]	-300	-	+300	mV
$V_{O(dif)}$	differential output voltage	CAN Active mode; dominant; Normal mode; V_{TXD} = 0 V; $t < t_{to(dom)TXD}$; 4.75 V ≤ V_{CC} ≤ 5.25 V [5]				
		R_L = 45 Ω to 65 Ω	1.5	-	2.75	V
		R_L = 45 Ω to 70 Ω	1.5	-	3.3	V
		R_L = 2240 Ω [3]	1.5	-	5	V
		CAN Active mode, recessive; CAN Listen-only or CAN Offline Bias mode; $V_{TXD} = V_{IO}$; no load	-50	-	+50	mV
		CAN Offline mode; no load	-0.2	-	+0.2	V
$V_{O(rec)}$	recessive output voltage	CAN Active, CAN ListenOnly or CAN Offline Bias mode; $V_{TXD} = V_{IO}$; VBATVCC = 1 or (VBATVCC = 0 and V_{BAT} ≥ 5.5 V); no load	2	2.5	3	V
		CAN Offline mode; no load	-0.1	0	+0.1	V
$V_{th(RX)dif}$	differential receiver threshold voltage	-12 V ≤ V_{CANH} ≤ +12 V; -12 V ≤ V_{CANL} ≤ +12 V				
		CAN Active, CAN ListenOnly or CAN Offline Bias mode	0.5	-	0.9	V
		CAN Offline mode	0.4	-	1.1	V
		out-of-bounds comparator; no load; CXLDE = 1	-0.45	-	-0.25	V

Table 57. Static characteristics...*continued*

T_{vj} = -40 °C to +150°C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 1.71 V to 5.5 V; V_{BAT} = 4.75 V to 40 V; R_L = 60 Ω unless specified otherwise; all voltages are defined with respect to ground; positive currents flow into the IC.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{rec(RX)}$	receiver recessive voltage	-12 V ≤ V_{CANH} ≤ +12 V; -12 V ≤ V_{CANL} ≤ +12 V				
		CAN Active, CAN ListenOnly or CAN Offline Bias mode	-8	-	+0.5	V
		CAN Offline mode	-8	-	+0.4	V
		out-of-bounds comparator; no load; CXLDE = 1	-0.25	-	+9	V
$V_{dom(RX)}$	receiver dominant voltage	-12 V ≤ V_{CANH} ≤ +12 V; -12 V ≤ V_{CANL} ≤ +12 V				
		CAN Active, CAN ListenOnly or CAN Offline Bias mode	0.9	-	9	V
		CAN Offline mode	1.1	-	9	V
		out-of-bounds comparator; no load; CXLDE = 1	-8	-	-0.45	V
$V_{hys(RX)dif}$	differential receiver hysteresis voltage	-12 V ≤ V_{CANH} ≤ +12 V; -12 V ≤ V_{CANL} ≤ +12 V; CAN Active, CAN ListenOnly or CAN Offline Bias mode; no load	50	-	-	mV
$I_{O(sc)}$	short-circuit output current	-15 V ≤ V_{CANH} ≤ +40 V; -15 V ≤ V_{CANL} ≤ +40 V	-	-	115	mA
$I_{O(sc)rec}$	recessive short-circuit output current	-27 V ≤ V_{CANH} ≤ +32 V; -27 V ≤ V_{CANL} ≤ +32 V; Normal or ListenOnly mode; V_{TXD} = V_{IO} for t > $t_{d(TXD-buspasrec)start}$[7]	-3	-	+3	mA
I_L	leakage current	V_{CC} = V_{IO} = V_{BAT} = 0 V or pins shorted to GND via 47 KΩ; V_{CANH} = V_{CANL} = 5 V;	-10	-	+10	µA
R_i	input resistance	-2 V ≤ V_{CANL} ≤ +7 V; -2 V ≤ V_{CANH} ≤ +7 V	16	32	50	kΩ
$ΔR_i$	input resistance deviation	0 V ≤ V_{CANL} ≤ +5 V; 0 V ≤ V_{CANH} ≤ +5 V	-3	-	+3	%
$R_{i(dif)}$	differential input resistance	-2 V ≤ V_{CANL} ≤ +7 V; -2 V ≤ V_{CANH} ≤ +7 V	32	64	100	kΩ
C_i	input capacitance	[3]	-	-	20	pF
$C_{i(dif)}$	differential input capacitance	[3]	-	-	10	pF
Signal Improvement function on CANH or CANL; +4.75 V ≤ V_{CC} ≤ +5.25 V; see Figure 14.						
$R_{i(actrec)}$	active recessive phase input resistance[8]	bus dominant-to-recessive transition; +2 V ≤ V_{CANH} ≤ V_{CC} - 2 V; +2 V ≤ V_{CANL} ≤ V_{CC} - 2 V	37.5	-	66.5	Ω
$R_{i(dif)actrec}$	active recessive phase differential input resistance[8]	$R_{i(dif)actrec}$ = $R_{i(actrec)CANH}$ + $R_{i(actrec)CANL}$	75	-	133	Ω
Temperature detection						
$T_{j(sd)}$	shutdown junction temperature	[3]	180	-	200	°C

Table 57. Static characteristics...*continued*

T_{vj} = -40 °C to +150°C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 1.71 V to 5.5 V; V_{BAT} = 4.75 V to 40 V; R_L = 60 Ω unless specified otherwise; all voltages are defined with respect to ground; positive currents flow into the IC.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{j(sd)rel}$	release shutdown junction temperature	[3]	175	-	195	°C

[1] All parameters are guaranteed over the junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage ranges.
[2] Undervoltage is detected between min and max values. Undervoltage is guaranteed to be detected below min value and guaranteed not to be detected above max value.
[3] Not tested in production; guaranteed by design.
[4] The pull-up resistance on pin SCSN is a differential resistance.
[5] The test circuit used to measure the bus output voltage symmetry and the common-mode voltages (which includes C_{SPLIT}) is shown in Figure 17.
[6] See Figure 11.
[7] This parameter is defined in ISO 11898-2:2024 as $t_{pas\_rec\_start}$ and is specified in the Dynamic Characteristics table (see Table 58 and Figure 14).
[8] Extended dominant and active recessive phases are not DC states and are only valid for a limited time after a dominant-to-recessive transition on pin TXD.

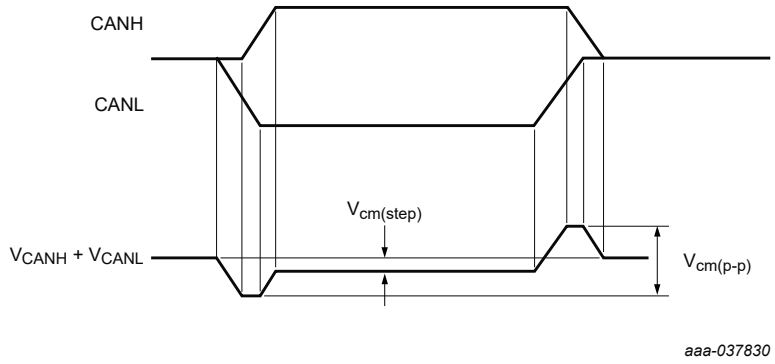


Figure 11. CAN bus common-mode voltage according to SAE 1939-14

11 Dynamic characteristics

Table 58. Dynamic characteristics

T_{vj} = -40 °C to +150 °C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 1.71 V to 5.5 V; V_{BAT} = 4.75 V to 40 V; R_L = 60 Ω unless specified otherwise; all voltages are defined with respect to ground.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CAN timing characteristics according to ISO 11898-2:2024; see Figure 12 and Figure 16						
$t_{d(TXDL-RXDL)}$	delay time from TXD LOW to RXD LOW	Normal mode	-	-	190	ns
$t_{d(TXDH-RXDH)}$	delay time from TXD HIGH to RXD HIGH	Normal mode	-	-	190	ns
CAN timing characteristics according to ISO 11898-2:2024; V_{CC} = 4.75 V to 5.25 V; see Figure 12, Figure 14 and Figure 16						
$t_{d(TXD-busdom)}$	delay time from TXD to bus dominant	Normal mode	-	-	80	ns
$t_{d(TXD-busrec)}$	delay time from TXD to bus recessive	Normal mode	-	-	80	ns
$t_{d(busdom-RXD)}$	delay time from bus dominant to RXD	Normal or ListenOnly mode	-	-	110	ns
$t_{d(busrec-RXD)}$	delay time from bus recessive to RXD	Normal or ListenOnly mode	-	-	110	ns
$t_{d(TXDL-RXDL)}$	delay time from TXD LOW to RXD LOW	Normal mode	-	-	190	ns
$t_{d(TXDH-RXDH)}$	delay time from TXD HIGH to RXD HIGH	Normal mode	-	-	190	ns
$t_{d(TXD-buspasrec)start}$	delay time from TXD to bus passive recessive start	Normal mode [2] [3]	-	-	530	ns
$t_{d(TXD-busactrec)start}$	delay time from TXD to bus active recessive start	Normal mode [2]	-	-	120	ns
$t_{d(TXD-busactrec)end}$	delay time from TXD to bus active recessive end	Normal mode [2]	355	-	-	ns
CAN FD timing characteristics according to ISO 11898-2:2024 parameter set C ($t_{bit(TXD)}$ ≥ 125 ns, up to 8 Mbit/s)[4]; V_{CC} = 4.75 V to 5.25 V; see Figure 12 and Figure 16						
$\Delta t_{bit(bus)}$	transmitted recessive bit width deviation	$\Delta t_{bit(bus)} = t_{bit(bus)} - t_{bit(TXD)}$	-10	-	+10	ns
Δt_{rec}	receiver timing symmetry	$\Delta t_{rec} = t_{bit(RXD)} - t_{bit(bus)}$	-20	-	+15	ns
$\Delta t_{bit(RXD)}$	received recessive bit width deviation	$\Delta t_{bit(RXD)} = t_{bit(RXD)} - t_{bit(TXD)}$	-30	-	+20	ns
CAN FD timing characteristics according to ISO 11898-2:2024 parameter set C ($t_{bit(TXD)}$ ≥ 125 ns, up to 8 Mbit/s)[4]; see Figure 12 and Figure 16						
$\Delta t_{bit(bus)}$	transmitted recessive bit width deviation	$\Delta t_{bit(bus)} = t_{bit(bus)} - t_{bit(TXD)}$	-15	-	+15	ns
Δt_{rec}	receiver timing symmetry	$\Delta t_{rec} = t_{bit(RXD)} - t_{bit(bus)}$	-25	-	+20	ns
$\Delta t_{bit(RXD)}$	received recessive bit width deviation	$\Delta t_{bit(RXD)} = t_{bit(RXD)} - t_{bit(TXD)}$	-35	-	+25	ns
Watchdog[2]						
t_{wd}	watchdog period	WDP = 000	9	10	11	ms
		WDP = 001	18	20	22	ms
		WDP = 010	45	50	55	ms
		WDP = 011	90	100	110	ms
		WDP = 100	180	200	220	ms
		WDP = 101	450	500	550	ms
		WDP = 110	900	1000	1100	ms
		WDP = 111	1800	2000	2200	ms

Table 58. Dynamic characteristics...*continued*

T_{vj} = -40 °C to +150 °C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 1.71 V to 5.5 V; V_{BAT} = 4.75 V to 40 V; R_L = 60 Ω unless specified otherwise; all voltages are defined with respect to ground.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dominant time-out times						
$t_{to(dom)TXD}$	TXD dominant time-out time	V_{TXD} = 0 V; Normal mode [2] [5]	0.8	-	4	ms
$t_{to(dom)bus}$	bus dominant time-out time	$V_{O(dif)}$ > 0.9 V; Normal or Listen Only mode [2] [5]	0.8	-	4	ms
Bus wake-up times; pins CANH and CANL; see Figure 6 and Figure 7						
$t_{wake(busdom)}$	bus dominant wake-up time	CAN Offline mode [2] [6]	0.5	-	1.45	µs
$t_{wake(busrec)}$	bus recessive wake-up time	CAN Offline mode [2] [6]	0.5	-	1.45	µs
$t_{to(wake)bus}$	bus wake-up time-out time	CAN Offline mode [2] [5]	0.8	-	9	ms
$t_{d(busact-bias)}$ [7]	bus bias reaction time	CAN Offline mode [2]	-	-	250	µs
$t_{to(silence)}$	bus silence time-out time	timer reset and restarted when bus changes from dominant to recessive or vice versa, except in Offline mode [2] [5]	0.6	-	1.2	s
Serial peripheral interface timing; pins SCSN, SCK, SDI and SDO; see Figure 13 [2]						
$t_{cy(clk)}$	clock cycle time	Normal, ListenOnly or Standby mode	250	-	-	ns
$t_{SPILEAD}$	SPI enable lead time	Normal, ListenOnly or Standby mode	50	-	-	ns
t_{SPILAG}	SPI enable lag time	Normal, ListenOnly or Standby	50	-	-	ns
$t_{clk(H)}$	clock HIGH time	Normal, ListenOnly or Standby mode	100	-	-	ns
$t_{clk(L)}$	clock LOW time	Normal, ListeOnly or Standby mode	100	-	-	ns
$t_{r(clk)}$	clock rise time	Normal, ListenOnly or Standby mode; 10 % to 90 %	-	-	20	ns
$t_{f(clk)}$	clock fall time	Normal, ListenOnly or Standby mode; 90 % to 10 %	-	-	20	ns
$t_{su(D)}$	data input set-up time	Normal, ListenOnly or Standby mode	50	-	-	ns
$t_{h(D)}$	data input hold time	Normal, ListenOnly or Standby mode	50	-	-	ns
$t_{v(Q)}$	data output valid time	C_L = 30 pF; Normal, ListenOnly or Standby mode; pin SDO	-	-	50	ns
$t_{d(SDI-SDO)}$	SDI to SDO delay time	C_L = 30 pF; Normal, ListenOnly or Standby mode; SPI address bits and read-only bit; pin SDO	-	-	50	ns
$t_{WH(S)}$	chip select pulse width HIGH	Normal, ListenOnly or Standby mode	250	-	-	ns

Table 58. Dynamic characteristics...*continued*

T_{vj} = -40 °C to +150 °C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 1.71 V to 5.5 V; V_{BAT} = 4.75 V to 40 V; R_L = 60 Ω unless specified otherwise; all voltages are defined with respect to ground.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(SCKL-SCSNL)}$	delay time from SCK LOW to SCSN LOW	Normal, ListenOnly or Standby mode; pin SCSN	50	-	-	ns
$t_{to(SPI)}$[8]	SPI time-out time	[5]	1.6	-	2.4	ms
CAN partial networking						
$N_{bit(idle)}$[7]	number of idle bits	before a SOF is accepted [2]	6	-	10	-
$t_{fltr(bit)dom}$	dominant bit filter time	arbitration bit rate ≤ 500 kbit/s; IDFS = 0x0 [2] [9]	5	-	17.5	%
		ISO bitfilter 1; IDFS = 0x1 [2] [9]	5	-	17.5	%
		ISO bitfilter 2; IDFS = 0x2 [2]	2.5	-	8.75	%
		IDFS = 0x3 [2]	18	-	93	ns
		IDFS = 0x4 [2]	42	-	119	ns
		IDFS = 0x5 [2]	67	-	145	ns
		IDFS = 0x6 [2]	91	-	170	ns
General purpose I/Os; pins GPIOx						
t_{fltr}	filter time	pin configured as input except for GPIOxFS = 0x03 (TXEN_N input) and GPIO2FS = 0x05 or 0x07 (TXD2 input) [10]	1	-	21	µs
		pin configured as TXEN_N input with GPIOxFS = 0x03 [10]	1	-	5	µs
$t_{w(min)}$	minimum pulse width	pin configured as output except when RXD2 option is selected for GPIO1 [2]	3	-	-	µs
Reset input/output; pin RST_N						
$t_{fltr(rst)}$	reset filter time	for externally triggered reset [10]	1	-	21	µs
$t_{d(rst)}$	reset delay time	internaly generated reset: pin held LOW for $t_{d(rst)}$ [2] [11]	1.8	-	2.2	ms
$t_{to(rst)}$	reset timeout time	[2] [5]	110	125	140	ms
$t_{rel(rst)}$	reset release time	[2] [12]	10	-	35	µs
Mode transitions; see Section 7.2, Figure 6 and Figure 7						
$t_{t(moch)}$	mode change transition time	[2]	-	-	50	µs
$t_{startup}$	start-up time	from V_{BAT} > $V_{uvd(VBAT)}$ for t > $t_{rec(uv)VBAT}$ until BOOT_OK [2]	-	-	1	ms
$t_{startup(RXD)}$	RXD start-up time	after local or remote wake-up detected [2] [13]	0	-	20	µs

Table 58. Dynamic characteristics...*continued*

T_{vj} = -40 °C to +150 °C; V_{CC} = 4.5 V to 5.5 V; V_{IO} = 1.71 V to 5.5 V; V_{BAT} = 4.75 V to 40 V; R_L = 60 Ω unless specified otherwise; all voltages are defined with respect to ground.[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{startup(INH)}$	INH start-up time	after local or remote wake-up detected; transition from Sleep to Standby [2] [14]	0	-	40	µs
$t_{t(snm)}$	SNM transition time	bus dominant time for Start-to-Normal mode boot [2] [15]	11	-	16	ms
Local wake-up input; pin WAKE, see Section 7.2.2 and Table 44						
t_{wake}	wake-up time	in response to a falling or rising edge on pin WAKE; Standby or Sleep mode [16]				
		short wake-up time: WFC = 0 [2]	20	-	50	µs
		long wake-up time: WFC = 1 [2]	12	-	18	ms
Undervoltage detection; see Table 7, Table 11 and Table 13[2]						
$t_{det(uv)}$	undervoltage detection time	≥ 100 mV input overdrive				
		on pin VBAT	-	-	30	µs
		on pin VCC	-	-	36	µs
		on pin VIO	-	-	51	µs
$t_{rec(uv)}$	undervoltage recovery time	≥ 100 mV input overdrive				
		on pin VBAT	-	-	50	µs
		on pin VCC	-	-	56	µs
		on pin VIO	-	-	46	µs
Overvoltage detection on pin VIO; ≥ 100 mV input overdrive; see Table 11[2]						
$t_{det(ov)}$	overvoltage detection time		-	-	86	µs
$t_{det(ov)long}$	long overvoltage detection time	[17]	150	200	250	µs
$t_{rec(ov)}$	overvoltage recovery time		-	-	77	µs
Limp/fail-safe output; pin LIMPFSO_N						
$t_{d(fdet-LF\_NL)}$	delay time from failure detection to LIMPFSO_N LOW	from detection of failure event to $V_{LIMPFSO\_N}$ falling to 10 % of V_{BAT}; 22 kΩ pull-up to V_{BAT} [2] [18]	7	12	14	µs

[1] All parameters are guaranteed over the junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage ranges.
[2] Not tested in production; guaranteed by design.
[3] If TXD goes LOW before the recessive transition has been completed, the bus switches to dominant.
[4] Compliance with parameter set C requirements implies compliance for parameter sets A ($t_{bit(TXD)}$ ≥ 500 ns, up to 2 Mbit/s) and B ($t_{bit(TXD)}$ ≥ 200 ns, up to 5 Mbit/s).
[5] Time-out occurs between the min and max values. Time-out is guaranteed not to occur below the min value; time-out is guaranteed to occur above the max value.
[6] A dominant/recessive phase shorter than the min value is guaranteed not be seen as a dominant/recessive bit; a dominant/recessive phase longer than the max value is guaranteed to be seen as a dominant/recessive bit.
[7] As specified in ISO 11898-2:024.
[8] See Section 7.12.1.
[9] Up to 2 Mbit/s data bit rate.
[10] Pulses shorter than the min value are guaranteed to be filtered out; pulses longer than the max value are guaranteed to be processed.
[11] RST_N is held LOW for a time between the min and max values. It's guaranteed not be held LOW before the min time and after the max time.

[12] The reset is released at a time between min and max values. It is guaranteed not to be released before the min time, and guaranteed to be released after the max time.
[13] When a wake-up is detected, RXD start-up time is between the min and max values. RXD cannot be relied on below the min value; RXD can be relied on above the max value; see Figure 6 and Figure 7.
[14] INH switches HIGH between the min and max values after a wake-up had been detected. INH is guaranteed to be floating below the min value and guaranteed to be HIGH above the max value; see Figure 6 and Figure 7.
[15] The transition occurs between the min and max times. The transition is guaranteed not to occur below the min value; the transition is guaranteed to occur above the max value.
[16] Wake-up occurs between min and max values. Wake-up is guaranteed not to occur below the min value; wake-up is guaranteed to occur above the max value.
[17] A long overvoltage will not be detected before the min time has elapsed, but will be detected, at the latest, by the time the max time has elapsed.
[18] LIMPFSO_N is guaranteed not to go LOW before the min value and guaranteed to be LOW after the max value.

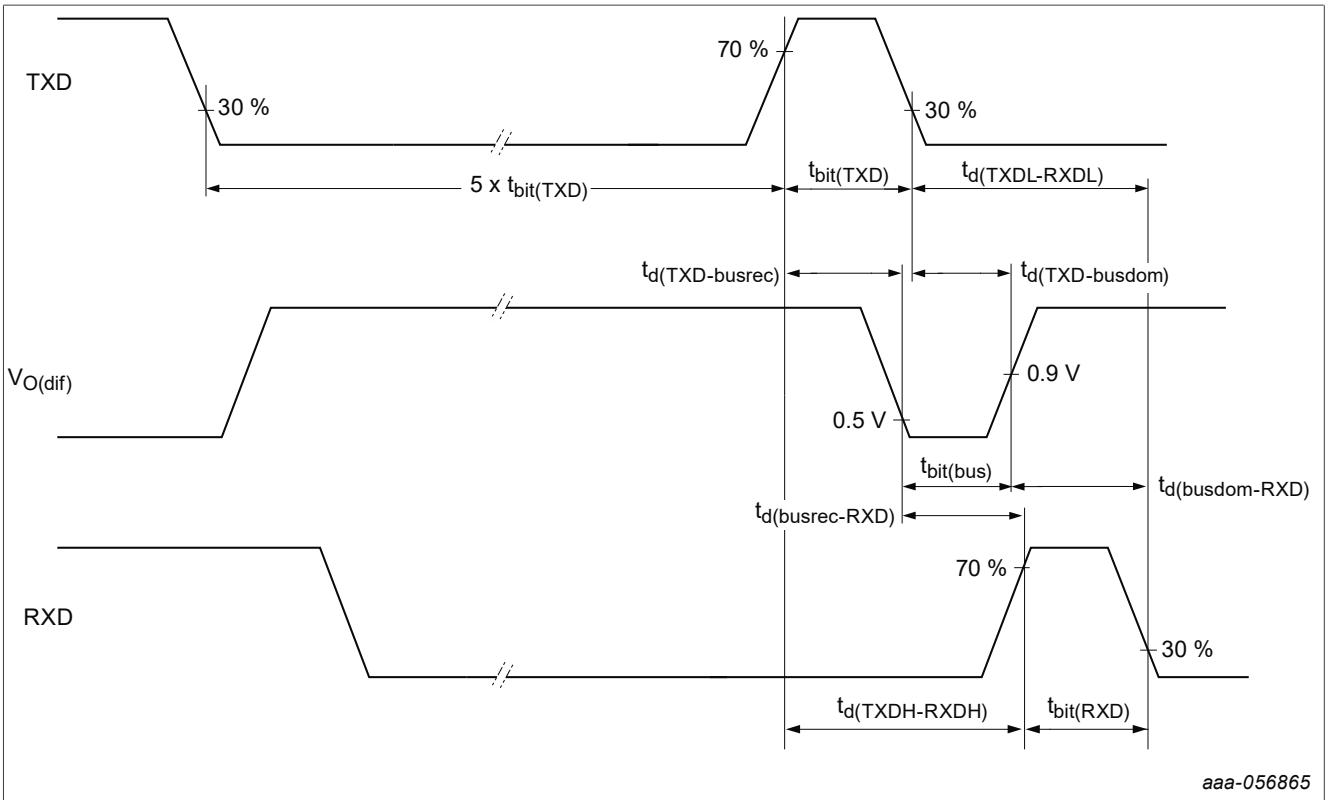
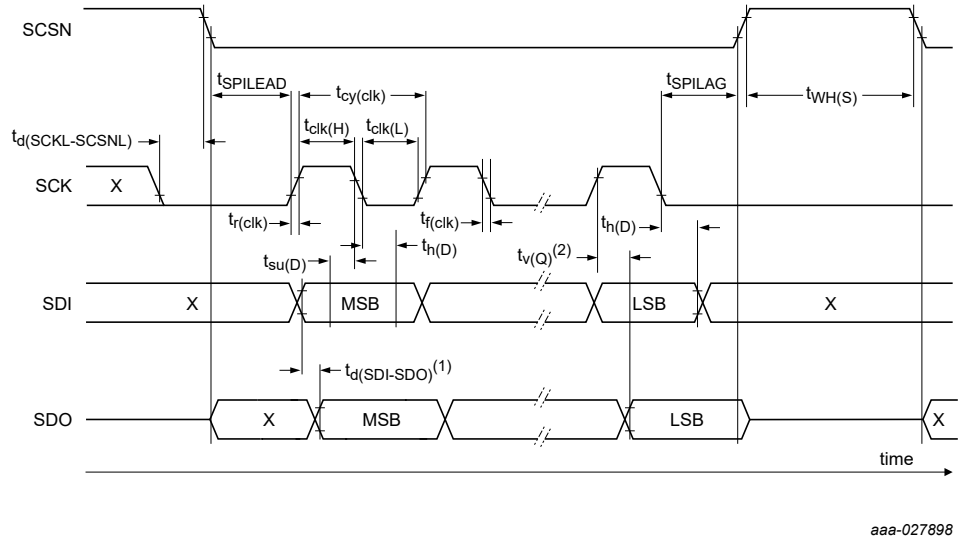


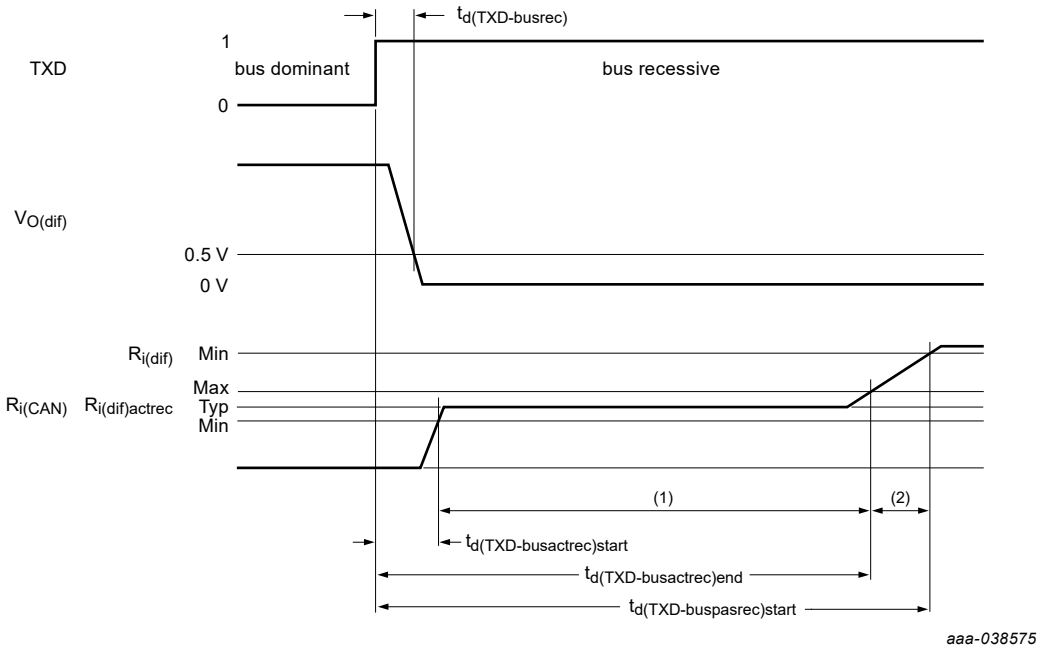
Figure 12. CAN transceiver timing diagram according to ISO 11898-2:2024



(1) The SDI to SDO delay time is valid for SPI address bits and the read-only bit.

(2) The data output valid time is valid for the SPI data bits.

Figure 13. SPI timing diagram



(1) Active recessive phase (2) Slow release phase.

Figure 14. Transmitter impedance and timing diagram for dominant-to-passive recessive transition according to ISO 11898-2:2024 parameter set C

12 Application information

An example 12 V application with components typically used with the TJA1466 is shown in Figure 15. See the application hints (Section 12.2) for further information about external components and PCB layout requirements.

12.1 Application diagram

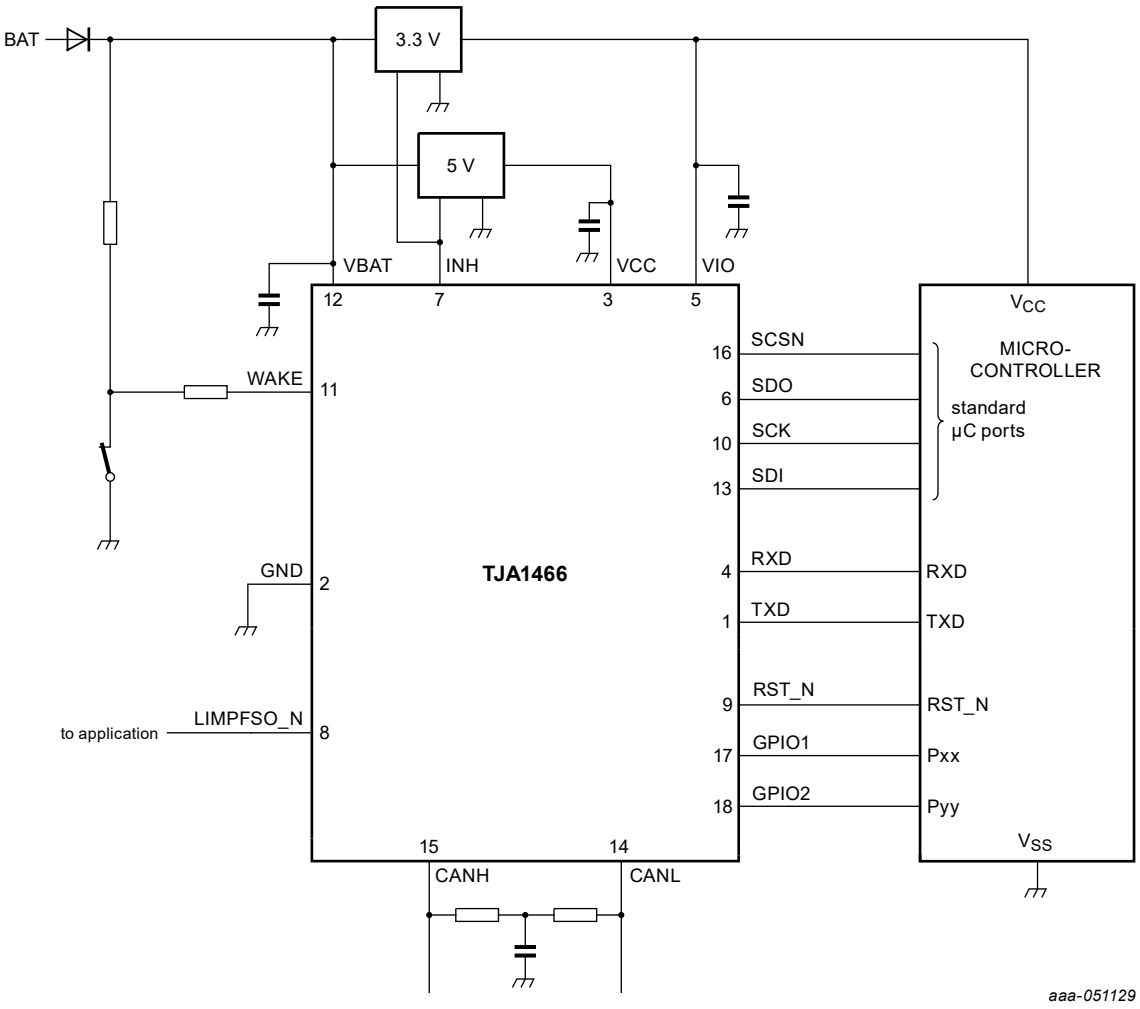


Figure 15. Typical TJA1466 application with a 3.3 V microcontroller

12.2 Application notes

Further information on the application of the TJA1466 can be found in NXP application notes AN14452 '*TJA1446, TJA1466 application note*', available on request from NXP Semiconductors.

13 Test information

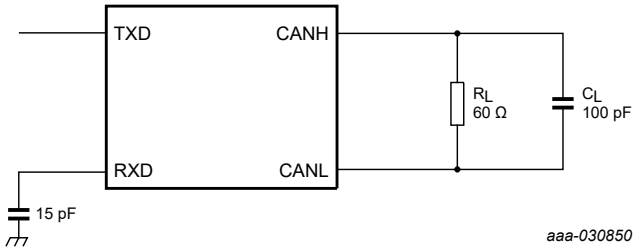


Figure 16. CAN transceiver timing test circuit

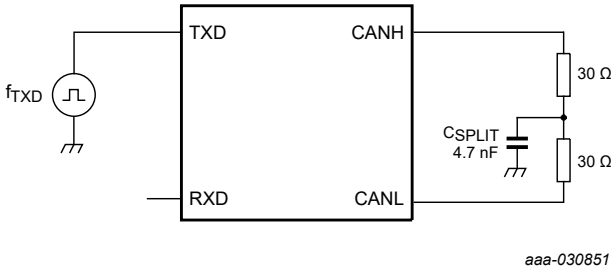


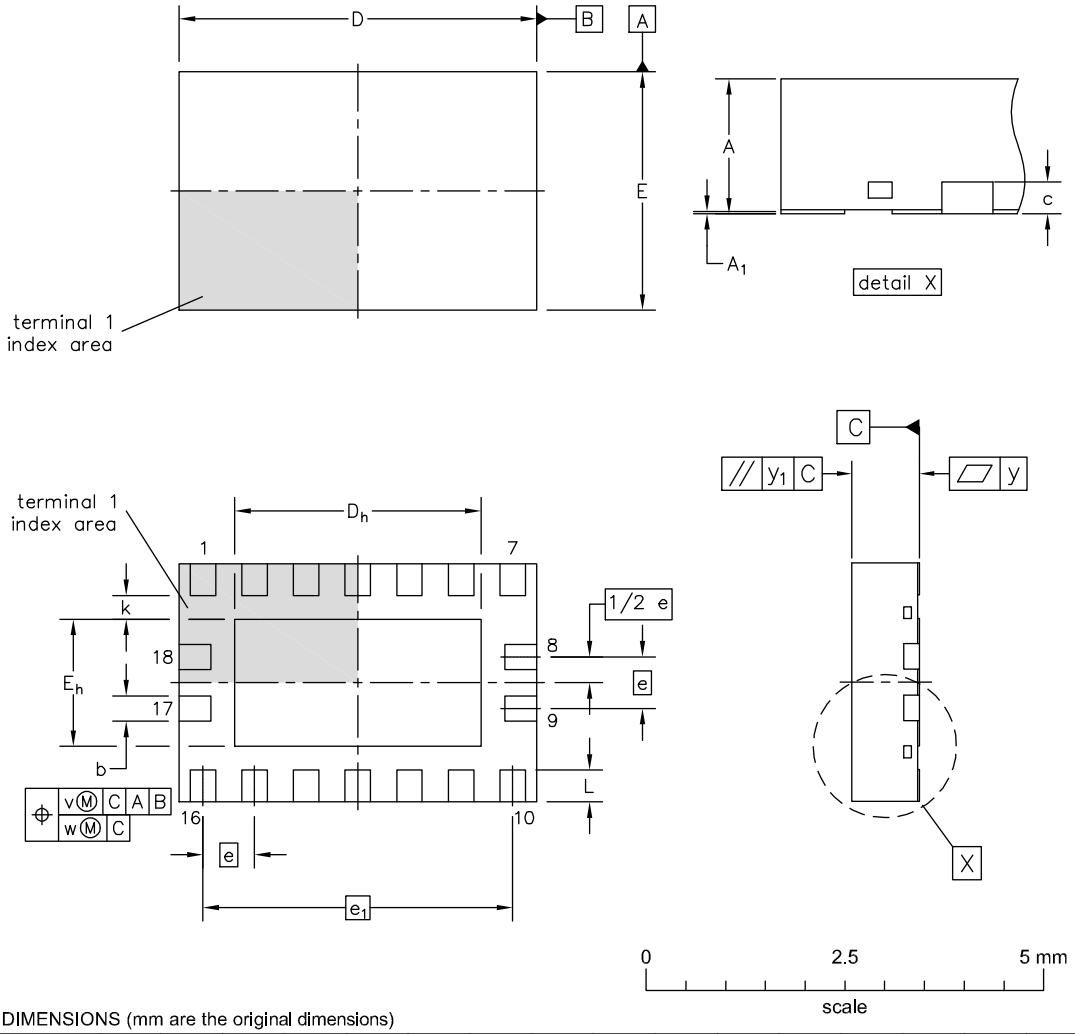
Figure 17. Test circuit for measuring transceiver driver symmetry

13.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 Rev-H - Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

14 Package outline

DHVQFN18: plastic dual in−line compatible thermal enhanced very thin quad flat package; no leads; 18 terminals; body 3.0 x 4.5 x 0.85 mm SOT2163−1



DIMENSIONS (mm are the original dimensions)

Unit[1]	A	A_1	b	c	D	D_h	E	E_h	e	e_1	k	L	v	w	y	y_1
max	1.00	0.05	0.35		4.60	3.15	3.10	1.65			0.35	0.45				
mm nom	0.85	0.03	0.32	0.20	4.50	3.10	3.00	1.60	0.65	3.90	0.30	0.40	0.10	0.05	0.05	0.10
min	0.80	0.00	0.29		4.40	3.05	2.90	1.55			0.25	0.35				

Note
1.Plastic or metal protusions of 0.075 mm maximum per side are not included.

DATE: 06 DEC 2022

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01851D	REVISION: O	

Figure 18. Package outline SOT2163-1 (DHVQFN18)

15 Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

16 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 “Surface mount reflow soldering description”*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 19) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 59 and Table 60

Table 59. SnPb eutectic process (from J-STD-020D)

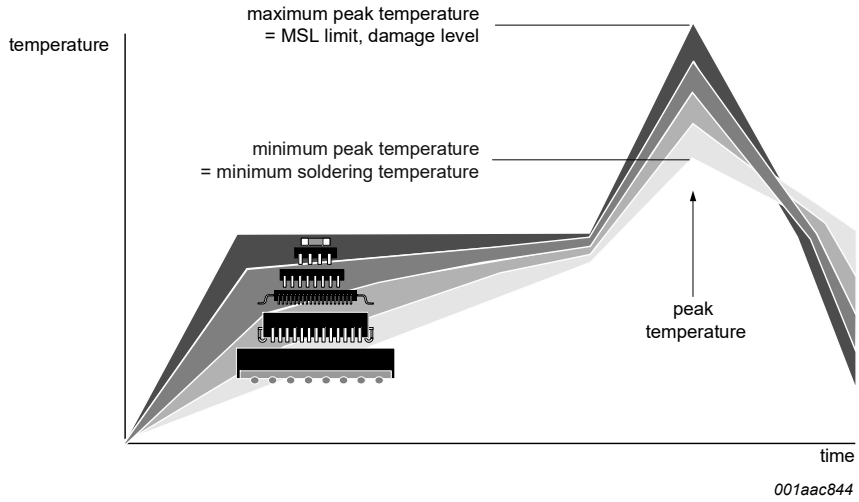
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 60. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 19.



MSL: Moisture Sensitivity Level

Figure 19. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

17 Appendix: ISO 11898-2:2024 parameter cross-reference lists

Table 61. ISO 11898-2:2024 to NXP data sheet parameter conversion[1]

ISO 11898-2:2024		NXP data sheet	
Parameter	**Notation**	**Symbol**	**Parameter**
HS-PMA maximum ratings of V_{CAN_H}, V_{CAN_L} and V_{Diff}			
Maximum rating	V_{Diff}	$V_{(CANH-CANL)}$	voltage between pin CANH and pin CANL
General maximum rating	V_{CAN_H} V_{CAN_L}	V_x	voltage on pin x
Optional: Extended maximum rating			
HS-PMA recessive output characteristics, bus biasing active/inactive			
Single ended output voltage on CAN_H	V_{CAN_H}	$V_{O(rec)}$	recessive output voltage
Single ended output voltage on CAN_L	V_{CAN_L}		
Differential output voltage	V_{Diff}	$V_{O(dif)}$	differential output voltage
HS-PMA dominant output characteristics			
Single ended voltage on CAN_H	V_{CAN_H}	$V_{O(dom)}$	dominant output voltage
Single ended voltage on CAN_L	V_{CAN_L}		
Differential voltage on normal bus load	V_{Diff}	$V_{O(dif)}$	differential output voltage
Differential voltage on effective resistance during arbitration			
Optional: Differential voltage on extended bus load range			
Maximum HS-PMA driver output current			
Absolute current on CAN_H	I_{CAN_H}	$I_{O(sc)}$	short-circuit output current
Absolute current on CAN_L	I_{CAN_L}		
HS-PMA static receiver input characteristics, bus biasing active/inactive			
Recessive state differential input voltage range Dominant state differential input voltage range	V_{Diff}	$V_{th(RX)dif}$	differential receiver threshold voltage
		$V_{rec(RX)}$	receiver recessive voltage
		$V_{dom(RX)}$	receiver dominant voltage
HS-PMA receiver input resistance (matching)			
Differential internal resistance	$R_{DIFF\_pas\_rec}$	$R_{i(dif)}$	differential input resistance
Single-ended internal resistance	$R_{SE\_pas\_rec\_H}$ $R_{SE\_pas\_rec\_L}$	R_i	input resistance
Matching of internal resistance	m_R	ΔR_i	input resistance deviation
HS-PMA maximum leakage currents on CAN_H and CAN_L, unpowered			
Leakage current on CAN_H, CAN_L	I_{CAN_H} I_{CAN_L}	I_L	leakage current
HS-PMA driver symmetry			
Driver symmetry	V_{sym_vcc}	V_{TXsym}	transmitter voltage symmetry
Optional HS-PMA transmit dominant time-out			
Transmit dominant time-out	t_{dom}	$t_{to(dom)TXD}$	TXD dominant time-out time

Table 61. ISO 11898-2:2024 to NXP data sheet parameter conversion[1]*...continued*

ISO 11898-2:2024		NXP data sheet	
Parameter	**Notation**	**Symbol**	**Parameter**
HS-PMA implementation loop delay requirements for parameter sets A, B and C			
Loop delay for parameter sets A and B	t_{Loop}	$t_{d(TXDH-RXDH)}$	delay time from TXD HIGH to RXD HIGH
Loop delay for parameter set C		$t_{d(TXDL-RXDL)}$	delay time from TXD LOW to RXD LOW
Propagation delay from TXD to CAN_H/CAN_L for parameter set C	$t_{prop(TXD\_BUS)}$	$t_{d(TXD-busdom)}$	delay time from TXD to bus dominant
		$t_{d(TXD-busrec)}$	delay time from TXD to bus recessive
Propagation delay from CAN_H/CAN_L to RXD for parameter set C	$t_{prop(BUS\_RXD)}$	$t_{d(busdom-RXD)}$	delay time from bus dominent to RXD
		$t_{d(busrec-RXD)}$	delay time from bus recessive to RXD
HS-PMA implementation data signal timing requirements for parameter sets A, B and C			
Transmitted recessive bit width variation	$t_{\Delta Bit(Bus)}$	$\Delta t_{bit(bus)}$	transmitted recessive bit width deviation
Received recessive bit width variation	$t_{\Delta Bit(RXD)}$	$\Delta t_{bit(RXD)}$	received recessive bit width deviation
Receiver timing symmetry	$t_{\Delta REC}$	Δt_{rec}	receiver timing symmetry
HS-PMA implementation SIC timing and impedance for parameter set C			
Differential internal resistance (CAN_H to CAN_L)	$R_{DIFF\_act\_rec}$	$R_{i(dif)actrec}$	active recessive phase differential input resistance
Internal single-ended resistance	$R_{SE\_act\_rec}$	$R_{i(actrec)}$	active recessive phase input resistance
Start time of active signal improvement phase	$t_{act\_rec\_start}$	$t_{d(TXD-busactrec)start}$	delay time from TXD to bus active recessive start
End time of active signal improvement phase	$t_{act\_rec\_end}$	$t_{d(TXD-busactrec)end}$	delay time from TXD to bus active recessive end
Start time of passive recessive phase	$t_{pas\_rec\_start}$	$t_{d(TXD-buspasrec)start}$	delay time from TXD to bus passive recessive start
PMA voltage wake-up control timing			
CAN activity filter time, long/short	t_{Filter}	$t_{wake(busdom)}$ $t_{wake(busrec)}$	bus dominant wake-up time bus recessive wake-up time
Wake-up time-out	t_{Wake}	$t_{to(wake)bus}$	bus wake-up time-out time
Wake-up pattern signaling	t_{Flag}	$t_{startup(RXD)}$	RXD start-up time
		$t_{startup(INH)}$	INH start-up time
		$t_{startup(ERR\_N)}$	ERR_N start-up time
Number of recessive bits before next SOF			
Number of recessive bits before a new SOF shall be accepted	n_{Bits_idle}	$N_{bit(idle)}$	number of idle bits before a SOF is accepted
BitFilter in CAN FD data phase			
CAN FD data phase bitfilter (option 1)	$\rho_{Bitfilter\_option1}$	$t_{fltr(bit)dom}$	dominant bit filter time
CAN FD data phase bitfilter (option 2)	$\rho_{Bitfilter\_option2}$		
HS-PMA bus biasing control timing			
Time-out for bus inactivity	$t_{Silence}$	$t_{to(silence)}$	bus silence time-out time
Bus bias reaction time	t_{Bias}	$t_{d(busact-bias)}$	bus bias reaction time

[1] A number of proprietary NXP parameters are equivalent to parameters defined in ISO 11898-2:2024, but use different symbols. This conversion table allows ISO parameters to be cross-referenced with their NXP counterparts. The NXP parameters are defined in the Static and Dynamic characteristics tables. The conversion table provides a comprehensive listing - individual devices may not include all parameters.

18 Appendix: TJA1445x/TJA1446x/TJA1465x/TJA1466x family overview

Table 62. Feature overview of the the complete TJA1445x/TJA1446x/TJA1465x/TJA1466x family.

	Partial Networking			V_{IO} supply			Data rate		Special features							
Device	Selective wake-up	CAN FD passive	CAN XL passive	1.8 V V_{IO}	3.3 V V_{IO}	5.0 V V_{IO}	Up to 5 Mbit/s CAN FD	Up to 8 Mbit/s CAN SIC	ISO 26262 ASIL B compliance	GPIO pins	TXEN_N pin	RST_N pin	FSO/LIMP pin	V_{IO} undervoltage monitoring	V_{IO} overvoltage monitoring	Q&A watchdog
TJA1445A	●	●		●	●	●	●		●					●		
TJA1445B	●	●		●	●	●	●		●	3	●			●		
TJA1446A	●	●		●			●		●	2		●	●	●	●	●
TJA1446B	●	●			●		●		●	2		●	●	●	●	●
TJA1446C	●	●				●	●		●	2		●	●	●	●	●
TJA1465A	●	●	●	●	●	●	●	●	●					●		
TJA1465B	●	●	●	●	●	●	●	●	●	3	●			●		
TJA1466A	●	●	●	●			●	●	●	2		●	●	●	●	●
TJA1466B	●	●	●		●		●	●	●	2		●	●	●	●	●
TJA1466C	●	●	●			●	●	●	●	2		●	●	●	●	●

19 Revision history

Table 63. Revision history

Document ID	Release date	Description
TJA1466 v.1.0	16 October 2024	Initial version

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

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