



# TEA1792T

## GreenChip synchronous rectifier controller

Rev. 2 — 9 July 2012

Product data sheet

## 1. General description

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The TEA1792T is a member of the new generation of Synchronous Rectifier (SR) controller ICs for switched mode power supplies. Its high level of integration allows the design of a cost-effective power supply with a very low number of external components.

The TEA1792T is a controller IC dedicated to synchronous rectification on the secondary side of discontinuous conduction mode and quasi-resonant flyback converters.

The TEA1792T is fabricated in a Silicon-On-Insulator (SOI) process.

## 2. Features and benefits

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### 2.1 Distinctive features

- Accurate synchronous rectification functionality
- Wide supply voltage range (8.5 V to 38 V)
- High level of integration, resulting in a very low external component count
- High driver output voltage of 10 V to drive all MOSFET brands to the lowest  $R_{DSon}$
- Selectable regulation level for driver stage

### 2.2 Green features

- Low current consumption
- High system efficiency from no load to full load

### 2.3 Protection features

- UnderVoltage Protection (UVP)

## 3. Applications

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- The TEA1792T is intended for adapters. The device can also be used in all other discontinuous conduction mode systems and quasi-resonant flyback systems that demand a highly efficient and cost-effective solution.

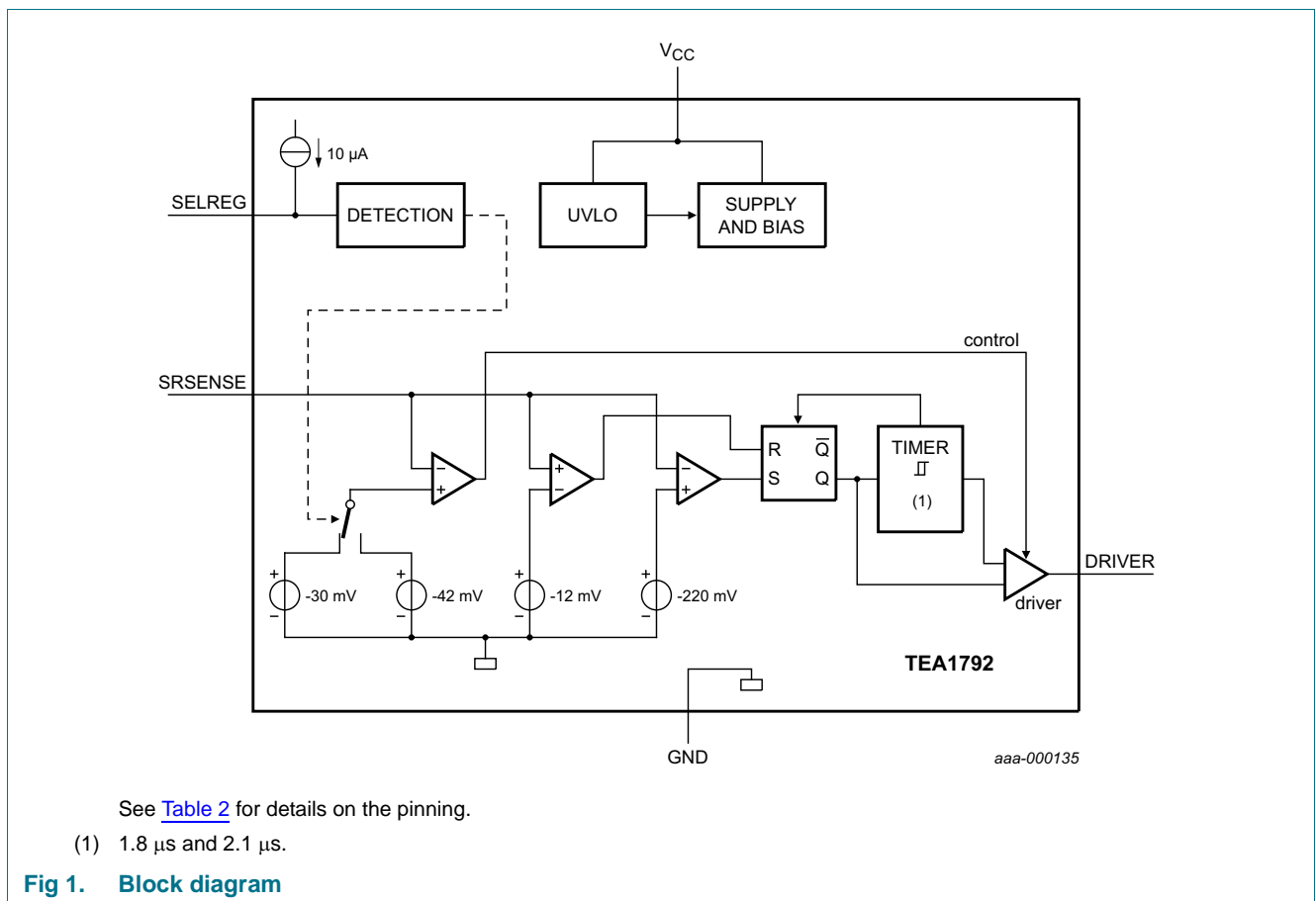


### 4. Ordering information

Table 1. Ordering information

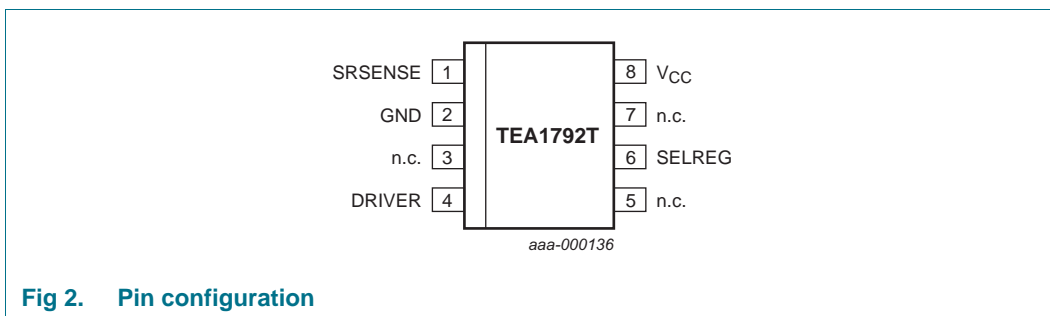
| Type number | Package |   | Version |
|-------------|---------|---|---------|
|             | Name    | Description   |         |
| TEA1792T/N1 | SO8     | plastic small outline package; 8 leads; body width 3.9 mm | SOT96-1 |

### 5. Block diagram



## 6. Pinning information

### 6.1 Pinning



### 6.2 Pin description

Table 2. Pin description

| Symbol          | Pin | Description                                 |
|-----------------|-----|---|
| SRSENSE         | 1   | synchronous timing input                    |
| GND             | 2   | ground                                      |
| n.c.            | 3   | not connected                               |
| DRIVER          | 4   | driver output for SR MOSFET                 |
| n.c.            | 5   | not connected                               |
| SELREG          | 6   | selection input for driver regulation level |
| n.c.            | 7   | not connected                               |
| V <sub>CC</sub> | 8   | supply voltage                              |

## 7. Functional description

### 7.1 Introduction

The TEA1792T is the controller for synchronous rectification used in discontinuous conduction mode and quasi-resonant flyback converters.

### 7.2 Start-up and UnderVoltage LockOut (UVLO)

The IC leaves the undervoltage lockout state and activates the synchronous rectifier circuitry when the voltage on the  $V_{CC}$  pin is above 8.5 V (typical). When the voltage drops below 8.0 V (typical), the undervoltage lockout state is entered again and the SR driver output is actively kept low.

### 7.3 Synchronous rectification

After a negative voltage lower than  $V_{act(drv)}$  (–220 mV typical) is sensed on the SRSENSE pin, the driver output voltage is driven HIGH. Then the external MOSFET is switched on. When the SRSENSE voltage rises to  $V_{reg(drv)}$  (–42 mV/–30 mV), the driver output voltage is regulated to maintain the  $V_{reg(drv)}$  on the SRSENSE pin. When the SRSENSE voltage is above the  $V_{deact(drv)}$  level (–12 mV typical), the driver output is pulled to ground.

After switch-on of the SR MOSFET, the input signal on the SRSENSE pin is blanked during the  $t_{act(sr)(min)}$  (1.8  $\mu$ s typical). This action eliminates false switch-off due to high frequency ringing at the start of the secondary stroke.

When the voltage on the SRSENSE pin is  $V_{reg(drv)}$ , the driver output voltage is reduced. This reduction enables the external power switch to be switched off quickly when the current through the switch reaches zero. The zero current switch-off removes the need for a separate Standby mode to maintain high efficiency during the no-load operation. The zero current is detected by sensing a  $V_{deact(drv)}$  (–12 mV typical) level on the SRSENSE pin (see [Figure 3](#)).

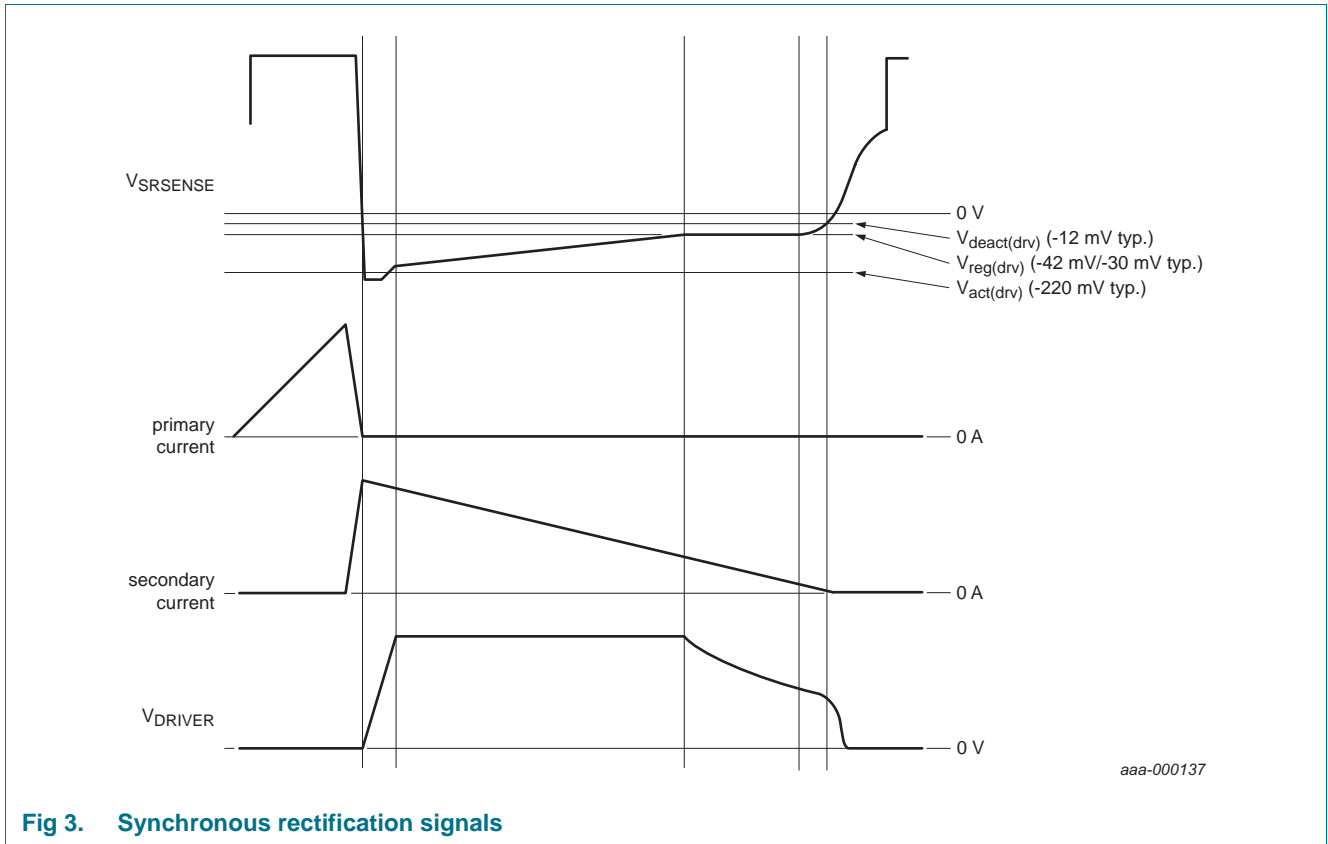


Fig 3. Synchronous rectification signals

The level of the driver regulation voltage  $V_{reg(drv)}$  can be selected using the SELREG pin. When this SELREG pin is grounded, the typical  $V_{reg(drv)}$  equals  $-42\text{ mV}$ . When the SELREG pin is left open, the  $V_{reg(drv)}$  level equals  $-30\text{ mV}$ .

Internally, the SELREG pin has a pull-up current source of  $10\text{ }\mu\text{A}$ . When this pin is short circuited to ground, the pin selects the lowest  $V_{reg(drv)}$ . If the pin is left open, the highest  $V_{reg(drv)}$  value is selected.

If the secondary stroke of the flyback converter is shorter than  $t_{act(sr)(min)}$  short time ( $1.8\text{ }\mu\text{s}$  typical), the driver output is disabled. This action guarantees stable operation for very low duty cycles. When the secondary stroke increases above  $t_{act(sr)(min)}$ , long time ( $2.1\text{ }\mu\text{s}$  typical), the driver output is again enabled.

### 7.4 Supply management

All internal reference voltages are derived from a temperature compensated, on-chip band gap circuit.

### 7.5 Driver

The driver circuit to the external power MOSFET gate has a typical source capability of  $400\text{ mA}$  and a typical sink capability of  $2.7\text{ A}$ . These capabilities permit fast switch-on and switch-off of the power MOSFET for efficient operation. The source stage is coupled to the timer (see [Figure 1](#)). When the timer has finished, the source capability is reduced to a small current ( $5\text{ mA}$  typical) capable of keeping the driver output voltage at its level.

The output voltage of the driver is limited to 10 V (typical). This high output voltage drives all MOSFET brands to the minimum on-state resistance.

During start-up conditions ( $V_{CC} < V_{\text{startup}}$ ) and undervoltage lockout the driver output voltage is actively pulled low.

## 8. Limiting values

**Table 3. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are measured with respect to ground (pin 2); positive currents flow into the chip. The voltage ratings and current ratings are valid provided the other ratings are not violated.*

| Symbol          | Parameter                       | Conditions                                    | Min  | Max  | Unit |    |
|-----------------|---------------------------------|---|------|------|------|----|
| <b>Voltages</b> |                                 |   |      |      |      |    |
| $V_{CC}$        | supply voltage                  | continuous                                    | -0.4 | +38  | V    |    |
| $V_{SRSENSE}$   | voltage on pin SRSENSE          | continuous                                    | -    | 120  | V    |    |
| $V_{SELREG}$    | voltage on pin SELREG           | continuous                                    | -0.4 | +5   | V    |    |
| <b>Currents</b> |                                 |   |      |      |      |    |
| $I_{DRIVER}$    | current on pin DRIVER           | duty cycle < 10 %                             | -0.8 | +3   | A    |    |
| $I_{SRSENSE}$   | current on pin SRSENSE          |   | -3   | -    | mA   |    |
| <b>General</b>  |                                 |   |      |      |      |    |
| $P_{tot}$       | total power dissipation         | $T_{amb} < 80\text{ °C}$                      | -    | 0.45 | W    |    |
| $T_{stg}$       | storage temperature             |   | -55  | +150 | °C   |    |
| $T_j$           | junction temperature            |   | -40  | +150 | °C   |    |
| $V_{ESD}$       | electrostatic discharge voltage | human body model; JEDEC Class 2; all pins     | [1]  | -2   | +2   | kV |
|                 |                                 | charged device model; JEDEC Class 3; all pins |      | -500 | +500 | V  |

[1] Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

## 9. Thermal characteristics

**Table 4. Thermal characteristics**

| Symbol        | Parameter                                   | Conditions       | Typ | Unit |
|---------------|---|------------------|-----|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | JEDEC test board | 157 | K/W  |
| $R_{th(j-c)}$ | thermal resistance from junction to case    | JEDEC test board | 90  | K/W  |

## 10. Characteristics

**Table 5. Characteristics**

$T_{amb} = 25\text{ °C}$ ;  $V_{CC} = 20\text{ V}$ ; all voltages are measured with respect to ground (pin 2); currents are positive when flowing into the IC; unless otherwise specified.

| Symbol   | Parameter                                     | Conditions  | Min      | Typ  | Max   | Unit    |
|--|---|---|----------|------|-------|---------|
| <b>Supply voltage management (pin V<sub>CC</sub>)</b>      |   |   |          |      |       |         |
| $V_{startup}$  | start-up voltage                              |   | 8.2      | 8.5  | 8.8   | V       |
| $V_{hys}$  | hysteresis voltage                            |   | [1] 0.35 | 0.5  | 0.65  | V       |
| $I_{CC(oper)}$   | operating supply current                      | $V_{CC} = 8\text{ V}$ ( $V_{CC} < V_{startup}$ )        | 0.2      | 0.25 | 0.4   | mA      |
|  |   | under normal operation; no load on pin DRIVER           | 0.8      | 1    | 1.2   | mA      |
| <b>Synchronous rectification sense input (pin SRSENSE)</b> |   |   |          |      |       |         |
| $V_{act(drv)}$   | driver activation voltage                     |   | -260     | -220 | -180  | mV      |
| $V_{reg(drv)}$   | driver regulation voltage                     | resistance between pins SELREG and GND < 15 k $\Omega$  | -55      | -42  | -30   | mV      |
|  |   | resistance between pins SELREG and GND > 700 k $\Omega$ | -38      | -30  | -22   | mV      |
| $V_{deact(drv)}$   | driver deactivation voltage                   |   | -        | -12  | -     | mV      |
| $t_{d(act)(drv)}$  | driver activation delay time                  |   | 50       | 75   | 100   | ns      |
| $t_{act(sr)(min)}$   | minimum synchronous rectification active time | short time  | 1.3      | 1.8  | 2.3   | $\mu$ s |
|  |   | long time   | 1.6      | 2.1  | 2.6   | $\mu$ s |
| $I_{o(SELREG)}$  | output current on pin SELREG                  | $V_{SELREG} = 2.5\text{ V}$                             | -12      | -10  | -8    | $\mu$ A |
| <b>Driver (pin DRIVER)</b>                                 |   |   |          |      |       |         |
| $I_{source}$   | source current                                | $V_{CC} = 15\text{ V}$ ; voltage on pin DRIVER = 2 V    |          |      |       |         |
|  |   | during minimum synchronous rectification time           | -0.45    | -0.4 | -0.35 | A       |
|  |   | minimum synchronous rectification time has ended        | -6       | -5   | -4    | mA      |
| $I_{sink}$   | sink current                                  | $V_{CC} = 15\text{ V}$                                  |          |      |       |         |
|  |   | voltage on pin DRIVER = 2 V                             | 1        | 1.4  | -     | A       |
|  |   | voltage on pin DRIVER = 9.5 V                           | 2.2      | 2.7  | -     | A       |
| $V_{o(max)}$   | maximum output voltage                        | $V_{CC} = 15\text{ V}$                                  | 9        | 10   | 12    | V       |

[1] The  $V_{CC}$  stop voltage is  $V_{startup} - V_{hys}$ .

### 11. Application information

A switched mode power supply with the TEA1792T consists of a primary side discontinuous conduction mode flyback controller, a transformer and an output stage with a feedback circuit. A MOSFET ( $Q_{sec}$ ) is used for low conduction losses in the output state. The TEA1792T controls this MOSFET.

The timing for the synchronous rectifier switch is derived from the voltage sensed on the SRSENSE pin. The resistor in the SRSENSE connection protects the TEA1792T from excessive voltages. The  $R_{SRSENSE}$  resistor is typically 1 k $\Omega$ . Higher values can impair correct timing, lower values do not provide sufficient protection.

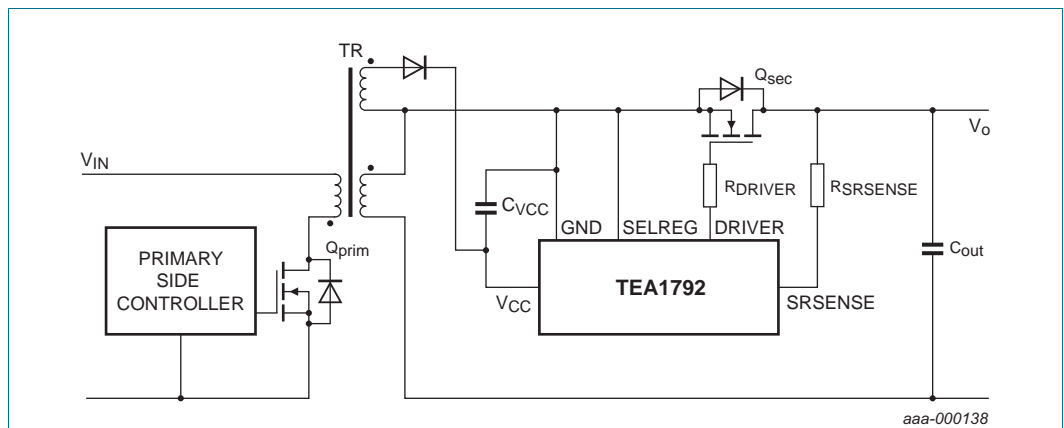


Fig 4. Application diagram high side rectification

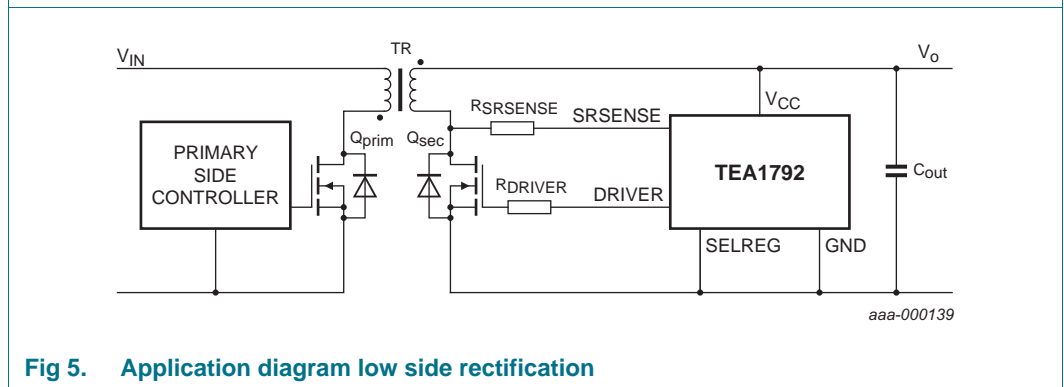


Fig 5. Application diagram low side rectification



12. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

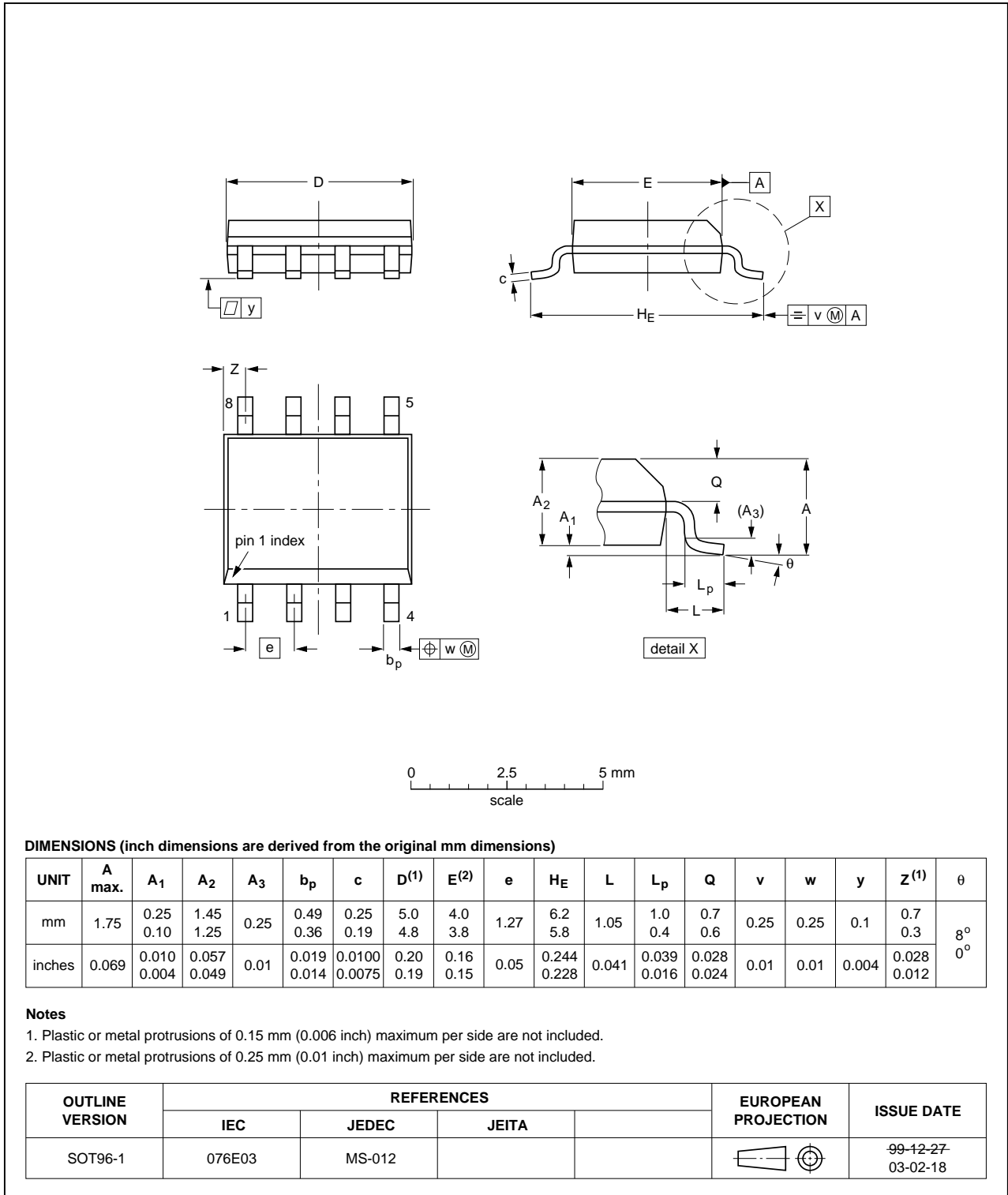


Fig 6. Package outline SOT96-1 (SO8)

## 13. Revision history

Table 6. Revision history

| Document ID    | Release date | Data sheet status    | Change notice | Supersedes     |
|----------------|--------------|----------------------|---------------|----------------|
| TEA1792T v.2   | 20120709     | Product data sheet   | -             | TEA1792T v.1.1 |
| TEA1792T v.1.1 | 20120126     | Objective data sheet | -             | TEA1792T v.1   |
| TEA1792T v.1   | 20110816     | Objective data sheet | -             | -              |

## 14. Legal information

### 14.1 Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition  |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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