

# OL2300

## Fractional-N PLL based transmitter

Rev. 2 — 28 October 2010

Product data sheet

## 1. General description

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The OL2300 is a UHF ASK/FSK fractional-N transmitter with a fully integrated fractional-N Phase-Locked Loop (PLL) frequency synthesizer and a power amplifier to drive an external antenna.

The OL2300 is especially designed for use in the Industrial Scientific Medical (ISM) frequency bands (315/434/868/915 MHz). Fine-tuning of the reference oscillator by means of fractional-N synthesis allows the compensation of manufacturing tolerances of the crystal. The device also includes an adjustable output power capability.

The OL2300 can be used for both ASK and FSK modulation with chip rates up to 112 kcps. Due to the high-level of integration, few external components are needed to construct a complete transmitter.

## 2. Features and benefits

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- Fully integrated fractional-N PLL frequency synthesizer
- Integrated VCO without external components
- Independent Power-down modes for oscillator and PLL
- Operating frequency: 315/434/869/915 MHz ISM/SRD bands
- OOK/ASK/FSK modulation
- Software programmable output power
- Software programmable modulation index for ASK
- Software programmable frequency deviation for FSK
- Software programmable multi channel capability
- Software programmable crystal trimming capability
- Low power operation
- Very low external component count
- Low pin-count
- Very small package



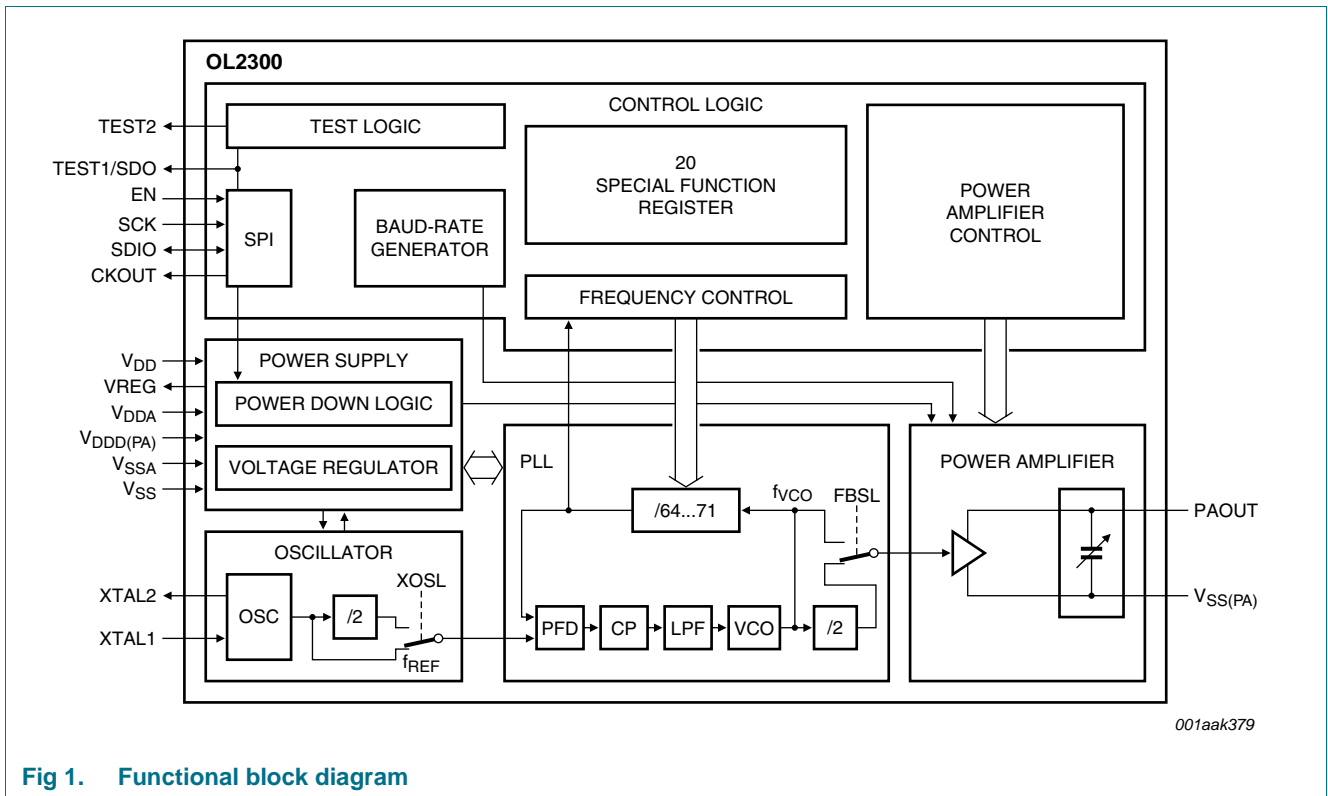
### 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
OL2300NHN	-25 °C to +85 °C	HVQFN16 <sup>[1]</sup>	plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 3 × 3 × 0.85 mm	SOT758-1

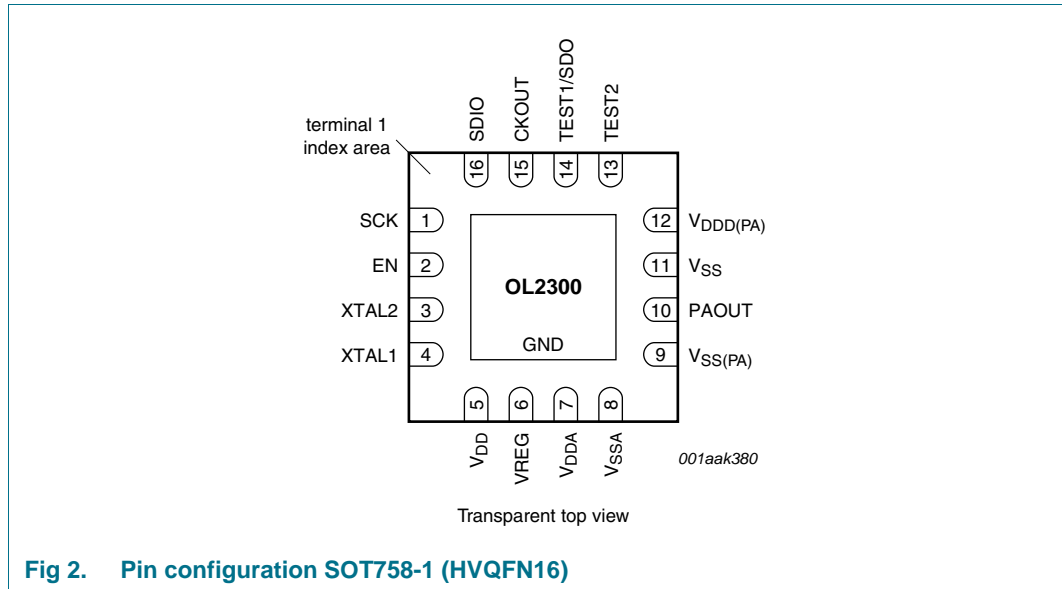
[1] When the exposed die attach pad is used, it must be connected to GND.

### 4. Functional diagram



## 5. Pinning information

### 5.1 Pinning



### 5.2 Pin description

**Table 2. Pin description**

Symbol	Pin	Description
SCK	1	serial interface clock input
EN	2	enable input
XTAL2	3	crystal oscillator 2
XTAL1	4	crystal oscillator 1
V <sub>DD</sub>	5	supply voltage
VREG	6	voltage regulator output
V <sub>DDA</sub>	7	analog supply voltage
V <sub>SSA</sub>	8	analog ground supply voltage
V <sub>SS(PA)</sub>	9	power amplifier ground supply voltage
PAOUT	10	power amplifier output
V <sub>SS</sub>	11	ground supply voltage
V <sub>DD(PA)</sub>	12	power amplifier digital supply voltage
TEST2	13	test output 2
TEST1/SDO	14	test output 1/serial data output
CKOUT	15	clock output
SDIO	16	serial interface data input/output

## 6. Functional description

### 6.1 Functional blocks overview

#### 6.1.1 Power management, voltage regulator

The supply voltage source is connected between pin  $V_{DD}$  and the pins  $V_{SS}$ ,  $V_{SSA}$  and  $V_{SS(PA)}$ .

An integrated low-dropout voltage regulator is used to supply the PLL and the PA-driver with a reduced, regulated voltage. This helps keep the current consumption and the supply voltage dependencies of the PLL as low as possible. The output of this regulator is pin  $V_{REG}$  which must be connected to an external blocking capacitor in order to guarantee stability of the regulator. A recommended set-up is shown in [Figure 23](#).

Two different regulator modes are available. For a detailed description see [Section 6.4.6](#).

Pin  $V_{DDA}$  is the positive supply voltage of the analog part of the PLL and pin  $V_{DDD(PA)}$  is the positive digital supply of the PLL prescaler and the PA-driver stage. Both pins should be connected to pin  $V_{REG}$ .

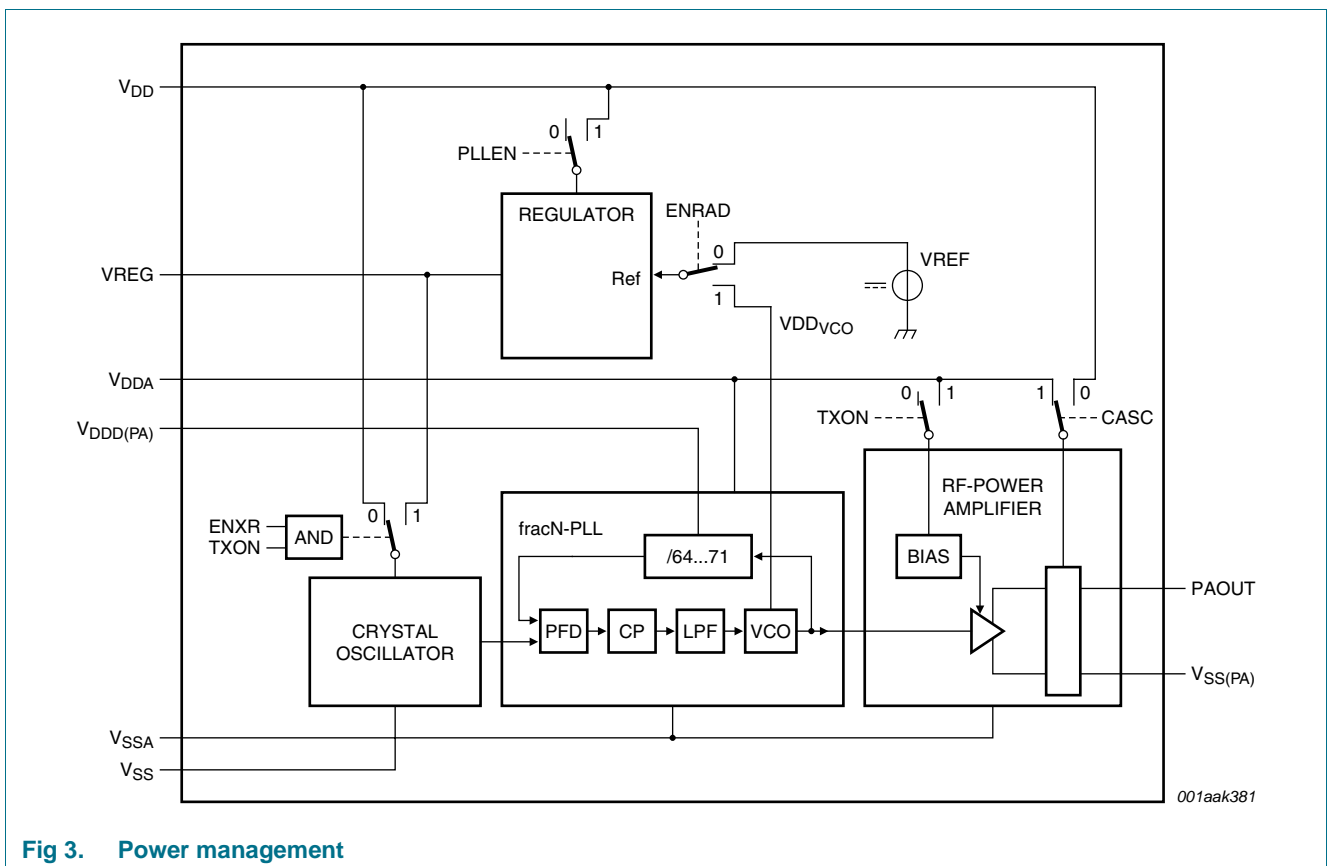


Fig 3. Power management

6.1.2 Interface and control logic

6.1.2.1 Configurable 3-wire or 4-wire interface

The OL2300 can be configured via a simple Serial Peripheral Interface (SPI). The interface itself can be configured for 3-wire or 4-wire mode. The 4-wire mode uses pin TEST1 as Serial Data Output SDO when the SDIO is used as input (see Figure 4).

EN pin must be set to enable communication via the 3 or 4-wire serial interface. If the EN pin is kept low for at least  $2^{16}$  XTAL clock pulses, the transmitter device will be reset, the bit-counter implemented inside the SPI counting the already transferred bits shall be set to zero, SCK and SDIO are disabled and the device will enter the Power-down mode (also the crystal oscillator is switched off). If the 4-wire interface has been used, a reset would also deactivate the SDO pin (set to 3-state; ENSDO is not influenced).

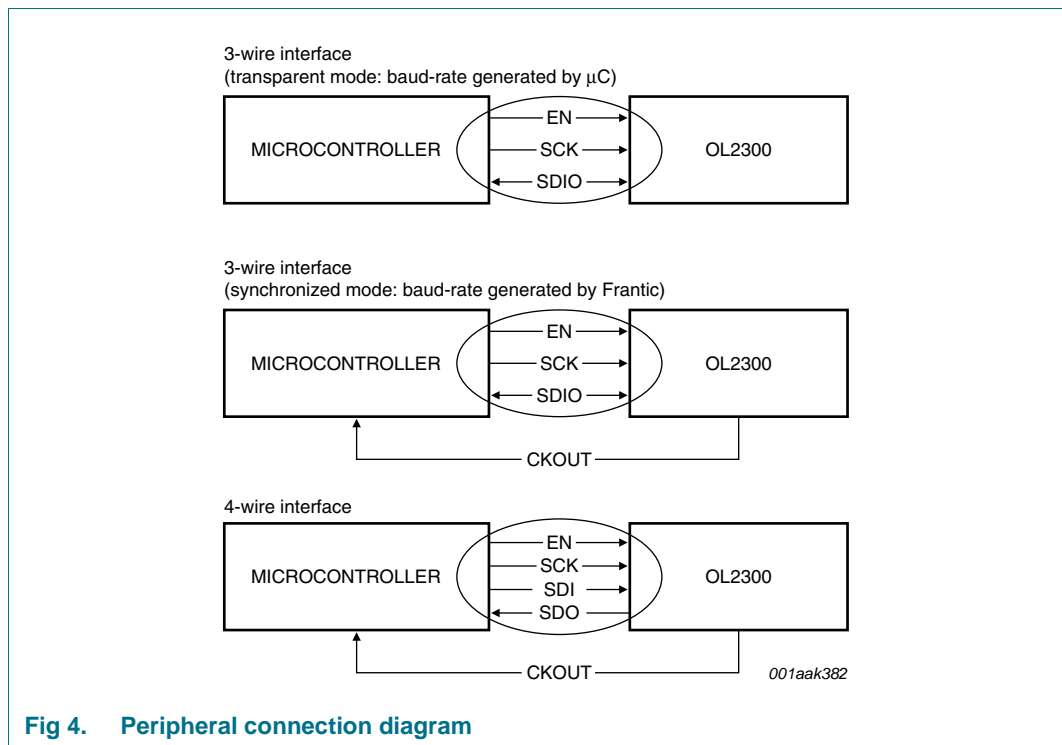


Fig 4. Peripheral connection diagram

After a transmit command the EN pin has an additional function: At the falling edge of the EN pin the level of the SDIO pin is latched and directly connected to the modulator input. In this case it is possible to intercept the RF data transmission without deactivating the PA and to loop the last transmitted bit while the SDIO interface is used for SFR configuration. Note that EN must not be low for more than  $2^{16}$  XTAL clock pulses otherwise the device will be reset.

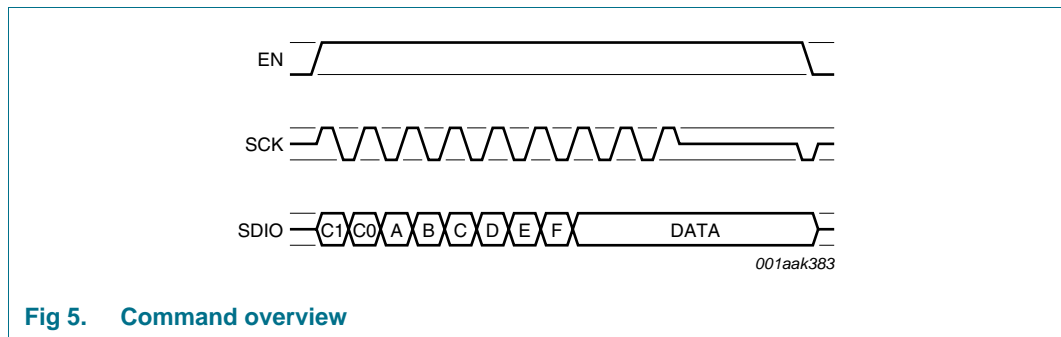
SCK pin is the clock input for the serial interface. Depending on the start-up condition of SCK at the rising edge of EN (see Section 6.7.9) each rising/falling edge of SCK shifts data into or gets data from the SPI register set. During RF data transmission the SCK is don't care (signal on SCK has no influence on interface).

**SDIO** is the configurable bidirectional data input/output pin of the serial interface. By default, the bidirectional mode is configured, so SDIO is used for both input and output data transmission. If ENSDO in register ACON2 is set, SDIO is used as input only and TEST1 is configured as data output SDO (4-wire interface). The SDO pin is high ohmic until data is written.

**Table 3. (Serial data output)/TEST1 control (ENSDO)**

ENSDO	SDO/TEST1 control state
0	pin TEST1 not used (only for test purposes)
1	pin TEST1 used as SDO (Serial Data Output)

Data in or data out operation is adapted automatically during SPI communication sequences.



**Fig 5. Command overview**

**Table 4. Command overview**

C1	C0	Command	A-F
0	0	write SFR	start address A5..A0
0	1	read SFR	start address A5..A0
1	0	transmit	transmit options

**6.1.3 Reference oscillator**

The reference oscillator is a Pierce type with automatic amplitude regulation and gain control to reduce the total current consumption. The device pins XTAL1 and XTAL2 connect the internal circuitry to the external reference crystal resonator and load capacitances. To get oscillation on the specified crystal frequency the input capacitances of the two XTAL pins and PCB parasitics must be considered. The oscillator typically operates at frequencies ranging from 9 MHz to 19 MHz to achieve the allowed transmission frequencies.

**6.1.4 Baud rate generator**

The output pin of the integrated baud rate generator CKOUT, will provide a clock, which is derived from the XTAL clock frequency. The baud rate is programmable by a special function register-set (BDSEL, SCSEL). CKOUT is not always active (see [Section 6.7.2](#)).

**6.1.5 Power amplifier**

The power amplifier is driven from the PLL synthesizer and operates in single-ended fashion, according to [Figure 9](#).

The power amplifier output (pin PAOUT) requires an external DC path to pin  $V_{DD}$ , established by the antenna loop or a dedicated bias coil. A dedicated ground pin ( $V_{SS(PA)}$ ) is provided to improve the RF properties of the circuitry and must be connected to pin  $V_{SS}$ . Best efficiency is achieved when the output voltage swing at pin PAOUT yields one volt less than two times the supply voltage:

$$V_{PAOUT} \text{ (p-p)} = (2V_{DDA} - I) \text{ V} \quad (1)$$

Three special-function-registers ACON0, ACON1 and ACON2 are available to control the output power of the 4 binary weighted output stages.

The Power amplifier also features three regulated and one unregulated (high power) output power modes, as selected by the control bits PAM1 and PAM0 located in the TXCON register. In regulated mode the input drive level of the amplifier is derived from an internal reference voltage and so the output power is stabilized against supply voltage and temperature variations over a wide range.

## 6.2 Transmitter operating modes

### 6.2.1 Power-down mode

If the EN pin is kept low for at least  $2^{16}$  XTAL clock pulses (~5 ms at a 13.08 MHz crystal frequency), the transmitter (PLL, Power amplifier and crystal oscillator) will be reset, the bitcounter inside the SPI counting the already transferred bits is set to zero, SCK and SDIO are disabled (also SDO, if used) and the device will enter the power-down mode. In this state the TXCON bit PLEN is cleared. The total current consumption is almost zero.

Another possibility to enter the Power-down mode is to set the PD bit in the TXCON register.

When the Power-down mode is left (by rising edge of EN) the PD bit is cleared.

### 6.2.2 XTAL active mode

With the rising edge of EN the Power-down mode is left and the crystal oscillator is activated. The XTAL clock will be stable after  $t_{set}$ . The SPI is activated, so the SFRs can be programmed. The XTAL Active mode can be left by either activating the PLL (set PLEN in TXCON) or by entering the Power-down mode.

### 6.2.3 PLL active mode

If the XTAL active mode is active and the crystal oscillator is settled, the PLL can be switched on (after  $t_{set}$ ). Setting the bit PLEN in the register TXCON directly powers on the PLL. The VCO output frequency will be stable after  $t_{ACQ}$ . This mode stays active as long as EN is kept 1 or as long as EN is kept 0 for a period shorter than  $2^{16}$  XTAL clock pulses. If EN is kept 0 for a longer period or the PD bit in TXCON is set, the device returns to the Power-down mode. By resetting the PLEN bit in TXCON the PLL is turned off and XTAL active mode is entered again. Another possibility to exit the PLL active mode is to send a dedicated SPI command (transmit command).

### 6.2.4 Transmitter Active mode

The Transmitter Active mode can only be entered upon an SPI command, which is only possible if the PLEN bit is set (with a previous SPI command). Dependent on the configuration coded into the transmit command, the Transmitter Active mode can be

exited when either EN is set LOW directly, or when EN is set LOW in a synchronized way with the edge of the last data-bit (in both cases the PLL Active mode is entered) or upon direct SPI register setting (then XTAL active mode is entered). If a POR or power fail condition occurs during a transmit sequence, the XTAL active mode is entered.

The transmitter is turned off by setting the PD bit in TXCON and the device enters the Power-down mode. This also occurs if EN is kept 0 for a period longer than  $2^{16}$  XTAL clock pulses.

When the device is in Transmitter Active mode, SPI communication (change of register contents) is possible (depending on the configuration settings), within one bit or during a constant bit stream.

For this feature EN must be set low directly after the beginning of one transmitted bit and then set high again. SPI communication is then enabled for commands. Transmitting new data can be re-activated by another dedicated transmit command. During the SPI communication the transmitted data will remain unchanged.

The power amplifier is activated by the first transmitted string and the baud rate generator is reset at this point. When the transmit-phase is interrupted by an SPI communication and the transmit-phase is re-started, the baud rate generator will remain synchronized with the previous string. No jitter will occur when switching from the previous to the next string.

After the transmission of data-bits the PLEN bit can be read. The brown out detection monitors the actual regulated supply voltage and indicates proper supply condition during the whole transmission phase. If PLEN is cleared, this indicates the supply voltage has dropped below the minimum required voltage level and the transmission will be interrupted. To restart a transmission a new transmit command must be sent once the PLL is re-enabled.



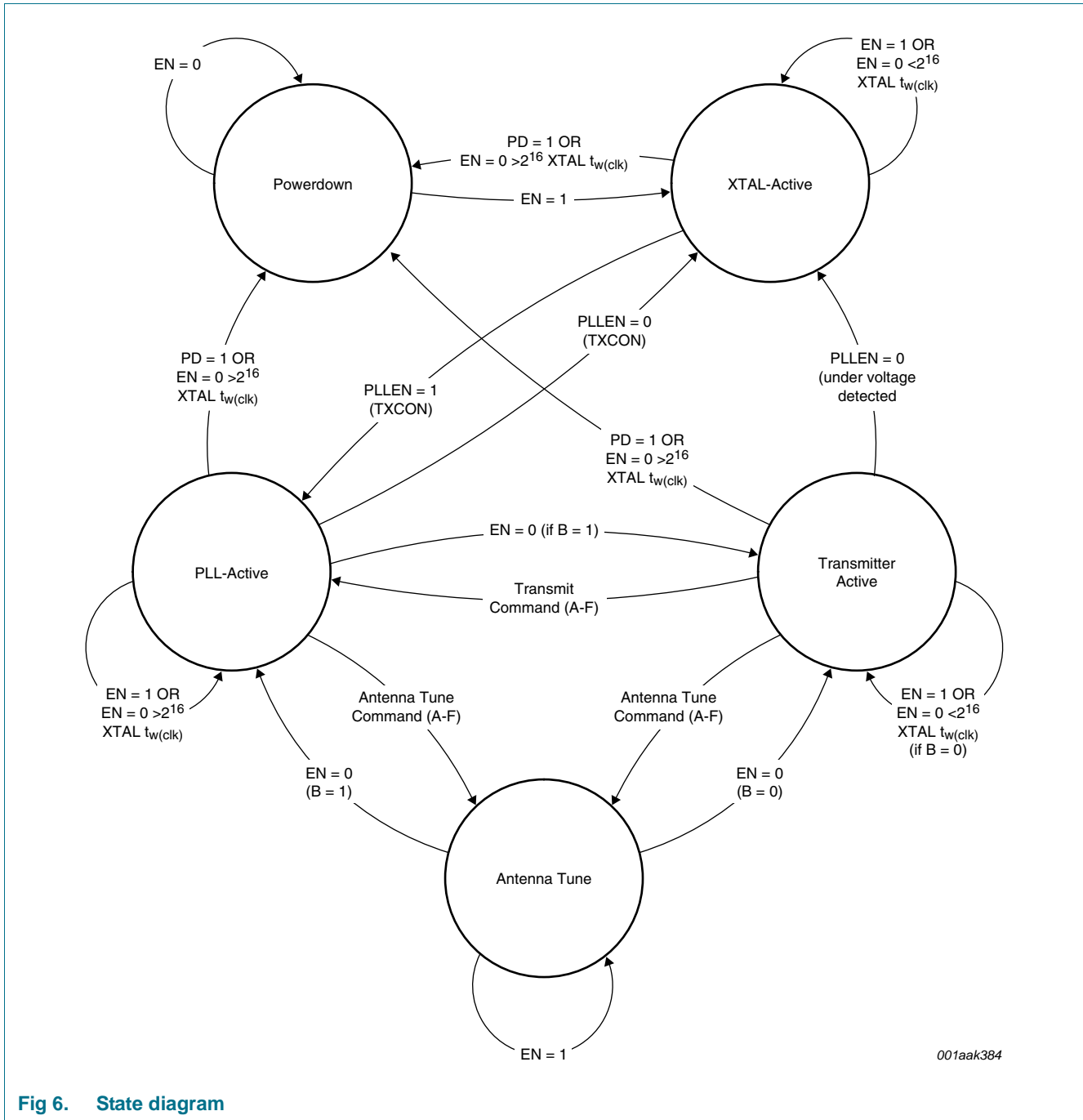


Fig 6. State diagram

### 6.3 Reference clock generation

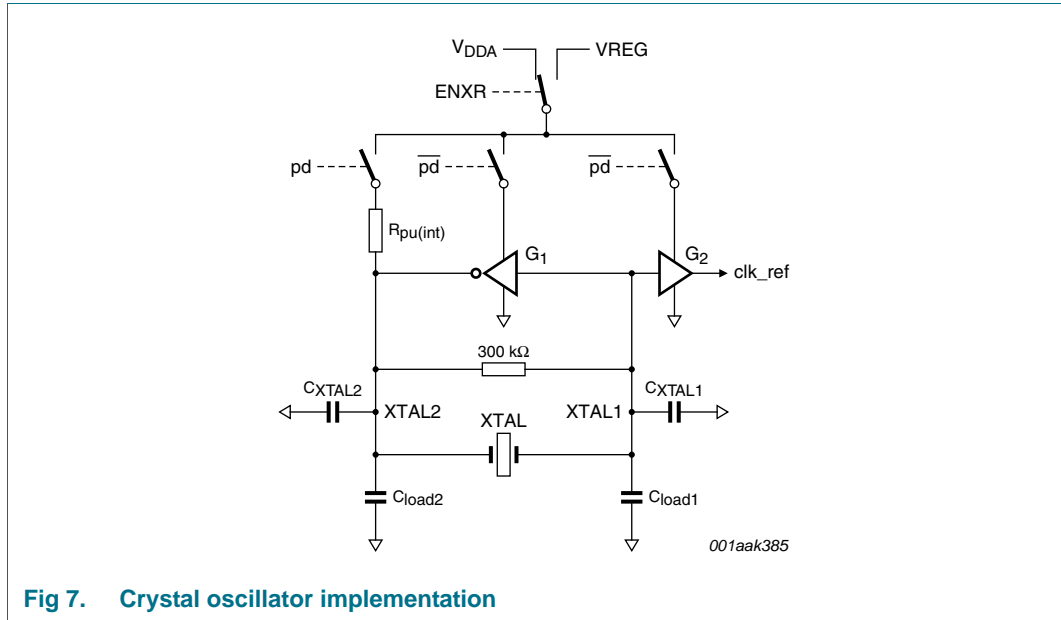
The crystal frequency is used as a reference for both the fractional-N PLL and the baud rate generation.

The oscillator is designed to work in parallel resonance mode of the crystal. In addition two external load capacitances are required to operate the crystal at the specified nominal frequency. For a calculation of the required capacitance the pin capacitors at XTAL1 and XTAL2 and the parasitic PCB stray capacitance have to be considered. The total load capacitance  $C_{load}$  is given by:

$$C_{load} = \frac{I}{\frac{I}{C_{load1} + C_{XTAL1}} + \frac{I}{C_{load2} + C_{XTAL2}}} + C_{PCB(par)} \tag{2}$$

**Table 5. Load capacitance calculation parameters**

Variable	Description
C <sub>load1</sub>	load capacitor at XTAL1
C <sub>load2</sub>	load capacitor at XTAL2
C <sub>XTAL1</sub>	pin capacitor at XTAL1
C <sub>XTAL2</sub>	pin capacitor at XTAL2
C <sub>PCB(par)</sub>	parasitic PCB capacitance



**Fig 7. Crystal oscillator implementation**

The oscillator is constructed using an inverting gain stage between the two XTAL pins with a clock buffer stage in series. The feedback resistor between XTAL1 and XTAL2 is used to define the DC operating point to keep the amplifier working in linear region.

The gain stage G1 features an automatic amplitude regulation. Maximum gain is required only during oscillator start-up where a short start-up time and also a high start-up margin are needed. If the amplitude exceeds (V<sub>DD</sub> – 0.5) V the gain is reduced to keep the current consumption as low as possible.

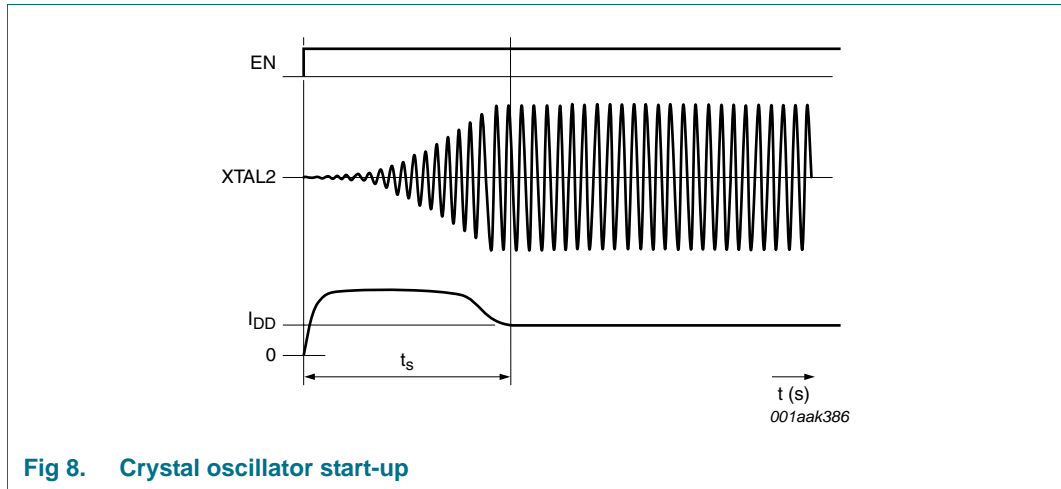


Fig 8. Crystal oscillator start-up

To additionally reduce the total current consumption the power supply of the crystal oscillator can be switched from  $V_{DDA}$  to the regulated supply voltage  $V_{REG}$  by setting the control bit ENXR in the special function register TXCON.

Table 6. Oscillator supply switch (ENXR)

ENXR	Selected XTAL oscillator power supply
0	$V_{DDA}$ , unregulated supply mode
1	$V_{REG}$ , regulated supply mode

If ENXR is set, the oscillator supply is automatically changed to a regulated supply when the transmit-state is entered. The XTAL supply is switched back to the unregulated supply when the transmit-state is exited.

In Power-down mode both gain stages are switched off and XTAL2 is defined by an internal pull-up resistor  $R_{pu(int)}$ .

Table 7. Address 0Eh; TXCON, transmitter control

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PD	PDCK	XOSL	FBSL	PAM1	PAM0	ENXR	PLLEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Drive level:

A typical calculation of the approximate power dissipated in a crystal is:

$$P_{max} = ESR_{typ} \times \frac{(2\pi f \times C_{load} \times V_{DD})^2}{2} \tag{3}$$

Example:

10 MHz crystal,  $C_{load} \sim 6$  pF,  $ESR \sim 20 \Omega$  at  $V_{DD} = 3$  V:  $P_{max} = 12.8 \mu W$

### 6.4 Power amplifier control and ASK modulation

For control of the output power and the modulation characteristics some special function register bits (ACON, PAM, CASC) are available.

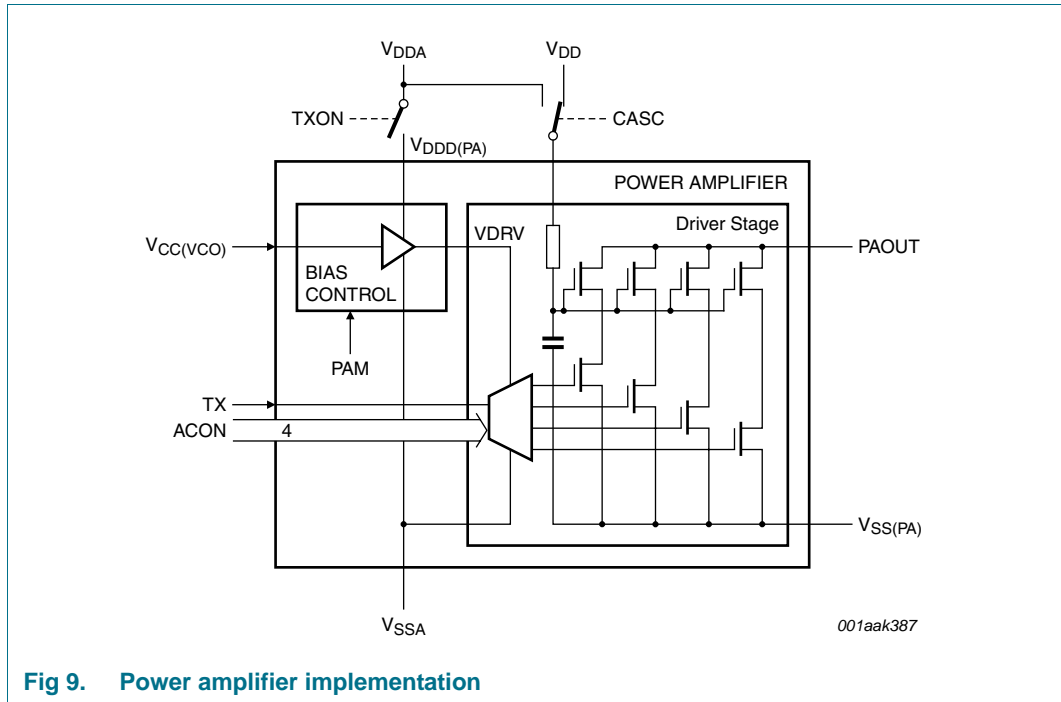


Fig 9. Power amplifier implementation

6.4.1 Power amplifier modes

The bits PAM0 and PAM1 located in the special function register TXCON can be used to choose between three regulated and one unregulated power modes. The regulated modes should be used for applications where the output power should be independent from changes of the supply voltage and ambient temperature.

Table 8. Address 0Eh; TXCON, transmitter control

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PD	PDCK	XOSL	FBSL	PAM1	PAM0	ENXR	PLLEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

For very high power applications the regulation mechanisms can be deactivated by using power mode 3 (see Table 6)

The best regulation characteristics are provided using the lowest power mode so the lowest acceptable power mode for the application should be selected and the exact output power controlled by means of the control signals ACON0, ACON1 and ACON2.

Table 9. Power amplifier modes

PAM1	PAM0	Power Mode	Comment
0	0	0	low power, highest stability <sup>[1]</sup>
0	1	1	medium power, medium stability
1	0	2	high power, low stability
1	1	3	maximum power, stabilization OFF

[1] The lowest supply voltage and temperature dependency is achievable with power mode 0.

The available output power is a function of the actual VCO frequency, so the higher the VCO frequency and its supply voltage ( $V_{DD(VCO)}$ ), the higher the output power becomes. A low VCO frequency selection is desirable for Japan due to the present limitations regarding radiated output power.

**6.4.2 ACON power amplifier amplitude control**

The control registers ACON0, ACON1 and ACON2, control the power amplifier driver stage in all four power modes for either amplitude fine-tuning or ASK modulation means.

The actual output power is set by three 4-bit values in the ASK modulation control registers ACON0, ACON1 and ACON2. Two different HIGH (AMH) levels and one LOW (AML) level are configurable.

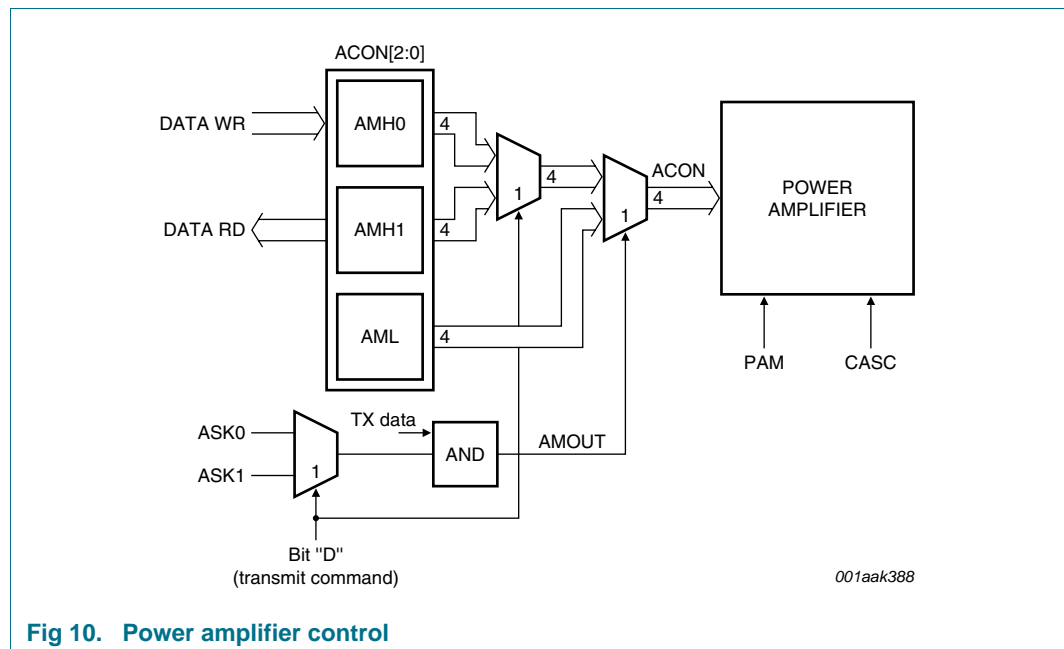
**6.4.3 ASK settings**

Amplitude modulation is achieved by switching between one of the high-levels (selected by control-bit D of the transmit-command) and the low-level in accordance with the control signal AMOUT, which is derived from the TXData, see [Figure 10](#) and [Figure 14](#).

**Table 10. Amplitude control for ASK, FSK**

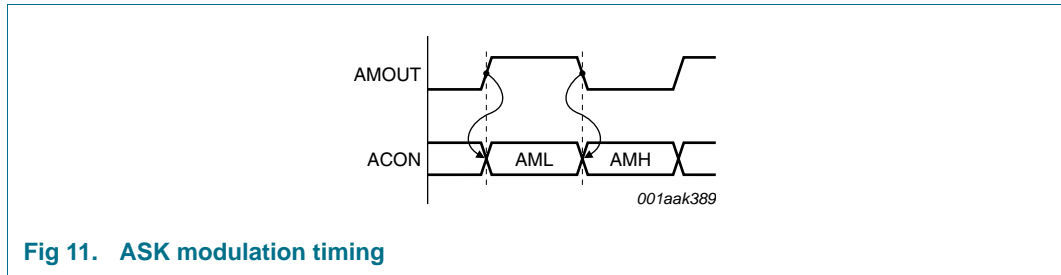
ASK1	ASK0	D	Mode	Amplitude control
X	0	0	FSK	ACON0
X	1	0	ASK	ACON0
0	X	1	FSK	ACON1
1	X	1	ASK	ACON1

ASK0 located in ACON0, and ASK1 located in ACON1 determine ASK or FSK operation.



**Fig 10. Power amplifier control**

If TXDATA is low then AMOUT is low and the amplitude is determined by the value of the transmit command bit 'D'. If the bit is set, the actual high-level is controlled by the four bits of AMH1[3:0] located in ACON1. Alternatively AMH0[3:0] from ACON0 would be used if 'D' is cleared.



**Fig 11. ASK modulation timing**

If TXDATA is high then AMOUT is set and the amplitude is given by the content AML[3:0] in register ACON2 and the settings of ASK0 and ASK1. If 'D' is cleared ASK0 located in register ACON0 determines between ASK and FSK operation. Alternatively if "D" is set, ASK1 is used. In both cases the selected ASK bit must be set to achieve amplitude modulation. If the selected ASK bit is cleared, AMOUT is kept low and the carrier remains unmodulated (used for FSK with continuous wave operation).

**Table 11. Address 0Ah; ACON0, ASK modulation control 0**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ASK0	X	X	X	AMH03	AMH02	AMH01	AMH00
R/W	-	-	-	R/W	R/W	R/W	R/W

**Table 12. Address 0Bh; ACON1, ASK modulation control 1**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ASK1	X	X	X	AMH13	AMH12	AMH11	AMH10
R/W	-	-	-	R/W	R/W	R/W	R/W

**Table 13. Address 0Ch; ACON2, ASK modulation control 2**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CASC	ENRAD	ENPF	ENSDO	AML3	AML2	AML1	AML0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

#### 6.4.4 SASK, Soft ASK mode

A 'soft' modulation scheme is implemented in order to reduce the ASK modulation bandwidth. The soft ASK shape is modelled by a linear interpolation approach.

Switching between the selected AMH and AML values is done in a linear way. The output power is changed by switching the four binary weighted PA output stages with a programmable timing configured with the bits RMP[6:0] of register MRCON (modulation ramp control).

The value of RMP[6:0] specifies the number of reference clocks (derived from the crystal frequency) between two consecutive power steps. Setting the bits RMP[6:0] to 0x0h results in immediate change between the values AMH and AML (normal ASK mode).

**Remark:** If bit XOSL in register TXCON is set, the reference clock applied to the SASK ramp control is the crystal clock divided by a factor 2 and the ramp time is doubled.

**Table 14. Address 0Dh; MRCON, modulation ramp control**[\[1\]](#)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	RMP6	RMP5	RMP4	RMP3	RMP2	RMP1	RMP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[1] MRCON is also used for soft-FSK.

The configured ramp time also defines the maximum possible data rate for ASK operation. The ramp time can be calculated by:

$$t_{SASK} = (AMH - AML) \times \frac{1}{f_{ref}} \times MRCON[6:0] \tag{4}$$

For RMP0 to RMP6 is not equal to 0, the maximum baud rate is given by:

$$f_{DATA}^{SASKmax} = \frac{1}{2 \times t_{SASK}} \tag{5}$$

For RMP0 to RMP6 is equal to 0 (normal ASK mode), the maximum baud rate is only limited by the baud rate generator (see [Section 6.1.4](#)) and the maximum channel bandwidth.

#### 6.4.5 CASC, cascode control signal

For a further improvement of the supply voltage stability also for high power modes, the cascode stage can be switched to the regulated power supply by setting bit CASC located in register ACON2. Note that the maximum output power is then reduced compared to the maximum available power in power-mode 3.

**Table 15. Cascode control flag (CASC)**

CASC	Cascode control state
0	Cascode stage switched to V <sub>DD</sub>
1	Cascode stage switched to V <sub>DDA</sub> (regulated)

#### 6.4.6 Voltage regulation and power fail detection

The integrated line regulator supports two different operation modes. The default mode is called ‘fixed low’ mode where the regulated supply voltage is derived from an internal, transistor threshold voltage based reference. After start-up of the PLL the second mode called adaptive mode can be entered by setting the SFR bit ENRAD.

#### 6.4.7 ENRAD, enable regulator adaptive mode

If set, the line regulator is switched to adaptive mode where the output voltage at VREG is directly derived from the VCOs power supply.

**Remark:** ENRAD must not be set until the PLL start-up has finished. It is strongly recommended to use the fixed mode during PLL start-up.

**Table 16. Voltage regulator control (ENRAD)**

ENRAD	Voltage regulator state
0	fixed output voltage, derived from internal reference
1	adaptive mode: regulated supply derived from VCO supply voltage

6.4.8 ENPF, enable power fail detection

If set, the built in power fail detection (brown out detection) is enabled. In this case the PLL and the PA are switched off if the supply voltage at  $V_{DD}$  is not sufficiently high to guarantee proper operation of the line regulator. This also includes the proper function of the PLL circuit.

Table 17. Power fail enable signal (ENPF)

ENPF	Power fail control state
0	power fail detection disabled
1	power fail detection enabled

The power fail detection can be selected for fixed and adaptive modes. The detection circuit is only active if transmission is active (the power amplifier must be enabled). It is recommended to set ENPF before the power amplifier is activated to ensure that the PLL is working properly but it is also possible to set ENPF if a transmission has already been started. In the latter case there is no guarantee that the PLL will operate at the correct frequency when the power amplifier is enabled.

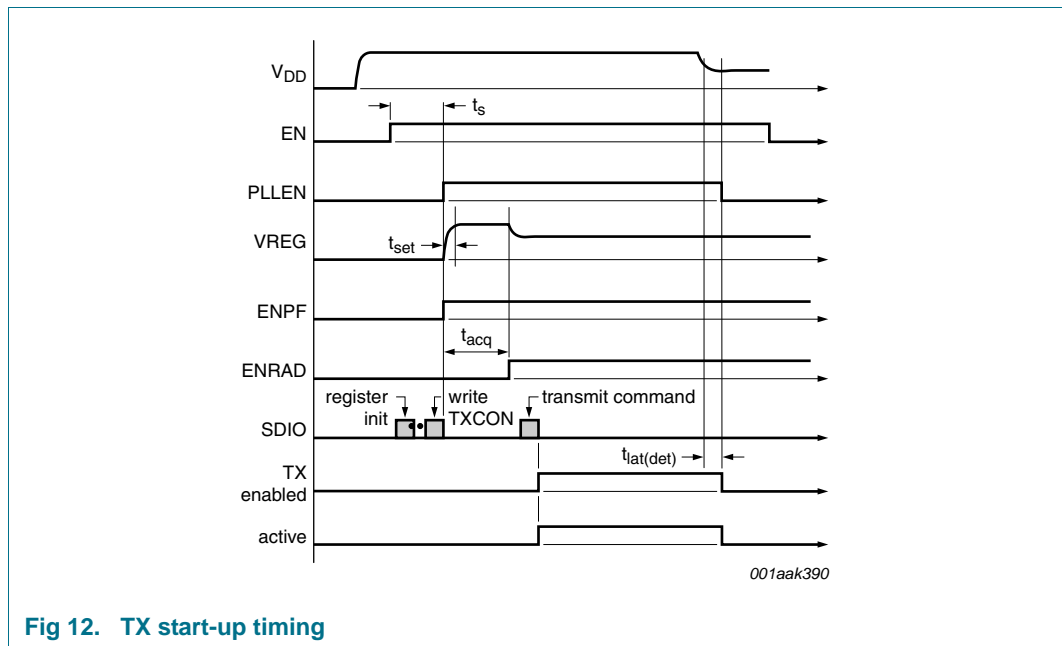


Fig 12. TX start-up timing

Once the power fail detection has detected a voltage drop at  $V_{DD}$  during transmission so that the remaining supply voltage is not sufficient to keep the PLL in save operation the PLLEN is immediately cleared, the power amplifier will be disabled and the transmission will be stopped. The two control signals ENPF and ENRAD (if adaptive mode is used) will stay enabled. The user must disable ENRAD before the next PLL activation otherwise a proper start-up of the PLL cannot be guaranteed.

If ENXR was set to operate the crystal oscillator using the regulated supply while the adaptive mode was active (ENRAD = 1), a power fail would instigate the crystal oscillator supply to switch from regulated to unregulated mode (the PA would also be deactivated). If the fixed mode was used a power-fail would not influence the supply to the oscillator.



### 6.5 Frequency control and FSK operation

FSK modulation is applied if the ASK control bit of the selected ACON register is cleared. ACON0 or ACON1 can then be selected for the FSK transmission amplitude setting dependent on the setting of the transmit-command control-bit 'D', (see [Table 10](#)).

### 6.6 Frequency control registers

The operation frequency is set by the content of the frequency control registers FC1 to FC4, which each have a width of 18 bits. The two MSBs of all four frequency control registers are located in the register FCA. The two corresponding 'LOW' bytes are located in FCxH and FCxL registers. The selection of the 'active' frequency control register is done directly with the transmit command (bits 'E' and 'F', see [Section 6.7.10](#)). See for frequency configuration 1 an example of the complete frequency setting.

**Table 18. Frequency control bits**

SFR	FCA				FC1H						
bit	F1C17	F1C16	F1C15	F1C14	F1C13	F1C12	F1C11	F1C10	F1C9	F1C8	
FCON	17	16	15	14	13	12	11	10	9	8	

**Table 19. Frequency control bits**

SFR	FC1L							
bit	F1C7	F1C6	F1C5	F1C4	F1C3	F1C2	F1C1	F1C0
FCON	7	6	5	4	3	2	1	0

#### 6.6.1 PLL operation frequency $f_{VCO}$

The PLL operation frequency is calculated by the following equations:

$$f_{VCO} = f_{ref} \times \left( \frac{f_C + 0.5}{32768} + 65 \right) \text{ Hz} \tag{6}$$

Frequency step width:  $f_{VCOstep} = \frac{f_{ref}}{32768} \text{ Hz}$

**Table 20. PLL operation frequency calculation parameters**

Variable	Description
$f_{VCO}$	VCO frequency
$f_{ref}$	PLL reference frequency <sup>[1]</sup>
$f_{VCOstep}$	minimum VCO frequency step
$f_{xtal}$	XTAL oscillator frequency
$f_{RF}$	RF frequency on PAOUT
FC	frequency control value (FCx register) <sup>[2]</sup>

[1]  $f_{ref}$  can be set to  $0.5f_{xtal}$  by a test-mode bit.

[2] In order to avoid fractional-N overflow don't use values above 163839.

- a)  $f_{ref} = f_{xtal}$ .
- b)  $f_{RF} = f_{VCO}$  for 868/915 MHz bands (FBSL set to 1).
- c)  $f_{RF} = f_{VCO}/2$  for 315/434 MHz bands (FBSL set to 0).
- d) FC = 0... 163839.

### 6.6.2 PLL frequency deviation (FSK)

The FSK frequency deviation is set as part of the FCON (FSK modulation control) register and has a width of 8 bits.

Table 21. Address 09h; FCON, modulation control

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FSK7	FSK 6	FSK 5	FSK 4	FSK 3	FSK 2	FSK 1	FSK 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

FSK deviation is calculated by:  $f_{DEV} = \pm f_{ref} \times \frac{FSK_{DEV}}{16384}$

Table 22. PLL frequency deviation calculation parameters

Variable	Description
$f_{DEV}$	FSK frequency deviation
$FSK_{DEF}$	FSK deviation value (FCON register) <sup>[1]</sup>
$f_{ref}$	PLL reference frequency

- [1]  $f_{ref}$  can be set to  $f_{xtal} / 2$  by a test-mode bit.
  - a)  $f_{ref} = f_{xtal}$
  - b)  $FSK_{DEV} = 0.255$

Table 23. Frequency selection limits

ISM-band (MHz)	$f_{xtal}$ (MHz)	min $f_{RF}$ (MHz)	max $f_{RF}$ (MHz)	step $f_{RF}$ (Hz)	min $f_{DEV}$ ( $\pm$ kHz)	max $f_{DEV}$ ( $\pm$ kHz)	step $f_{DEV}$ (Hz)
315	9.185183	298.51852	321.48127	140.15	0.560	143	560
434	13.08148	425.14815	457.85155	199.61	0.800	204	800
868	12.85185	835.37038	899.62903	392.21	0.785	200	785
915	13.55555	881.11112	948.88826	413.68	0.827	211	827

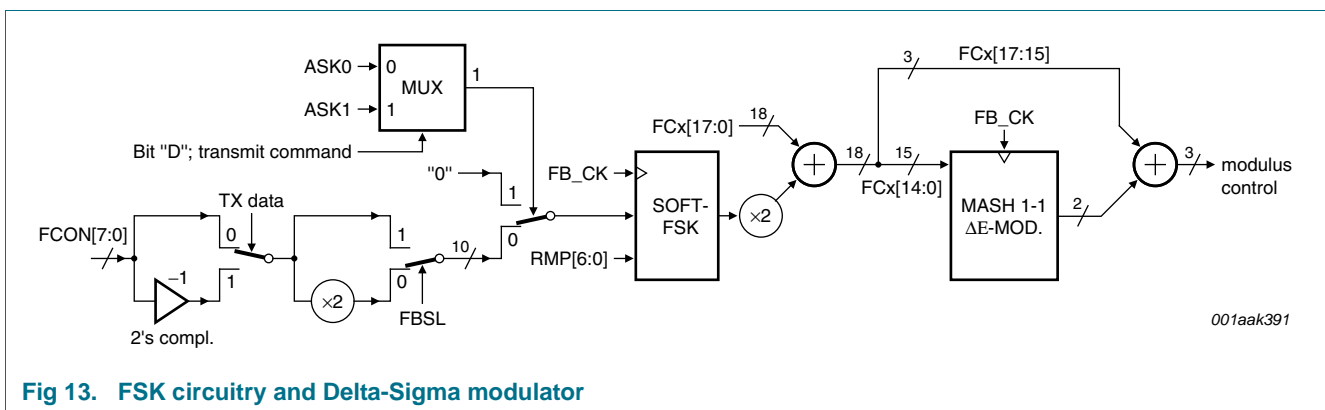


Fig 13. FSK circuitry and Delta-Sigma modulator

### 6.6.3 Oscillator and feedback divider settings

In order to allow operation for all ISM bands different oscillator divider and PLL divider settings can be selected with the special function register bits XOSL and FBSL located in register TXCON (See Figure 1).

**Table 24. Address 0Eh; TXCON, transmitter control register<sup>[1]</sup>**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PD	PDCK	XOSL	FBSL	PAM1	PAM0	ENXR	PLLEN

[1] All bits R/W.

Setting the bit XOSL enables the XTAL clock divider that lowers the reference clock frequency of the PLL by a factor of 2. This allows for example the use of an 18 MHz crystal for the 315 MHz ISM band.

If the 868 MHz band or the 915 MHz band is selected, bit FBSL must be set to 1. In this case the power amplifier is driven by the VCO frequency. In other cases bit FBSL has to be cleared and the PA is driven by the VCO frequency divided by 2.

**Table 25. Oscillator and feedback divider settings**

f <sub>xtal</sub> (MHz)	XOSL	FBSL	f <sub>PLL</sub> (MHz)	f <sub>RF</sub> (MHz)
13.08	0	0	868	434
13.08	0	1	868	868
13.08	1	0	434	217 <sup>[1]</sup>
13.08	1	1	434	434

[1] Not a valid ISM band.

### 6.6.4 FSK mode selection

In order to achieve a narrower signal bandwidth of the FSK spectrum a GFSK-like modulation, referred to as a Soft-FSK scheme is implemented. The Soft-FSK shape is modelled by a linear interpolation approach.

The FSK frequency shifting is done in a linear way between (f<sub>RF</sub> - f<sub>DEV</sub>) and (f<sub>RF</sub> + f<sub>DEV</sub>).

**Table 26. Address 0Dh; MRCON, modulation ramp control**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	RMP6	RMP5	RMP4	RMP3	RMP2	RMP1	RMP0
-	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The clock frequency of f<sub>ref</sub> is changed by a configurable number of steps which are stored in the register MRCON (modulation ramp control). Setting the register MRCON to 00h results in normal FSK operation.

The Soft-FSK ramp time is calculated by:

$$t_{FSK} = (2 - FBSL) \frac{2 \times FSK_{DEV} \times RMP}{f_{ref}} \tag{7}$$

**Example:**

f<sub>ref</sub> = 13.08 MHz, FCON = 0Fh ⇒ f<sub>DEV</sub> = ±11,975 kHz.

For MRCON = 2Ah the frequency step width will result in:

$$f_{step} = 2 \times 11975 / 42 = 570.24 \text{ Hz.}$$



The baud rate division ratio is:  $CLK_{BD} = \frac{CLK_{PSC}}{2 \times (N + I)}$

**Remark:** For synchronization reasons both baud rate counter and afterscaler are kept in reset state while the power amplifier is turned off. The prescaler will be clocked continuously whenever the XTAL oscillator is running.

**Table 28. Baud rate division ratio values**

BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0	Baud rate division ratio: N
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
....								
1	1	1	1	1	1	1	1	255

### 6.7.2 Clock generation/selection

The special function register SCSEL contains the configuration bits CSS[2:0] for the clock source selection, the bits PSC[2:0] for the prescaler control and ASC[2:0] for the afterscaler control.

**Table 29. Address 10h; SCSEL, scaler selection**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CSS2	CSS1	CSS0	PSC2	PSC1	PSC0	ASC1	ASC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The bit PDCK in the TXCON register determines the activity of the CKOUT signal. If PDCK is cleared, CKOUT will be active.

**Table 30. Address 0Eh; TXCON, transmitter control**

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PD	PDCK	XOSL	FBSL	PAM1	PAM0	ENXR	PLLEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

CKOUT is defined with the settings of CSS[2:0] from register SCSEL and can be configured as prescaler output or baud rate output (See [Table 31](#)).

If CSS2 is cleared then CKOUT is set to baud rate, prescaler or static high or low, dependent on CSS1 and CSS0 settings if transmit state is active and set to 3-state if transmission is inactive.

If CSS2 is set then CKOUT is set according to the configuration of CSS1 and CSS0 and 3-state mode is not entered during transmission.

**Table 31. Clock Source Selection (CSS)**

CSS2	CSS1	CSS0	CKOUT
0	0	0	3-state if TX disabled; LOW if TX enabled
0	0	1	3-state if TX disabled; prescaler clock if TX enabled
0	1	0	3-state if TX disabled; baud rate clock if TX enabled
0	1	1	3-state if TX disabled; inverted baud rate if TX enabled
1	0	0	LOW

**Table 31. Clock Source Selection (CSS) ...continued**

CSS2	CSS1	CSS0	CKOUT
1	0	1	prescaler clock <sup>[1]</sup>
1	1	0	LOW if TX disabled; baud rate clock if TX enabled
1	1	1	HIGH if TX disabled; inverted baud rate clock if TX enabled

[1] If the bit PDCK in register TXCON is set, CKOUT is set 3-state (independent from the CSS[2:0] settings).

### 6.7.3 Prescaler

The Prescaler clock is the reference clock divided by 1, 2, 4, 8 to 128. The division ratio is set in the PSC[2:0] bits (See [Table 32](#)).

**Table 32. Prescaler Control (PSC)**

PSC2	PSC1	PSC0	Division ratio
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16 <sup>[1]</sup>
1	0	1	32
1	1	0	64
1	1	1	128

[1] Reset/Power-on state: if SDIO is low at the rising edge of EN a division ratio of 16 will be applied, otherwise the division ratio will remain unchanged.

### 6.7.4 After-scaler

The after-scaler clock is the baud rate clock divided by 1, 2, 4 and 8. The division ratio is set in the ASC[2:0] bits (see [Table 33](#)).

**Table 33. After-Scaler Control (ASC)<sup>[1]</sup>**

ASC1	ASC0	Division ratio
0	0	1
0	1	2
1	0	4
1	1	8

[1] The after-scaler is only active in the transmit mode when the power amplifier is switched on.

### 6.7.5 TXDATA output

The TXDATA output is synchronized with the reference clock even in transparent transmission mode where the data is selected from SDIO and fed directly to the power amplifier control stage (see [Figure 10](#)).

### 6.7.6 Synchronous mode

When operating the device in synchronous mode data is clocked on the rising edge of CKOUT. It is possible to invert this clock signal as described in [Table 31](#). Inverting this signal has the effect of clocking the data presented at SDIO on the falling edge of CKOUT. The clock for the data generator has a dedicated afterscaler, therefore the CKOUT signal can run at a higher frequency if desired, as described in [Table 33](#).

### 6.7.7 General SPI information

The chip is configured via the serial SPI interface, consisting of an 8-bit shift register and twenty 8-bit registers holding the configuration data.

Data can be exchanged with multiple 8-bit frames (auto increment) or in portions of 8 bits (1 byte), which could be of advantage if a hardware SPI-interface is used. Data in the shift register is loaded into the addressed register with the last edge of SCK within the last bit of the transferred byte.

#### 6.7.7.1 SPI special function register-set

All registers are able to read or write via the SPI communication and are therefore arranged as a block with 20 addressable bytes.

Some of the bits of the registers indicate the state of the implemented TX state-machine and can alter without SPI transmission. (e.g. the 'PD bit' can be automatically set if EN is kept low for a number of XTAL clocks pulses or via dedicated SPI communication). Other bits only can be altered via SPI communication. (e.g. the frequency setting for the baud rate generator BD[7:0] or the configuration bits for the TX state-machine).

In order to change the operating mode of the transmitter, the special function register bits PD or PLEN of register TXCON must be accessed. To change from one state to another via SPI communication without intermediate states, these state describing bits are arranged in one byte. The byte will be written after completion of the byte transfer.

All the registers keep the stored information in power-down state but if a dynamic power-on reset occurs (can be evaluated by checking the PLEN bit after transmission) the registers content may change. Only register TXCON is reset to a default state. All other registers must be reset to ensure proper function after a dynamic reset.

### 6.7.8 SFR summary

**Table 34. Special function register summary<sup>[1]</sup>**

Name	Description	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset value <sup>[2]</sup>
FC1H	frequency configuration 1 high byte	00h	F1C15	F1C14	F1C13	F1C12	F1C11	F1C10	F1C9	F1C8	xxxx xxxx b
FC1L	frequency configuration 1 low byte	01h	F1C7	F1C6	F1C5	F1C4	F1C3	F1C2	F1C1	F1C0	xxxx xxxx b
FC2H	frequency configuration 2 high byte	02h	F2C15	F2C14	F2C13	F2C12	F2C11	F2C10	F2C9	F2C8	xxxx xxxx b
FC2L	frequency configuration 2 low byte	03h	F2C7	F2C6	F2C5	F2C4	F2C3	F2C2	F2C1	F2C0	xxxx xxxx b
FC3H	frequency configuration 3 high byte	04h	F3C15	F3C14	F3C13	F3C12	F3C11	F3C10	F3C9	F3C8	xxxx xxxx b
FC3L	frequency configuration 3 low byte	05h	F3C7	F3C6	F3C5	F3C4	F3C3	F3C2	F3C1	F3C0	xxxx xxxx b
FC4H	frequency configuration 4 high byte	06h	F4C15	F4C14	F4C13	F4C12	F4C11	F4C10	F4C9	F4C8	xxxx xxxx b
FC4L	frequency configuration 4 low byte	07h	F4C7	F4C6	F4C5	F4C4	F4C3	F4C2	F4C1	F4C0	xxxx xxxx b
FCA	MSB for all frequency configurations	08h	F4C17	F4C16	F3C17	F3C16	F2C17	F2C16	F1C17	F1C16	xxxx xxxx b
FCON	FSK modulation control	09h	FSK7	FSK6	FSK5	FSK4	FSK3	FSK2	FSK1	FSK0	xxxx xxxx b
ACON0	ASK modulation control 0	0Ah	ASK0	X	X	X	AMH03	AMH02	AMH01	AMH00	xxxx xxxx b
ACON1	ASK modulation control 1	0Bh	ASK1	X	X	X	AMH13	AMH12	AMH11	AMH10	xxxx xxxx b
ACON2	ASK modulation control 2	0Ch	CASC	ENRAD	ENPF	ENSDO	AML3	AML2	AML1	AML0	x0xx xxxx b
MRCON	modulation ramp control	0Dh	X	RMP6	RMP5	RMP4	RMP3	RMP2	RMP1	RMP0	xxxx xxxx b
TXCON	transmitter control	0Eh	PD	PDCK	XOSL	FBSL	PAM1	PAM0	ENXR	PLLEN	00xx xxx0 b
BDSEL	baud rate selection	0Fh	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0	xxxx xxxx b
SCSEL	scaler selection	10h	CSS2	CSS1	CSS0	PSC2	PSC1	PSC0	ASC1	ASC0	1011 00xx b
X	X	11h	X	X	X	X	X	X	X	X	xxxx xxxx b
TEST1	TEST1	12h	X	X	X	X	X	X	X	X	-
TEST2	TEST2	13h	X	X	X	X	X	X	X	X	-

[1] Bits marked 'X' are reserved for future use or device test. Any read operation yields an undefined result

[2] Reset condition after reset command (en set low for at least 2<sup>16</sup> reference clock cycles). Register SCSEL and bit of TXCON are reset only if SDIO = 0.



6.7.9 General SFR access information

If SCK is high at the rising edge of EN the data is transferred with the rising edge of SCK and if SCK is low at the rising edge of EN, the data is transferred with the falling edge of SCK (as shown in the write and read-access diagrams). Please note these statements are true at every rising edge of EN.

EN must be forced low after the last bit of all transmitted bytes in order to signal the end of transmission.

**Remark:** if EN is kept low for  $2^{16}$  pulses the power down state is entered and the crystal oscillator is switched off.

6.7.9.1 SFR block diagram

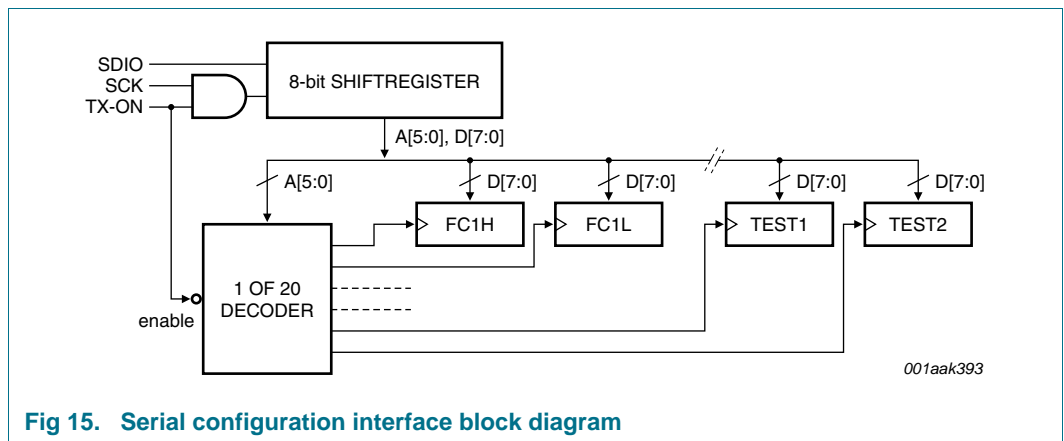


Fig 15. Serial configuration interface block diagram

6.7.9.2 Write access to SFR

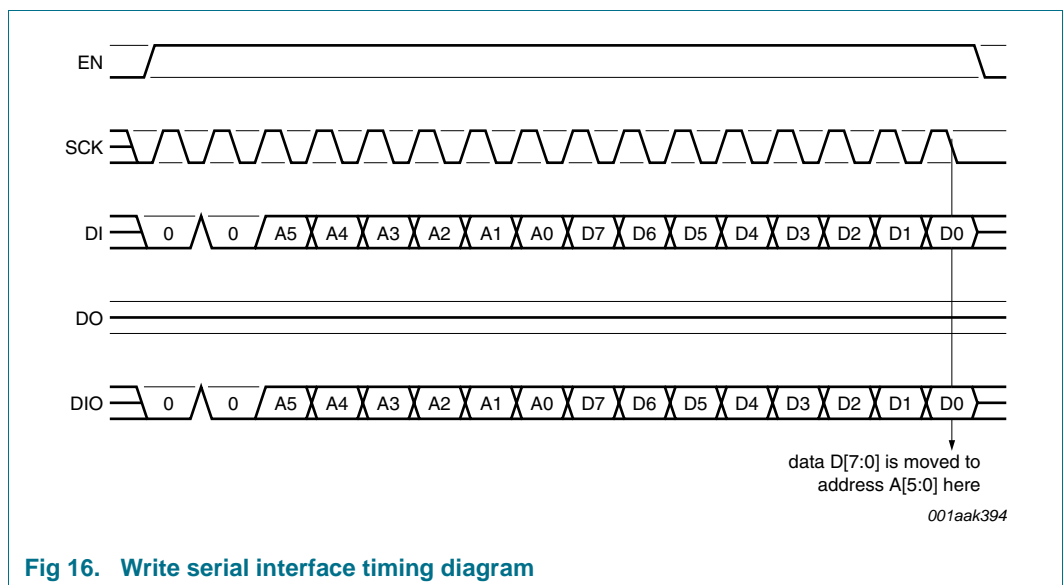


Fig 16. Write serial interface timing diagram

6.7.9.3 Read access to SFR

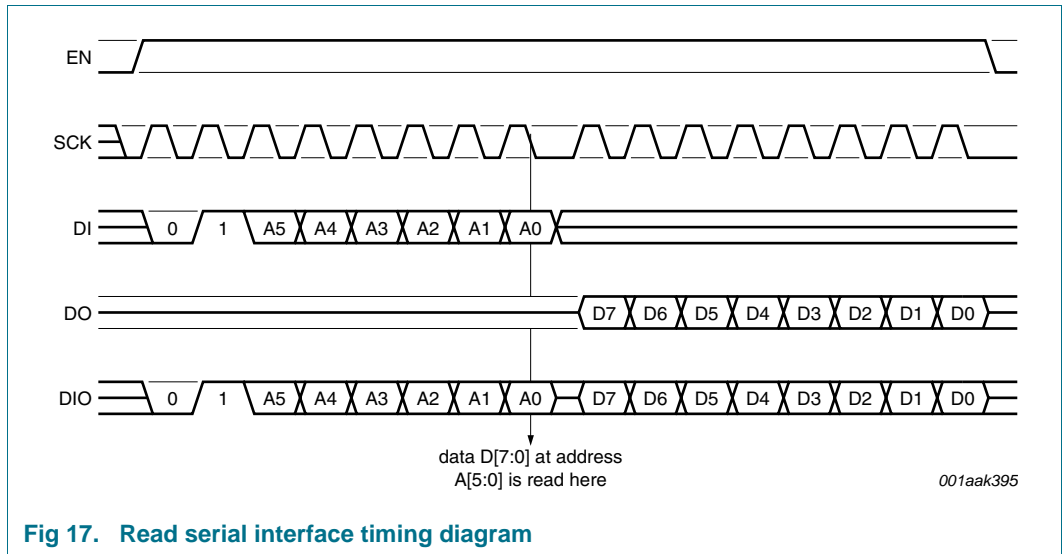
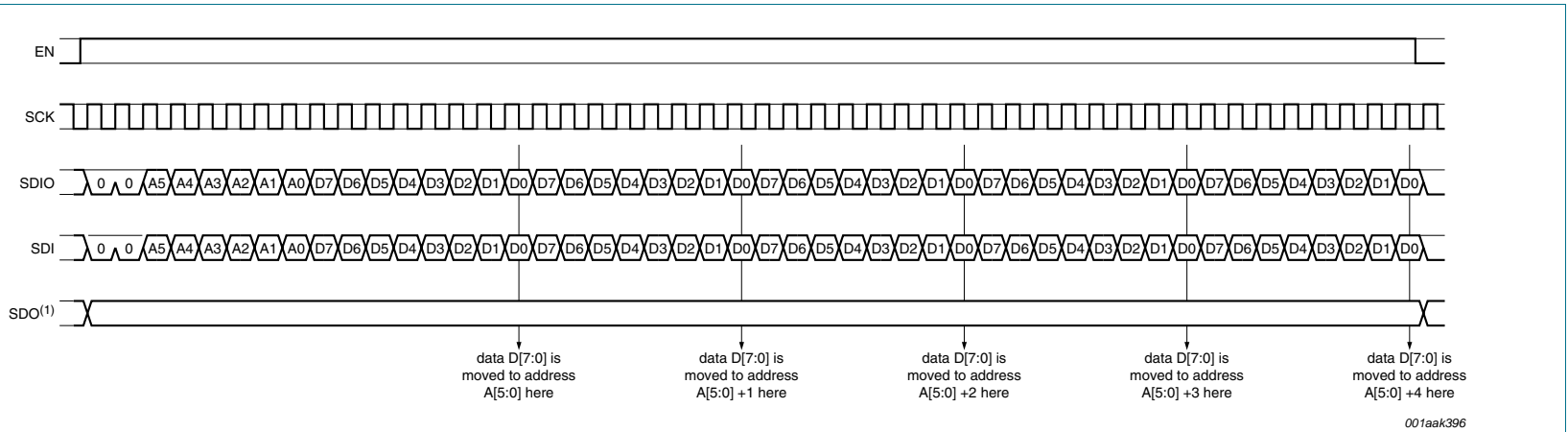


Fig 17. Read serial interface timing diagram

6.7.9.4 Access to SFR with auto-increment function

If the SPI clock SCK is still applied after the first transferred 8 data bits, the auto-increment function automatically increases the address for the following next 8 data bits by one. This enables writing data to a contiguous range of bytes without the need to set the address for every single data-byte. The auto-increment function is terminated with the falling edge of EN.

6.7.9.5 Write access to SFR with auto-increment function

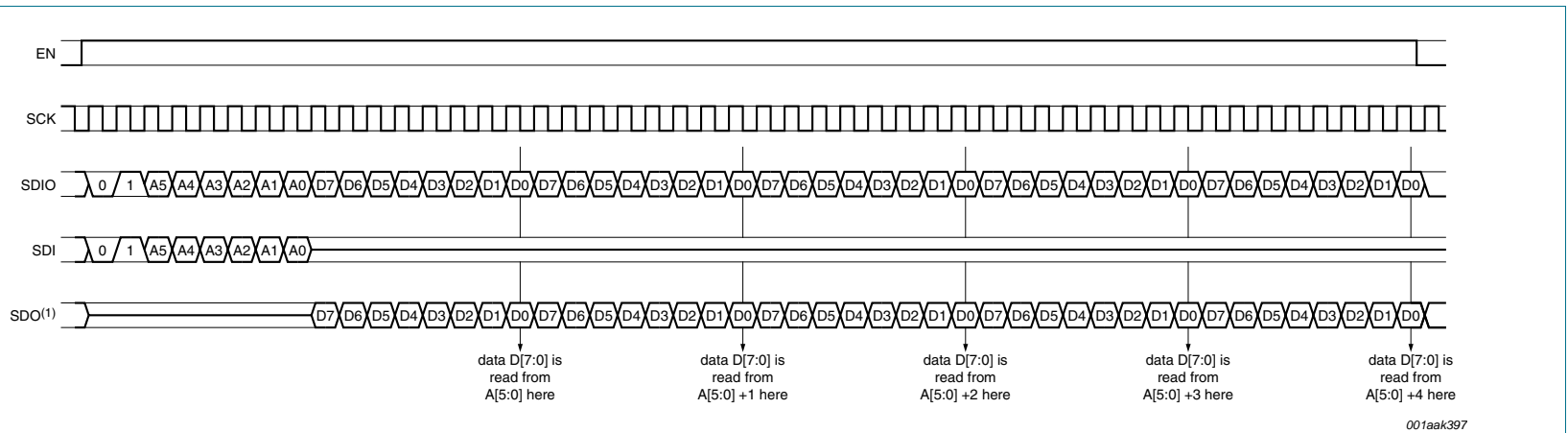


EN must be forced low after registers have been written/read in order to signal end of Write/Read. The diagram shows an example, where 5 successive bytes are stored.

- (1) If configured as data output.

Fig 18. Write serial interface auto-increment timing diagram

6.7.9.6 Read access to SFR with auto-increment function



EN must be forced low after registers have been written/read in order to signal end of Write/Read. The diagram shows an example, where 5 successive bytes are stored.

- (1) If configured as data output.

Fig 19. Read serial interface auto-increment timing diagram

## 6.7.10 Transmit data command

### 6.7.10.1 Transmit configuration

Some transmit-configuration bits must be sent via SPI before every transmit command. (A to F, see [Figure 20 “Transmit data timing diagram”](#)).

Other configuration settings are stored in the registers and the state machine retains them until these bits are altered.

## 6.7.11 Description of the configuration bits

### 6.7.11.1 Synchronization

**Bit A = 1:** Synchronization of the data at the falling or at the rising edge of SCK with the baud rate clock ( $CLK_{ASC}$ ) (also dependent of register setting).

**Bit A = 0:** No synchronization of the transmit-data.

### 6.7.11.2 Power amplifier

The power amplifier is always turned on with the ninth nonsignificant edge of SCK. Configuration bit B is used to turn off the power amplifier.

**Bit B = 1:** The power amplifier is turned off after the falling edge of EN (synchronized with baud rate, if enabled). Data is transmitted after the power amplifier is turned on. During transmission EN must be kept 1 and the data at SDIO is transmitted transparently or synchronized with the baud rate.

**Bit B = 0:** Data transmission starts after the power amplifier is turned on. With the falling edge of EN the actual data bit at SDIO is latched and a constant carrier will be transmitted either in NRZ mode (bit C = 0) or with Manchester coding (bit C = 1) until the power amplifier is turned off.

### 6.7.11.3 Data coding

**Bit C = 1:** Data is XOR d (Manchester generation) with baud rate clock. If C=1 the value of 'A' will be ignored and the data transmission will be done synchronized to the baud rate clock.

**Bit C = 0:** NRZ mode selected.

### 6.7.11.4 Modulation and power settings

**Bit D = 1:** Modulation and amplitude/power settings of ACON1 are applied (according to [Figure 10](#)).

**Bit D = 0:** Modulation and amplitude/power settings of ACON0 are applied (according to [Figure 10](#)).

### 6.7.11.5 Frequency settings

**Bits E, F:** Selection of frequency configuration registers.

Table 35. Frequency selection (Bit E, Bit F)

Bit E	Bit F	FCON
0	0	FCC1H, FCC1L, F1C16, F1C17
0	1	FCC2H, FCC2L, F2C16, F2C17
1	0	FCC3H, FCC3L, F3C16, F3C17
1	1	FCC4H, FCC4L, F4C16, F4C17

6.7.11.6 Transmission command

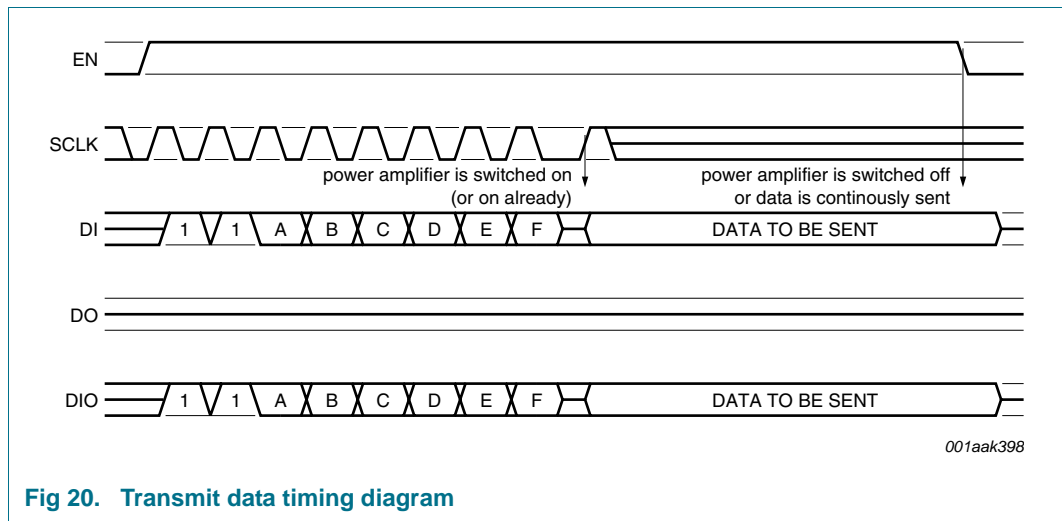


Fig 20. Transmit data timing diagram

A to F contain configuration information for the transmit-operation.

6.7.11.7 Transparent data transmission (example)

**Bit A = 0:** no synchronization of the transmit data

**Bit B = 1:** The power amplifier is turned off after the falling edge of EN. Data is transmitted after the power amplifier is turned on. During transmission EN must be kept 1 and the data at SDIO is transmitted transparently.

**Bit C = 0:** NRZ mode selected.

**Bit D = 0:** Modulation and amplitude/power settings of ACON0 are applied (according to [Figure 10](#)).

**Bit E = 0, F = 0:** selection of frequency configuration register FC1.

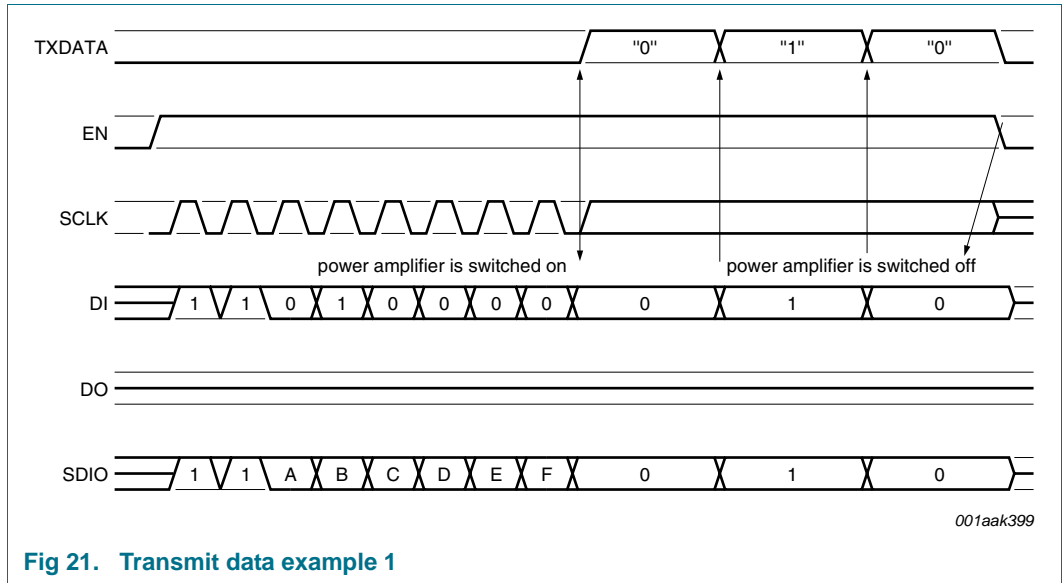


Fig 21. Transmit data example 1

#### 6.7.11.8 Synchronized data transmission (example):

**Phase 1:** Data transmission (See [Figure 22](#))

**Bit A = 1:** Synchronization of the data with the baud rate clock  $CLK_{ASC}$  (= afterscaler clock output, see [Figure 13](#))

**Bit B = 0:** Data transmission starts after the power amplifier is turned on. With the falling edge of EN the actual data bit at SDIO is latched and a constant carrier will be transmitted with Manchester coding (bit C = 1) until the power amplifier is turned off.

**Bit C = 1:** Data is XOR'd (Manchester generation) with baud rate clock. The value of 'A' will be ignored and the data transmission will be done synchronized to the baud rate clock.

**Bit D = 0:** Modulation and amplitude/power settings of ACON0 are applied (according to [Figure 10](#)).

**Bit E = 0, F = 0:** selection of frequency configuration register FC1.

**Phase 2:** End of data transmission (See [Figure 22](#))

**Bit A = 1:** Data synchronization with the baud rate clock  $CLK_{ASC}$  (= afterscaler clock output, see [Figure 14](#))

**Bit B = 1:** The power amplifier is turned off after falling edge of EN (synchronized with baud rate). Data is transmitted after the power amplifier is turned on. During transmission EN must be kept 1 and the data at SDIO is transmitted synchronized with the baud rate.

**Bit C = 1:** Data is XOR'd (Manchester generation) with baud rate clock. The value of 'A' will be ignored and the data transmission will be done synchronized to the baud rate clock.

**Bit D = 0:** Modulation and amplitude/power settings of ACON0 are applied (according to [Figure 10](#)).

**Bit E = 0, F = 0:** Selection of frequency configuration register FC1.

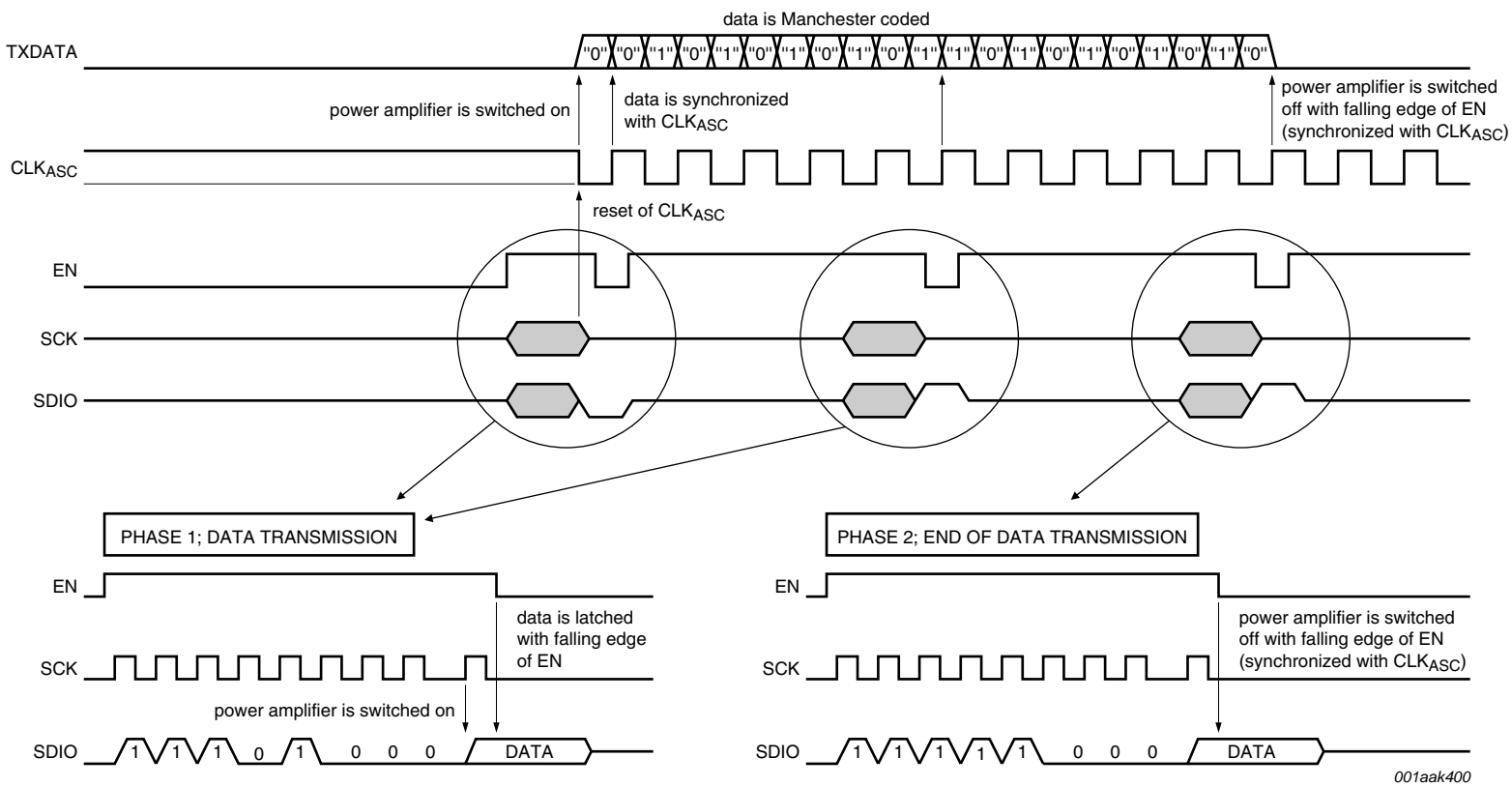


Fig 22. Transmit data example 2



## 7. Limiting values

**Table 36. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>IO</sub>	input/output voltage	any I/O pin and pins: V <sub>DD</sub> , V <sub>REG</sub> , V <sub>DDA</sub> , V <sub>DDPA</sub> to V <sub>SS</sub> , V <sub>SSA</sub> , V <sub>SSPA</sub>	-0.5	+3.6	V
		any I/O pin to V <sub>SS</sub>	-0.5	V <sub>DD</sub> + 0.3	V
		pin PAOUT to V <sub>SS(PA)</sub>	-0.5	+7.2	V
I <sub>oM</sub>	peak output current	I/O pins	-	15	mA
I <sub>lu</sub>	latch-up current		[1]	100	mA
V <sub>ESD</sub>	electrostatic discharge voltage	human body model	[2]	2	kV
		machine model	[3]	200	V
P	power dissipation		-	120	mW
T <sub>amb</sub>	ambient temperature	package HVQFN16	-25	+85	°C
T <sub>stg</sub>	storage temperature		-55	+125	°C

[1] According to JEDEC, JESD 78.

[2] According to JEDEC, JESD 22-A114.

[3] According to JEDEC, JESD 22-A115.

## 8. Characteristics

**Table 37. Characteristics**

T<sub>amb</sub> = -25 °C to +85 °C, V<sub>DD</sub> = 2.7 V, V<sub>SS</sub> = 0 V; capacitor (47 nF) connected between V<sub>REG</sub> and V<sub>SS</sub> (unless otherwise specified).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>DD</sub>	supply voltage		1.7	-	3.6	V
		XTAL oscillator	1.7	-	3.6	V
		PLL	[1]	2.1	-	3.6
f <sub>TX</sub>	transmitter frequency	package HVQFN16	300	-	920	MHz
f <sub>VCO</sub>	VCO frequency		300	-	920	MHz
f <sub>xtal</sub>	crystal frequency		9	-	19	MHz

### Power fail detection

V <sub>uvd</sub>	undervoltage detection voltage	ENRAD = 0; T <sub>amb</sub> = 25 °C	1.85	2.0	2.15	V
		ENRAD = 1; f <sub>PLL</sub> = 868 MHz				
		T <sub>amb</sub> = -25 °C	-	2.0	2.25	V
		T <sub>amb</sub> = +25 °C	-	1.95	-	V
		T <sub>amb</sub> = +85 °C	1.7	1.9	-	V
		ENRAD = 1; f <sub>PLL</sub> = 630 MHz				
		T <sub>amb</sub> = -25 °C	-	1.8	2.0	V
		T <sub>amb</sub> = +25 °C	-	1.75	-	V
		T <sub>amb</sub> = +85 °C	1.5	1.7	-	V
t <sub>lat(det)</sub>	detection latency time	power fail	-	0.5	1	μs

**Table 37. Characteristics ...continued**

$T_{amb} = -25\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ ,  $V_{DD} = 2.7\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ; capacitor (47 nF) connected between VREG and  $V_{SS}$  (unless otherwise specified).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Voltage regulator</b>						
$t_{d(\text{start})}$	start delay time		-	5	20	$\mu\text{s}$
$C_{VREG}$	capacitance on pin VREG		[1] 22	47	-	nF

- [1] The available supply voltage range can be extended using the undervoltage detection circuitry in adaptive mode. If enabled, the minimum PLL supply voltage corresponds with the actual undervoltage detection voltage ( $V_{uvd}$ ), which is a function of the PLL frequency ( $f_{PLL}$ ).

**Table 38. Current consumption**

$T_{amb} = -25\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ ,  $V_{DD} = 2.7\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ; capacitor (47 nF) connected between VREG and  $V_{SS}$  (unless otherwise specified).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Power-down</b>						
$I_{DD}$	supply current	power-down mode	-	50	1000	nA
<b>XTAL active</b>						
$I_{DD}$	supply current	XTAL on, PLL off, PA off				
		$f_{xtal} = 9.18\text{ MHz}$	-	180	380	$\mu\text{A}$
		$f_{xtal} = 13.08\text{ MHz}$	-	250	450	$\mu\text{A}$
		$f_{xtal} = 18.37\text{ MHz}$	-	270	550	$\mu\text{A}$
		crystal oscillator start-up	-	-	6	mA
<b>PLL active, ENRAD = 0</b>						
$I_{DD}$	supply current	XTAL on, PLL on, PA off	[1][2]			
		$f_{PLL} = 434\text{ MHz}$	-	1.3	2.0	mA
		$f_{PLL} = 630\text{ MHz}$	-	1.9	2.9	mA
		$f_{PLL} = 869\text{ MHz}$	-	2.7	4.0	mA
<b>Transmitter active, PAM = 2, AMH = '1111', CASC = 1</b>						
$I_{DD}$	supply current	XTAL on, PLL on, PA on	[3]			
		$f_{TX} = 315\text{ MHz}$ ; $f_{PLL} = 630\text{ MHz}$	5.5	7.0	8.5	mA
		$f_{TX} = 434\text{ MHz}$ ; $f_{PLL} = 869\text{ MHz}$	6.8	8.8	10.8	mA
		$f_{TX} = 869\text{ MHz}$	6.5	8.5	10.5	mA
<b>Transmitter active, PAM = 3, AMH = '1111', CASC = 0</b>						
$I_{DD}$	supply current	XTAL on, PLL on, PA on	[3][4]			
		$f_{TX} = 315\text{ MHz}$ ; $f_{PLL} = 630\text{ MHz}$	7.5	11.5	17.6	mA
		$f_{TX} = 434\text{ MHz}$ ; $f_{PLL} = 869\text{ MHz}$	8.0	12.0	19.0	mA
		$f_{TX} = 868\text{ MHz}$	10.0	14.5	19.0	mA

- [1] Total current consumption when the PLL is running is  $I_{DD}$  (XTAL active) +  $\Delta I_{DD}$  (PLL active)

- [2] PLL supply current may be reduced slightly (single digit percent range) by selecting the adaptive voltage regulator mode (ENRAD = 1).

- [3] Load tank circuit according to [Figure 23](#).

- [4] Maximum power setting.

## 8.1 Serial interface characteristics

**Table 39. I/O pins (SCK, EN, SDIO, SDO, CKOUT)**

$T_{amb} = -25\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ ,  $V_{DD} = 2.7\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ; capacitor (47 nF) connected between VREG and  $V_{SS}$  (unless otherwise specified).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL}$	LOW-level input voltage		-0.1	-	$0.2V_{DD}$	V
$V_{IH}$	HIGH-level input voltage		$0.8V_{DD}$	-	$V_{DD} + 0.1$	V
$I_{IL}$	LOW-level input current	$V_{IL} = 0\text{ V}$	-	-	0.5	$\mu\text{A}$
$I_{IH}$	HIGH-level input current	$V_{IH} = V_{DD}$	-	-	0.5	$\mu\text{A}$
$V_{OL}$	LOW-level output voltage	$I_O = 4\text{ mA}$	-	-	0.4	V
$V_{OH}$	HIGH-level output voltage	$I_O = -4\text{ mA}$	$V_{DD} - 0.4$	-	-	V
$C_i$	input capacitance	on any pin; $V_{IN} = 0.1\text{ V RMS}$ ; $f = 1\text{ MHz}$	-	1.6	2	pF

**Table 40. Timing specifications**

$T_{amb} = -25\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ ,  $V_{SS} = 0\text{ V}$ ; capacitor (47 nF) connected between VREG and  $V_{SS}$  (unless otherwise specified).

Symbol	Parameter	Conditions	Min	Max	Unit
<b>pin SCK (input clock)</b>					
$f_{i(\text{clk})}$	clock input frequency		-	2	MHz
$t_{w(\text{clk})}$	clock pulse width		200	-	ns
$t_{r(\text{clk})}$	clock rise time		-	50	ns
$t_{f(\text{clk})}$	clock fall time		-	50	ns
<b>pin EN (enable)</b>					
$t_{w(\text{EN})}$	pulse width on pin EN		500	-	ns
$t_r$	rise time		-	50	ns
$t_f$	fall time		-	50	ns
<b>pin SDIO (serial data)</b>					
$t_{su(\text{SDIO})}$	SDIO set-up time		[1] -	20	ns
$t_{h(\text{SDIO})}$	SDIO hold time		[2] -	20	ns
$t_{v(\text{SDO})}$	SDO valid time		[3] -	50	ns

[1] Minimum time SDIO must be settled before clock edge.

[2] Minimum time SDIO must be hold after clock edge.

[3] Settling time of SDO after clock edge (only for 4-wire interface).

**Table 41. Transmitter AC/DC conditions**

$T_{amb} = -25\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ ,  $V_{DD} = 2.7\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ; capacitor (47 nF) connected between VREG and  $V_{SS}$  (unless otherwise specified).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>XTAL oscillator</b>						
$R_s$	series resistance	start-up margin; $T_{amb} = 25\text{ }^{\circ}\text{C}$ ; $C1 = C2 = 15\text{ pF}$	[1][2][3]			
		$f_{\text{xtal}} = 9.18\text{ MHz}$	2.2	4.1	-	$\text{k}\Omega$
		$f_{\text{xtal}} = 13.08\text{ MHz}$	1.4	2.5	-	$\text{k}\Omega$
		$f_{\text{xtal}} = 18.37\text{ MHz}$	700	1300	-	$\Omega$

**Table 41. Transmitter AC/DC conditions ...continued**

$T_{amb} = -25\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ ,  $V_{DD} = 2.7\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ; capacitor (47 nF) connected between VREG and  $V_{SS}$  (unless otherwise specified).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$C_i$	input capacitance	pin XTAL1; $T_{amb} = 25\text{ }^{\circ}\text{C}$	-	3.5	3.9	pF	
		pin XTAL2; $T_{amb} = 25\text{ }^{\circ}\text{C}$	-	2.1	2.9	pF	
$t_s$	settling time		-	0.5	1.5	ms	
<b>PLL synthesizer</b>							
$B_{PLL(loop)}$	PLL loop bandwidth	$f_{xtal} = 9.18\text{ MHz}$	[4]	-	50	-	kHz
		$f_{xtal} = 13.08\text{ MHz}$	-	-	70	-	kHz
		$f_{xtal} = 18.37\text{ MHz}$	-	-	100	-	kHz
$\varphi_n$	phase noise	PAM = 3; AMH = '1111'; CASC = 0; $f_{TX} = 315\text{ MHz}$ and $f_{TX} = 434\text{ MHz}$	[5]	-	-	-	
		10 kHz offset	-	-78	-72	dBc/Hz	
		100 kHz offset	-	-76	-70	dBc/Hz	
		1 MHz offset	-	-87	-81	dBc/Hz	
$\varphi_n$	phase noise	PAM = 3; AMH = '1111'; CASC = 0; $f_{TX} = 869\text{ MHz}$	[6]	-	-	-	
		10 kHz offset	-	-81	-75	dBc/Hz	
		100 kHz offset	-	-79	-73	dBc/Hz	
		1 MHz offset	-	-90	-84	dBc/Hz	
$\alpha_{resp(sp)}$	spurious response	PAM = 2, AMH = '1111'; CASC = 1; $f_{TX} \pm f_{xtal}$		-	-	-	
		$f_{TX} = 315\text{ MHz}$ ; $f_{xtal} = 18.37\text{ MHz}$	-	-42	-32	dBc	
		$f_{TX} = 434\text{ MHz}$ ; $f_{xtal} = 13.08\text{ MHz}$	-	-43	-33	dBc	
		$f_{TX} = 869\text{ MHz}$ ; $f_{xtal} = 13.08\text{ MHz}$	[6]	-46	-34	dBc	
$t_{acq}$	acquisition time		-	0.1	0.5	ms	
<b>Power amplifier[5]</b>							
$P_{O(max)}$	maximum output power	PAM = 3; AMH = '1111'; CASC = 0; $V_{DD} = 3.6\text{ V}$ ; $T_{amb} = 25\text{ }^{\circ}\text{C}$		-	-	-	
		$f_{out} = 315\text{ MHz}$	-	-	12	dBm	
		$f_{out} = 434\text{ MHz}$	-	-	12	dBm	
$P_{O(nom)}$	nominal output power	PAM = 2, AMH = '1111'; CASC = 1; $T_{amb} = 25\text{ }^{\circ}\text{C}$		-	-	-	
		$f_{out} = 315\text{ MHz}$ ; $f_{PLL} = 630\text{ MHz}$	3.0	4.7	6.4	dBm	
		$f_{out} = 434\text{ MHz}$ ; $f_{PLL} = 869\text{ MHz}$	4.3	6	7.7	dBm	
$\Delta P_o$	output power variation	$P_o$ as a function of supply voltage; $V_{DD} = 2.1\text{ V}$ to $3.6\text{ V}$ ; PAM = 2; AMH = '1111'; CASC = 1; $T_{amb} = 25\text{ }^{\circ}\text{C}$	-1.5	-	+0.8	dBm	
		$P_o$ as a function of temperature; PAM = 2; AMH = '1111'; CASC = 1	-1.2	-	+1.2	dBm	

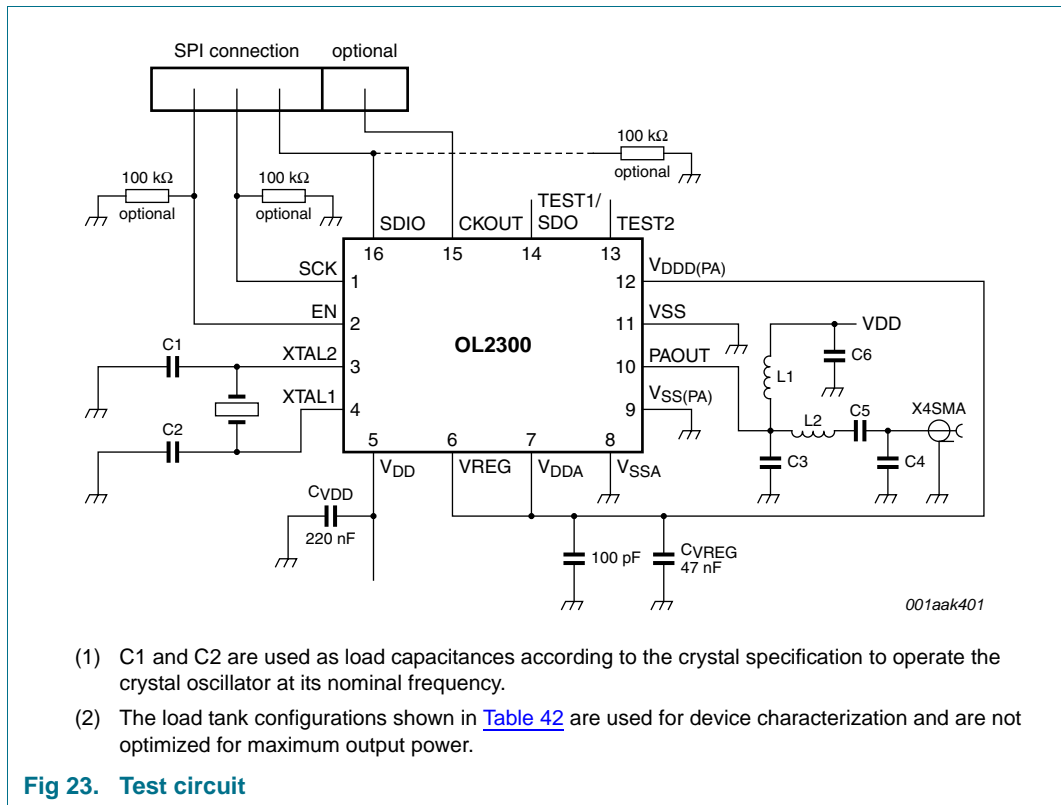
**Table 41. Transmitter AC/DC conditions ...continued**

$T_{amb} = -25\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ ,  $V_{DD} = 2.7\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ; capacitor (47 nF) connected between VREG and  $V_{SS}$  (unless otherwise specified).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Modulation<sup>[7]</sup></b>						
$f_{mod}$	modulation frequency	ASK	-	-	56	kHz
		FSK	-	-	56	kHz

- [1] Maximum resistance that can be put in series with the crystal without causing oscillation dropouts
- [2] The given  $R_s$  (Oscillation margin) is tested and guaranteed only at room temperature ( $T_{amb} = 25\text{ }^{\circ}\text{C}$ ). The minimum value occurs at high temperature and a minimum supply voltage of  $V_{DD} = 2.1\text{ V}$ .
- [3] To guarantee sufficient oscillation start-up margin every reference application board must be individually checked by the customer.
- [4] Derived from simulation, not tested.
- [5] Load tank circuit according to [Figure 23](#).
- [6] Valid only for HVQFN16 package at 869 MHz.
- [7] The value of general supply block capacitor  $C_{VDD}$  should be at least 2 times that of  $C_{VREG}$ .

## 9. Test information



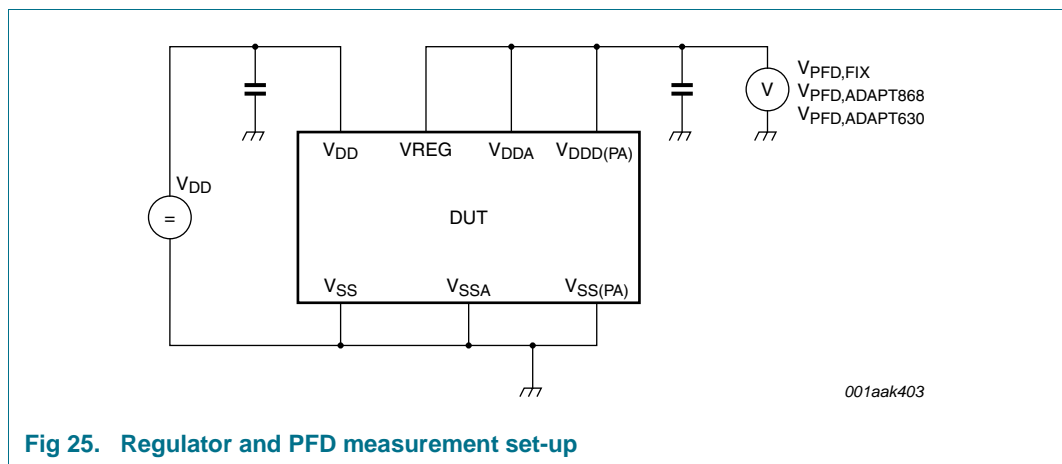
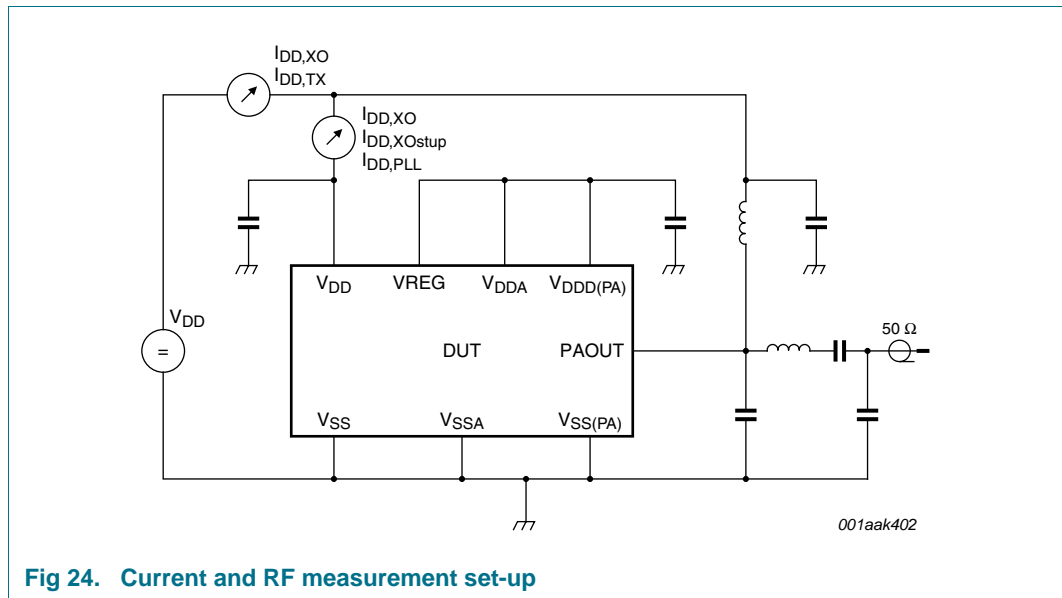
**Table 42. Load tank circuit configuration for ~200 Ω**

Component	315 MHz	434 MHz	868 MHz
L1	82 nH	68 nH	47 nH
L2	47 nH	27 nH	10 nH
C3	~5.6 pF	~4.1 pF	~2.2 pF

Table 42. Load tank circuit configuration for ~200 Ω ...continued

Component	315 MHz	434 MHz	868 MHz
C4	6.8 pF	4.7 pF	5.6 pF
C5	47 pF	27 pF	15 pF
C6	100 pF	100 pF	100 pF

9.1 Test setup



10. Package outline

HVQFN16: plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 3 x 3 x 0.85 mm

SOT758-1

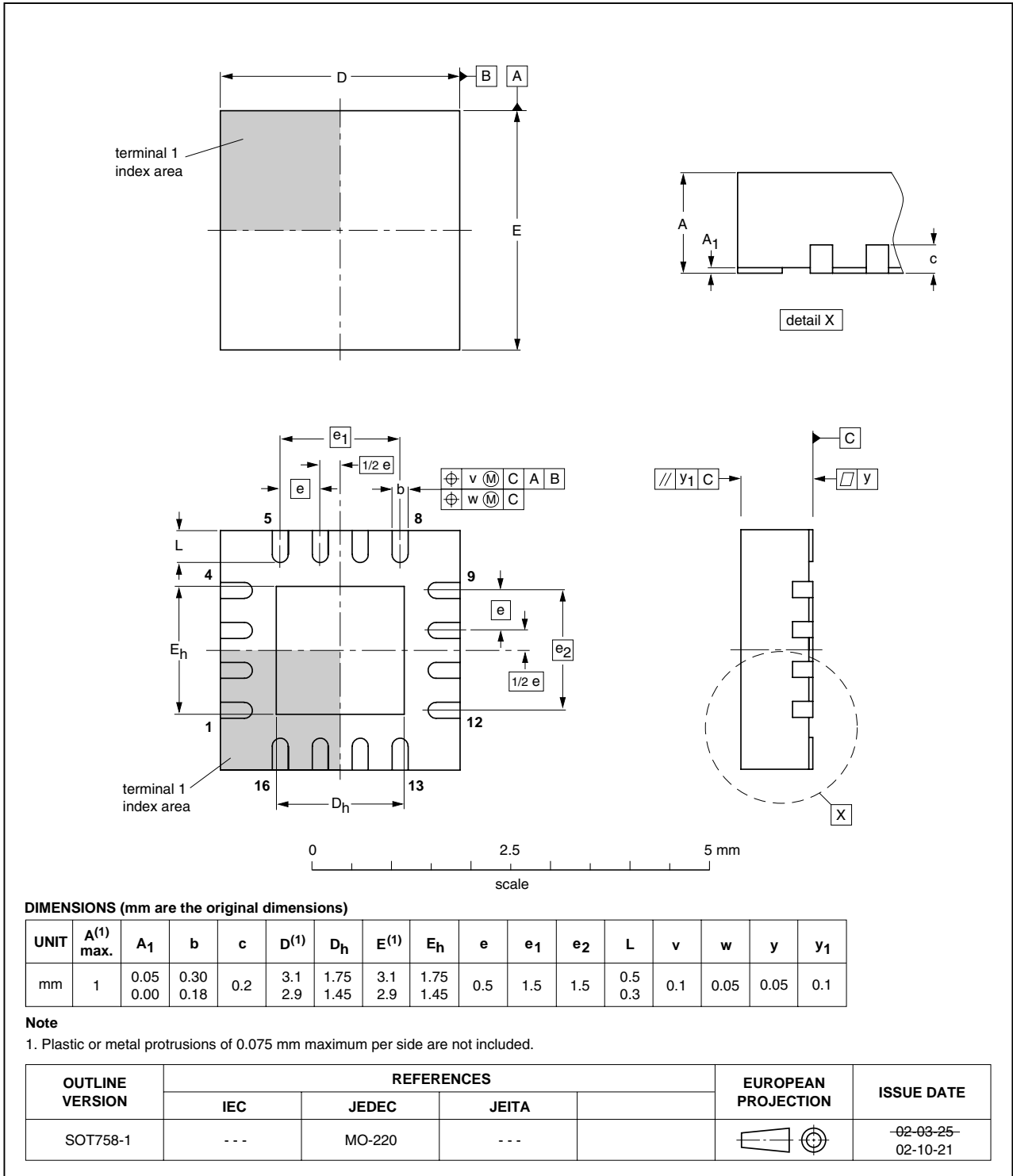


Fig 26. Package outline SOT758-1 (HVQFN16)

## 11. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

### 11.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 11.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 11.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities



## 11.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 27](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 43](#) and [44](#)

**Table 43. SnPb eutectic process (from J-STD-020C)**

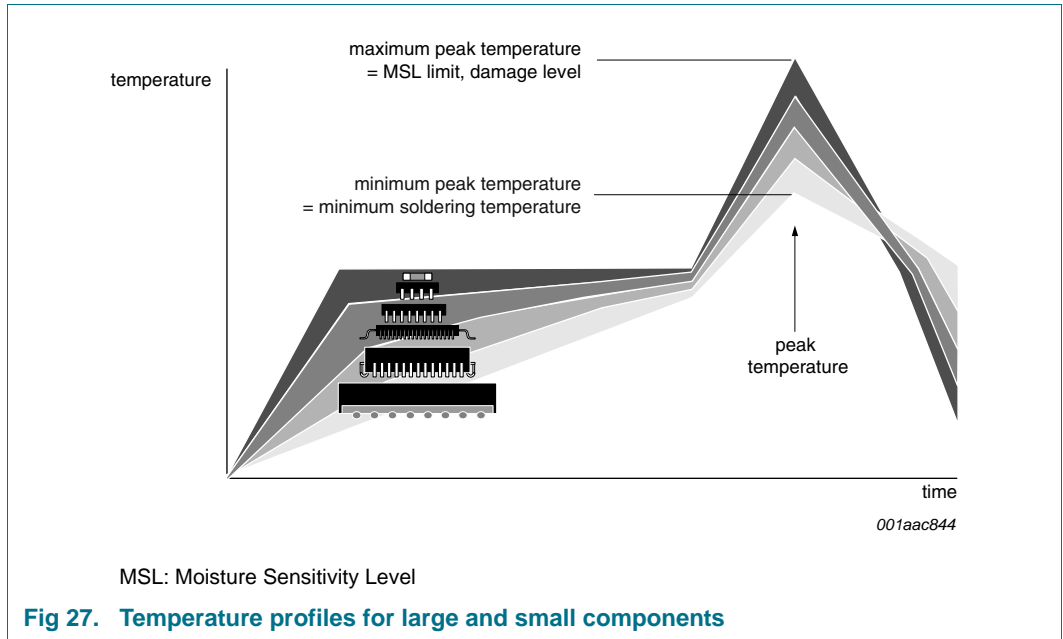
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm <sup>3</sup> )	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

**Table 44. Lead-free process (from J-STD-020C)**

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm <sup>3</sup> )		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 27](#).



For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

## 12. Abbreviations

Table 45. Abbreviations

Acronym	Description
ASK	Amplitude-Shift Keying
FSK	Frequency-Shift Keying
ISM	Industrial Scientific Medical
OOK	ON-Off Keying
PLL	Phase-Locked Loop
SPI	Serial Peripheral Interface
SRD	Short Range Devices
VCO	Voltage Controlled Oscillator
CMOS	Complementary Metal-Oxide Semiconductor
IF	Intermediate Frequency
NMOS	Negative Metal-Oxide Semiconductor
NRZ	Non-Return to Zero
PCB	Printed-Circuit Board
SRD	Short Range Devices

## 13. Revision history

Table 46. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
OL2300 v.2	20101028	Product data sheet	-	OL2300 v.1
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Section 1</a>: corrected the chip rate to 112 kcps</li> <li>• <a href="#">Figure 1</a>: "Antenna Tuning" block removed</li> <li>• <a href="#">Table 41</a>: modulation frequency changed to <math>f_{\text{mod}} = 56 \text{ kHz}</math></li> <li>• <math>T_{\text{amb}} = -25 \text{ }^{\circ}\text{C}</math> to <math>+85 \text{ }^{\circ}\text{C}</math> throughout the document</li> </ul>			
OL2300 v.1	20091116	Product data sheet	-	-

## 14. Legal information

### 14.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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Date of release: 28 October 2010

Document identifier: OL2300

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