PCA9452

Power management IC for i.MX 93 application processor

Rev. 1.0 — 27 September 2023 **Product data sheet**

1 General description

The PCA9452 is a single chip AEC Q100 grade 2 automotive Power Management IC (PMIC) specifically designed to support i.MX 93x family processor in automotive applications.

The device provides six high efficiency step-down regulators, five LDOs, one 400 mA load switch, 2-channel level translator and 32.768 kHz crystal oscillator driver. Three buck regulators support dynamic voltage scaling (DVS) feature along with programmable ramping up and down time and those buck regulators support remote sense to compensate IR drop to load from buck regulator. This device is characterized across -40 °C to 105 °C ambient temperature range.

Six step-down regulators are designed to providing power for i.MX 93x application processor and DRAM memory. The LDO1 features very low quiescent current to provide power for Secure Non-Volatile Storage (SNVS) since this LDO is always ON when input voltage is valid.

The PCA9452 integrates logic translator which is a 2-bit, dual supply translating transceiver with auto direction sensing. It enables bidirectional voltage level translation. It can be used as I2C level translator. The 400 mA load switch is to supply 3.3 V power supply to SD card, which has internal discharge resistor.

The PCA9452 is offered in 56-pin HVQFN package, 8 mm x 8 mm, 0.5 mm pitch.

2 Features and benefits

- AEC Q100 grade 2 compliant
- Six High Efficiency step down regulators
  - One 6 A dual-phase buck regulator with DVS feature and remote sense (BUCK1 and BUCK3 work in dual-phase mode)
  - One 3 A buck regulators with DVS feature and remote sense
  - One 3 A buck regulator
  - Two 2 A buck regulators
- Five Linear regulators
  - Two 10 mA LDOs
  - One 150 mA LDO
  - One 200 mA LDO
  - One 300 mA LDO
- 400 mA Load Switch with a built-in active discharge resistor
- 32.768 kHz Crystal oscillator driver and buffer output
- Two channel logic level translator
- Power control IO
  - Power ON/OFF control
  - Standby/Run mode control
- Fm+ 1 MHz I^2C-bus interface
- ESD protection
  - Human Body Model (HBM) : +/- 2000 V

  - Charged Device Model (CDM) : +/-500 V
- 8 mm x 8 mm, 56 pin HVQFN with 0.5 mm pitch

3 Applications

- Automotive infotainment
- Heads up display (HUD)
- GPS
- Monitoring system

4 Ordering information

Table 1. Ordering information

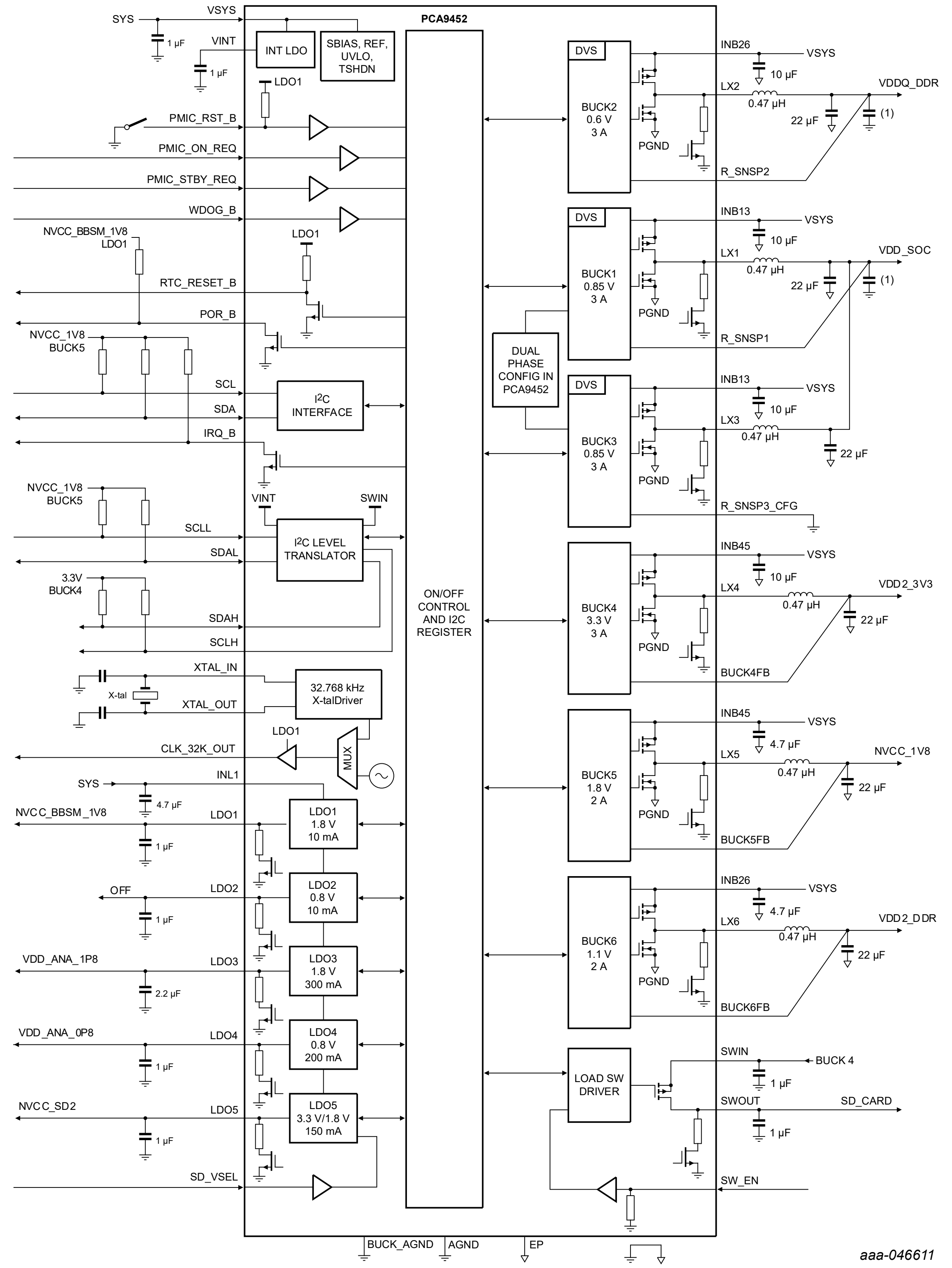
Type number	Topside marking	AP platform	Package		
			Name	Description	Version
PCA9452AHN	PCA9452A	i.MX 93x auto	HVQFN56	plastic thermal enhanced very thin quad flat package; no leads; 56 terminals; body 8 x 8 x 0.85 mm	SOT684-30(DD)

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Ambient Temperature range
PCA9452AHN	PCA9452AHNMP	HVQFN56	REEL 13" Q2 DP	2000	-40 °C to +105 °C
PCA9452AHN	PCA9452AHNK	HVQFN56	TRAY MULTIPLE DP BAKEABLE	1300	-40 °C to +105 °C
PCA9452AHN	PCA9452AHNE	HVQFN56	ONE TRAY DP BAKEABLE	260	-40 °C to +105 °C

5 Block diagram



(1) Decoupling capacitor in MCU side.

Figure 1. Block diagram

6 Pinning information

6.1 Pinning

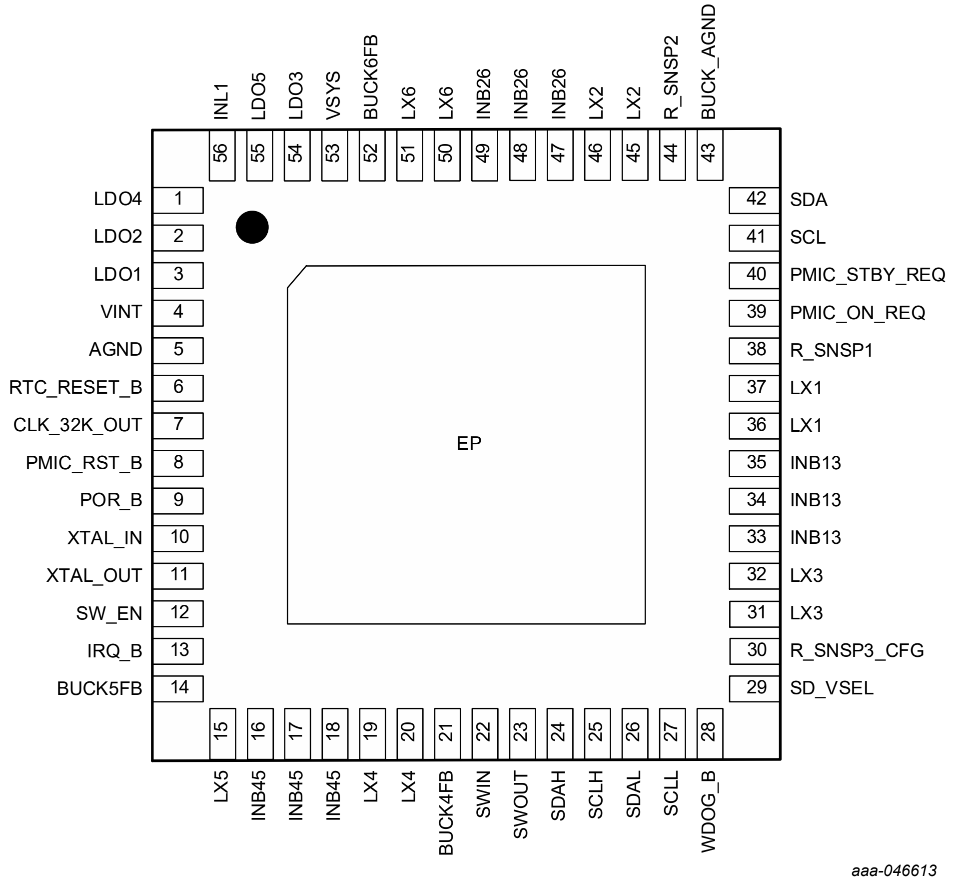


Figure 2. PCA9452 pin map – top view

6.2 Pin description

Table 3. Pin description

Pin description			
Symbol	**Pin**	**Type**	**Description**
LDO4	1	P	LDO4 output. Bypass with a 1 µF to Ground.
LDO2	2	P	LDO2 output. Bypass with a 1 µF to Ground.
LDO1	3	P	LDO1 output. Bypass with a 1 µF to Ground.
VINT	4	P	Internal Power supply output pin. Bypass with 1 µF to Ground.
AGND	5	GND	Analog ground pin. It should be connected to ground plane through Via. Do not short to EP directly on top layer
RTC_RESET_B	6	DO	Reset output pin. It is High-Z after LDO1 voltage is good. It is internally pulled up with LDO1 power rail
CLK_32K_OUT	7	DO	32.768 kHz clock CMOS output with LDO1 power rail.

Table 3. Pin description*...continued*

Pin description			
Symbol	**Pin**	**Type**	**Description**
PMIC_RST_B	8	DI	PMIC reset input pin. It is internally pulled up with LDO1 power rail. Once it is asserted LOW, PMIC performs reset.
POR_B	9	DO	Power On reset output pin. Open drain output requiring external pull up resistor.
XTAL_IN	10	AI	32.768 kHz crystal oscillator input, tie to GND if X-tal is not used
XTAL_OUT	11	AO	32.768 kHz crystal oscillator output, leave float if X-tal is not used
SW_EN	12	DI	Load switch enable input pin. It has internal 1.5 MΩ pull down resistor.
IRQ_B	13	DO	Open drain output to indicate Interrupt issued.
BUCK5FB	14	AI	Buck5 output voltage sensing pin
LX5	15	P	Buck5 switching node
INB45	16,17,18	P	Buck4 / Buck5 Input pins. Bypass with 10 μF and 4.7 μF to Ground
LX4	19,20	P	Buck4 switching node
BUCK4FB	21	AI	Buck4 output voltage sensing pin
SWIN	22	P	Load switch input pin, Bypass with a 1 μF to Ground.
SWOUT	23	P	Load switch output pin, Bypass with a 1 μF to Ground.
SDAH	24	DIO	Level translator high voltage IO pin, SDA referenced to SWIN, 3.3 V
SCLH	25	DO	Level translator high voltage IO pin, SCL referenced to SWIN, 3.3 V
SDAL	26	DIO	Level translator low voltage IO pin, SDA referenced to VINT, 1.8 V
SCLL	27	DO	Level translator low voltage IO pin, SCL referenced to VINT, 1.8 V
WDOG_B	28	DI	Active LOW watchdog reset input pin from application processor.
SD_VSEL	29	DI	LDO5 voltage selection input pin. LDO5 output is 3.3 V when it is driven LOW and 1.8 V when driven HIGH.
R_SNSP3_CFG	30	AI	Buck3 output voltage remote sense pin. This pin is tied to GND where Buck1 and Buck3 are configured as dual phase buck regulator.
LX3	31,32	P	Buck3 switching node If BUCK3 is not used by shorting R_SNSP3_CFG to VSYS, leave LX3 pins floating.
INB13	33,34,35	P	Buck1 / Buck3 Input. Bypass with two 10 μF to Ground
LX1	36,37	P	Buck1 switching node
R_SNSP1	38	AI	Buck1 output voltage remote sensing pin
PMIC_ON_REQ	39	DI	PMIC ON input from Application processor. When it is asserted HIGH, the device starts power on sequence.
PMIC_STBY_REQ	40	DI	Standby mode input from Application processor. When it is asserted HIGH, device enters STANDBY mode.
SCL	41	DI	I^2C serial clock pin
SDA	42	DIO	I^2C serial data pin
BUCK_AGND	43	GND	Buck reference GND for BUCK1,2,3. It should be connected to ground plane through Via. Do not short to EP directly on top layer

Table 3. Pin description*...continued*

Pin description			
Symbol	**Pin**	**Type**	**Description**
R_SNSP2	44	AI	Buck2 output voltage remote sensing pin
LX2	45,46	P	Buck2 switching node
INB26	47,48,49	P	Buck2 / Buck6 Input. Bypass with 10 µF and 4.7 µF to Ground
LX6	50,51	P	Buck6 switching node
BUCK6FB	52	AI	Buck6 output voltage sensing pin
VSYS	53	P	Internal power input. Bypass with a 1 µF to Ground
LDO3	54	P	LDO3 output. Bypass with a 2.2 µF to Ground.
LDO5	55	P	LDO5 output. Bypass with a 1 µF to Ground.
INL1	56	P	Power input pin for LDO1, LDO2, LDO3, LDO4 and LDO5. Bypass with a 4.7 µF to Ground.
EP		GND	Exposed PAD. All bucks’ PGND are internally connected.

7 Functional description

7.1 Features

The PCA9452 is an automotive power management integrated circuit (PMIC) designed to be the primary power management for NXP application processors i.MX 93x.

- Buck regulators
  - BUCK1/BUCK3: Dual-phase, 0.65 V to 2.2375 V, 12.5 mV step, 6000 mA
  - BUCK2: 0.6 V to 2.1875 V, 12.5 mV step, 3000 mA
  - BUCK4: 0.6 V to 3.4 V, 25 mV step, 3000 mA
  - BUCK5, BUCK6: 0.6 V to 3.4 V, 25 mV step, 2000 mA
  - Dynamic Voltage scaling on BUCK1, BUCK2 and BUCK3
  - Support remote sensing on BUCK1, BUCK2 and BUCK3
  - Monitor fault condition
- LDO regulators
  - LDO1, 1.6 V to 1.9 V, 3.0 V to 3.3 V 100 mV step, 10 mA
  - LDO2, 0.8 V to 1.15 V with 50 mV step, 10 mA
  - LDO3, 0.8 V to 3.3 V with 100 mV step, 300 mA
  - LDO4, 0.8 V to 3.3 V with 100 mV step, 200 mA
  - LDO5, 1.8 V to 3.3 V with 100 mV step, 150 mA, voltage selection through SD_VSEL pin
  - Monitor fault condition
- 400 mA Load switch for SD card
  - Built-in OCP protection
  - GPIO/I^{2}C control
  - Built-in active discharge resistor
- I^{2}C level translator
- 32.768 kHz crystal oscillator driver
  - Mux output with internal 32 kHz output
- Protection and monitoring: Soft start, power rails fault detection, UVLO, thermal shutdown

- Configurable reset from WDOGB, PMIC_RST_B and SW_RST register
- Power control IO
  - PMIC_ON_REQ, PMIC_STBY_REQ
- Fm+ 1 MHz I^2C-bus interface
- Type 3 PCB applicable

7.2 Functional diagram

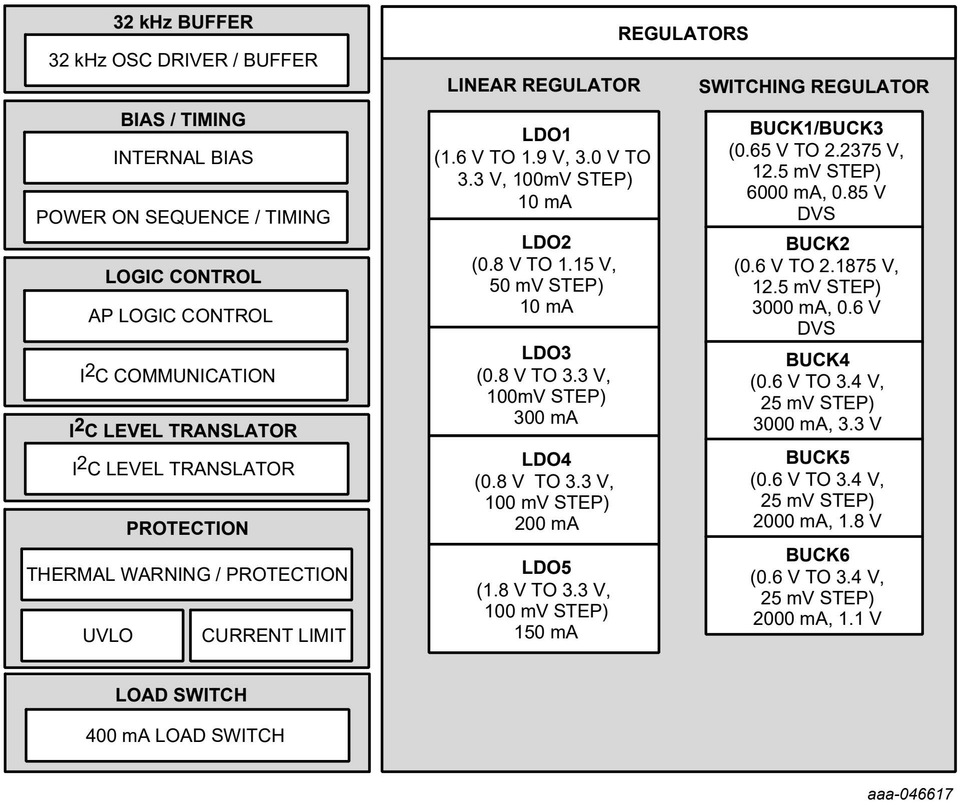


Figure 3. Functional internal block diagram

7.3 Power modes

PCA9452 has eight power modes: OFF, READY, SNVS, RUN, STANDBY, PWRDN, PWRUP and FAULT_SD. Figure 4 shows the state transition diagram showing the conditions to enter and exit each state.

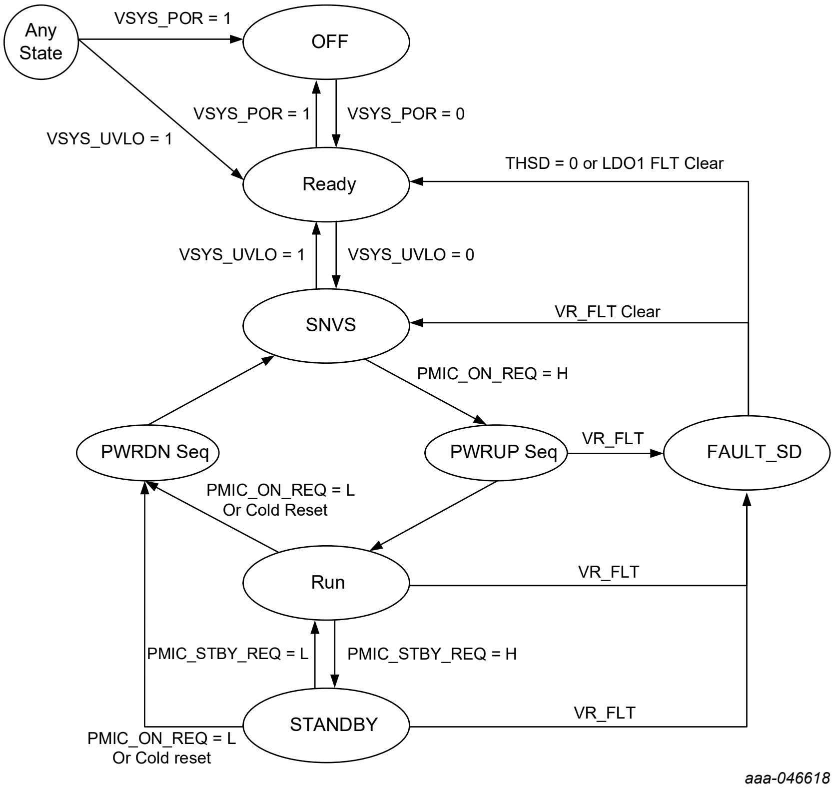


Figure 4. Power states diagram

7.3.1 Off mode

PCA9452 enters OFF mode from any state when VSYS falls below V_{SYS_POR} threshold. All regulators are off and all registers get reset in this mode.

7.3.2 READY mode

PCA9452 enters READY mode from OFF mode when VSYS is higher than V_{SYS_POR}. Internal LDO VINT is enabled and loads MTP data to registers. Once MPT loading is done, it is ready to transition to SNVS mode.

7.3.3 SNVS mode

PCA9452 enters Secure Non-Volatile Storage (SNVS) mode when VSYS exceeds V_{SYS_UVLO} threshold. LDO1 is powered up and 32.768 kHz buffer starts running. RTC_RESET_B is pulled HIGH in t_{RTC_RST} after LDO1 voltage comes up.

PMIC_ON_REQ input is masked until RTC_RESET_B is released. If PMIC_ON_REQ is asserted HIGH in this mode, PCA9452 starts power up sequence.

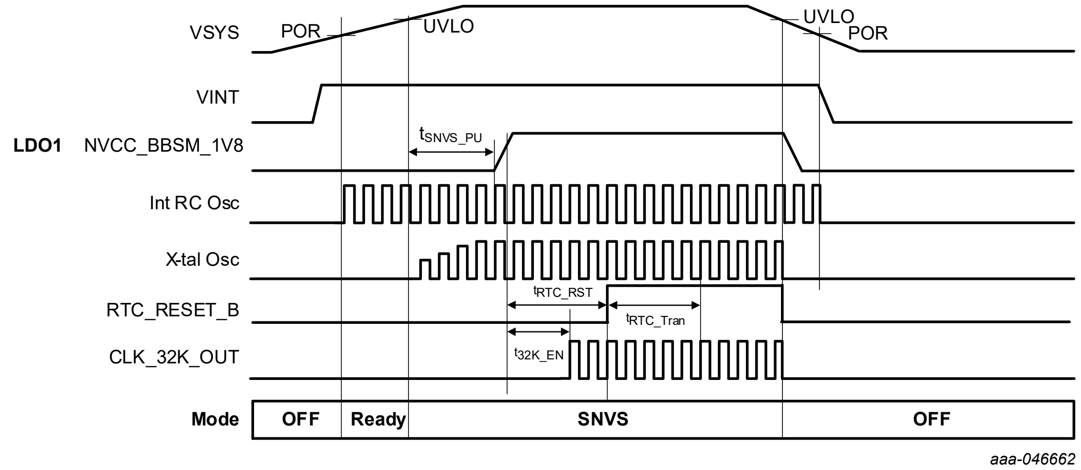


Figure 5. SNVS mode ON/OFF sequence

Table 4. SNVS mode

Time	Description	Value
t_{SNVS_PU}	Time to LDO1 turn on from VSYS UVLO detected	20 ms
t_{RTC_RST}	Time to RTC_RESET_B release from LDO1 POK	20 ms
t_{32K_EN}	Time to 32k buffer Enable from LDO1 POK	10 ms
t_{RTC_Tran}	Time to transition to Xtal output from RC osc after RTC_RESET_B release	1 sec

7.3.4 PWRUP mode

After RTC_RESET_B is released in SNVS mode, it starts power up with pre-defined sequence when PMIC_ON_REQ is asserted HIGH for longer than debounce time, t_{ON_DEB}, which is programmable in PWR_CTRL reg. Buck1 begins turning ON at first and then each power rail is followed with t_{step} after POK of predecessor power rail. During PWRUP mode, PMIC_STBY_REQ signal is masked until POR_B is released. The PWRUP mode ends up releasing POR_B and PCA9452 transitions to RUN mode.

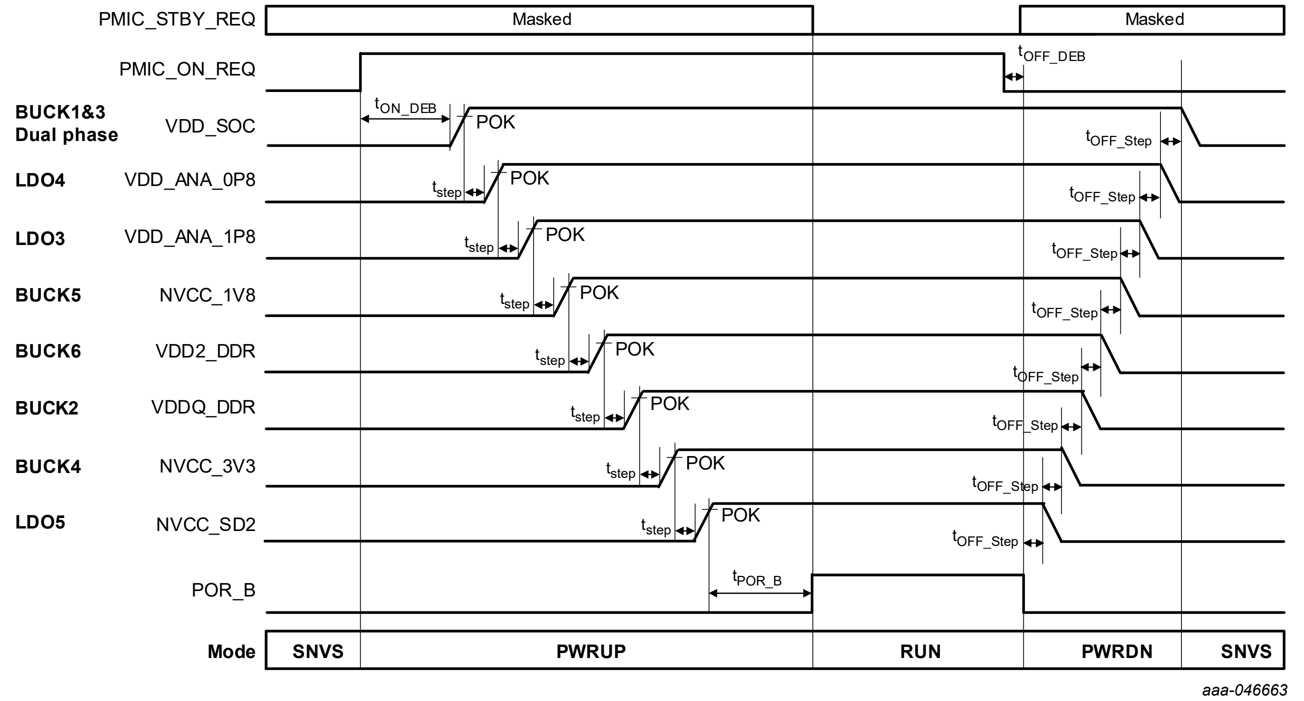


Figure 6. Power ON/OFF sequence

Table 5. Power up sequence

Regulator	PCA9452
LDO1	Always ON, 1.8 V
LDO2	OFF
BUCK1, BUCK3 (Dual Phase)	T1, 0.85 V
BUCK2	T6, 0.6 V
BUCK4	T7, 3.3 V
BUCK5	T4, 1.8 V
BUCK6	T5, 1.1 V
LDO3	T3, 1.8 V
LDO4	T2, 0.8 V
LDO5	T8, 1.8 V/3.3 V

Table 6. PWRUP mode

Time	Description	Value
t_{ON_DEB}	Time to power-on start from PMIC_ON_REQ high	20 ms
t_{STEP}	Time to next power rail ON from prev rail POK	2 ms
t_{PORB}	Time to POR_B release from the last rail POK	20 ms
t_{OFF_STEP}	Time to next power rail off from prev rail off	8 ms

Table 6. PWRUP mode*...continued*

Time	Description	Value
t_{OFF_DEB}	Time to POR_B low from PMIC_ON_REQ falling	120 µs

If any of regulators does not generate POK within $t_{FLT\_SH\_PU}$ after receiving digital enable during PWRUP mode, it transitions to Fault_SD mode.

7.3.5 PWRDN mode

When PMIC_ON_REQ is LOW for t_{OFF_DEB} in RUN or STANDBY mode, PCA9452 enters PWRDN mode. It starts with pulling down POR_B, turns off each power rail in t_{OFF_STEP} and transitions to SNVS mode.

7.3.6 RUN mode

PCA9452 operates in RUN mode when PMIC_ON_REQ is driven HIGH and PMIC_STBY_REQ is driven LOW. BUCK1, BUCK2, and BUCK3 output voltages are set to BUCK1OUT_DVS0, BUCK2OUT_DVS0 and BUCK3OUT_DVS0 register values, respectively. When PMIC_STBY_REQ is asserted HIGH in this mode, it transitions to STANDBY mode. After PMIC_ON_REQ is asserted LOW, it moves to PWRDN mode.

7.3.7 STANDBY mode

PCA9452 transitions to STANDBY mode from RUN mode when both PMIC_ON_REQ and PMIC_STBY_REQ are driven HIGH. BUCK1 output voltage is set to BUCK1OUT_DVS1.

If PMIC_ON_REQ is asserted LOW, then it transitions to PWRDN mode. If PMIC_STBY_REQ is driven LOW, then it transitions to RUN mode.

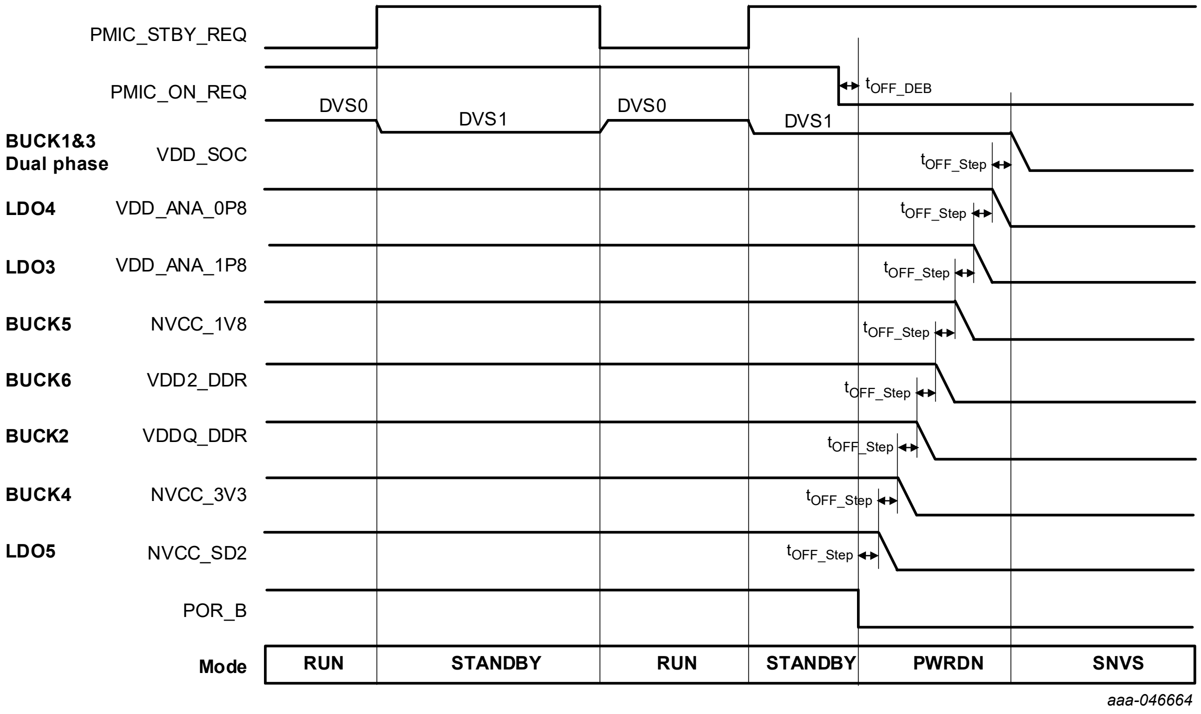


Figure 7. PCA9452 mode transition

Table 7. Power modes summary

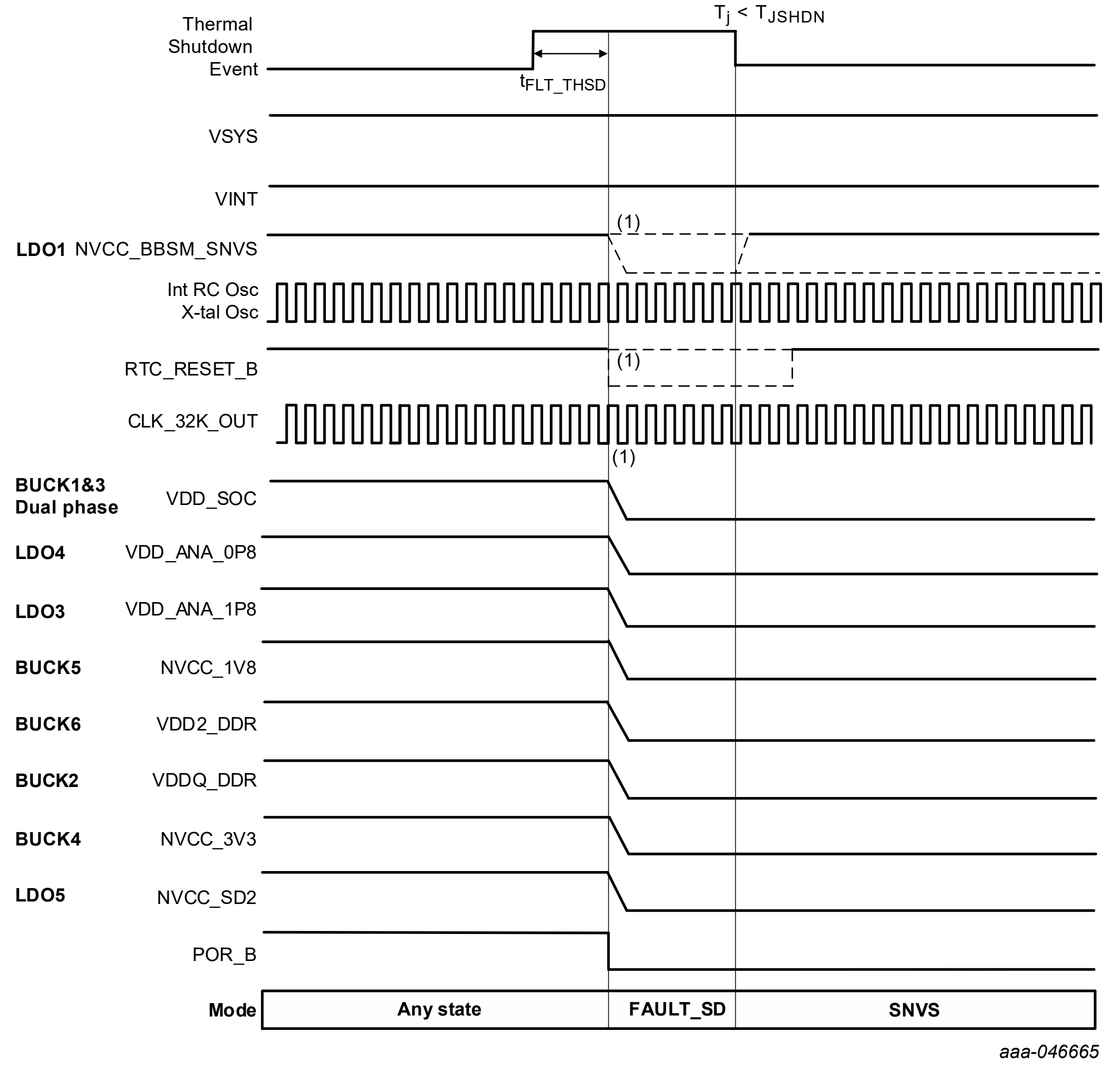
X: Don't care

Power mode	VSYS	PMIC_ON_REQ	PMIC_STBY_REQ
OFF	VSYS < V_{SYS_POR}	X	X
READY	VSYS > V_{SYS_POR}	X	X
SNVS	VSYS > V_{SYS_UVLO}	Low	X
STANDBY	VSYS > V_{SYS_UVLO}	High	High
RUN	VSYS > V_{SYS_UVLO}	High	Low

7.3.8 FAULT_SD

PCA9452 has three types of fault sources:

1. **Thermal shutdown**: Transition to SNVS mode or READY mode after FAULT_SD mode. When junction temperature reaches T_{JSHDN}, it enters FAULT_SD mode after t_{FLT_THSD} where regulators are turned off simultaneously. It stays at FAULT_SD until junction temperature falls below T_{JSHDN}. If the temperature drops below T_{JSHDN}, then it moves to READY state if LDO1 fault is triggered when thermal shutdown happens; it moves to SNVS mode if LDO1 fault is not triggered when thermal shutdown happens.



(1) If LDO1 fault occurs when junction temperature reaches thermal shutdown threshold, LDO1/RTC_RESETB/CLK_32K_OUT is turned off. Otherwise, they are kept on.

Figure 8. PCA9452 FAULT_SD from thermal shutdown

Table 8. t_{FLT_THSD}

Time	Description	Value
t_{FLT_THSD}	Time to reset released from Fault event	120 μs

2. **Voltage regulator fault during power-up**: Transition to READY mode or SNVS mode after FAULT_SD mode. Any POK of voltage regulators does not come up within $t_{FLT\_SD\_PU}$ after regulator is enabled during power-up sequence; it stops power-up sequence and then moves to FAULT_SD where all regulators are turned off. It stays at FAULT_SD for $t_{FLT\_SD\_STAY}$ and transitions to READY mode or SNVS mode.
3. **Voltage regulator fault in STANDBY and RUN MODE**: Move to FAULT_SD mode in $t_{FLT\_SD\_WAIT}$ after Fault is detected. Transition to SNVS mode or READY mode after FAULT_SD mode when fault is removed. During RUN and STANDBY mode, VR Fault status bit in VRFLT1_STS and VRFLT2_STS registers is latched to “1” when corresponding regulator voltage falls below POK threshold for t_{DEB_POKB}, or POK does not go HIGH within $t_{FLT\_POK\_MSK}$ after regulator is enabled.

If the fault status bit is masked in VRFLT1_MASK and VRFLT2_MASK registers, it does not enter FAULT_SD mode; instead, PCA9452 stays at current mode. If the fault register bit is unmasked, it starts $t_{FLT\_SD\_WAIT}$ timer. Application processor can determine to enter FAULT_SD mode or not, by masking the VR Fault status bit in VRFLTx_MASK registers before the timer expires. PCA9452 enters FAULT_SD mode when the timer expires. PCA9452 stays at FAULT_SD mode for $t_{FLT\_SD\_STAY}$.

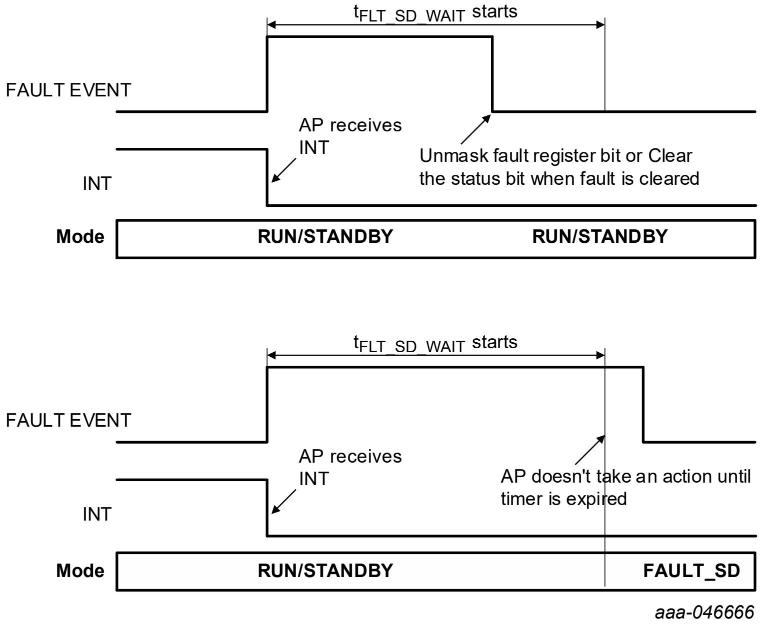
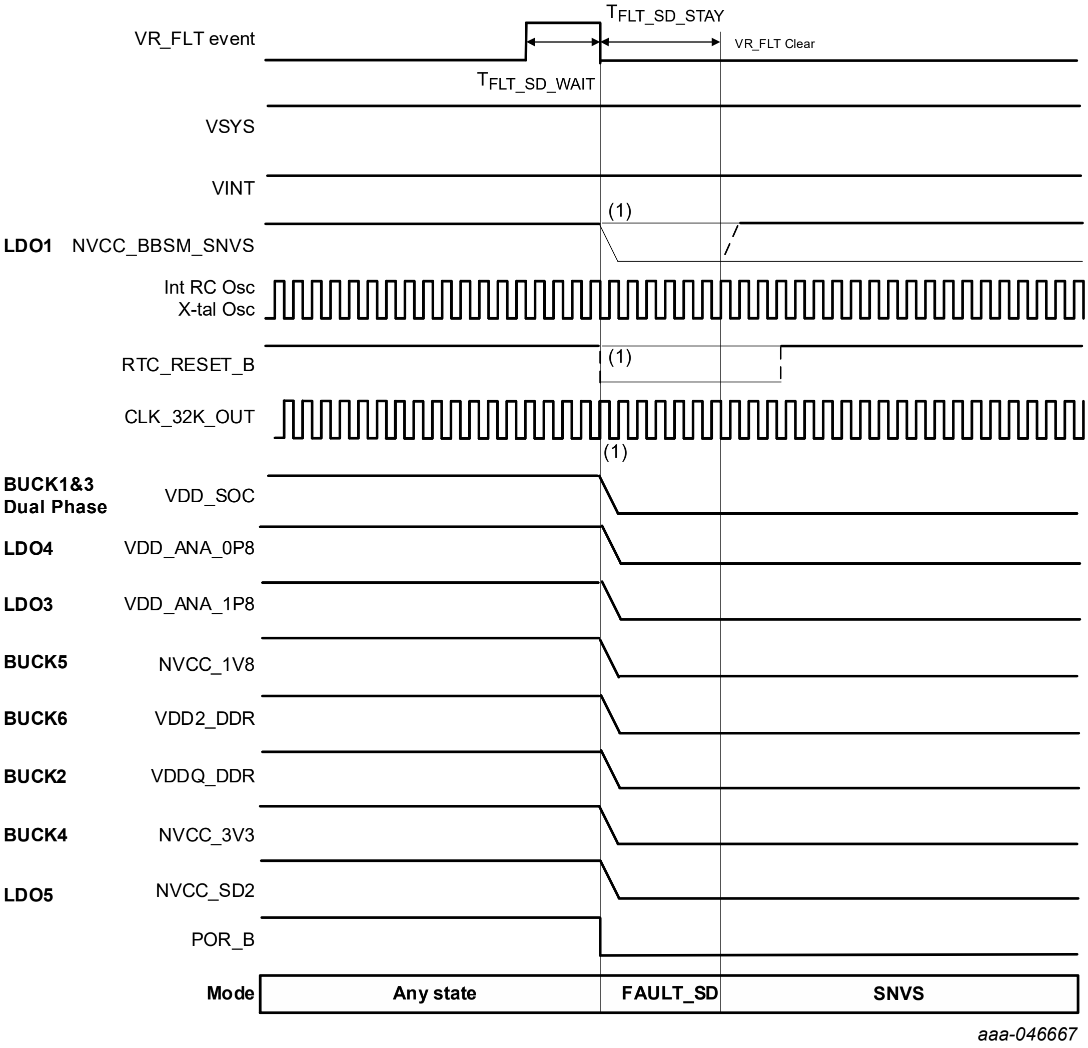


Figure 9. PCA9452 fault event

PCA9452 moves to READY mode after FAULT_SD mode if the regulator fault is caused by LDO1. Otherwise, it moves to SNVS mode after FAULT_SD.

If LDO1 has a fault in SNVS mode, then it enters FAULT_SD mode regardless of VRFLT1 Mask bit.

PCA9452 does not enter FAULT_SD mode from load switch overcurrent fault.



(1) If VR fault is caused by LDO1, then LDO1/RCT_REST_B/CLK_32K_OUT turns off; otherwise, they stay on.

Figure 10. PCA9452 FAULT_SD from VR Fault except LDO1 in RUN/STANDBY

Table 9. $t_{FLT\_SD\_WAIT}$

Time	Description	Value
$t_{FLT\_SD\_WAIT}$	Time to reset released from Fault event	100 ms

7.4 PMIC reset

The PCA9452 PMIC has three reset inputs: WDOG_B pin, PMIC_RST_B pin, and I^{2}C reset bit.

The reset behavior is configured in RESET_CTRL register for WDOG_B pin and PMIC_RST_B pin. I^{2}C reset behavior is configured in SW_RST register.

Table 10. 0x08 – RESET_CTRL

0x08 – RESET_CTRL				**Reset Type**	**S**
Bit	**Name**	**Type**	**Reset**	**Description**	
7:6	WDOG_B_CFG	R/W	00	When WDOG_B is asserted to L, PMIC behavior **00b = WDOG_B reset is disabled** 01b = Warm Reset, POR_B pin is asserted LOW for 20 ms 10b = Cold Reset, All voltage regulators are recycled except LDO1 11b = Cold Reset, All voltage regulators are recycled	
5:4	PMIC_RST_CFG	R/W	10	When PMIC_RST_B is asserted to L, PMIC behavior 00b = PMIC_RST_B reset is disabled 01b = Warm Reset, POR_B pin is asserted LOW for 20 ms **10b = Cold Reset, All voltage regulators are recycled except LDO1** 11b = Cold Reset, All voltage regulators are recycled	

Table 11. 0x06 – SW_RST

0x06 – SW_RST				**Reset Type**	**O**
Bit	**Name**	**Type**	**Reset**	**Description**	
7:0	SW_RST	R/W	0x00	Software reset register. This register read back to “0x00” right after writing the value. 0x00 = No action 0x05 = Reset all registers to default value 0x14 = Cold reset (Power recycle all regulators except LDO1 and CLK_32K_OUT) 0x35 = Warm Reset (Toggle POR_B for 20 ms) 0x64 = Cold reset (Power recycle all regulators) Others = No action	

When WDOG_B is asserted LOW, it resets depending on WDOG_B_CFG bit configuration. When the bits are set to 2b00, the reset by WDOG_B pin is disabled. If the bits are set to 2b01, warm reset is performed, where POR_B is pulled LOW for 20 ms and reset I^2C O type registers to default value keeping power rails remaining ON. If the bits are set to 2b11, it performs Cold reset, where all voltage regulators except LDO1 are power recycled and I^2C O type registers get reset to default value.

When PMIC_RST_B is asserted LOW, it also gets reset depending on PMIC_RST_CFG bits configuration. When the bits are set to 2b00, any reset by PMIC_RST_B pin is disabled. If the bits are set to 2b01, warm reset is performed, which pulls POR_B low for 20 ms and resets I^2C O type registers to default value keeping power rails remaining ON.

Cold reset event is generated by either of I^2C reset, WDOG_B falling edge or PMIC_RST_B falling edge after debounce time. Once it is detected, POR_B is pulled LOW and takes power down sequence. For cold reset from WDOG_B and I^2C reset, PCA9452 stays at RESET for $t_{RESTART}$ and then starts power on sequence even though WDOG_B pin is still LOW. For cold reset from PMIC_RST_B, $t_{RESTART}$ timer starts after PMIC_RST_B is asserted HIGH, in other words, PCA9452 starts power on sequence in $t_{RESTART}$ after PMIC_RST_B pin is released HIGH.

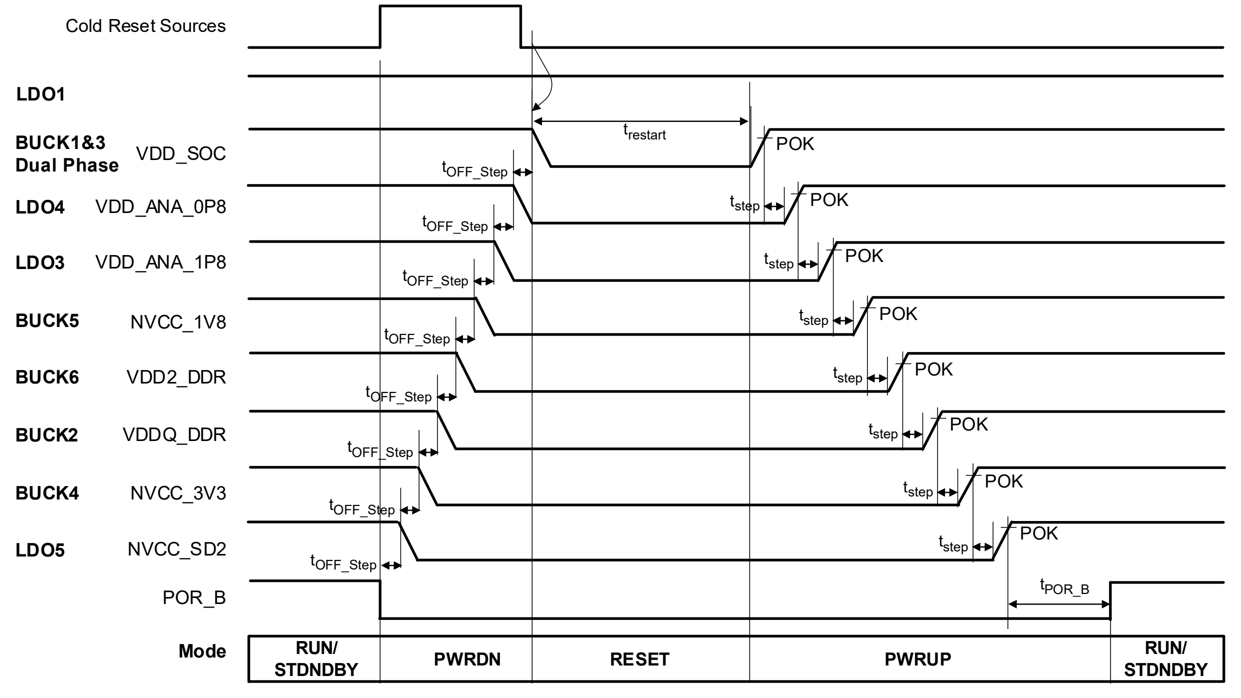


Figure 11. PCA9452 Cold reset

Table 12. $t_{RESTART}$

Time	Description	Value
$t_{RESTART}$	Time to power ON seq from end of power OFF seq during cold reset	250 ms

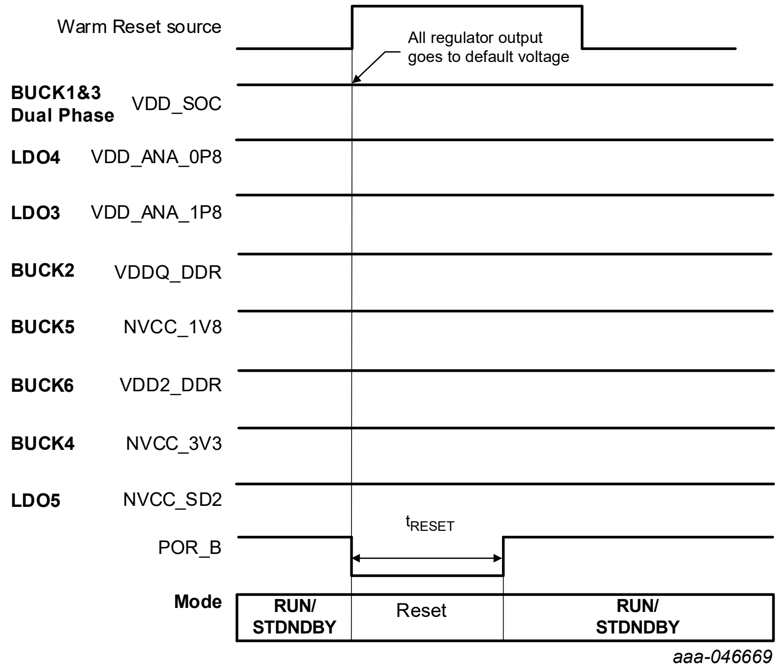


Figure 12. Warm reset

Table 13. t_{RESET}

Time	Description	Value
t_{RESET}	POR_B low time at Warm reset	20 ms

7.5 Regulator control in each power mode

Table 14 shows PCA9452 regulator ON/OFF control in each power mode by default. It can be reconfigured through I^2C registers.

Table 14. PCA9452 Regulator control summary

Power Rail		Default Voltage	OFF	SNVS	STANDBY	RUN
LDO1	NVCC_BBSM_SNVS	1.8 V	OFF	ON	ON	ON
BUCK1&3 Dual Phase	VDD_SOC	0.85 V	OFF	OFF	ON	ON
LDO4	VDD_ANA_0P8	0.8 V	OFF	OFF	ON	ON
LDO3	VDD_ANA_1P8	1.8 V	OFF	OFF	ON	ON
BUCK5	NVCC_1V8	1.8 V	OFF	OFF	ON	ON
BUCK6	VDD2_DDR	1.1 V	OFF	OFF	ON	ON
BUCK2	VDDQ_DDR	0.6 V	OFF	OFF	ON	ON
BUCK4	NVCC_3V3	3.3 V	OFF	OFF	ON	ON
LDO5	NVCC_SD2	3.3 V / 1.8 V	OFF	OFF	ON	ON

7.6 Regulator summary

The PCA9452 features six buck regulators, five linear regulators, and one load switch to supply voltage rails powering for the application processor and peripheral devices. The buck regulators are supplied directly from the main input supply, the input to all of the buck regulators must be tied to VSYS, whether they are powered on or off.

7.6.1 Buck regulator

The PCA9452 has six high-efficiency low Iq buck regulators. Each buck regulator features soft start and overcurrent protection. Buck regulator operates in two modes, PFM, and PWM mode. It automatically transitions from PFM to PWM mode when FPWM bit is set to “0”. Internal active discharge resistor is installed in each buck regulator output to discharge voltage on output capacitors when regulator is off. It is configurable through I^2C register. Table 15 shows buck regulator summary.

BUCK1 and BUCK3 can be configured as dual-phase buck and provide up to 6 A.

Table 15. PCA9452 buck summary

Buck#	INPUT PIN	Default VOUT [V]	Vout range [V]	Step size [mV]	Default ON/ OFF	Current rating [mA]
BUCK1 & 3 dual phase	INB13	0.85	0.65 - 2.2375	12.5	ON	6000
BUCK2	INB26	0.6	0.6 - 2.1875	12.5	ON	3000
BUCK4	INB45	3.3	0.6 - 3.4	25	ON	3000
BUCK5	INB45	1.8	0.6 - 3.4	25	ON	2000
BUCK6	INB26	1.1	0.6 - 3.4	25	ON	2000

7.6.1.1 Dynamic voltage scaling

BUCK1, BUCK2, and BUCK3 support Dynamic Voltage Scaling (DVS). If PRESET_EN bit in BUCK123_DVS register is set to 1, BUCK1/BUCK2/BUCK3 outputs are controlled by Bx_DVS_PRESET bits in BUCK123_DVS. It enables those buck outputs to be controlled by writing one register at a time.

If PRESET_EN bit is set to 0, those buck regulator outputs are determined by BUCKxOUT_DVS0 and BUCKxOUT_DVS1 depending on PMIC_STBY_REQ pin. When PMIC_STBY_REQ is asserted LOW, BUCKxOUT_DVS0 register determines each buck output voltage; if the PMIC_STBY_REQ is asserted HIGH, BUCKxOUT_DVS1 register is selected as each buck output voltage. Figure 13 shows the DVS voltage section diagram.

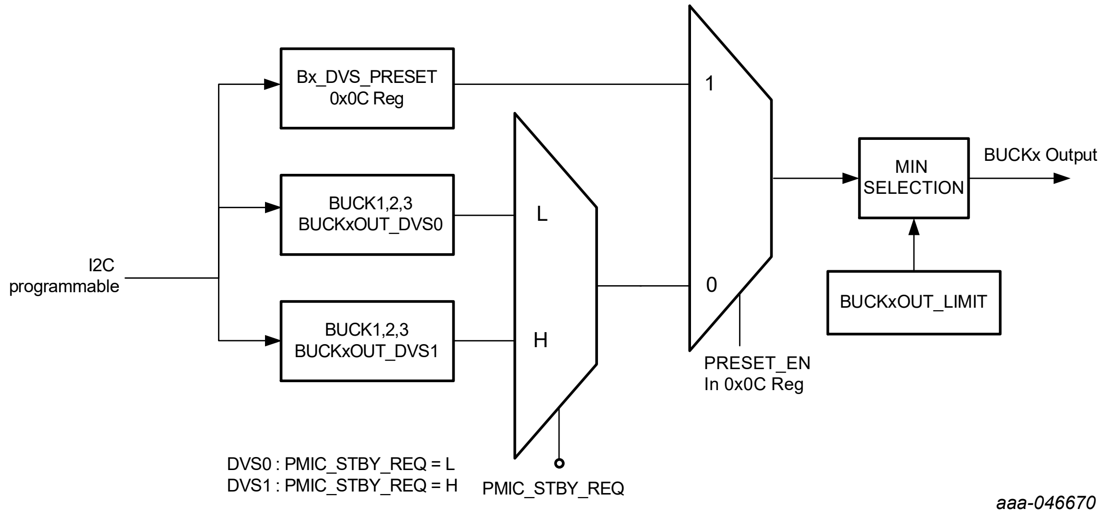


Figure 13. DVS functional diagram

The programmable voltage rampup and ramp-down are applied during the DVS voltage transition. The RAMP[7:6] bits configure the ramp rate in each BUCKxCTRL register.

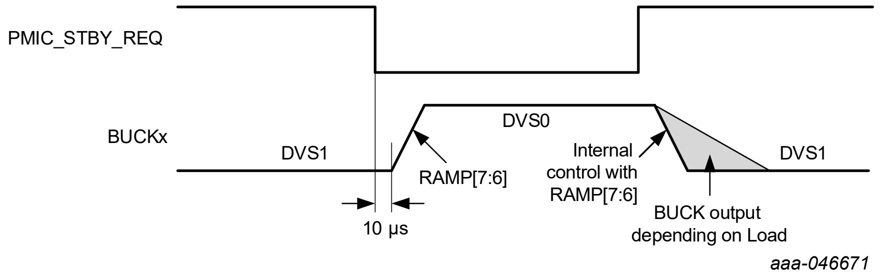


Figure 14. DVS timing

7.6.1.2 Buck output limiting

Application processor may accidentally write higher voltage than absolute maximum voltage rating of its power input, it may cause significant damage on application processor. PCA9452 has registers to limit the maximum voltage to prevent such an incident.

The maximum output of BUCK1, BUCK2, and BUCK3 is limited by BUCKxOUT_LIMIT, respectively. Even if Buck output is configured to be higher than the limit voltage configured in BUCKxOUT_LIMIT register, the actual buck output is clamped to the limiting voltage set by BUCKxOUT_LIMIT register.

7.6.1.3 Dual-phase configuration

With BUCK3 MTP bit being programmed, BUCK1 and BUCK3 are configured as dual phase buck by connecting R_SNSP3_CFG pin to GND, where this dual phase buck regulator is controlled through BUCK1 registers. All BUCK3 registers are not responsive under dual-phase configuration.

With the same BUCK3 MTP bit configuration, when R_SNSP3_CFG pin is tied to INB13, BUCK3 is disabled. BUCK1 supplies VDD_SOC in i.MX 93x application processor.

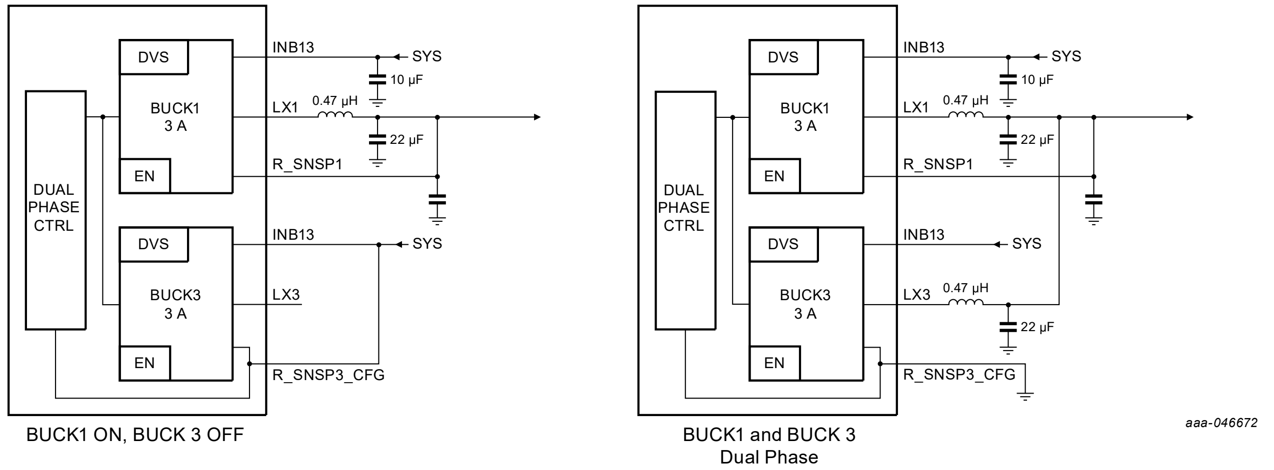


Figure 15. BUCK1 and BUCK3 configuration

7.6.2 LDO and load switch

The PCA9452 has five LDOs and one load switch. LDO1 supplies SNVS core in application processor. This LDO features ultra-low quiescent current, 2 µA typical, since it is always ON when VSYS is valid.

For all LDOs and the load switch, each has designated active discharge resistor configurable through I^2C.

Table 16. LDO summary

LDO#	INPUT PIN	Default VOUT [V]	VOUT range [V]	Step size [mV]	Default ON/ OFF	Current rating [mA]
LDO1	INL1	1.8	1.6-1.9, 3.0-3.3	100	ON	10
LDO2	INL1	-	-	-	OFF	10
LDO3	INL1	1.8	0.8 - 3.3	100	ON	300
LDO4	INL1	0.8	0.8 - 3.3	100	ON	200
LDO5	INL1	3.3/1.8	1.8 - 3.3	100	ON	150
SW	SWIN	-	-	-	OFF	400

7.7 32 kHz crystal oscillator driver

The PCA9452 consists of a crystal oscillator driver with an external load capacitor and CLK_32K_OUT buffer referenced to LDO1 voltage. When VSYS exceeds POR threshold and internal power VINT is good, internal 32 kHz oscillator and 32.768 kHz crystal oscillator start oscillating. Crystal oscillator typically takes few seconds to be stabilized.

PCA9452 outputs the internal 32 kHz RC oscillator initially, while internal counter counts crystal oscillator output in t_{RTC_Tran} after RTC_RESET_B is released. If the counter reaches 100, then CLK_32K_OUT buffer input is switched to the external crystal oscillator from internal 32 kHz oscillator.

Clock stretch is applied during this clock source transition to prevent unwanted glitch. If external 32.768 kHz crystal oscillator is not populated, CLK_32K_OUT pin outputs 32 kHz clock from internal 32 kHz oscillator.

For more detailed information on selecting crystal oscillator and load capacitance, refer to Section 9.2.2.

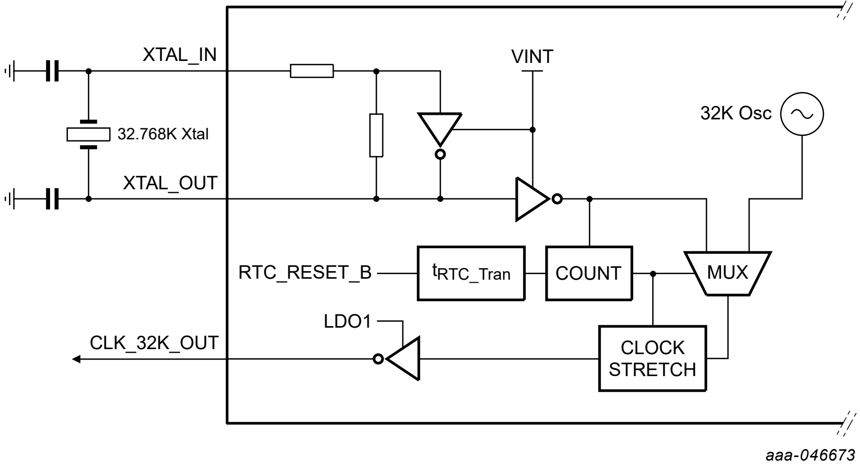


Figure 16. 32 kHz Crystal oscillator driver block diagram

7.8 Load switch

PCA9452 integrates 400 mA load switch which supplies SD card VDD. SWIN is connected to BUCK4 output, 3.3 V, in this application. It is enabled by SW_EN pin or SW_EN[1:0] bits in LOADSW_CTRL register. It has soft start feature to reduce inrush current during turn-on.

This load switch has over current protection and short circuit protection by monitoring voltage difference between SWIN and SWOUT. When the switch current exceeds overcurrent threshold (I_{OC}) for overcurrent debounce time (t_{OC_DEB}), SW_OCP bit in VRFLT1_STS register is set to 1, and SW_OC[1:0] configuration in LOADSW_CTRL register determines the fault behavior. When the switch current exceeds short-circuit current threshold (I_{SC}), SW_OCP bit in VRFLT1_STS register is set to 1, and switch is turned off right away.

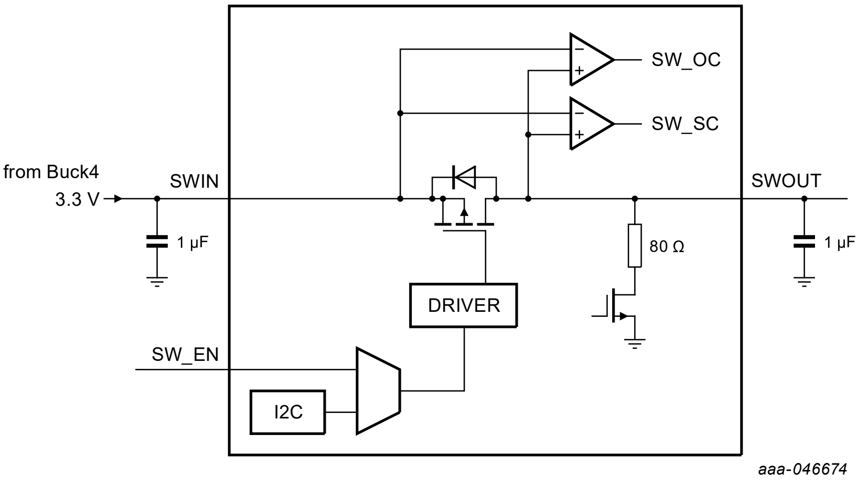


Figure 17. Load switch internal block diagram

7.9 I^{2}C level translator

PCA9452 I^{2}C level translator is a "switch" type voltage translator; it employs two key circuits to enable voltage translation:

1. A pass-gate transistor (N-channel) that ties the ports together.

2. An output edge-rate accelerator that detects and accelerates rising edges on the I/O pins.

The gate bias voltage of the pass gate transistor (T3) is set at approximately one threshold voltage above the VCC level of the low-voltage side. During a LOW-to-HIGH transition, the output one-shot accelerates the output transition by switching on the PMOS transistors (T1, T2), bypassing the 10 kΩ pullup resistors and increasing current drive capability. The one-shot is activated once the input transition reaches approximately VCCI/2; it is deactivated approximately 50 ns after the output reaches VCCO/2. During the acceleration time, the driver output resistance is between approximately 50 Ω and 70 Ω. To avoid signal contention and minimize dynamic ICC, the user should wait for the one-shot circuit to turn off before applying a signal in the opposite direction. Pullup resistors are included in the device for DC current sourcing capability.

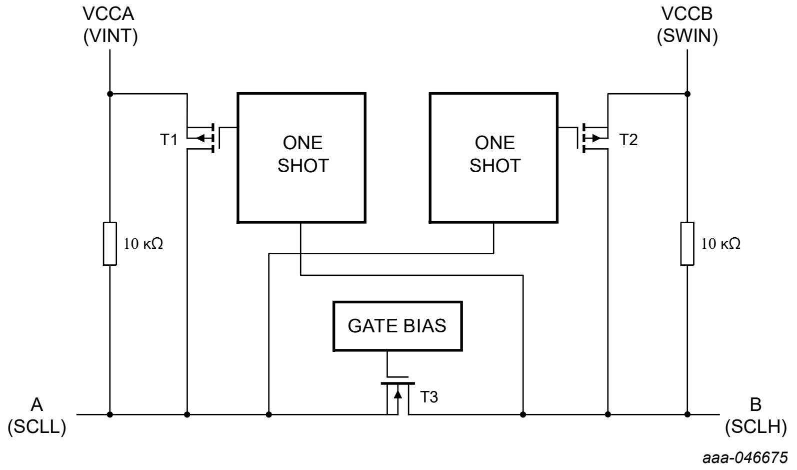


Figure 18. Architecture of I^2C level translator (one channel)

Each A port I/O has an internal 10 kΩ pullup resistor to VCCA, and each B port I/O has an internal 10 kΩ pullup resistor to VCCB. If a smaller value of pullup resistor is required, an external resistor must be added parallel to the internal 10 kΩ, which affects the VOL level. When Level translator is disabled through I^2C, the internal pullup resistors are disconnected.

PCA9452 I^2C level translator is controlled by I^2C register, CONFIG2 Reg. When disabled, all I/Os assume the high-impedance OFF-state. The enable time (t_{en}) indicates the amount of time the user must allow for one one-shot circuitry to become operational after it is enabled.

7.10 Interrupt management

The IRQ_B pin is an interface to the software-controlled system that indicates any interrupt bit status change of INT1 register. The IRQ_B pin is pulled LOW when any unmasked interrupt bit status is changed and it is released HIGH once application processor read INT1 register.

The INT1 bits are latched to 1 whenever corresponding STATUS1 bits change and the latch is cleared when the INT1 register is read. The INT1_MASK bits are used to enable or disable individual interrupt bits of INT1 register. The STATUS1 register indicates the status and is not latched.

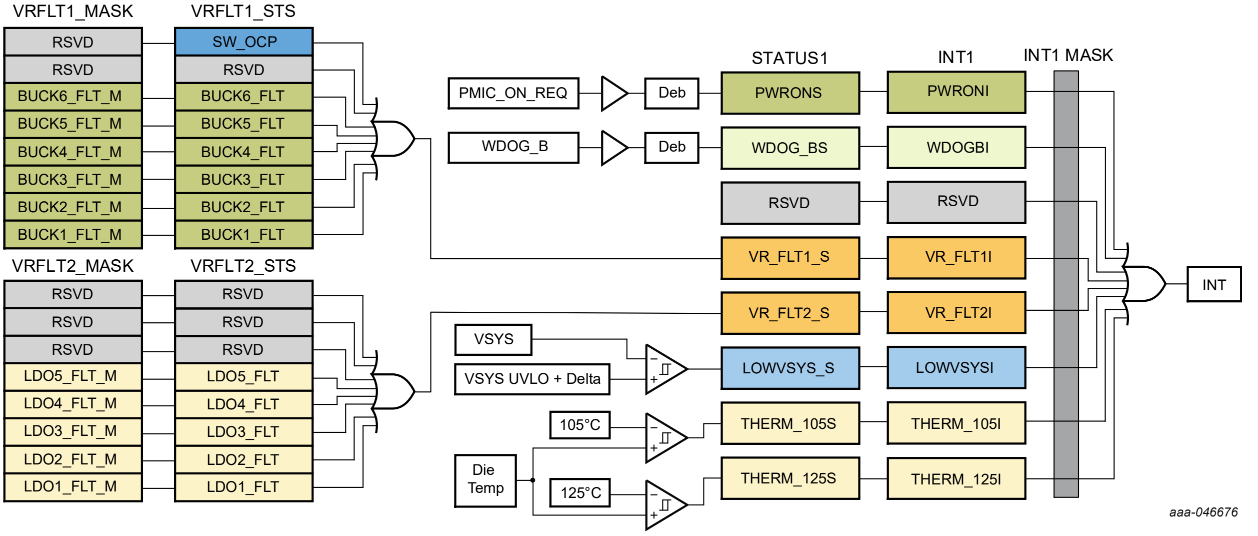


Figure 19. Interrupt diagram

8 Software interface

PCA9452 implements I^{2}C-bus target interface which interfaces with the host system. The host processor can issue commands, monitor status and receive response through this bus. A detailed description of the I^{2}C-bus specification, with applications, is given in UM10204, "I^{2}C-bus specification and user manual" [Ref. 4]. PCA9452 supports I^{2}C-bus data transfers in Standard-mode (100 kbit/s), Fast-mode (400 kbit/s) and Fast-mode plus (1 Mbit/s).

The I^{2}C address at Power-On Reset is shown in Table 17.

Table 17. I^{2}C target address

7-bit target Address	8-bit Write Address	8-bit Read Address
0x25, 0b 010 0101	0x4A, 0b 0100 1010	0x4B, 0b 0100 1011

There are three I^{2}C register reset types:

- **Type S1**: Reset condition = VSYS < V_{SYS_POR}
- **Type S**: Reset condition = VSYS < V_{SYS_UVLO}
- **Type O**: Reset condition = (VSYS < V_{SYS_UVLO}) || (Cold Reset) || (Warm Reset) || (Falling edge of PMIC_ON_REQ) || (SW_RST) || (FAULT_SD)

8.1 Register map

Table 18. Register map

Add	Name	Description								R/W	Reset Type	Reset Value
		B7	B6	B5	B4	B3	B2	B1	B0			
0x00	Device_ID	CHIP_ID				RSVD				R	S	0x90
0x01	INT1	PWERONI	WDOGBI	RSVD	VR_FLT1I	VR_FLT2I	LOWVSYSI	THERM_105I	THERM_125I	R/C	S	0x00
0x02	INT1_MSK	PWRONI_M	WDOGB_M	RSVD	VR_FLT1_M	VR_FLT2_M	LOWVSYS_M	THERM_105_M	THERM_125_M	R/W	S	0xFF
0x03	STATUS1	PWRONS	WDOGBS	RSVD	VR_FLT1S	VR_FLT2S	LOWVSYSS	THERM_105S	THERM_125S	R	S	0x00
0x04	STATUS2	RSVD	RSVD	RSVD	RSVD	POWER_STATUS				R	S1	0x00
0x05	PWRON_STAT	PWRON	WDOG	SW_RST	PMIC_RST	RSVD	RSVD	RSVD	RSVD	R/C	S	0x00
0x06	SW_RST	SW_RST								R/W	O	0x00
0x07	PWR_CTRL	Ton_Deb		Toff_Deb	Tstep		Toff_step		Trestart	R/W	S	0x4C
0x08	RESET_CTRL	WDOGB_CFG		PMIC_RST_CFG		RSVD	T_PMIC_RST_DEB			R/W	S	0x21
0x09	CONFIG1	LOW_VSYS		VSYS_UVLO		RSVD	RSVD	tFLT_SD_WAIT	THERM_SD_DIS	R/W	S1	0x50
0x0A	CONFIG2	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	I2C_LT_EN		R/W	O	0x00
0x0C	BUCK123_DVS	PRESET_EN	B3_DVS_PRESET		B1_DVS_PRESET		B2_DVS_PRESET			R/W	O	0xA8
0x0D	BUCK1OUT_LIMIT	RSVD	B1_LIMIT							R/W	O	0x1C
0x0E	BUCK2OUT_LIMIT	RSVD	B2_LIMIT							R/W	O	0x28
0x0F	BUCK3OUT_LIMIT	RSVD	B3_LIMIT							R/W	O	0x1C
0x10	BUCK1CTRL	RAMP		RSVD	DVS_CTRL	BUCK1AD	FPWM	B1_ENMODE		R/W	O	0x49
0x11	BUCK1OUT_DVS0	RSVD	B1_DVS0							R/W	O	0x10
0x12	BUCK1OUT_DVS1	RSVD	B1_DVS1							R/W	O	0x10
0x13	BUCK2CTRL	RAMP		RSVD	DVS_CTRL	BUCK2AD	FPWM	B2_ENMODE		R/W	O	0x49
0x14	BUCK2OUT_DVS0	RSVD	B2_DVS0							R/W	O	0x00
0x15	BUCK2OUT_DVS1	RSVD	B2_DVS1							R/W	O	0x00
0x16	BUCK3CTRL	RAMP		RSVD	DVS_CTRL	BUCK3AD	FPWM	B3_ENMODE		R/W	O	0x49
0x17	BUCK3OUT_DVS0	RSVD	B3_DVS0							R/W	O	0x10
0x18	BUCK3OUT_DVS1	RSVD	B3_DVS1							R/W	O	0x10
0x19	BUCK4CTRL	RSVD	RSVD	RSVD	RSVD	BUCK4AD	FPWM	B4_ENMODE		R/W	O	0x09
0x1A	BUCK4OUT	RSVD	B4_OUT							R/W	O	0x6C
0x1B	BUCK5CTRL	RSVD	RSVD	RSVD	RSVD	BUCK5AD	FPWM	B5_ENMODE		R/W	O	0x09
0x1C	BUCK5OUT	RSVD	B5_OUT							R/W	O	0x30
0x1D	BUCK6CTRL	RSVD	RSVD	RSVD	RSVD	BUCK6AD	FPWM	B6_ENMODE		R/W	O	0x09
0x1E	BUCK6OUT	RSVD	B6_OUT							R/W	O	0x14
0x20	LDO_AD_CTRL	LDO1_AD	LDO2_AD	LDO3_AD	LDO4_AD	LDO5_AD	RSVD	RSVD	RSVD	R/W	O	0xF8
0x21	LDO1CTRL	ENMODE		RSVD	RSVD	RSVD	L1_OUT			R/W	O	0xC2
0x22	LDO2CTRL	ENMODE		RSVD	RSVD	RSVD	L2_OUT			R/W	O	0x00
0x23	LDO3CTRL	ENMODE		RSVD	L3_OUT					R/W	O	0x4A
0x24	LDO4CTRL	ENMODE		RSVD	L4_OUT					R/W	O	0x40
0x25	LDO5CTRL_L	ENMODE		RSVD	RSVD	L5_OUT_L				R/W	O	0x4F
0x26	LDO5CTRL_H	RSVD	RSVD	RSVD	RSVD	L5_OUT_H				R/W	O	0x00
0x27	RSVD	RSVD								R/W	O	0x00
0x28	RSVD	RSVD								R/W	O	0x00
0x29	RSVD	RSVD								R/W	O	0x00
0x2A	LOADSW_CTRL	SW_AD	RSVD	RSVD	SW_SC	SW_OC		SWEN		R/W	O	0x85
0x2B	VRFLT1_STS	SW_OCP	RSVD	BUCK6_FLT	BUCK5_FLT	BUCK4_FLT	BUCK3_FLT	BUCK2_FLT	BUCK1_FLT	R/W/C	S	0x00
0x2C	VRFLT2_STS	RSVD	RSVD	RSVD	LDO5_FLT	LDO4_FLT	LDO3_FLT	LDO2_FLT	LDO1_FLT	R/W/C	S	0x00
0x2D	VRFLT1_MASK	RSVD	RSVD	BUCK6_FLT_M	BUCK5_FLT_M	BUCK4_FLT_M	BUCK3_FLT_M	BUCK2_FLT_M	BUCK1_FLT_M	R/W	S	0x3F

Table 18. Register map*...continued*

Add	Name	Description								R/W	Reset Type	Reset Value
		B7	B6	B5	B4	B3	B2	B1	B0			
0x2E	VRFLT2_MASK	RSVD	RSVD	RSVD	LDO5_ FLT_M	LDO4_ FLT_M	LDO3_ FLT_M	LDO2_ FLT_M	LDO1_ FLT_M	R/W	S	0x1F

8.2 Register details

8.2.1 0x00 Device_ID

The device identification code stores a unique identifier for each version and/or revision of a PCA9452, so that the connected processor recognizes it automatically.

Table 19. 0x00 Device ID

0x00 – Device_ID				Reset Type	S
Bit	**Name**	**Type**	**Reset**	**Description**	
7:4	CHIP_ID	R	1001	Chip ID 1001b = PCA9452	
3:0	RSVD	R	0000	Reserved	

8.2.2 0x01 INT1

Interrupt source register. Either of unmasked register bits is set to 1, IRQB pin is pulled LOW. This register is Read and Clear.

Table 20. 0x01 INT1

0x01 – INT1				Reset Type	S
Bit	**Name**	**Type**	**Reset**	**Description**	
7	PWRONI	R/C	0	PWRON interrupt bit 0b = PWRONS bit has not been changed 1b = PWRONS bit has been changed	
6	WDOGBI	R/C	0	WDOGB interrupt bit 0b = WDOG_BS bit has not been changed 1b = WDOG_BS bit has been changed	
5	RSVD	R/C	0	Reserved	
4	VR_FLT1I	R/C	0	Voltage regulator Group1 Fault interrupt 0b = VR_FLT1S bit has not been changed 1b = VR_FLT1S bit has been changed	
3	VR_FLT2I	R/C	0	Voltage regulator Group2 Fault interrupt 0b = VR_FLT2S bit has not been changed 1b = VR_FLT2S bit has been changed	
2	LOWVSYSI	R/C	0	Low-SYS Voltage interrupt bit 0b = LOWVSYSS bit has not been changed 1b = LOWVSYSS bit has been changed	
1	THERM_105I	R/C	0	Die temperature 105 °C interrupt 0b = THERM_105S bit has not been changed 1b = THERM_105S bit has been changed	
0	THERM_125I	R/C	0	Die temperature 125 °C interrupt	

Table 20. 0x01 INT1*...continued*

0x01 – INT1				Reset Type	S
Bit	**Name**	**Type**	**Reset**	**Description**	
				0b = THERM_125S bit has not been changed 1b = THERM_125S bit has been changed	

8.2.3 0x02 INT1_MSK

The INT1_MSK register enables the masking (disabling) of the different interrupt signals of register INT1. When unmasked, interrupt events trigger the IRQB pin to be pulled LOW when the matching flag bit in the register INT1 is set.

Table 21. 0x02 INT1_MSK

0x02 – INT1_MSK				Reset Type	S
Bit	**Name**	**Type**	**Reset**	**Description**	
7	PWRON_M	R/W	1	PWRONI interrupt mask bit 0b = Enable PWRONI interrupt **1b = Mask PWRONI interrupt**	
6	WDOGB_M	R/W	1	WDOGBI interrupt mask bit 0b = Enable WDOGBI interrupt **1b = Mask WDOGBI interrupt**	
5	RSVD	R/W	1	Reserved	
4	VR_FLT1_M	R/W	1	VR_FLT1I interrupt mask bit 0b = Enable VR_FLT1I interrupt **1b = Mask VR_FLT1I interrupt**	
3	VR_FLT2_M	R/W	1	VR_FLT2I interrupt mask bit 0b = Enable VR_FLT2I interrupt **1b = Mask VR_FLT2I interrupt**	
2	LOWVSYS_M	R/W	1	LOWVINI interrupt mask bit 0b = Enable LOWVINI interrupt **1b = Mask LOWVINI interrupt**	
1	THERM_105_M	R/W	1	THERM_105 interrupt mask bit 0b = Enable THERM_105 interrupt **1b = Mask THERM_105 interrupt**	
0	THERM_125_M	R/W	1	THERM_125 interrupt mask bit 0b = Enable THERM_125 interrupt **1b = Mask THERM_125 interrupt**	

8.2.4 0x03 STATUS1

STATUS1 register shows status. Any status bit change set corresponding interrupt bit to 1.

Table 22. 0x03 STATUS1

0x03 – STATUS1				Reset Type	S
Bit	**Name**	**Type**	**Reset**	**Description**	
7	PWRONS	R	0	PMIC_ON_REQ pin status after debounce time **0b = PMIC_ON_REQ pin is low**	

Table 22. 0x03 STATUS1*...continued*

0x03 – STATUS1				Reset Type	S
Bit	**Name**	**Type**	**Reset**	**Description**	
				1b = PMIC_ON_REQ pin is high	
6	WDOG_BS	R	0	WDOG_B pin status **0b = WDOG_B pin is low** 1b = WDOG_B pin is high	
5	RSVD	R	0	Reserved	
4	VR_FLT1S	R	0	Voltage Regulator Fault status, See 0x2B Register. **0b = All voltage regulators are OK** 1b = Either of voltage regulators is in Fault state	
3	VR_FLT2S	R	0	Voltage Regulator POK status, See 0x2C Registers. **0b = All voltage regulators are OK** 1b = Either of voltage regulators is in Fault state	
2	LOWVSYSS	R	0	VSYS low voltage status **0b = VSYS > Low VSYS threshold** 1b = VSYS ≤ Low VSYS threshold	
1	THERM_105S	R	0	Die temperature 105 °C statue **0b = Die temperature is below 105 °C** 1b = Die temperature is above 105 °C	
0	THERM_125S	R	0	Die temperature 125 °C statue **0b = Die temperature is below 125 °C** 1b = Die temperature is above 125 °C	

8.2.5 0x04 STATUS2

STATUS1 register shows current PCA9452 power mode.

Table 23. 0x04 STATUS2

0x04 – STATUS2				Reset Type	S1
Bit	**Name**	**Type**	**Reset**	**Description**	
7:4	RSVD	R	0000	Reserved	
3:0	POWER_STATUS	R	0000	Current PCA9452 power status 0000b = OFF 0001b = READY 0010b = SNVS 0011b = PWRUP 0100b = RUN 0101b = STANDBY 0110b = PWRDN 0111b = WARM RESET 1000b = COLD RESET 1001b = FAULT Shutdown 1010b – 1111b = Reserved	

8.2.6 0x05 PWRON_STAT

Power ON source register. It is latched to 1 until the bit is read back.

Table 24. 0x05 PWRON_STAT

0x05 – PWRON_STAT				**Reset Type**	**S**
Bit	**Name**	**Type**	**Reset**	**Description**	
7	PWRON	R/C	0	1b = Power ON triggered by PMIC_ON_REQ. This bit will be set right after completing power-up sequence.	
6	WDOG	R/C	0	1b = This bit is set after cold reset by WDOGB pin	
5	SW_RST	R/C	0	1b = This bit is set after cold reset by SW_RST bit	
4	PMIC_RST	R/C	0	1b = This bit is set after cold reset by PMIC_RST_B	
3	RSVD	R/C	0	Reserved	
2	RSVD	R/C	0	Reserved	
1	RSVD	R/C	0	Reserved	
0	RSVD	R/C	0	Reserved	

8.2.7 0x06 SW_RST

Software reset register

Table 25. 0x06 SW_RST

0x06 – SW_RST				**Reset Type**	**O**
Bit	**Name**	**Type**	**Reset**	**Description**	
7:0	SW_RST	R/W	0x00	Software reset register. This register is read back to “0x00” right after writing the value. 0x00 = No action 0x05 = Reset all registers to default value 0x14 = Cold reset (Power recycle all regulators except LDO1 and CLK_32K_OUT) 0x35 = Warm Reset (Toggle POR_B for 20 ms) 0x64 = Cold reset (Power recycle all regulators) Others = No action	

8.2.8 0x07 PWR_CTRL

Debounce timer configuration register.

Table 26. 0x07 PWR_CTRL

0x07 – PWR_CTRL				**Reset Type**	**S**
Bit	**Name**	**Type**	**Reset**	**Description**	
7:6	Ton_Deb	R/W	01	Debounce time for PMIC_ON_REQ high. 00b = 120 μs **01b = 20 ms** 10b = 100 ms 11b = 750 ms	
5	Toff_Deb	R/W	0	Debounce time for PMIC_ON_REQ is asserted LOW	

Table 26. 0x07 PWR_CTRL*...continued*

0x07 – PWR_CTRL				**Reset Type**	**S**
Bit	**Name**	**Type**	**Reset**	**Description**	
				0b = 120 µs **1b = 2 ms**	
4:3	Tstep	R/W	01	Time step configuration during power-on sequence 00b = 1 ms **01b = 2 ms** 10b = 4 ms 11b = 8 ms	
2:1	Toff_step	R/W	10	Time step configuration during power down sequence 00b = 2 ms 01b = 4 ms **10b = 8 ms** 11b = 16 ms	
0	Trestart	R/W	0	Time to stay off regulators during Cold reset **0b = 250 ms** 1b = 500 ms	

8.2.9 0x08 RESET_CTRL

Reset behavior configuration register

Table 27. 0x08 RESET_CTRL

0x08 – RESET_CTRL				**Reset Type**	**S**
Bit	**Name**	**Type**	**Reset**	**Description**	
7:6	WDOG_B_CFG	R/W	00	When WDOG_B is asserted LOW, PMIC reset behavior **00b = WDOG_B reset is disabled** 01b = Warm Reset, POR_B pin is asserted LOW for 20 ms 10b = Cold Reset, All voltage regulators are recycled except LDO1 11b = Cold Reset, All voltage regulators are recycled	
5:4	PMIC_RST_CFG	R/W	10	When PMIC_RST_B is asserted LOW, PMIC reset behavior 00b = PMIC_RST_B reset is disabled 01b = Warm Reset, POR_B pin is asserted LOW for 20 ms **10b = Cold Reset, All voltage regulators are recycled except LDO1** 11b = Cold Reset, All voltage regulators are recycled	
3	RSVD	R/W	0	Reserved	
2:0	T_PMIC_RST_DEB	R/W	001	PMIC_RST_B debounce time 000b = 10 ms **001b = 50 ms** 010b = 100 ms 011b = 500 ms 100b = 1 sec 101b = 2 sec 110b = 4 sec 111b = 8 sec	

8.2.10 0x09 CONFIG1

VSYS_UVLO and LOW VSYS configuration register

Table 28. 0x09 CONFIG1

0x09 – CONFIG1				Reset Type	S1
Bit	**Name**	**Type**	**Reset**	**Description**	
7:6	LOW_VSYS	R/W	01	Low VSYS threshold above V_{SYS_UVLO} 00b = 100 mV **01b = 200 mV** 10b = 300 mV 11b = 400 mV	
5:4	VSYS_UVLO	R/W	01	VSYS UVLO threshold 00b = 2.85 V **01b = 3.0 V** 10b = 3.15 V 11b = 3.3 V	
3:2	RSVD	R/W	00	Reserved	
1	tFLT_SD_WAIT	R/W	0	Wait time for AP action when regulator fault occurs **0b = 100 ms** 1b = 120 µs	
0	THERM_SD_DIS	R/W	0	Thermal shutdown disable bit **0b = Enable Thermal shutdown** 1b = Disable Thermal shutdown	

8.2.11 0x0A CONFIG2

I^2C level translator control register

Table 29. 0x0A CONFIG2

0x0A – CONFIG2				Reset Type	O
Bit	**Name**	**Type**	**Reset**	**Description**	
7	RSVD	R/W	0	Reserved	
6:4	RSVD	R/W	000	Reserved	
3:2	RSVD	R/W	00	Reserved	
1:0	I2C_LT_EN	R/W	00	I^2C level translator enable **00b = Forcedly Disable** 01b = Enable only when STANDBY and RUN mode 10b = Enable only when RUN mode 11b = Forcedly enable	

8.2.12 0x0C BUCK123_DVS

BUCK1, BUCK2, BUCK3 DVS control register with preset value

Table 30. 0x0C BUCK123_DVS

0x0C – BUCK123_DVS				Reset Type	O
Bit	**Name**	**Type**	**Reset**	**Description**	
7	PRESET_EN	R/W	1	BUCK123 output voltage selection 0b = BUCK voltage is determined by each BUCKxOUT_DVS0 or BUCKxOUT_DVS1. **1b = BUCK voltage is determined by Bx_DVS_PRESET bits.**	
6:5	B3_DVS_PRESET	R/W	01	BUCK3 Preset voltage option 00b = 0.80 V **01b = 0.85 V** 10b = 0.90 V 11b = 0.95 V	
4:3	B1_DVS_PRESET	R/W	01	BUCK1 (SOC) Preset voltage option 00b = 0.80 V **01b = 0.85 V** 10b = 0.90 V 11b = 0.95 V	
2:0	B2_DVS_PRESET	R/W	000	BUCK2 Preset voltage option **000b = 0.6 V** 001b = 0.7 V 010b = 0.8 V 011b = 0.9 V 100b – 111b = 1.1 V	

8.2.13 0x0D BUCK1OUT_LIMIT

BUCK1 output voltage limit register

Table 31. 0x0D BUCK1OUT_LIMIT

0x0D – BUCK1OUT_LIMIT				Reset Type	O
Bit	**Name**	**Type**	**Reset**	**Description**	
7	RSVD	R/W	0	Reserved	
6:0	B1_LIMIT	R/W	001 1100	BUCK1 output voltage limit Programmable from 0.65 V to 2.2375 V in 12.5 mV step Default = 1.0 V	

8.2.14 0x0E BUCK2OUT_LIMIT

BUCK2 output voltage limit register

Table 32. 0x0E BUCK2OUT_LIMIT

0x0E – BUCK2OUT_LIMIT				Reset Type	O
Bit	**Name**	**Type**	**Reset**	**Description**	
7	RSVD	R/W	0	Reserved	
6:0	B2_LIMIT	R/W	010 1000	BUCK2 output voltage limit Programmable from 0.60 V to 2.1875 V in 12.5 mV step Default = 1.1 V	

8.2.15 0x0F BUCK3OUT_LIMIT

BUCK3 output voltage limit register.

Table 33. 0x0F BUCK3OUT_LIMIT

0x0F – BUCK3OUT_LIMIT				Reset Type	O
Bit	**Name**	**Type**	**Reset**	**Description**	
7	RSVD	R/W	0	Reserved	
6:0	B3_LIMIT	R/W	001 1100	BUCK3 output voltage limit Programmable from 0.65 V to 2.2375 V in 12.5 mV step Default = 1.0 V	

8.2.16 0x10 BUCK1CTRL

BUCK1 control register for Ramp, DVS control, Active discharge, FPWM and Enable.

Table 34. 0x10 BUCK1CTRL

0x10 – BUCK1CTRL				Reset Type	O
Bit	**Name**	**Type**	**Reset**	**Description**	
7:6	RAMP	R/W	01	Buck1 DVS speed 00b = 25 mV / 1 µs **01b = 25 mV / 2 µs** 10b = 25 mV / 4 µs 11b = 25 mV / 8 µs	
5	RSVD	R/W	0	Reserved	
4	DVS_CTRL	R/W	0	DVS Control configuration **0b = BUCK voltage is determined by BUCK1VOUT_DVS0 register regardless of PMIC_STBY_REQ** 1b = DVS control through PMIC_STBY_REQ	
3	BUCK1AD	R/W	1	Buck1 Active discharge 0b = Always disable Active discharge resistor **1b = Enable Active discharge resistor when regulator is OFF**	
2	FPWM	R/W	0	Forced PWM mode **0b = Automatic PFM and PWM mode transition** 1b = Forced PWM mode	
1:0	B1_ENMODE	R/W	01	Buck1 enable mode 00b = OFF **01b = ON by PMIC_ON_REQ = H** 10b = ON by PMIC_ON_REQ = H && PMIC_STBY_REQ = L 11b = Reserved	

8.2.17 0x11 BUCK1OUT_DVS0

BUCK1 DVS output voltage PMIC_STBY_REQ = L

Table 35. 0x11 BUCK1OUT_DVS0

0x11 – BUCK1OUT_DVS0				**Reset Type**	**O**
Bit	**Name**	**Type**	**Reset**	**Description**	
7	RSVD	R/W	0	Reserved	
6:0	B1_DVS0	R/W	001 0000	BUCK1 DVS0 Output voltage Programmable from 0.65 V to 2.2375 V in 12.5 mV step Default = 0.85 V	

8.2.18 0x12 BUCK1OUT_DVS1

BUCK1 DVS output voltage PMIC_STBY_REQ = H

Table 36. 0x12 BUCK1OUT_DVS1

0x12 – BUCK1OUT_DVS1				**Reset Type**	**O**
Bit	**Name**	**Type**	**Reset**	**Description**	
7	RSVD	R/W	0	Reserved	
6:0	B1_DVS1	R/W	001 0000	BUCK1 DVS1 Output voltage Programmable from 0.65 V to 2.2375 V in 12.5 mV step Default = 0.85 V	

8.2.19 0x13 BUCK2CTRL

BUCK2 control register for Ramp, DVS control, Active discharge, FPWM, and Enable.

Table 37. 0x13 BUCK2CTRL

0x13 – BUCK2CTRL				**Reset Type**	**O**
Bit	**Name**	**Type**	**Reset**	**Description**	
7:6	RAMP	R/W	01	Buck2 DVS speed 00b = 25 mV / 1 µs **01b = 25 mV / 2 µs** 10b = 25 mV / 4 µs 11b = 25 mV / 8 µs	
5	RSVD	R/W	0	Reserved	
4	DVS_CTRL	R/W	0	DVS Control configuration **0b = BUCK2VOUT_DVS0 register determines BUCK voltage regardless of PMIC_STBY_REQ** 1b = DVS control through PMIC_STBY_REQ	
3	BUCK2AD	R/W	1	Buck2 Active discharge 0b = Always disable Active discharge resistor **1b = Enable Active discharge resistor when regulator is OFF**	
2	FPWM	R/W	0	Forced PWM mode **0b = Automatic PFM and PWM mode transition** 1b = Forced PWM mode	
1:0	B2_ENMODE	R/W	01	Buck2 enable mode 00b = OFF **01b = ON by PMIC_ON_REQ = H** 10b = ON by PMIC_ON_REQ = H && PMIC_STBY_REQ = L	

Table 37. 0x13 BUCK2CTRL*...continued*

0x13 – BUCK2CTRL				Reset Type	O
Bit	**Name**	**Type**	**Reset**	**Description**	
				11b = Always ON	

8.2.20 0x14 BUCK2OUT_DVS0

BUCK2 DVS output voltage PMIC_STBY_REQ = L

Table 38. 0x14 BUCK2OUT_DVS0

0x14 – BUCK2OUT_DVS0				Reset Type	O
Bit	**Name**	**Type**	**Reset**	**Description**	
7	RSVD	R/W	0	Reserved	
6:0	B2_DVS0	R/W	000 0000	BUCK2 DVS0 Output voltage Programmable from 0.60 V to 2.1875 V in 12.5 mV step Default = 0.6 V	

8.2.21 0x15 BUCK2OUT_DVS1

BUCK2 DVS output voltage PMIC_STBY_REQ = H

Table 39. 0x15 BUCK2OUT_DVS1

0x15 – BUCK2OUT_DVS1				Reset Type	O
Bit	**Name**	**Type**	**Reset**	**Description**	
7	RSVD	R/W	0	Reserved	
6:0	B2_DVS1	R/W	000 0000	BUCK2 DVS1 Output voltage Programmable from 0.60 V to 2.1875 V in 12.5 mV step Default = 0.6 V	

8.2.22 0x16 BUCK3CTRL

BUCK3 control register for Ramp, DVS control, Active discharge, FPWM, and Enable.

Table 40. 0x16 BUCK3CTRL

0x16 – BUCK3CTRL				Reset Type	O
Bit	**Name**	**Type**	**Reset**	**Description**	
7:6	RAMP	R/W	01	Buck3 DVS speed 00b = 25 mV / 1 µs **01b = 25 mV / 2 µs** 10b = 25 mV / 4 µs 11b = 25 mV / 8 µs	
5	RSVD	R/W	0	Reserved	
4	DVS_CTRL	R/W	0	DVS Control configuration **0b = BUCK3VOUT_DVS0 register determines BUCK voltage regardless of PMIC_STBY_REQ** 1b = DVS control through PMIC_STBY_REQ	
3	BUCK3AD	R/W	1	Buck3 Active discharge	

Table 40. 0x16 BUCK3CTRL*...continued*

0x16 – BUCK3CTRL				**Reset Type**	**O**
Bit	**Name**	**Type**	**Reset**	**Description**	
				0b = Always disable Active discharge resistor **1b = Enable Active discharge resistor when regulator is OFF**	
2	FPWM	R/W	0	Forced PWM mode **0b = Automatic PFM and PWM mode transition** 1b = Forced PWM mode	
1:0	B3_ENMODE	R/W	01	Buck3 enable mode 00b = OFF **01b = ON by PMIC_ON_REQ = H** 10b = ON by PMIC_ON_REQ = H && PMIC_STBY_REQ = L 11b = Always ON	

8.2.23 0x17 BUCK3OUT_DVS0

BUCK3 DVS output voltage PMIC_STBY_REQ = L

Table 41. 0x17 BUCK3OUT_DVS0

0x17 – BUCK3OUT_DVS0				**Reset Type**	**O**
Bit	**Name**	**Type**	**Reset**	**Description**	
7	RSVD	R/W	0	Reserved	
6:0	B3_DVS0	R/W	001 0000	BUCK3 DVS0 Output voltage Programmable from 0.65 V to 2.2375 V in 12.5 mV step Default = 0.85 V	

8.2.24 0x18 BUCK3OUT_DVS1

BUCK3 DVS output voltage PMIC_STBY_REQ = H

Table 42. 0x18 BUCK3OUT_DVS1

0x18 – BUCK3OUT_DVS1				**Reset Type**	**O**
Bit	**Name**	**Type**	**Reset**	**Description**	
7	RSVD	R/W	0	Reserved	
6:0	B3_DVS1	R/W	001 0000	BUCK3 DVS1 Output voltage Programmable from 0.60 V to 2.1875 V in 12.5 mV step Default = 0.8 V	
6:0	B3_DVS1	R/W	001 0000	BUCK3 DVS1 Output voltage Programmable from 0.65 V to 2.2375 V in 12.5 mV step Default = 0.85 V	

Table 43. BUCK1, BUCK3 Output voltage table

Code	**Voltage**	**Code**	**Voltage**	**Code**	**Voltage**	**Code**	**Voltage**
0x00	0.6500 V	0x20	1.0500 V	0x40	1.4500 V	0x60	1.8500 V
0x01	0.6625 V	0x21	1.0625 V	0x41	1.4625 V	0x61	1.8625 V

Table 43. BUCK1, BUCK3 Output voltage table*...continued*

Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
0x02	0.6750 V	0x22	1.0750 V	0x42	1.4750 V	0x62	1.8750 V
0x03	0.6875 V	0x23	1.0875 V	0x43	1.4875 V	0x63	1.8875 V
0x04	0.7000 V	0x24	1.1000 V	0x44	1.5000 V	0x64	1.9000 V
0x05	0.7125 V	0x25	1.1125 V	0x45	1.5125 V	0x65	1.9125 V
0x06	0.7250 V	0x26	1.1250 V	0x46	1.5250 V	0x66	1.9250 V
0x07	0.7375 V	0x27	1.1375 V	0x47	1.5375 V	0x67	1.9375 V
0x08	0.7500 V	0x28	1.1500 V	0x48	1.5500 V	0x68	1.9500 V
0x09	0.7625 V	0x29	1.1625 V	0x49	1.5625 V	0x69	1.9625 V
0x0A	0.7750 V	0x2A	1.1750 V	0x4A	1.5750 V	0x6A	1.9750 V
0x0B	0.7875 V	0x2B	1.1875 V	0x4B	1.5875 V	0x6B	1.9875 V
0x0C	0.8000 V	0x2C	1.2000 V	0x4C	1.6000 V	0x6C	2.0000 V
0x0D	0.8125 V	0x2D	1.2125 V	0x4D	1.6125 V	0x6D	2.0125 V
0x0E	0.8250 V	0x2E	1.2250 V	0x4E	1.6250 V	0x6E	2.0250 V
0x0F	0.8375 V	0x2F	1.2375 V	0x4F	1.6375 V	0x6F	2.0375 V
0x10	0.8500 V	0x30	1.2500 V	0x50	1.6500 V	0x70	2.0500 V
0x11	0.8625 V	0x31	1.2625 V	0x51	1.6625 V	0x71	2.0625 V
0x12	0.8750 V	0x32	1.2750 V	0x52	1.6750 V	0x72	2.0750 V
0x13	0.8875 V	0x33	1.2875 V	0x53	1.6875 V	0x73	2.0875 V
0x14	0.9000 V	0x34	1.3000 V	0x54	1.7000 V	0x74	2.1000 V
0x15	0.9125 V	0x35	1.3125 V	0x55	1.7125 V	0x75	2.1125 V
0x16	0.9250 V	0x36	1.3250 V	0x56	1.7250 V	0x76	2.1250 V
0x17	0.9375 V	0x37	1.3375 V	0x57	1.7375 V	0x77	2.1375 V
0x18	0.9500 V	0x38	1.3500 V	0x58	1.7500 V	0x78	2.1500 V
0x19	0.9625 V	0x39	1.3625 V	0x59	1.7625 V	0x79	2.1625 V
0x1A	0.9750 V	0x3A	1.3750 V	0x5A	1.7750 V	0x7A	2.1750 V
0x1B	0.9875 V	0x3B	1.3875 V	0x5B	1.7875 V	0x7B	2.1875 V
0x1C	1.0000 V	0x3C	1.4000 V	0x5C	1.8000 V	0x7C	2.2000 V
0x1D	1.0125 V	0x3D	1.4125 V	0x5D	1.8125 V	0x7D	2.2125 V
0x1E	1.0250 V	0x3E	1.4250 V	0x5E	1.8250 V	0x7E	2.2250 V
0x1F	1.0375 V	0x3F	1.4375 V	0x5F	1.8375 V	0x7F	2.2375 V

Table 44. BUCK2 Output voltage table

Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
0x00	0.6000 V	0x20	1.0000 V	0x40	1.4000 V	0x60	1.8000 V
0x01	0.6125 V	0x21	1.0125 V	0x41	1.4125 V	0x61	1.8125 V
0x02	0.6250 V	0x22	1.0250 V	0x42	1.4250 V	0x62	1.8250 V

Table 44. BUCK2 Output voltage table*...continued*

Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
0x03	0.6375 V	0x23	1.0375 V	0x43	1.4375 V	0x63	1.8375 V
0x04	0.6500 V	0x24	1.0500 V	0x44	1.4500 V	0x64	1.8500 V
0x05	0.6625 V	0x25	1.0625 V	0x45	1.4625 V	0x65	1.8625 V
0x06	0.6750 V	0x26	1.0750 V	0x46	1.4750 V	0x66	1.8750 V
0x07	0.6875 V	0x27	1.0875 V	0x47	1.4875 V	0x67	1.8875 V
0x08	0.7000 V	0x28	1.1000 V	0x48	1.5000 V	0x68	1.9000 V
0x09	0.7125 V	0x29	1.1125 V	0x49	1.5125 V	0x69	1.9125 V
0x0A	0.7250 V	0x2A	1.1250 V	0x4A	1.5250 V	0x6A	1.9250 V
0x0B	0.7375 V	0x2B	1.1375 V	0x4B	1.5375 V	0x6B	1.9375 V
0x0C	0.7500 V	0x2C	1.1500 V	0x4C	1.5500 V	0x6C	1.9500 V
0x0D	0.7625 V	0x2D	1.1625 V	0x4D	1.5625 V	0x6D	1.9625 V
0x0E	0.7750 V	0x2E	1.1750 V	0x4E	1.5750 V	0x6E	1.9750 V
0x0F	0.7875 V	0x2F	1.1875 V	0x4F	1.5875 V	0x6F	1.9875 V
0x10	0.8000 V	0x30	1.2000 V	0x50	1.6000 V	0x70	2.0000 V
0x11	0.8125 V	0x31	1.2125 V	0x51	1.6125 V	0x71	2.0125 V
0x12	0.8250 V	0x32	1.2250 V	0x52	1.6250 V	0x72	2.0250 V
0x13	0.8375 V	0x33	1.2375 V	0x53	1.6375 V	0x73	2.0375 V
0x14	0.8500 V	0x34	1.2500 V	0x54	1.6500 V	0x74	2.0500 V
0x15	0.8625 V	0x35	1.2625 V	0x55	1.6625 V	0x75	2.0625 V
0x16	0.8750 V	0x36	1.2750 V	0x56	1.6750 V	0x76	2.0750 V
0x17	0.8875 V	0x37	1.2875 V	0x57	1.6875 V	0x77	2.0875 V
0x18	0.9000 V	0x38	1.3000 V	0x58	1.7000 V	0x78	2.1000 V
0x19	0.9125 V	0x39	1.3125 V	0x59	1.7125 V	0x79	2.1125 V
0x1A	0.9250 V	0x3A	1.3250 V	0x5A	1.7250 V	0x7A	2.1250 V
0x1B	0.9375 V	0x3B	1.3375 V	0x5B	1.7375 V	0x7B	2.1375 V
0x1C	0.9500 V	0x3C	1.3500 V	0x5C	1.7500 V	0x7C	2.1500 V
0x1D	0.9625 V	0x3D	1.3625 V	0x5D	1.7625 V	0x7D	2.1625 V
0x1E	0.9750 V	0x3E	1.3750 V	0x5E	1.7750 V	0x7E	2.1750 V
0x1F	0.9875 V	0x3F	1.3875 V	0x5F	1.7875 V	0x7F	2.1875 V

8.2.25 0x19 BUCK4CTRL

BUCK4 control register for Active discharge, FPWM and Enable.

Table 45. 0x19 BUCK4CTRL

0x19 – BUCK4CTRL				Reset Type	O
Bit	**Name**	**Type**	**Reset**	**Description**	
7:4	RSVD	R/W	0000	Reserved	

Table 45. 0x19 BUCK4CTRL*...continued*

0x19 – BUCK4CTRL				**Reset Type**	**O**
Bit	**Name**	**Type**	**Reset**	**Description**	
3	BUCK4AD	R/W	1	Buck4 Active discharge 0b = Always disable Active discharge resistor **1b = Enable Active discharge resistor when regulator is OFF**	
2	FPWM	R/W	0	Forced PWM mode **0b = Automatic PFM and PWM mode transition** 1b = Forced PWM mode	
1:0	B4_ENMODE	R/W	01	Buck4 enable mode 00b = OFF **01b = ON by PMIC_ON_REQ = H** 10b = ON by PMIC_ON_REQ = H && PMIC_STBY_REQ = L 11b = Always ON	

8.2.26 0x1A BUCK4OUT

BUCK4 output voltage configuration register

Table 46. 0x1A BUCK4OUT

0x1A – BUCK4OUT				**Reset Type**	**O**
Bit	**Name**	**Type**	**Reset**	**Description**	
7	RSVD	R/W	0	Reserved	
6:0	B4_OUT	R/W	110 1100	BUCK4 Output voltage Programmable from 0.60 V to 3.40 V in 25 mV step Default = 3.3 V	

8.2.27 0x1B BUCK5CTRL

BUCK5 control register for Active discharge, FPWM, and Enable.

Table 47. 0x1B BUCK5CTRL

0x1B – BUCK5CTRL				**Reset Type**	**O**
Bit	**Name**	**Type**	**Reset**	**Description**	
7:4	RSVD	R/W	0000	Reserved	
3	BUCK5AD	R/W	1	Buck5 Active discharge 0b = Always disable Active discharge resistor **1b = Enable Active discharge resistor when regulator is OFF**	
2	FPWM	R/W	0	Forced PWM mode **0b = Automatic PFM and PWM mode transition** 1b = Forced PWM mode	
1:0	B5_ENMODE	R/W	01	Buck5 enable mode 00b = OFF **01b = ON by PMIC_ON_REQ = H** 10b = ON by PMIC_ON_REQ = H && PMIC_STBY_REQ = L 11b = Always ON	

8.2.28 0x1C BUCK5OUT

BUCK5 output voltage configuration register

Table 48. 0x1C BUCK5OUT

0x1C – BUCK5OUT				Reset Type	O
Bit	**Name**	**Type**	**Reset**	**Description**	
7	RSVD	R/W	0	Reserved	
6:0	B5_OUT	R/W	011 0000	BUCK5 Output voltage Programmable from 0.60 V to 3.40 V in 25 mV step Default = 1.8 V	

8.2.29 0x1D BUCK6CTRL

BUCK6 control register for Active discharge, FPWM, and Enable.

Table 49. 0x1D BUCK6OUT

0x1D – BUCK6OUT				Reset Type	O
Bit	**Name**	**Type**	**Reset**	**Description**	
7:4	RSVD	R/W	0000	Reserved	
3	BUCK6AD	R/W	1	Buck6 Active discharge 0b = Always disable Active discharge resistor **1b = Enable Active discharge resistor when regulator is OFF**	
2	FPWM	R/W	0	Forced PWM mode **0b = Automatic PFM and PWM mode transition** 1b = Forced PWM mode	
1:0	B6_ENMODE	R/W	01	Buck6 enable mode 00b = OFF **01b = ON by PMIC_ON_REQ = H** 10b = ON by PMIC_ON_REQ = H && PMIC_STBY_REQ = L 11b = Always ON	

8.2.30 0x1E BUCK6OUT

BUCK6 output voltage configuration register

Table 50. 0x1E BUCK6CTRL

0x1E – BUCK6CTRL				Reset Type	O
Bit	**Name**	**Type**	**Reset**	**Description**	
7	RSVD	R/W	0	Reserved	
6:0	B6_OUT	R/W	001 0100	BUCK6 Output voltage Programmable from 0.60 V to 3.40 V in 25 mV step Default = 1.1 V	

Table 51. BUCK4, BUCK5, BUCK6 Output voltage table

Code	Voltage	Code	Voltage	Code	Voltage	Code	Voltage
0x00	0.600 V	0x20	1.400 V	0x40	2.200 V	0x60	3.000 V
0x01	0.625 V	0x21	1.425 V	0x41	2.225 V	0x61	3.025 V
0x02	0.650 V	0x22	1.450 V	0x42	2.250 V	0x62	3.050 V
0x03	0.675 V	0x23	1.475 V	0x43	2.275 V	0x63	3.075 V
0x04	0.700 V	0x24	1.500 V	0x44	2.300 V	0x64	3.100 V
0x05	0.725 V	0x25	1.525 V	0x45	2.325 V	0x65	3.125 V
0x06	0.750 V	0x26	1.550 V	0x46	2.350 V	0x66	3.150 V
0x07	0.775 V	0x27	1.575 V	0x47	2.375 V	0x67	3.175 V
0x08	0.800 V	0x28	1.600 V	0x48	2.400 V	0x68	3.200 V
0x09	0.825 V	0x29	1.625 V	0x49	2.425 V	0x69	3.225 V
0x0A	0.850 V	0x2A	1.650 V	0x4A	2.450 V	0x6A	3.250 V
0x0B	0.875 V	0x2B	1.675 V	0x4B	2.475 V	0x6B	3.275 V
0x0C	0.900 V	0x2C	1.700 V	0x4C	2.500 V	0x6C	3.300 V
0x0D	0.925 V	0x2D	1.725 V	0x4D	2.525 V	0x6D	3.325 V
0x0E	0.950 V	0x2E	1.750 V	0x4E	2.550 V	0x6E	3.350 V
0x0F	0.975 V	0x2F	1.775 V	0x4F	2.575 V	0x6F	3.375 V
0x10	1.000 V	0x30	1.800 V	0x50	2.600 V	0x70	3.400 V
0x11	1.025 V	0x31	1.825 V	0x51	2.625 V	0x71	3.400 V
0x12	1.050 V	0x32	1.850 V	0x52	2.650 V	0x72	3.400 V
0x13	1.075 V	0x33	1.875 V	0x53	2.675 V	0x73	3.400 V
0x14	1.100 V	0x34	1.900 V	0x54	2.700 V	0x74	3.400 V
0x15	1.125 V	0x35	1.925 V	0x55	2.725 V	0x75	3.400 V
0x16	1.150 V	0x36	1.950 V	0x56	2.750 V	0x76	3.400 V
0x17	1.175 V	0x37	1.975 V	0x57	2.775 V	0x77	3.400 V
0x18	1.200 V	0x38	2.000 V	0x58	2.800 V	0x78	3.400 V
0x19	1.225 V	0x39	2.025 V	0x59	2.825 V	0x79	3.400 V
0x1A	1.250 V	0x3A	2.050 V	0x5A	2.850 V	0x7A	3.400 V
0x1B	1.275 V	0x3B	2.075 V	0x5B	2.875 V	0x7B	3.400 V
0x1C	1.300 V	0x3C	2.100 V	0x5C	2.900 V	0x7C	3.400 V
0x1D	1.325 V	0x3D	2.125 V	0x5D	2.925 V	0x7D	3.400 V
0x1E	1.350 V	0x3E	2.150 V	0x5E	2.950 V	0x7E	3.400 V
0x1F	1.375 V	0x3F	2.175 V	0x5F	2.975 V	0x7F	3.400 V

8.2.31 0x20 LDO_AD_CTRL

LDO active discharge resistor configuration register\

Table 52. 0x20 LDO_AD_CTRL

0x20 – LDO_AD_CTRL				**Reset Type**	**O**
Bit	**Name**	**Type**	**Reset**	**Description**	
7	LDO1_AD	R/W	1	LDO1 Active discharge enable 0b = Always disable Active discharge resistor **1b = Enable Active discharge resistor when regulator is OFF**	
6	LDO2_AD	R/W	1	LDO2 Active discharge enable 0b = Always disable Active discharge resistor **1b = Enable Active discharge resistor when regulator is OFF**	
5	LDO3_AD	R/W	1	LDO3 Active discharge enable 0b = Always disable Active discharge resistor **1b = Enable Active discharge resistor when regulator is OFF**	
4	LDO4_AD	R/W	1	LDO4 Active discharge enable 0b = Always disable Active discharge resistor **1b = Enable Active discharge resistor when regulator is OFF**	
3	LDO5_AD	R/W	1	LDO5 Active discharge enable 0b = Always disable Active discharge resistor **1b = Enable Active discharge resistor when regulator is OFF**	
2:0	RSVD	R/W	0	Reserved	

8.2.32 0x21 LDO1CTRL

LDO1 control register for enable and voltage

Table 53. 0x21 LDO1CTRL

0x21 – LDO1CTRL				**Reset Type**	**O**
Bit	**Name**	**Type**	**Reset**	**Description**	
7:6	ENMODE	R/W	11	LDO1 Enable mode 00b = OFF 01b = ON by PMIC_ON_REQ = H 10b = ON by PMIC_ON_REQ = H && PMIC_STBY_REQ = L **11b = Always ON** * When LDO1 is turned off, PCA9452 transitions to READY mode	
5:3	RSVD	R/W	000	Reserved	
2:0	L1_OUT	R/W	010	LDO1 output voltage Programmable from 1.6 V – 1.9 V, 3.0 V – 3.3 V in 100 mV step 000b = 1.6 V 001b = 1.7 V **010b = 1.8 V** 011b = 1.9 V 100b = 3.0 V 101b = 3.1 V 110b = 3.2 V 111b = 3.3 V	

8.2.33 0x22 LDO2CTRL

LDO2 control register for enable and voltage

Table 54. 0x22 LDO2CTRL

0x22 – LDO2CTRL				**Reset Type**	**O**
Bit	**Name**	**Type**	**Reset**	**Description**	
7:6	ENMODE	R/W	00	LDO2 Enable mode **00b = OFF** 01b = ON by PMIC_ON_REQ = H 10b = ON by PMIC_ON_REQ = H && PMIC_STBY_REQ = L 11b = Reserved	
5:3	RSVD	R/W	000	Reserved	
2:0	L2_OUT	R/W	000	LDO2 output voltage Programmable from 0.8 V to 1.15 V in 50 mV step **000b = 0.8 V** 001b = 0.85 V 010b = 0.9 V 011b = 0.95 V 100b = 1.0 V 101b = 1.05 V 110b = 1.1 V 111b = 1.15 V	

8.2.34 0x23 LDO3CTRL

LDO3 control register for enable and voltage

Table 55. 0x23 LDO3CTRL

0x23 – LDO3CTRL				**Reset Type**	**O**
Bit	**Name**	**Type**	**Reset**	**Description**	
7:6	ENMODE	R/W	01	LDO3 Enable mode 00b = OFF **01b = ON by PMIC_ON_REQ = H** 10b = ON by PMIC_ON_REQ = H && PMIC_STBY_REQ = L 11b = Reserved	
5	RSVD	R/W	0	Reserved	
4:0	L3_OUT	R/W	0 1010	LDO3 output voltage Programmable from 0.8 V to 3.3 V in 100 mV steps, see Table 58	

Table 56. LDO3 output voltage

0x00: 0.80 V	0x8: 1.60 V	0x10: 2.40 V	0x18: 3.20 V
0x01: 0.90 V	0x9: 1.70 V	0x11: 2.50 V	0x19: 3.30 V
0x02: 1.00 V	**0xA: 1.80 V**	0x12: 2.60 V	0x1A: 3.30 V
0x03: 1.10 V	0xB: 1.90 V	0x13: 2.70 V	0x1B: 3.30 V
0x04: 1.20 V	0xC: 2.00 V	0x14: 2.80 V	0x1C: 3.30 V

Table 56. LDO3 output voltage*...continued*

0x05: 1.30 V	0xD: 2.10 V	0x15: 2.90 V	0x1D: 3.30 V
0x06: 1.40 V	0xE: 2.20 V	0x16: 3.00 V	0x1E: 3.30 V
0x07: 1.50 V	0xF: 2.30 V	0x17: 3.10 V	0x1F: 3.30 V

8.2.35 0x24 LDO4CTRL

LDO4 control register for enable and voltage

Table 57. 0x24 LDO4CTRL

0x24 – LDO4CTRL				**Reset Type**	**O**
Bit	**Name**	**Type**	**Reset**	**Description**	
7:6	ENMODE	R/W	01	LDO4 Enable mode 00b = OFF **01b = ON by PMIC_ON_REQ = H** 10b = ON by PMIC_ON_REQ = H && PMIC_STBY_REQ = L 11b = Reserved	
5	RSVD	R/W	0	Reserved	
4:0	L4_OUT	R/W	0 0000	LDO4 output voltage Programmable from 0.8 V to 3.3 V in 100 mV step, see Table 58	

Table 58. LDO4 output voltage

0x00: 0.80 V	0x8: 1.60 V	0x10: 2.40 V	0x18: 3.20 V
0x01: 0.90 V	0x9: 1.70 V	0x11: 2.50 V	0x19: 3.30 V
0x02: 1.00 V	0xA: 1.80 V	0x12: 2.60 V	0x1A: 3.30 V
0x03: 1.10 V	0xB: 1.90 V	0x13: 2.70 V	0x1B: 3.30 V
0x04: 1.20 V	0xC: 2.00 V	0x14: 2.80 V	0x1C: 3.30 V
0x05: 1.30 V	0xD: 2.10 V	0x15: 2.90 V	0x1D: 3.30 V
0x06: 1.40 V	0xE: 2.20 V	0x16: 3.00 V	0x1E: 3.30 V
0x07: 1.50 V	0xF: 2.30 V	0x17: 3.10 V	0x1F: 3.30 V

8.2.36 0x25 LDO5CTRL_L

LDO5 control register for enable and voltage when SD_VSEL is LOW.

Table 59. 0x25 LDO5CTRL_L

0x25 – LDO5CTRL_L				**Reset Type**	**O**
Bit	**Name**	**Type**	**Reset**	**Description**	
7:6	ENMODE	R/W	01	LDO5 Enable mode 00b = OFF **01b = ON by PMIC_ON_REQ = H** 10b = ON by PMIC_ON_REQ = H && PMIC_STBY_REQ = L 11b = Reserved	
5:4	RSVD	R/W	00	Reserved	

Table 59. 0x25 LDO5CTRL_L*...continued*

0x25 – LDO5CTRL_L				**Reset Type**	**O**
Bit	**Name**	**Type**	**Reset**	**Description**	
3:0	L5_OUT_L	R/W	1111	LDO5 output voltage when SD_VSEL = Low Programmable from 1.8 V to 3.3 V in 100 mV step, see Table 60	

Table 60. LDO5 output voltage when SD_VSEL = Low

0x00: 1.80 V	0x4: 2.20 V	0x8: 2.60 V	0xC: 3.00 V
0x01: 1.90 V	0x5: 2.30 V	0x9: 2.70 V	0xD: 3.10 V
0x02: 2.00 V	0x6: 2.40 V	0xA: 2.80 V	0xE: 3.20 V
0x03: 2.10 V	0x7: 2.50 V	0xB: 2.90 V	**0xF: 3.30 V**

8.2.37 0x26 LDO5CTRL_H

LDO5 control register for enable and voltage when SD_VSEL is HIGH.

Table 61. 0x26 LDO5CTRL_H

0x26 – LDO5CTRL_H				**Reset Type**	**O**
Bit	**Name**	**Type**	**Reset**	**Description**	
7:6	RSVD	R/W	00	Reserved	
5:4	RSVD	R/W	00	Reserved	
3:0	L5_OUT_H	R/W	0000	LDO5 output voltage when SD_VSEL = HIGH Programmable from 1.8 V to 3.3 V in 100 mV step, see Table 62	

Table 62. LDO5 output voltage when SD_VSEL = HIGH

0x00: 1.80 V	0x4: 2.20 V	0x8: 2.60 V	0xC: 3.00 V
0x01: 1.90 V	0x5: 2.30 V	0x9: 2.70 V	0xD: 3.10 V
0x02: 2.00 V	0x6: 2.40 V	0xA: 2.80 V	0xE: 3.20 V
0x03: 2.10 V	0x7: 2.50 V	0xB: 2.90 V	0xF: 3.30 V

8.2.38 0x2A LOADSW_CTRL

Load switch control register for active discharge, short/over current and enable.

Table 63. 0x2A LOADSW_CRTL

0x2A – LOADSW_CTRL				**Reset Type**	**O**
Bit	**Name**	**Type**	**Reset**	**Description**	
7	SW_AD	R/W	1	Load switch active discharge 0b = Always disable active discharge resistor **1b = Enable active discharge resistor when it is OFF**	
6:5	RSVD	R/W	00	Reserved	
4	SW_SC	R/W	0	When switch detects short circuit current **0b = Turned OFF and set SWEN[1:0] are set to 00b automatically**	

Table 63. 0x2A LOADSW_CRTL*...continued*

0x2A – LOADSW_CTRL				Reset Type	O
Bit	**Name**	**Type**	**Reset**	**Description**	
				1b = Turned off and restart in 100 ms	
3:2	SW_OC	R/W	01	When load switch detects over current 00b = Turned OFF and set SWEN[1:0] are set to 00b automatically **01b = Turned off and restart in 100 ms** 10b, 11b = stay ON	
1:0	SWEN	R/W	01	SW Enable control 00b = Forcedly OFF **01b = Enabled by SW_EN pin** 10b = Forcedly ON 11b = Forcedly ON	

8.2.39 0x2B VRFLT1_STS

Voltage regulator fault status register. It is latched to 1 once corresponding regulator is detected until overwriting “1” to the register. If “1” is overwritten, the corresponding bit is newly updated by current status.

Table 64. 0x2B VRFLT1_STS

0x2B – VRFLT1_STS				Reset Type	S
Bit	**Name**	**Type**	**Reset**	**Description**	
7	SW_OCP	R/W/C	0	Load SW OCP status, deglitched with $t_{DEB\_POKB\_SW}$ **0 = Load SW does not exceed current limit or is OFF** 1 = Load SW exceeded current limit	
6	RSVD	R/W/C	0	Reserved	
5	BUCK6_FLT	R/W/C	0	BUCK6 Fault status, deglitched with t_{DEB_POKB} **0b = BUCK6 output is good or BUCK6 is OFF** 1b = BUCK6 output falls below 80 % of target	
4	BUCK5_FLT	R/W/C	0	BUCK5 Fault status, deglitched with t_{DEB_POKB} **0b = BUCK5 output is good or BUCK5 is OFF** 1b = BUCK5 output falls below 80 % of target	
3	BUCK4_FLT	R/W/C	0	BUCK4 Fault status, deglitched with t_{DEB_POKB} **0b = BUCK4 output is good or BUCK4 is OFF** 1b = BUCK4 output is below 80 %	
2	BUCK3_FLT	R/W/C	0	BUCK3 Fault status, deglitched with t_{DEB_POKB} **0b = BUCK3 output is good or BUCK3 is OFF** 1b = BUCK3 output falls below 80 % of target	
1	BUCK2_FLT	R/W/C	0	BUCK2 Fault status, deglitched with t_{DEB_POKB} **0b = BUCK2 output is good or BUCK2 is OFF** 1b = BUCK2 output falls below 80 % of target	
0	BUCK1_FLT	R/W/C	0	BUCK1 Fault status, deglitched with t_{DEB_POKB} **0b = BUCK1 output is good or BUCK1 is OFF** 1b = BUCK1 output falls below 80 % of target	

8.2.40 0x2C VRFLT2_STS

Voltage regulator fault status register. It is latched to 1 once corresponding regulator is detected until overwriting “1” to the register. If “1” is overwritten, the corresponding bit is newly updated by current status.

Table 65. 0x2C VRFLT2_STS

0x2C – VRFLT2_STS				**Reset Type**	**S**
Bit	**Name**	**Type**	**Reset**	**Description**	
7:5	RSVD	R/W/C	000	Reserved	
4	LDO5_FLT	R/W/C	0	LDO5 Fault status, deglitched with t_{DEB_POKB} **0b = LDO5 output is good or LDO5 is OFF** 1b = LDO5 output falls below 80 % of target	
3	LDO4_FLT	R/W/C	0	LDO4 Fault status, deglitched with t_{DEB_POKB} **0b = LDO4 output is good or LDO4 is OFF** 1b = LDO4 output falls below 80 % of target	
2:1	RSVD	R/W/C	0	Reserved	
0	LDO1_FLT	R/W/C	0	LDO1 Fault status, deglitched with t_{DEB_POKB} **0b = LDO1 output is good or LDO1 is OFF** 1b = LDO1 output falls below 80 % of target	

8.2.41 0x2D VRFLT1_MASK

VR fault mask bit. Once the bit is masked, PCA9452 does not enter Fault shutdown even if fault condition of corresponding regulator happens.

Table 66. 0x2D VRFLT1_MASK

0x2D – VRFLT1_MASK				**Reset Type**	**S**
Bit	**Name**	**Type**	**Reset**	**Description**	
7:6	RSVD	R/W	0	Reserved	
5	BUCK6_FLT_M	R/W	1	BUCK6 FLT mask 0b = Unmask **1b = Masked**	
4	BUCK5_FLT_M	R/W	1	BUCK5 FLT mask 0b = Unmask **1b = Masked**	
3	BUCK4_FLT_M	R/W	1	BUCK4 FLT mask 0b = Unmask **1b = Masked**	
2	BUCK3_FLT_M	R/W	1	BUCK3 FLT mask 0b = Unmask **1b = Masked**	
1	BUCK2_FLT_M	R/W	1	BUCK2 FLT mask 0b = Unmask **1b = Masked**	
0	BUCK1_FLT_M	R/W	1	BUCK1 FLT mask 0b = Unmask **1b = Masked**	

8.2.42 0x2E VRFLT2_MASK

VR fault mask bit. Once the bit is masked, PCA9452 does not enter Fault shutdown even if fault condition of corresponding regulator happens.

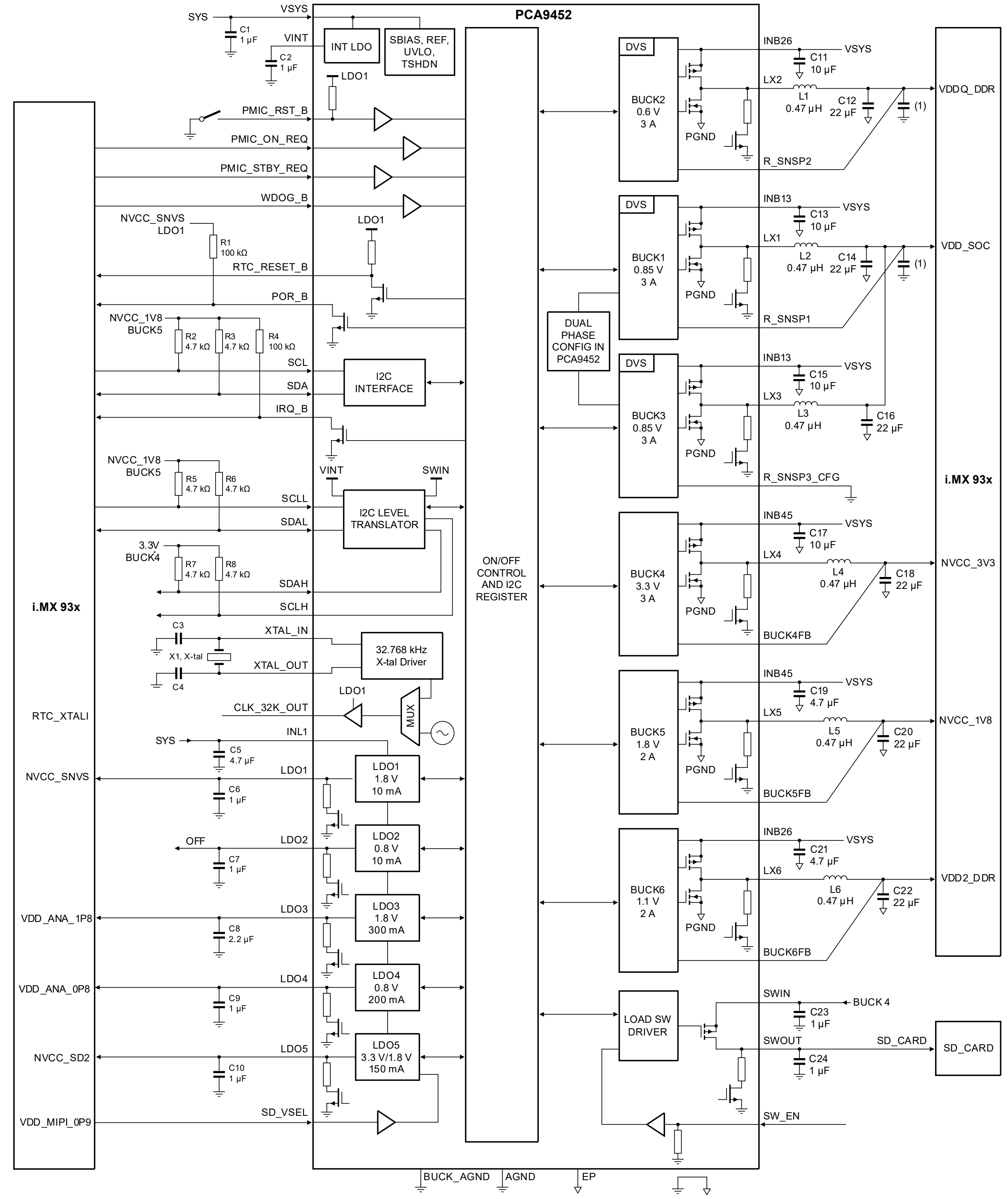
Table 67. 0x2E VRFLT2_MASK

0x2E – VRFLT2_MASK				**Reset Type**	**S**
Bit	**Name**	**Type**	**Reset**	**Description**	
7:5	RSVD	R/W/C	0	Reserved	
4	LDO5_FLT_M	R/W	1	LDO5 FLT mask 0b = Unmask **1b = Masked**	
3	LDO4_FLT_M	R/W	1	LDO4 FLT mask 0b = Unmask **1b = Masked**	
2	LDO3_FLT_M	R/W	1	LDO3 FLT mask 0b = Unmask **1b = Masked**	
1	LDO2_FLT_M	R/W	1	LDO2 FLT mask 0b = Unmask **1b = Masked**	
0	LDO1_FLT_M	R/W	1	LDO1 FLT mask 0b = Unmask **1b = Masked**	

9 Application design-in information

9.1 Reference schematic

PCA9452 reference schematic with i.MX 93x is illustrated in Figure 20.



aaa-046677

(1) Decoupling capacitor in MCU side.

Figure 20. Application schematic

9.2 Typical application

The PCA9452 devices have only a few design requirements. Use the following parameters for the design.

- 1 μF bypass capacitor on VINT and VSYS, located as close as possible to those pins to ground
- Input capacitors must be present on the INB and INL supplies if used
- Output inductors and capacitors must be used on the outputs of the BUCK converters if used
- Output capacitors must be used on the outputs of the LDOs

9.2.1 Detailed design procedure

9.2.2 Inductor selection for buck converters

Each of the converters in the PCA9452 typically use a 0.47 μH output inductor which has to be rated for its DC resistance and saturation current. The DC resistance of the inductance influences directly the efficiency of the converter. Therefore, an inductor with lowest DC resistance must be selected for highest efficiency.

Equation 1 calculates the maximum inductor current under static load conditions. The saturation current of the inductor must be rated higher than the maximum inductor current as calculated with Equation 2. This is needed because during heavy load transient the inductor current rises above the calculated value.

$$\Delta \mathrm{I}_L = Vout \times \frac{1-\frac{Vout}{Vinmax}}{L \times f} \tag{1}$$

$$\mathrm{I}_{L.max} = \mathrm{I}_{out.max} \times \frac{\Delta \mathrm{I}_L}{2} \tag{2}$$

Where

f = switching frequency (2 MHz)

L = Inductance

ΔI_L = Peak to peak inductor ripple current

$I_{L.max}$ = Maximum inductor current

A conservative approach is to select the inductor current rating just for the maximum switch current of the PCA9452.

9.2.3 Output capacitor selection for buck converters

The fast response adaptive constant ON time control scheme of the buck converters implemented in the PCA9452 allow the use of small ceramic capacitors with a typical value of 22 μF for each converter without having large output voltage under and overshoots during heavy load transients. Ceramic capacitors having low ESR values have the lowest output voltage ripple and are recommended.

If ceramic output capacitors are used, the capacitor RMS ripple current rating always meets the application requirements. Just for completeness, the RMS ripple current is calculated in Equation 3.

$$I_{RMS.COUT} = \mathrm{Vout} \times \frac{1-\frac{\mathrm{Vout}}{\mathrm{Vin}}}{\mathrm{L} \times \mathrm{f}} \times \frac{1}{2\sqrt{3}} \tag{3}$$

At nominal load current, the inductive converters operate in PWM mode. The overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta \mathrm{Vout} = \mathrm{Vout} \times \frac{1\text{-}\frac{Vout}{Vin}}{\mathrm{L} \times \mathrm{f}} \times \left(\frac{1}{8 \times Cout \times f} + ESR \right) \tag{4}$$

Where:

The highest output voltage ripple occurs at the highest input voltage Vin.

At light load currents, the converters operate in PFM mode and the output voltage ripple is dependent on the output capacitor value. The output voltage ripple is set by the internal comparator delay and the external capacitor. The typical output voltage ripple is less than 1 % of the nominal output voltage.

9.2.4 Input capacitor selection for buck converters

Low ESR input capacitor is highly recommended for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes because of the nature of buck converter. Each DC-DC converter requires a 10 μF ceramic input capacitor on its input pins. The input capacitor could be increased without any limit for better input voltage filtering.

9.3 Layout guide

Figure 21 shows layout guidance.

All components related to the power stage should be kept as close to the PMIC as possible, especially decoupling input and output capacitors. Place these components in order of priority:

- Input capacitor of the buck regulators
- LDO capacitors
- VSYS and VINT capacitors
- Buck regulator inductors
- Buck regulator output capacitors

Care must be taken with BUCKxFB pins traces. These signals are susceptible to noise and must be routed far away from power, clock, or high power signals, like the ones on the INBxx, and LXx pins. The exposed pad (EP) is the power ground of all bucks which is relatively noisy. AGND is the analog ground. Do not connect AGND to EP on the top layer. Connect AGND to main ground by via. Avoid separating the main ground under PCA9452 which may increase the return path. Make sure that there are enough vias to connect EP to system main ground.

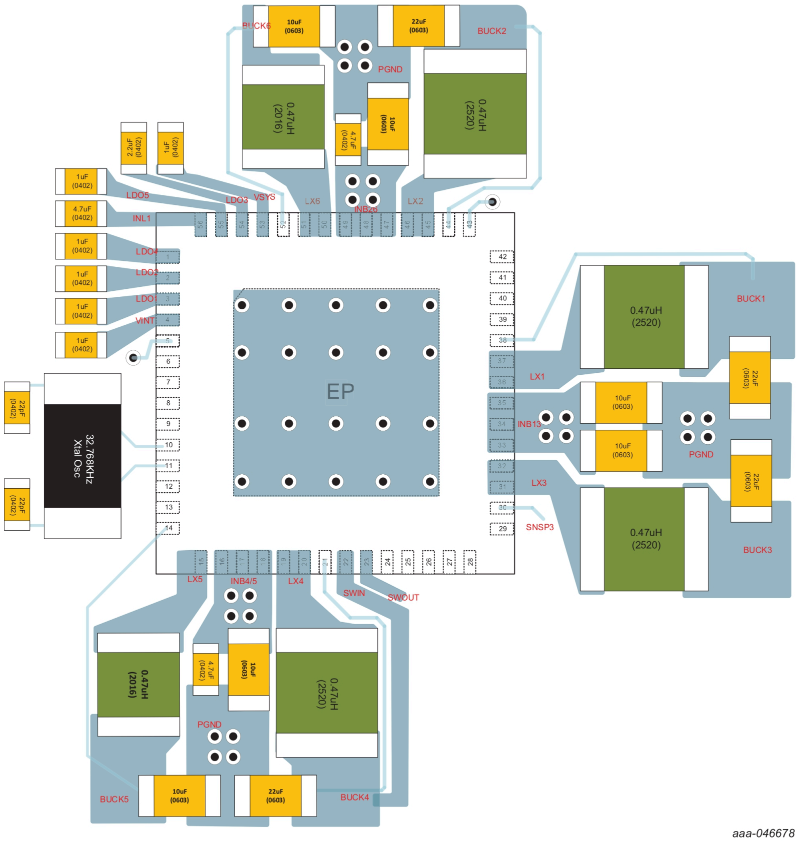


Figure 21. PCA9452 layout

10 Limiting values

Table 68. Limiting values (Absolute Maximum Ratings)

Explanation	Pin	Conditions	Min	Max	Unit
Voltage range (with respect to EP)	VSYS, INB13, INB26, INB45, INL1, SWIN		-0.5	+6.0	V
	SWOUT		-0.5	SWIN + 0.5	V
	LX1, LX3		-0.5	INB13 + 0.5	V
	LX2, LX6		-0.5	INB26 + 0.5	V
	LX4, LX5		-0.5	INB45 + 0.5	V
	R_SNSP1, R_SNSP2, R_SNSP3_CFG		-0.5	VSYS + 0.5	V
	BUCK_AGND, AGND		-0.5	+0.5	
	BUCK4FB, BUCK5FB, BUCK6FB		-0.5	VSYS + 0.5	V
	LDO1, LDO2, LDO3, LDO4, LDO5		-0.5	V_{INL1} + 0.5	V
	XTAL_IN, XTAL_OUT		-0.5	VSYS + 0.5	V
	RTC_RESET_B, PMIC_RST_B, CLK_32K_OUT		-0.5	LDO1 + 0.5	V
	PMIC_ON_REQ, POR_B PMIC_STBY_REQ, WDOG_B, IRQ_B, SCL, SDA, SD_VSEL, SW_EN		-0.5	VSYS + 0.5	V
	SCLH, SDAH		-0.5	SWIN + 0.5	V
	SCLL, SDAL		-0.5	VINT + 0.5	
	VINT		-0.5	+2.0	V
Output Current	LX1, LX2, LX3, LX4	RMS current		5.0	A
	LX5, LX6	RMS current		4.0	A
	SWIN, SWOUT	RMS current		0.5	A
Junction temperature			-40	+150	°C
V_{ESD}	All pins	HBM (JS-001)	-2	+2	kV
		CDM (JS-002)	-500	+500	V
	Corner pins	CDM (JS-002)	-750	+750	V

11 Recommended operating conditions

Table 69. Recommended operating conditions

Explanation	Pin	Conditions	Min	Max	Unit
Voltage range (with respect to EP)	VSYS, INL1		2.7	5.5	V
	INB13, INB26, INB45		2.7	5.5	V
	SWIN, SWOUT		2.7	5.5	V
Junction temperature			-40	+125	°C

Table 69. Recommended operating conditions*...continued*

Explanation	Pin	Conditions	Min	Max	Unit
Ambient temperature			-40	+105	°C
Storage temperature			-65	+150	°C

12 Thermal characteristics

Table 70. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	JESD51-7, 2s2p	[1] [2] [3]	42.2	°C/W
$\Psi_{j\text{-}top}$	junction to top of package	JESD51-7, 2s2p	[1] [2] [3]	7.3	°C/W

[1] Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment

[2] Thermal test board meets JEDEC specification for this package (JESD51-7)

[3] Heat dissipation on die: 0.812W

13 Electrical Characteristics

13.1 Top level parameter

Table 71. Top level parameter

Unless otherwise specified, VSYS = 3.8 V, V_{INBx} = 3.8 V, V_{INL1} = 3.8 V, T_{amb}= -40 °C ~ +105 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Quiescent Current						
I_{Q_SNVS}	VSYS SNVS Current	LDO1 is ON and no load, other regulators are OFF, CLK_32K_OUT enabled, PMIC_ON_REQ = L, T_{amb}= 25 °C		23	TBD	µA
		LDO1 is ON and no load, other regulators are OFF, CLK_32K_OUT enabled, PMIC_ON_REQ = L, T_{amb}= -40 °C ~105 °C		23	TBD	µA
$I_{Q\_STANDBY}$	VSYS Standby Current	LDO1, LDO3, LDO4, LDO5, BUCK1, BUCK3, BUCK4, BUCK5, BUCK6 are ON and no load. PMIC_ON_REQ = H, PMIC_STBY_REQ = H		220	TBD	µA
VSYS						
V_{SYS_UVLO}	VSYS UVLO	Rising – MTP Programmable 00b = 2.85 V **01b = 3.0 V** 10b = 3.15 V 11b = 3.3 V	2.85	3.0	3.15	V
$V_{SYS\_UVLO\_H}$	VSYS UVLO Hysteresis	Falling		200		mV
V_{SYS_POR}	VSYS POR	Rising	2.2	2.4	2.6	V
$V_{SYS\_POR\_H}$	VSYS POR Hysteresis	Falling		200		mV

Table 71. Top level parameter*...continued*

Unless otherwise specified, VSYS = 3.8 V, V_{INBx} = 3.8 V, V_{INL1} = 3.8 V, T_{amb}= -40 °C ~ +105 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VINT						
V_{INT}	Internal Power supply LDO	VSYS = 3.8 V	1.7	1.8	1.9	V
Low VSYS						
V_{LOW_VSYS}	Low VSYS	Low VSYS threshold above V_{SYS_UVLO}, LOW_VSYS [7:6] = 01b	150	200	250	mV
$V_{LOW\_VSYS\_HYS}$	Low VSYS Hysteresis			110		mV
Thermal Shutdown						
T_{JSHDN}	Thermal Shutdown	Tj Rising, 15 °C hysteresis		150		°C
T_{J105}	Thermal interrupt1	Tj Rising, 15 °C hysteresis	95	105	125	°C
T_{J125}	Thermal interrupt2	Tj Rising, 15 °C hysteresis	115	125	145	°C
Logic and Control signals						
V_{IL}	Input Low level	PMIC_ON_REQ, PMIC_STBY_REQ, WDOG_B, SD_VSEL, SW_EN, PMIC_RST_B			0.4	V
V_{IH}	Input High level	PMIC_ON_REQ, PMIC_STBY_REQ, WDOG_B, SD_VSEL, SW_EN, PMIC_RST_B	1.4			V
I_{LEAK}	Logic Input leakage current	PMIC_ON_REQ, PMIC_STBY_REQ, WDOG_B, SD_VSEL: V_{Logic} = 5.5 V, VSYS = 5.5 V	-0.5		+0.5	μA
R_{PD}	Internal Pull-down resistor	SW_EN		1.2		MΩ
V_{OL}	Output Low level	RTC_RESET_B, IRQB, POR_B, I_{OL} = 6mA			0.4	V
R_{PU}	Internal Pull-up resistor	RTC_RESET_B, PMIC_RST_B to LDO1		100		KΩ
Logic signal						
V_{IL}	Input Low level	R_SNSP3_CFG[1]			0.4	V
V_{IH}	Input High level	R_SNSP3_CFG[1]	1.4			V
I_{LEAK}	Logic Input leakage current	R_SNSP3_CFG[1] V_{Logic} = 5.5 V, VSYS = 5.5 V	-1		+1	μA
Timing spec						
t_{DEB_POKB}	Debounce time of regulator POKB		320	400	480	us
$t_{DEB\_POKB\_SW}$	Debounce time of Load SW POKB		240	300	360	us
t_{DEB_WDOGB}	Debounce time of WDOG_B		90	120	150	us
$t_{DEB\_PMIC\_RST\_B}$	Debounce time of PMIC_RST_B	T_PMIC_RST_DEB[2:0] = 001b	40	50	60	ms
t_{SNVS_PU}	Time to 90 % of LDO1 from VSYS UVLO detected		16	20	24	ms
t_{RTC_RST}	Time to RTC_RESET_B release from LDO1 POK		16	20	24	ms
t_{32K_EN}	Time to 32K buffer enable from LDO POK		8	10	12	ms

Table 71. Top level parameter*...continued*

Unless otherwise specified, VSYS = 3.8 V, V_{INBx} = 3.8 V, V_{INL1} = 3.8 V, T_{amb}= -40 °C ~ +105 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{RTC_TRAN}	Time to transition to Xtal osc after RTC_RESET_B release		0.8	1	1.2	sec
t_{ON_DEB}	PMIC_ON_REQ high debounce time	Programmable, t_{ON_DEB}[1:0] = 01b	16	20	24	ms
t_{STEP}	Time step to turn on each regulator	Programmable, t_{STEP}[1:0] = 01b	1.6	2	2.4	ms
t_{OFF_STEP}	Time step to turn off each regulator	Programmable, t_{OFF_STEP}[1:0] = 10b	6	8	10	ms
t_{OFF_DEB}	PMIC_ON_REQ low debounce time	Programmable, t_{OFF_DEB} = 0b	90	120	150	µs
t_{PORB}	Time from LDO5 POK to POR_B release during power on seq		16	20	24	ms
$t_{FLT\_SD\_PU}$	Fault time to POK after regulator enable during power up sequence	At power up sequence	8	10	12	ms
$t_{FLT\_POK\_MSK}$	POK mask time when regulator is enabled at RUN/Standby mode		1.6	2	2.4	ms
t_{FLT_THSD}[2]	Time to enter FAULT_SD when thermal Fault occurs		170	210	250	µs
$t_{FLT\_SD\_STAY}$	Time to stay at FAULT_SD to move other mode		80	100	120	ms
$t_{FLT\_SD\_WAIT}$	Wait time to enter FAULT_ SD after fault interrupt	At Standby and Run mode, programmable, tFLT_SD_WAIT = 0b1	80	100	120	ms
$t_{RESTART}$	Wait time to start power up after power down at cold reset	Programmable, Trestart = 0b	200	250	300	ms
t_{WRESET}	POR_B low time at Warm reset		16	20	24	ms

[1] BUCK3 MTP bit needs to be programmed.
[2] Guaranteed by design

13.2 I^{2}C level translator

Table 72. I^{2}C level translator

Unless otherwise specified, VSYS = 3.8 V, V_{INBx} = 3.8 V, V_{INL1} = 3.8 V, T_{amb}= -40 °C ~ +105 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDDH	Operating voltage	Internally tied to SWIN	2.7		5.5	V
I_{VDDH}	Shutdown current	SWIN = 3.3 V, I2C_LT_EN bit = 0b		1	5	µA
I_{VDDH}	Active current	SWIN = 3.3 V, I2C_LT_EN bit = 1b, SCLL, SDAL = 1.8 V		60	90	µA
I_{VDDH}	Active current	SWIN = 3.3 V, I2C_LT_EN bit = 1b, SCLL, SDAL = 0 V		715	850	µA
V_{IH}	High level input voltage	SWIN = 3.3 V, I2C_LT_EN bit = 1b	VINT – 0.2			V

Table 72. I^{2}C level translator*...continued*

Unless otherwise specified, VSYS = 3.8 V, V_{INBx} = 3.8 V, V_{INL1} = 3.8 V, T_{amb}= -40 °C ~ +105 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	SWIN = 3.3 V, I2C_LT_EN bit = 1b			0.15	V
V_{OH}	High level output voltage	SWIN = 3.3 V, I2C_LT_EN bit = 1b, I_{OL} = 20 µA	0.75 * SWIN			V
V_{OL}	Low level output voltage	SWIN = 3.3 V, I2C_LT_EN bit = 1b, I_{OL} = 1 mA			0.4	V
$C_{I/O}$ [1]	Input Output capacitance	SWIN = 3.3 V		5		pF
t_{PHL}[1]	High to Low propagation delay	SWIN = 3.3 V, SCL/SDA to SCLH/SDAH		4.0	4.7	ns
t_{PLH}[1]	Low to High propagation delay	SWIN = 3.3 V, SCL/SDA to SCLH/SDAH		5.0	6.8	ns
t_{PHL}[1]	High to Low propagation delay	SWIN = 3.3 V, SCLH/SDAH to SCL/SDA		6.0	7.0	ns
t_{PLH}[1]	Low to High propagation delay	SWIN = 3.3 V, SCLH/SDAH to SCL/SDA		4.0	4.5	ns
t_{en}[1]	Enable time	SWIN = 3.3 V, from I^{2}C enable		100		us
f_{data}[1]	Data rate				20	Mbps

[1] Guaranteed by design

13.3 Dual-phase BUCK1/BUCK3

Table 73. Dual-phase BUCK1/BUCK3

Unless otherwise specified, VSYS = 3.8 V, V_{INBx} = 3.8 V, V_{INL1} = 3.8 V, V_{BUCK1} = 0.85 V, C_{OUT} = 44 µF, T_{amb}= -40 °C ~ +105 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{INB13}	Input voltage range	INB13 pin	2.85		5.5	V
$I_{Shutdown}$	Shutdown current	Regulator disabled, V_{INB13} = 5.0 V		0.2		µA
I_Q	Quiescent current	Regulator enabled, No load, No switching		20		µA
I_{OUT_MAX}	Max Output Current		4000			mA
V_{BUCK1}	Programmable Output voltage range	I^{2}C programmable, 12.5 mV step	0.6		2.1875	V
V_{BUCK1_OUT}	DC Output Voltage Accuracy	V_{INB13} = 3.8 V, V_{BUCK1_OUT} = 0.85 V, IOUT = 0A, FPWM mode	-2		2	%
$\Delta V_{OUT(\Delta VINB)}$	DC Line regulation	V_{INB13} = 3V to 5 V, I_{OUT}= I_{OUT_MAX}		2		mV/V
$\Delta V_{OUT(\Delta IOUT)}$	DC Load regulation	0 mA < I_{OUT} < I_{OUT_MAX}, V_{BUCK1_OUT} = 0.85 V		3		mV/A
$\Delta V_{OUT(\Delta IOUT)}$	Transient Load Response	I_{OUT} changes 0 to I_{OUT_MAX} (1A/us slope), V_{BUCK1_OUT} = 0.85 V		50		mV
ΔV_{OUT}	Output voltage Ripple	FPWM mode		10		mV

Table 73. Dual-phase BUCK1/BUCK3*...continued*

Unless otherwise specified, VSYS = 3.8 V, V_{INBx} = 3.8 V, V_{INL1} = 3.8 V, V_{BUCK1} = 0.85 V, C_{OUT} = 44 μF, T_{amb}= -40 °C ~ +105 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SW}	Switching Frequency in CCM			2		MHz
R_{DSON}	High Side P-FET R_{DSON}	V_{INB13} = 3.8 V		87		mΩ
	Low Side N-FET R_{DSON}	V_{INB13} = 3.8 V		45		mΩ
I_{LIM}	High side current limit	V_{INB13} = 3.8 V	4.0	4.5	5.0	A
	Low side current limit	V_{INB13} = 3.8 V	2.5	3.0	3.7	A
t_{START}	Startup time	EN rising to 90 % of output voltage		250	500	μs
V_{RAMP}	Output voltage slew rate	Programmable, RAMP[1:0] = 01b		12.5		mV/us
V_{soft_strup}	Soft-start slew rate			12.5		mV/us
R_{DIS}	Output Active Discharge Resistance			100	150	Ω
POK	Output Power good			85	95	%
L	Inductor value			0.47		μH
C_{OUT}	Output capacitance	Minimum nominal capacitance	44		88	μF

13.4 BUCK2

Table 74. BUCK2

Unless otherwise specified, VSYS = 3.8 V, V_{INBx} = 3.8 V, V_{INL1} = 3.8 V, V_{BUCK2} = 0.6 V, C_{OUT} = 22 μF, T_{amb}= -40 °C ~ +105 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{INB26}	Input voltage range	INB26 pin	2.85		5.5	V
$I_{Shutdown}$	Shutdown current	Regulator disabled, V_{INB26} = 5.0 V		0.1		μA
I_Q	Quiescent current	Regulator enabled, No load, No switching		20		μA
I_{OUT_MAX}	Max Output Current		3000			mA
V_{BUCK2}	Programmable Output voltage range	I^2C programmable, 12.5 mV step	0.6		2.1875	V
V_{BUCK2_OUT}	DC Output Voltage Accuracy	V_{INB26} = 3.8 V, V_{BUCK2_OUT} = 0.6 V, IOUT = 0A, FPWM mode	-2		2	%
$\Delta V_{OUT(\Delta VINB)}$	DC Line regulation	V_{INB26} = 3V to 5 V, I_{OUT}= I_{OUT_MAX}		2		mV/V
$\Delta V_{OUT(\Delta IOUT)}$	DC Load regulation	0 mA < I_{OUT} < I_{OUT_MAX}, V_{BUCK2_OUT} = 0.6 V		3		mV/A
$\Delta V_{OUT(\Delta IOUT)}$	Transient Load Response	I_{OUT} changes 0 to I_{OUT_MAX} (1A/us slope), V_{BUCK2_OUT} = 0.6 V		50		mV
ΔV_{OUT}	Output voltage Ripple	FPWM mode		10		mV
f_{SW}	Switching Frequency in CCM			2		MHz
R_{DSON}	High Side P-FET R_{DSON}	V_{INB26} = 3.8 V		87		mΩ

Table 74. BUCK2*...continued*

Unless otherwise specified, VSYS = 3.8 V, V_{INBx} = 3.8 V, V_{INL1} = 3.8 V, V_{BUCK2} = 0.6 V, C_{OUT} = 22 µF, T_{amb}= -40 °C ~ +105 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Low Side N-FET R_{DSON}	V_{INB26} = 3.8 V		45		mΩ
I_{LIM}	High side current limit	V_{INB26} = 3.8 V	4.0	4.5	5.0	A
	Low side current limit	V_{INB26} = 3.8 V	2.5	3.0	3.7	A
t_{START}	Startup time	EN rising to 90 % of output voltage		250	500	µs
V_{RAMP}	Output voltage slew rate	Programmable, RAMP[1:0] = 01b		12.5		mV/us
V_{soft_strup}	Soft-start slew rate			12.5		mV/us
POK	Output Power good		75	85	95	%
R_{DIS}	Output Active Discharge Resistance			100	150	Ω
L	Inductor value			0.47		µH
C_{OUT}	Output capacitance	Minimum nominal capacitance	22		44	µF

13.5 BUCK4

Table 75. BUCK4

Unless otherwise specified, VSYS = 3.8 V, V_{INBx} = 3.8 V, V_{INL1} = 3.8 V, V_{BUCK4} = 3.3 V, C_{OUT} = 22 µF, T_{amb}= -40 °C ~ +105 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{INB45}	Input voltage range	INB45 pin	2.85		5.5	V
$I_{Shutdown}$	Shutdown current	Regulator disabled, V_{INB45} = 5.0 V		0.1		µA
I_Q	Quiescent current	Regulator enabled, No load, No switching		20		µA
I_{OUT_MAX}	Max Output Current		3000			mA
V_{BUCK4}	Programmable Output voltage range	I^2C programmable, 25 mV step	0.6		3.4	V
V_{BUCK4_OUT}	DC Output Voltage Accuracy	V_{INB45} = 3.8 V, V_{BUCK4_OUT} = 3.3 V, IOUT = 0A, FPWM mode	-2		2	%
$\Delta V_{OUT(\Delta VINB)}$	DC Line regulation	V_{INB45} = 4 V to 5 V, I_{OUT}= I_{OUT_MAX}		2		mV/V
$\Delta V_{OUT(\Delta IOUT)}$	DC Load regulation	0 mA < I_{OUT} < I_{OUT_MAX}, V_{BUCK4_OUT} = 3.3 V		6		mV/A
$\Delta V_{OUT(\Delta IOUT)}$	Transient Load Response	I_{OUT} changes 0 to I_{OUT_MAX} (1A/us slope), V_{BUCK4_OUT} = 3.3 V		160		mV
ΔV_{OUT}	Output voltage Ripple	FPWM mode		10		mV
f_{SW}	Switching Frequency in CCM			2		MHz
R_{DSON}	High Side P-FET R_{DSON}	V_{INB45} = 3.8 V		87		mΩ
	Low Side N-FET R_{DSON}	V_{INB45} = 3.8 V		45		mΩ
I_{LIM}	High side current limit	V_{INB45} = 3.8 V	4.0	4.5	5.0	A
	Low side current limit	V_{INB45} = 3.8 V	2.5	3.0	3.7	A

Table 75. BUCK4*...continued*

Unless otherwise specified, VSYS = 3.8 V, V_{INBx} = 3.8 V, V_{INL1} = 3.8 V, V_{BUCK4} = 3.3 V, C_{OUT} = 22 µF, T_{amb}= -40 °C ~ +105 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{START}	Startup time	EN rising to 90 % of output voltage		250	500	µs
V_{soft_strup}	Soft-start slew rate			12.5		mV/us
POK	Output Power good		75	85	95	%
R_{DIS}	Output Active Discharge Resistance			100	150	Ω
L	Inductor value			0.47		µH
C_{OUT}	Output capacitance	Minimum nominal capacitance	22		44	µF

13.6 BUCK5

Table 76. BUCK5

Unless otherwise specified, VSYS = 3.8 V, V_{INBx} = 3.8 V, V_{INL1} = 3.8 V, V_{BUCK5} = 1.8 V, C_{OUT} = 22 µF, T_{amb}= -40 °C ~ +105 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{INB45}	Input voltage range	INB45 pin	2.85		5.5	V
$I_{Shutdown}$	Shutdown current	Regulator disabled, V_{INB45} = 5.0 V		0.1		µA
I_Q	Quiescent current	Regulator enabled, No load, No switching		20		µA
I_{OUT_MAX}	Max Output Current		2000			mA
V_{BUCK5}	Programmable Output voltage range	I^2C programmable, 25 mV step	0.6		3.4	V
V_{BUCK5_OUT}	DC Output Voltage Accuracy	V_{INB45} = 3.8 V, V_{BUCK5_OUT} = 1.8 V, IOUT = 0A, FPWM mode	-2		2	%
$\Delta V_{OUT(\Delta VINB)}$	DC Line regulation	V_{INB45} = 3V to 5 V, I_{OUT}= I_{OUT_MAX}		2		mV/V
$\Delta V_{OUT(\Delta IOUT)}$	DC Load regulation	0 mA < I_{OUT} < I_{OUT_MAX}, V_{BUCK5_OUT} = 1.8 V		7		mV/A
$\Delta V_{OUT(\Delta IOUT)}$	Transient Load Response	I_{OUT} changes 0 to I_{OUT_MAX} (1A/us slope), V_{BUCK5_OUT} = 1.8 V		50		mV
ΔV_{OUT}	Output voltage Ripple	FPWM mode		22		mV
f_{SW}	Switching Frequency in CCM			2		MHz
R_{DSON}	High Side P-FET R_{DSON}	V_{INB45} = 3.8 V, including bonding wire		130		mΩ
	Low Side N-FET R_{DSON}	V_{INB45} = 3.8 V, including bonding wire		70		mΩ
I_{LIM}	High side current limit	V_{INB45} = 3.8 V	3.0	3.5	4.0	A
	Low side current limit	V_{INB45} = 3.8 V	1.5	2	2.7	A
t_{START}	Startup time	EN rising to 90 % of output voltage		250	500	µs
V_{soft_strup}	Soft-start slew rate			12.5		mV/us

Table 76. BUCK5*...continued*

Unless otherwise specified, VSYS = 3.8 V, V_{INBx} = 3.8 V, V_{INL1} = 3.8 V, V_{BUCK5} = 1.8 V, C_{OUT} = 22 µF, T_{amb}= -40 °C ~ +105 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
POK	Output Power good		75	85	95	%
R_{DIS}	Output Active Discharge Resistance			100	150	Ω
L	Inductor value			0.47		µH
C_{OUT}	Output capacitance	Minimum nominal capacitance	22		44	µF

13.7 BUCK6

Table 77. BUCK6

Unless otherwise specified, VSYS = 3.8 V, V_{INBx} = 3.8 V, V_{INL1} = 3.8 V, V_{BUCK6} = 1.1 V, C_{OUT} = 22 µF, T_{amb}= -40 °C ~ +105 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{INB26}	Input voltage range	INB26 pin	2.85		5.5	V
$I_{Shutdown}$	Shutdown current	Regulator disabled, V_{INB26} = 5.0 V		0.1		µA
I_Q	Quiescent current	Regulator enabled, No load, No switching		20		µA
I_{OUT_MAX}	Max Output Current		2000			mA
V_{BUCK6}	Programmable Output voltage range	I^2C programmable, 25 mV step	0.6		3.4	V
V_{BUCK6_OUT}	DC Output Voltage Accuracy	V_{INB26} = 3.8 V, V_{BUCK6_OUT} = 1.1 V, IOUT = 0A, FPWM mode	-2		2	%
$\Delta V_{OUT(\Delta VINB)}$	DC Line regulation	V_{INB26} = 3V to 5 V, I_{OUT}= I_{OUT_MAX}		2		mV/V
$\Delta V_{OUT(\Delta IOUT)}$	DC Load regulation	0 mA < I_{OUT} < I_{OUT_MAX}, V_{BUCK6_OUT} = 1.1 V		6		mV/A
$\Delta V_{OUT(\Delta IOUT)}$	Transient Load Response	I_{OUT} changes 0 to I_{OUT_MAX} (1A/us slope), V_{BUCK6_OUT} = 1.1 V		50		mV
ΔV_{OUT}	Output voltage Ripple	FPWM mode		18		mV
f_{SW}	Switching Frequency in CCM			2		MHz
R_{DSON}	High Side P-FET R_{DSON}	V_{INB26} = 3.8 V		130		mΩ
	Low Side N-FET R_{DSON}	V_{INB26} = 3.8 V		70		mΩ
I_{LIM}	High side current limit	V_{INB26} = 3.8 V	3.0	3.5	4.0	A
	Low side current limit	V_{INB26} = 3.8 V	1.5	2	2.7	A
t_{START}	Startup time	EN rising to 90 % of output voltage		250	500	µs
V_{soft_strup}	Soft-start slew rate			12.5		mV/us
POK	Output Power good		75	85	95	%
R_{DIS}	Output Active Discharge Resistance			100	150	Ω
L	Inductor value			0.47		µH

Table 77. BUCK6*...continued*

Unless otherwise specified, VSYS = 3.8 V, V_{INBx} = 3.8 V, V_{INL1} = 3.8 V, V_{BUCK6} = 1.1 V, C_{OUT} = 22 µF, T_{amb}= -40 °C ~ +105 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{OUT}	Output capacitance	Minimum nominal capacitance	22		44	µF

13.8 LDO1

Table 78. LDO1

Unless otherwise specified, VSYS = 3.8 V, V_{INBx} = 3.8 V, V_{INL1} = 3.8 V, V_{LDO1} = 1.8 V, C_{INL1} = 4.7 µF, C_{OUT} = 1 µF, T_{amb}= -40 °C ~ +105 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Input voltage range	INL1 pin	2.85		5.5	V
I_Q	Quiescent current	Regulator enabled, No load		2		µA
I_{OUT_MAX}	Maximum Output DC Current	V_{IN} > 2.85 V, V_{LDO1} = 1.8 V	10			mA
I_{LIMIT}	Short Current Limit	Output shorted to GND	30		60	mA
V_{DO}	Dropout Voltage	$I_{OUT} = I_{OUT\_MAX,}$ V_{IN} = 3.2 V, L1_ OUT[2:0]= 0x7, 3.3 V		35	60	mV
V_{LDO1}	Nominal output voltage	I^2C Programmable, 100 mV step	1.6		3.3	V
	Default voltage			1.8		V
	DC accuracy	V_{LDO1} = 1.8 V, I_{Load} = 5mA	-3		3	%
V_{NOISE}	Output noise	f = 10 Hz to 10 kHz, I_{OUT} = 10 % of $I_{MAX,}$ V_{LDO1} = 1.8 V		400		µV
$\Delta V_{OUT(\Delta VINL)}$	DC Line regulation	V_{LDO1} +0.3V < V_{IN} < 5.5 V, $I_{OUT(LDO1)}$ = 10 % of I_{OUT_MAX}		0.2	0.5	%/V
$\Delta V_{OUT(\Delta IOUT)}$	DC Load regulation	V_{IN} = V_{LDO1} +0.3V to 5.5 V, 0 mA < I_{OUT} < I_{OUT_MAX}		0.5	1	%
$\Delta V_{OUT(\Delta VINL)}$	Transient Line Response	V_{LDO1} +0.3V < V_{IN} < 5.5 V, $I_{OUT(LDO1)}$ = 10 % of $I_{OUT\_MAX,}$ tr = 10 µs		0.5		%/V
$\Delta V_{OUT(\Delta IOUT)}$	Transient Load Response	V_{IN} = V_{LDO1} +0.3V to 5.5 V, 1 mA < I_{OUT} < I_{OUT_MAX} , tr = 10 µs, V_{LDO1} = 1.8 V	-3		3	%
PSRR	Power Supply Rejection ratio	f = 10 Hz to 10 kHz, I_{OUT} = 10 % of I_{OUT_MAX}		45		dB
V_{soft_strup}	Soft-start slew rate	I_{OUT} = 0 mA, 10 % to 90 % of V_{LDO1}		15		mV/µs
V_{ov_srtup}	Overshoot at startup	I_{OUT} = 0 mA			10	mV
t_{en}	Enable time	EN rising to 90 % of output voltage		150		µs
POK	Output Power good	Percentage of V_{LDO1} configuration	75	85	92	%
R_{DIS}	Active Discharge Resistance			100	150	Ω
C_{OUT}	Output capacitance	Minimum nominal capacitance	1		2	µF

13.9 LDO2

Table 79. LDO2

Unless otherwise specified, VSYS = 3.8 V, V_{INBx} = 3.8 V, V_{INL1} = 3.8 V, V_{LDO2} = 0.8 V, C_{INL1} = 4.7 μF, C_{OUT} = 1 μF, T_{amb}= -40 °C ~ +105 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Input voltage range	INL1 pin	2.85		5.5	V
I_Q	Quiescent current	Regulator enabled, No load		2		μA
I_{OUT_MAX}	Maximum Output DC Current	V_{IN} > 2.8 V, V_{LDO2} = 0.8 V	10			mA
I_{LIMIT}	Short Current Limit	Output shorted to GND	30		60	mA
V_{DO}	Dropout Voltage	$I_{OUT} = I_{OUT\_MAX,}$		35	60	mV
V_{LDO2}	Nominal output voltage	I^2C Programmable, 50 mV step	0.8		1.5	V
	Default voltage			0.8		V
	DC accuracy	V_{LDO2} = 0.8 V, I_{Load} = 5mA	-3		3	%
V_{NOISE}	Output noise	f = 10 Hz to 10 kHz, I_{OUT} = 10 % of $I_{MAX,}$ V_{LDO2} = 0.8 V		400		μV
$\Delta V_{OUT(\Delta VINL)}$	DC Line regulation	V_{LDO2} +0.3V < V_{IN} < 5.5 V, $I_{OUT(LDO2)}$ = 10 % of I_{OUT_MAX}		0.2	0.5	%/V
$\Delta V_{OUT(\Delta IOUT)}$	DC Load regulation	V_{IN} = V_{LDO2} +0.3V to 5.5 V, 0 mA < I_{OUT} < I_{OUT_MAX}		0.5	1	%
$\Delta V_{OUT(\Delta VINL)}$	Transient Line Response	V_{LDO2} +0.3V < V_{IN} < 5.5 V, $I_{OUT(LDO2)}$ = 10 % of I_{OUT_MAX}, tr = 10 μs		0.5		%/V
$\Delta V_{OUT(\Delta IOUT)}$	Transient Load Response	V_{IN} = V_{OUT} +0.3V to 5.5 V, 1 mA < I_{OUT} < I_{OUT_MAX} , tr = 10 μs, V_{LDO2} = 0.8 V	-3		3	%
PSRR	Power Supply Rejection ratio	f = 10 Hz to 10 kHz, I_{OUT} = 10 % of I_{OUT_MAX}		60		dB
V_{soft_strup}	Soft-start slew rate	I_{OUT} = 0 mA, 10 % to 90 % of V_{LDO2}		15		mV/μs
V_{ov_srtup}	Overshoot at startup	I_{OUT} = 0 mA			10	mV
t_{EN}	Enable time	EN rising to 90 % of output voltage		100		μs
POK	Output Power good	Percentage of V_{LDO2} configuration	75	85	92	%
R_{DIS}	Active Discharge Resistance			100	150	Ω
C_{OUT}	Output capacitance	Minimum nominal capacitance	1			μF

13.10 LDO3

Table 80. LDO3

Unless otherwise specified, VSYS = 3.8 V, V_{INBx} = 3.8 V, V_{INL1} = 3.8 V, V_{LDO3} = 1.8 V, C_{INL1} = 4.7 μF, C_{OUT} = 2.2 μF, T_{amb}= -40 °C ~ +105 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Input voltage range	INL1	2.85		5.5	V

Table 80. LDO3*...continued*

Unless otherwise specified, VSYS = 3.8 V, V_{INBx} = 3.8 V, V_{INL1} = 3.8 V, V_{LDO3} = 1.8 V, C_{INL1} = 4.7 μF, C_{OUT} = 2.2 μF, T_{amb}= -40 °C ~ +105 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{Shutdown}$	Shutdown current	Regulator disabled, V_{IN} = 5.0 V		0.1		μA
I_Q	Quiescent current	Regulator enabled, No load		15		μA
I_{OUT_MAX}	Maximum Output DC Current	V_{IN} > 2.8 V, V_{LDO3} = 1.8 V	300			mA
I_{LIMIT}	Short Current Limit	Output shorted to GND	310		480	mA
V_{DO}	Dropout Voltage	I_{OUT} = $I_{OUT\_MAX,}$ V_{IN} = 3.2 V, L3_ OUT[4:0] = 0x1F, 3.3 V		70	100	mV
V_{LDO3}	Nominal output voltage	I^2C Programmable, 100 mV step	0.8		3.3	V
	Default voltage			1.8		V
	DC accuracy	V_{LDO3} = 1.8 V, I_{Load} = 5mA	-3		3	%
V_{NOISE}	Output noise	f = 10 Hz to 10 kHz, I_{OUT} = 10 % of $I_{MAX,}$ V_{LDO3} = 1.8 V		150		μV
$\Delta V_{OUT(\Delta VINL)}$	DC Line regulation	V_{LDO3} +0.3V < V_{IN} < 5.5 V, $I_{OUT(LDO3)}$ = 10 % of I_{OUT_MAX}		0.2	0.5	%/V
$\Delta V_{OUT(\Delta IOUT)}$	DC Load regulation	V_{IN} = V_{LDO3} +0.3V to 5.5 V, 0 mA < I_{OUT} < I_{OUT_MAX}		0.6		%
$\Delta V_{OUT(\Delta VINL)}$	Transient Line Response	V_{LDO3} +0.3V < V_{IN} < 5.5 V, $I_{OUT(LDO3)}$ = 10 % of I_{OUT_MAX}, tr = 10 μs		0.5		%/V
$\Delta V_{OUT(\Delta IOUT)}$	Transient Load Response	V_{IN} = V_{LDO3} +0.3V to 5.5 V, 1 mA < I_{OUT} < I_{OUT_MAX} , tr = 10 μs, V_{LDO3} = 1.8 V, T_{amb}= 25 °C	-3		3	%
PSRR	Power Supply Rejection ratio	f = 10 Hz to 10 kHz, I_{OUT} = 10 % of I_{OUT_MAX}		55		dB
V_{soft_strup}	Soft-start slew rate	I_{OUT} = 0 mA, 10 % to 90 % of V_{LDO3}		15		mV/μs
V_{ov_srtup}	Overshoot at startup	I_{OUT} = 0 mA			10	mV
t_{EN}	Enable time	EN rising to 90 % of output voltage		150		μs
POK	Output Power good	Percentage of V_{LDO3} configuration	75	85	92	%
R_{DIS}	Active Discharge Resistance			100	150	Ω
C_{OUT}	Output capacitance	Minimum nominal capacitance	2.2			μF

13.11 LDO4

Table 81. LDO4

Unless otherwise specified, VSYS = 3.8 V, V_{INBx} = 3.8 V, V_{INL1} = 3.8 V, V_{LDO4} = 0.8 V, C_{INL1} = 4.7 μF, C_{OUT} = 1 μF, T_{amb}= -40 °C ~ +105 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Input voltage range	INL1	2.85		5.5	V
$I_{Shutdown}$	Shutdown current	Regulator disabled, V_{IN} = 5.0 V		0.1		μA

Table 81. LDO4*...continued*

Unless otherwise specified, VSYS = 3.8 V, V_{INBx} = 3.8 V, V_{INL1} = 3.8 V, V_{LDO4} = 0.8 V, C_{INL1} = 4.7 μF, C_{OUT} = 1 μF, T_{amb}= -40 °C ~ +105 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_Q	Quiescent current	Regulator enabled, No load		15		μA
I_{OUT_MAX}	Maximum Output DC Current	V_{IN} > 2.8, V_{LDO4} = 0.8 V	200			mA
I_{LIMIT}	Short Current Limit	Output shorted to GND	210		330	mA
V_{DO}	Dropout Voltage	I_{OUT} = I_{OUT_MAX}, V_{IN} = 3.2 V, L4_OUT[4:0] = 0x1F, 3.3 V		60	100	mV
V_{LDO4}	Nominal output voltage	I^2C Programmable, 100 mV step	0.8		3.3	V
	Default voltage			0.8		V
	DC accuracy	V_{LDO4} = 0.8 V, I_{Load} = 5mA	-3		3	%
V_{NOISE}	Output noise	f = 10 Hz to 10 kHz, I_{OUT} = 10 % of I_{MAX}, V_{LDO4} = 0.8 V		150		μV
$\Delta V_{OUT(\Delta VINL)}$	DC Line regulation	V_{LDO4} +0.3V < V_{IN} < 5.5 V, $I_{OUT(LDO4)}$ = 10 % of I_{OUT_MAX}		0.2	0.5	%/V
$\Delta V_{OUT(\Delta IOUT)}$	DC Load regulation	V_{IN} = V_{LDO4} +0.3V to 5.5 V, 0 mA < I_{OUT} < I_{OUT_MAX}		0.9		%
$\Delta V_{OUT(\Delta VINL)}$	Transient Line Response	V_{LDO4} +0.3V < V_{IN} < 5.5 V, $I_{OUT(LDO4)}$ = 10 % of I_{OUT_MAX}, tr = 10 μs		0.5		%/V
$\Delta V_{OUT(\Delta IOUT)}$	Transient Load Response	V_{IN} = V_{LDO4} +0.3V to 5.5 V, 1 mA < I_{OUT} < I_{OUT_MAX} , tr = 10 μs, V_{LDO4} = 0.8 V, T_{amb}= 25 °C	-4		4	%
PSRR	Power Supply Rejection ratio	f = 10 Hz to 10 kHz, I_{OUT} = 10 % of I_{OUT_MAX}		60		dB
V_{soft_strup}	Soft-start slew rate	I_{OUT} = 0 mA, 10 % to 90 % of V_{LDO4}		20		mV/μs
V_{ov_srtup}	Overshoot at startup	I_{OUT} = 0 mA			10	mV
t_{en}	Enable time	EN rising to 90 % of output voltage		100		μs
POK	Output Power good	Percentage of V_{LDO4} configuration	75	85	92	%
R_{DIS}	Active Discharge Resistance			100	150	Ω
C_{OUT}	Output capacitance	Minimum nominal capacitance	1		2	μF

13.12 LDO5

Table 82. LDO5

Unless otherwise specified, VSYS = 3.8 V, V_{INBx} = 3.8 V, V_{INL1} = 3.8 V, V_{LDO5} = 3.3 V, C_{INL1} = 4.7 μF, C_{OUT} = 1 μF, T_{amb}= -40 °C ~ +105 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Input voltage range	INL1 pin	2.85		5.5	V
$I_{Shutdown}$	Shutdown current	Regulator disabled, V_{IN} = 5.0 V		0.1		μA
I_Q	Quiescent current	Regulator enabled, No load		15		μA

Table 82. LDO5*...continued*

Unless otherwise specified, VSYS = 3.8 V, V_{INBx} = 3.8 V, V_{INL1} = 3.8 V, V_{LDO5} = 3.3 V, C_{INL1} = 4.7 µF, C_{OUT} = 1 µF, T_{amb}= -40 °C ~ +105 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{OUT_MAX}	Maximum Output DC Current	V_{IN} > 2.8 V, V_{LDO5} = 3.3 V	150			mA
I_{LIMIT}	Short Current Limit	Output shorted to GND	160		280	mA
V_{DO}	Dropout Voltage	I_{OUT} = $I_{OUT\_MAX,}$ V_{IN} = 3.2 V, L5_ OUT_L[3:0] = 0xF, 3.3 V		50	100	mV
V_{LDO5}	Nominal output voltage	I^2C Programmable, 100 mV step	1.8		3.3	V
	Default voltage	SD_VSEL = Low		3.3		V
		SD_VSEL = High		1.8		V
	DC accuracy	V_{LDO5} = 1.8 V, I_{Load} = 5mA	-3		3	%
V_{NOISE}	Output noise	f = 10 Hz to 10 kHz, I_{OUT} = 10 % of $I_{MAX,}$ V_{LDO5} = 3.3 V		300		µV
$\Delta V_{OUT(\Delta VINL)}$	DC Line regulation	V_{LDO5} +0.3V < V_{IN} < 5.5 V, $I_{OUT(LDO5)}$ = 10 % of I_{OUT_MAX}		0.2	0.5	%/V
$\Delta V_{OUT(\Delta IOUT)}$	DC Load regulation	V_{IN} = V_{LDO5} +0.3V to 5.5 V, 0 mA < I_{OUT} < I_{OUT_MAX}		0.3		%
$\Delta V_{OUT(\Delta VINL)}$	Transient Line Response	V_{LDO5} +0.3V < V_{IN} < 5.5 V, $I_{OUT(LDO5)}$ = 10 % of I_{OUT_MAX}		0.5		%/V
$\Delta V_{OUT(\Delta IOUT)}$	Transient Load Response	V_{IN} = V_{LDO5} +0.3V to 5.5 V, 1 mA < I_{OUT} < I_{OUT_MAX} , tr = 10 µs, V_{LDO5} = 3.3 V, T_{amb}= 25 °C	-3		3	%
PSRR	Power Supply Rejection ratio	f = 10 Hz to 10 kHz, I_{OUT} = 10 % of I_{OUT_MAX}		50		dB
V_{soft_strup}	Soft-start slew rate	I_{OUT} = 0 mA, 10 % to 90 % of V_{LDO5}		15		mV/µs
V_{ov_srtup}	Overshoot at startup	I_{OUT} = 0 mA			10	mV
t_{en}	Enable time	EN rising to 90 % of output voltage		200		µs
POK	Output Power good	Percentage of V_{LDO5} configuration	75	85	92	%
R_{DIS}	Active Discharge Resistance			100	150	Ω
C_{OUT}	Output capacitance	Minimum nominal capacitance	1		2	µF

13.13 Load SW

Table 83. Load SW

Unless otherwise specified, VSYS = 3.8 V, V_{INBx} = 3.8 V, V_{INL1} = 3.8 V, V_{SWIN} = 3.8 V, C_{SWIN} = C_{SWOUT} = 1 µF, T_{amb}= -40 °C ~ +105 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{SWIN}	Input voltage range	SWIN	2.8		5.5	V
I_Q	Quiescent current	Switch enabled, No load, V_{SWIN} = 3.3 V		5	8	µA
I_{SHDN}	Shut down current	SWEN = 0 V, V_{SWIN} = 3.3 V		1	2.5	µA

Table 83. Load SW*...continued*

Unless otherwise specified, VSYS = 3.8 V, V_{INBx} = 3.8 V, V_{INL1} = 3.8 V, V_{SWIN} = 3.8 V, C_{SWIN} = C_{SWOUT} = 1 µF, T_{amb}= -40 °C ~ +105 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{OC}	OverCurrent Threshold		450	800		mA
I_{SC}	Short circuit current threshold			2		A
R_{DSON}	Switch ON resistance	V_{SWIN} = 3.3 V, I_{LOAD} = 200 mA, including bonding wire resistance		200	270	mΩ
t_{en}	Enable time	Time to SWOUT 10 % from EN pin high, V_{SWIN} = 3.3 V		90	120	us
t_{ON}	Output rise time	CL = 10uF, V_{SWIN} = 3.3 V, SWOUT 10 % to 90 %		200	500	us
R_{DIS}	Active Discharge Resistance	SWEN = 0 V		80	120	Ω

13.14 32 kHz internal oscillator

Table 84. 32 kHz internal oscillator

Unless otherwise specified, VSYS = 3.8 V, V_{INBx} = 3.8 V, V_{INL1} = 3.8, T_{amb}= -40 °C ~ +105 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_32K}	Clock frequency	Internal Oscillator	29	32.77	36	kHz
f_{CLK}	Clock frequency	External 32.768 kHz crystal oscillator		32.768		kHz
t_{RTCSTB}	Oscillator stabilization time			1000		ms
Duty	Output Duty cycle		30	50	70	%
V_{OL}	Output Low level	I_{OL} = 1 mA			0.4	V
V_{OH}	Output High level	V_{LDO1} = 1.8 V, I_{OL} = 1 mA	1.6			V

13.15 I^2C interface and logic I/O

Table 85. I^2C interface and logic I/O

Unless otherwise specified, VSYS = 3.8 V, V_{INBx} = 3.8 V, V_{INL1} = 3.8, T_{amb}= -40 °C ~ +105 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SCL, SDA						
f_{I2C}	I^2C c lock frequency		-	-	1	MHz
V_{IH}	High-level Input voltage	SCL, SDA; VSYS= 3.0 V to 5.5 V	1.2	-	-	V
V_{IL}	Low-level Input voltage	SCL, SDA; VSYS= 3.0 V to 5.5 V	-	-	0.4	V
V_{hys}	Hysteresis of Schmitt trigger inputs		0.01	-	-	V
V_{OL}	Low-level output voltage	SDA, Iload = 20 mA, VSYS = 3.0 V to 5.5 V	0	-	0.4	V

Table 85. I^{2}C interface and logic I/O*...continued*

Unless otherwise specified, VSYS = 3.8 V, V_{INBx} = 3.8 V, V_{INL1} = 3.8, T_{amb}= -40 °C ~ +105 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{HD,STA}$	Hold time (repeated) START condition	Fast mode plus; After this period, the first clock pulse is generated	0.26	-	-	μs
t_{LOW}	LOW period of I^{2}C clock	Fast mode plus	0.5	-	-	μs
t_{HIGH}	HIGH period of I^{2}C clock	Fast mode plus	0.26	-	-	μs
$t_{SU,STA}$	Setup time (repeated) START condition	Fast mode plus	0.26	-	-	μs
$t_{HD,DAT}$	Data Hold time	Fast mode plus	0	-	-	μs
$t_{SU,DAT}$	Data Setup time	Fast mode plus	50	-	-	ns
t_r	Rise time of I2C_SCL and I2C_SDA signals	Fast mode plus	-	-	120	ns
t_f	Fall time of I2C_SCL and I2C_SDA signals	Fast mode plus	-	-	120	ns
$t_{SU,STO}$	Setup time for STOP condition	Fast mode plus	0.26	-	-	μs
t_{BUF}	Bus free time between STOP and START condition	Fast mode plus	0.5	-	-	μs
$t_{VD,DAT}$	Data valid time	Fast mode plus		-	0.45	μs
$t_{VD,ACK}$	Data valid acknowledge time	Fast mode plus		-	0.45	μs
t_{SP}	Pulse width of spikes that must be suppressed by input filter		0	-	50	ns

14 Package outline

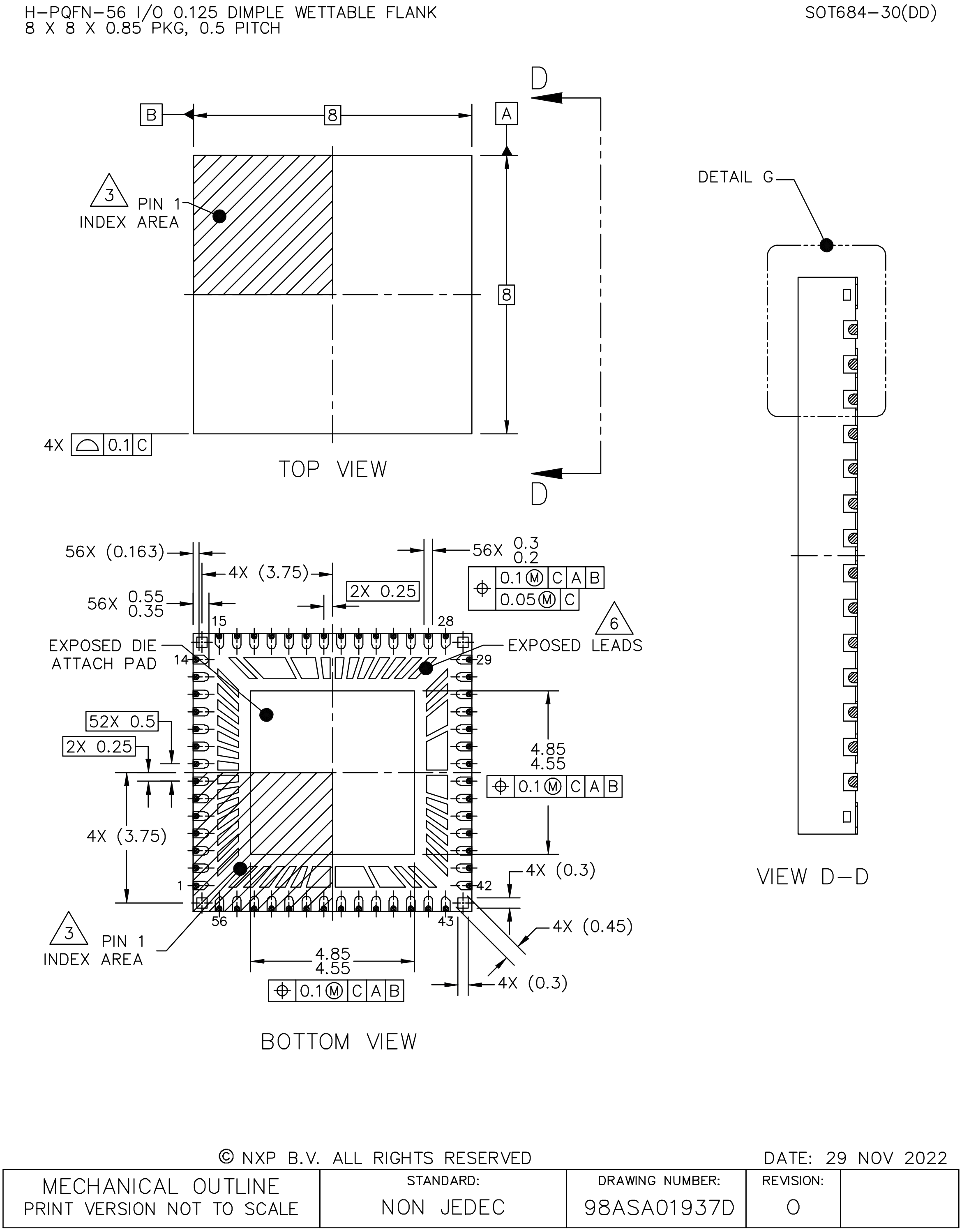
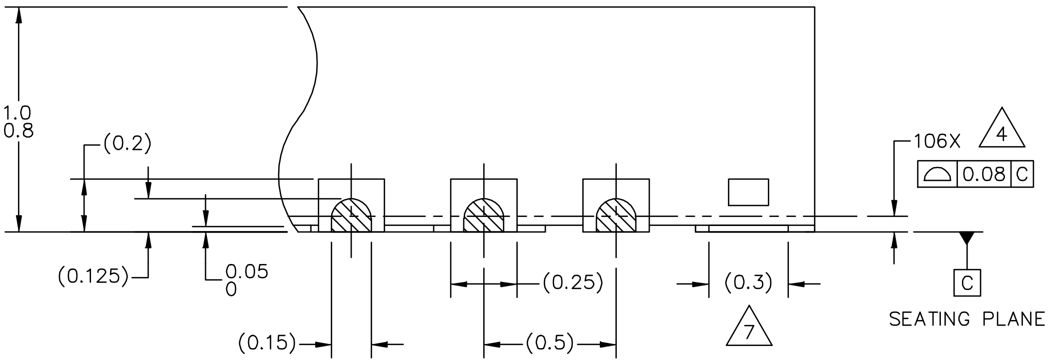


Figure 22. Package outline HVQFN56 (SOT684-30(DD))

H-PQFN-56 I/O 0.125 DIMPLE WETTABLE FLANK
8 X 8 X 0.85 PKG, 0.5 PITCH

SOT684-30(DD)



DETAIL G
VIEW ROTATED 90° CW

DATE: 29 NOV 2022

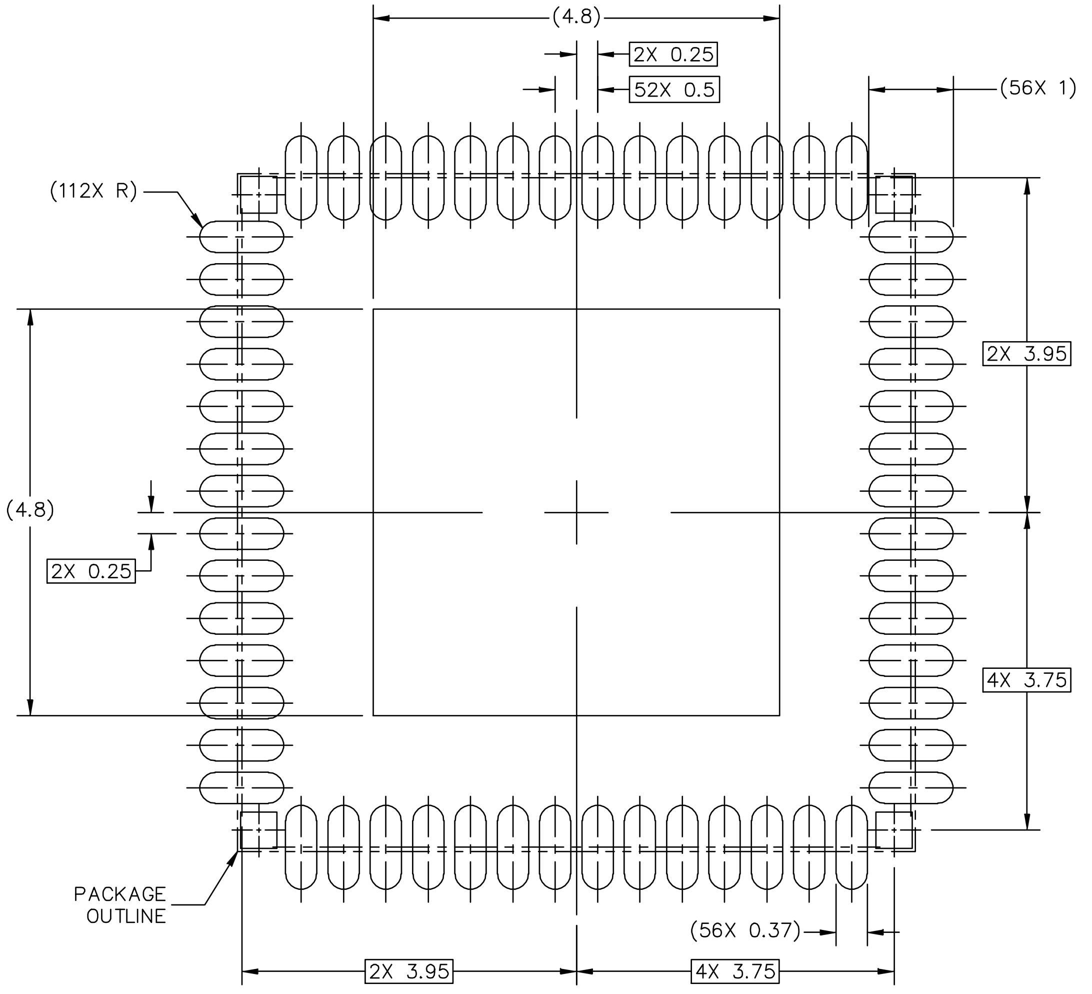
MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01937D	REVISION: 0	

Figure 23. Package outline HVQFN56 (SOT684-30(DD)) detail

15 Soldering

H-PQFN-56 I/O 0.125 DIMPLE WETTABLE FLANK
8 X 8 X 0.85 PKG, 0.5 PITCH

SOT684-30(DD)



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

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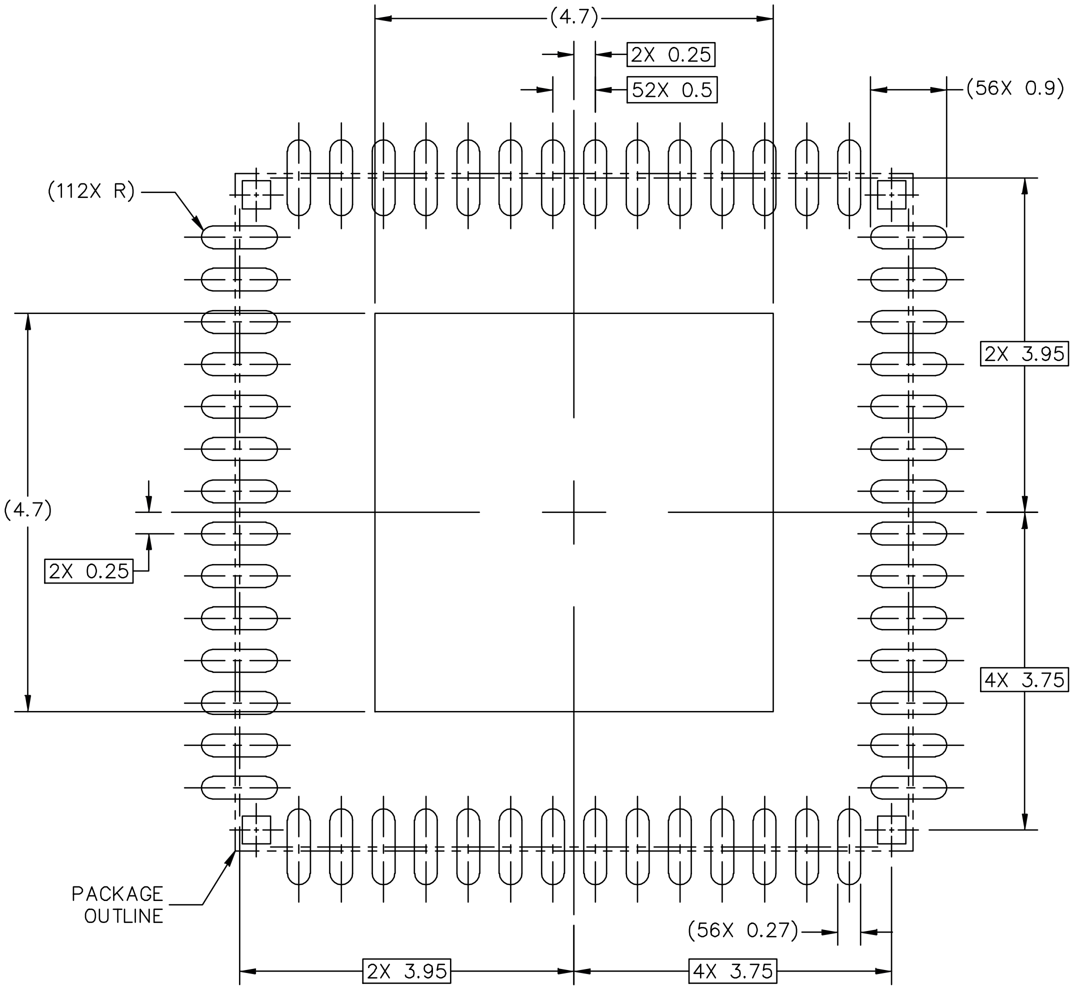
Figure 24. Reflow soldering footprint for HVQFN56 (SOT684-30(DD)); solder mask opening pattern

H-PQFN-56 I/O 0.125 DIMPLE WETTABLE FLANK SOT684-30(DD)
8 X 8 X 0.85 PKG, 0.5 PITCH



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

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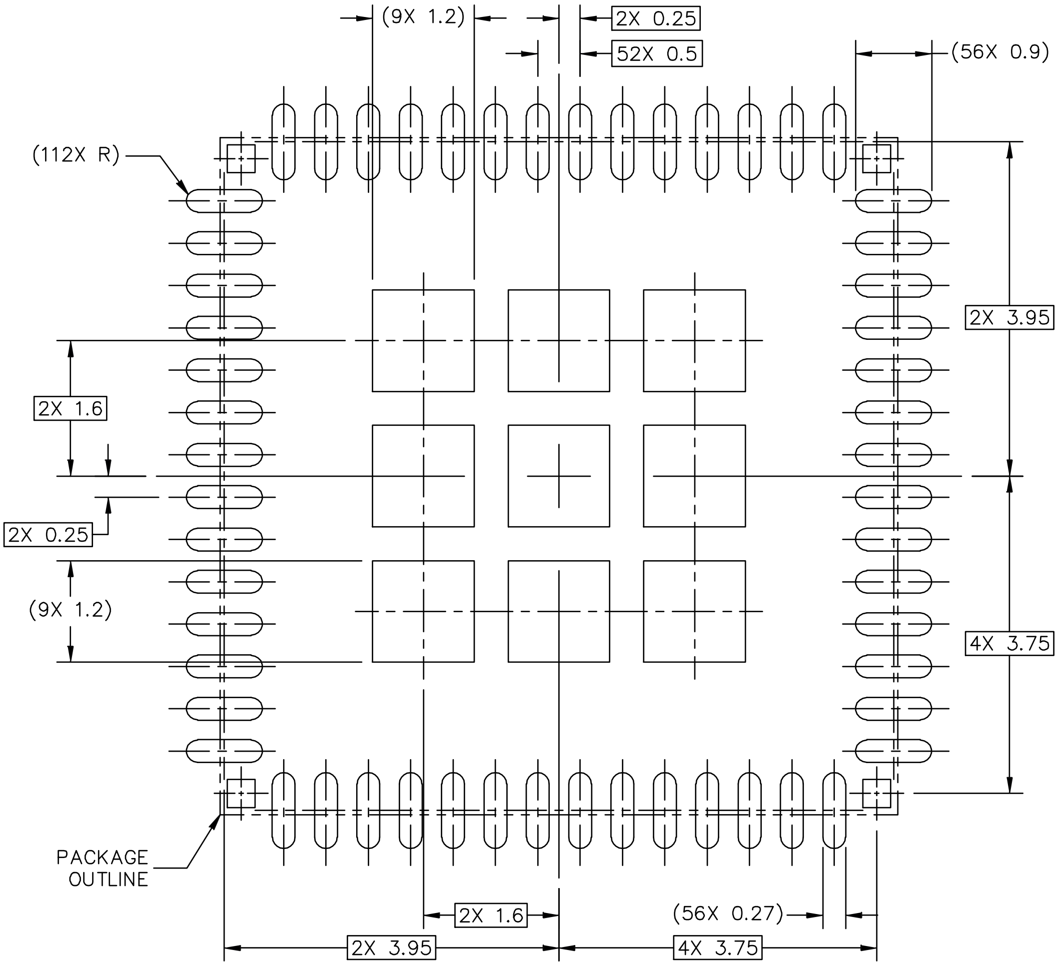
DATE: 29 NOV 2022

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01937D	REVISION: O	

Figure 25. Reflow soldering footprint for HVQFN56 (SOT684-30(DD)); I/O pads and solderable area

H-PQFN-56 I/O 0.125 DIMPLE WETTABLE FLANK
8 X 8 X 0.85 PKG, 0.5 PITCH

SOT684-30(DD)



RECOMMENDED STENCIL THICKNESS 0.125

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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DATE: 29 NOV 2022

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01937D	REVISION: O	

Figure 26. Reflow soldering footprint for HVQFN56 (SOT684-30(DD)); solder paste stencil

H–PQFN–56 I/O 0.125 DIMPLE WETTABLE FLANK
8 X 8 X 0.85 PKG, 0.5 PITCH

SOT684–30(DD)

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. COPLANARITY APPLIES TO LEADS, DIE ATTACH FLAG AND CORNER NON–FUNCTIONAL PADS.
5. MIN. METAL GAP FOR LEAD TO EXPOSED PAD SHALL BE 0.2 MM.
6. EXPOSED INNER LEADS ARE NOT TO BE SOLDERED TO THE PCB. THIS AREA MUST BE COVERED BY SOLDERMASK IN ORDER TO ROUTE IN THIS AREA.
7. ANCHORING PADS.

DATE: 29 NOV 2022

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01937D	REVISION: 0	

Figure 27. Reflow soldering footprint for HVQFN56 (SOT684-30(DD)); note

16 Revision history

Table 86. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9452 v.1.0	20230927	Product data sheet	-	-

17 Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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Tables

Figures

Contents

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