NX5P3363/Q100

USB PD and Type-C current-limited power switch

Rev. 1.1 — 10 September 2024 **Product data sheet**

1 General description

The NX5P3363/Q100 is a precision adjustable current-limited power switch for USB PD application. The device includes undervoltage lockout, overtemperature protection, and reverse current protection circuits to automatically isolate the switch terminals when a fault condition occurs. The 29 V tolerance on VBUS pin ensures the device is able to work on a USB PD port; a current limit input (ILIM) pin defines the overcurrent limit threshold; an open-drain fault output ($\overline{\text{FLT}}$) indicates when a fault condition has occurred.

The overcurrent limit threshold can be programmed from 400 mA to 3.3 A, using an external resistor between the ILIM pin and GND pin. In the overcurrent condition, the device clamps the output current to the value set by ILIM and keeps the switch on while asserting the $\overline{\text{FLT}}$ flag.

To minimize current surges during normal turn on, the device has built-in soft start by limiting the power switch turn on slew rate. However, user can disable the soft start and request a fast output by pulling FO pin HIGH.

A fast recovery reverse current protection (RCP) circuit has been added to the switch to prevent reverse current flowing back to power source at all times. When exiting from reverse current protection state, the power MOSFET turns on within 50 µs. The fast RCP recovery ensures the voltage on VBUS doesn’t drop too much in a power source swap application.

NX5P3363/Q100 is offered in a 2.2 x 2.2 mm, 16 bump WLCSP package.

2 Features and benefits

- VIN supply voltage range from 4.0 V to 5.5 V
- All time reverse current protection with ultra fast RCP recovery
- Adjustable current limit from 400 mA to 3.3 A
- Clamped current output in overcurrent condition
- 29 V high voltage tolerance on VBUS pin
- Low ON resistance of the power FETs: 35 mΩ (typical) in total
- Surge protection: IEC61000-4-5 exceeds ±80 V on VBUS
- Over temperature protection
- Qualified in accordance with AEC-Q100 Grade 3 compliance
- Safety approvals
  - UL 62368-1, 2nd edition, file no. 20170804-E470128
  - IEC 62368-1, 2nd edition, file no. DK-65509-UL
- ESD protection
  - IEC61000-4-2 contact discharge exceeds 8 kV on VBUS
  - HBM ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 2 kV
  - CDM AEC standard Q100-01 (JESD22-C101E) exceeds 500 V
- Specified from -40 °C to +85 °C ambient temperature

3 Applications

- Automotive USB Type-C port
- Automotive power switch

4 Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
NX5P3363UK/Q100	X5PT7	WLCSP16	wafer level chip-scale package; 16 bumps; 2.2 x 2.2 mm x 0.555 mm (backside coating included)	SOT1394-3

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
NX5P3363UK/Q100	NX5P3363UKZ/Q100	WLCSP16	REEL 7" Q1/T1 *SPECIAL MARK CHIPS DP	3000	T_{amb} = -40 °C to +85 °C

5 Marking

Table 3. Marking

Line	Marking	Description
A	X5PT7	basic type name
B	mmmmmmnn	wafer lot code (mmmmmm) and wafer number (nn)
C	XtDYYWW	manufacturing code: X = foundry location t = assembly location D = RoHS code (dark green) YY = assembly year code WW = assembly week code

6 Functional diagram

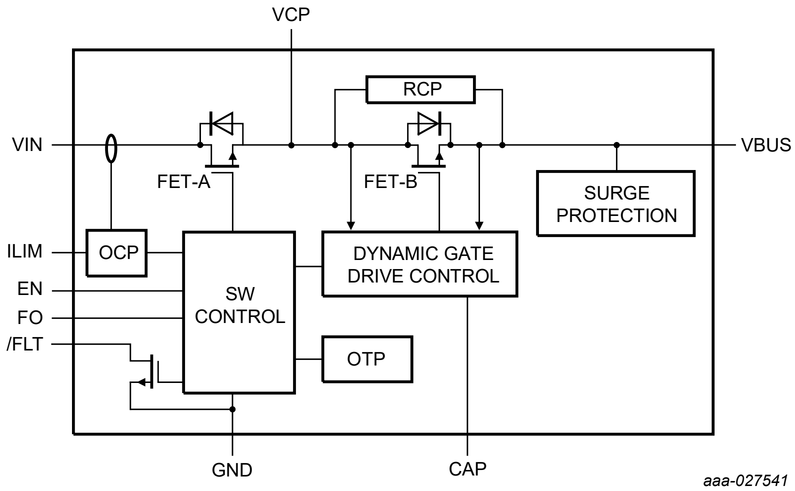


Figure 1. Block diagram

7 Pinning information

7.1 Pinning

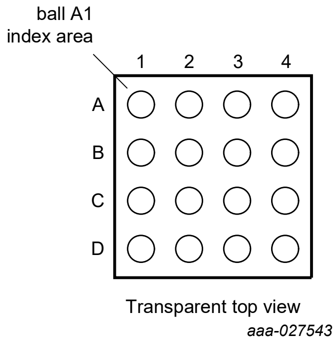


Figure 2. Pin configuration for WLCSP16

	1	2	3	4
A	VIN	VIN	ILIM	/FLT
B	VCP	VCP	GND	EN
C	VCP	VBUS	GND	FO
D	VBUS	VBUS	GND	CAP

Transparent top view

aaa-023807

Figure 3. Ball mapping for WLCSP16

7.2 Pin description

Table 4. Pin description

Symbol	Pin	Description
VIN	A1, A2	Input voltage
VCP	B1, B2, C1	Central point of two power MOSFETs
VBUS	C2, D1, D2	Output voltage
ILIM	A3	Current limiter. Connect a resistor to GND to adjust the current limit level
$\overline{FLT}$	A4	Fault condition indicator (open-drain output)
EN	B4	Enable input (active HIGH with internal 1 MΩ pull down resister)
GND	B3, C3, D3	Ground (0 V)
FO	C4	Fast turn on. Pull this pin HIGH to enable fast turn-on feature. 1 MΩ pull down resister integrated.
CAP	D4	Connect a capacitor to GND

8 Functional description

Table 5. Function table

H = HIGH voltage level; L = LOW voltage level

EN	FO	VIN	$\overline{FLT}$	Main Power Switch
X	X	< 4.0 V	Z	under voltage lockout, Switch open
L	X	4.0 V to 5.5 V	Z	disabled; switch open
H	L	4.0 V to 5.5 V	Z	enabled; switch turns on with slew rate control
H	H	4.0 V to 5.5 V	Z	enabled; switch turns on without slew rate control; fast turn on
H	X	4.0 V to 5.5 V	L	In current limit condition or over temperature protection
X	X	4.0 V to 5.5 V and VIN <= VBUS	Z	Reverse protection; switch open

8.1 EN input

When the EN is set LOW, all the FETs are disabled, and the device enters low-power mode disabling all protection circuits and setting the $\overline{FLT}$ output high impedance. When EN is set HIGH, all protection circuits are enabled and then, if no fault condition exists, the main power MOSFETs turn on.

8.2 Fast recovery RCP

NX5P3363/Q100 uses dynamic gate drive control loop to implement reverse-current protection. During normal operation, device always tries to regulate the VBUS output voltage to be VIN - 70 mV.

When the load current produces a drop voltage greater than 70 mV, the gate control loop drives the power MOS to lower its R_{DSon} to try to achieve the 70 mV. In the heavy load condition, the gate control loop keeps increasing the gate driving current of the MOSFET until it is fully on and remains fully on if the voltage drop at that time still exceeds 70 mV.

In light load condition, when the drop voltage is below 70 mV, the gate control loop reduces the gate driving current to increase the R_{DSon} to try to achieve the 70 mV drop voltage, which leads to the complete shutdown of the power MOSFET in reverse voltage condition.

If VBUS voltage is higher than VIN when enabling the device, the power MOSFET never turns on. The device always does a pre-check before switching on the power MOSFETs.

In the RCP state, EN is HIGH; when the VBUS drops below VIN, the device exits the RCP state and turns on the power FET again within 50 µS. The fast recovery of the power MOSFET is assisted by the external boost capacitor at CAP pin. The boost capacitor is charged whenever EN is pulled HIGH.

The input voltage level of FO pin has nothing to do with RCP recovery time.

8.3 VBUS hot plug-in RCP

The RCP circuit, together with dynamic gate drive control circuit, acts like an "ideal diode". This protects the VIN lifting from reverse current when VBUS has a hot plug-in during the following conditions and limits the VIN voltage lift < 400 mV. Refer to NX5P3363/Q100 ground pin.

- VBUS < 24 V, plug-in when NX5P3363/Q100 is on
- C_{IN} is in the range of 57 µF to 100 µF
- C_{BUS} is in the range of 10 µF to 22 µF

If the VBUS, C_{IN}, C_{BUS} are not in the range or conditions, there may be more reverse current and the VIN voltage lift depends on the conditions.

8.4 Fast Turn ON

In order to reduce the power on inrush current, NX5P3363/Q100 deploys slew rate control for normal turn on; there is approximately 2 ms rising time. However, in the fast role swap application, fast turn on is requested. The customer achieves this by pulling FO pin HIGH. By doing this, rise time is reduced to the 100 μS level. There is an internal 1 MΩ pull-down resister on this pin. The fast turn on is achieved by turn off short circuit protection and OCP feature in the fast start stage; typically 220 μs. It is recommended to add a 10 μF capacitor close to VIN pin to limit the inrush current in fast turn on mode.

The feature only applies to fast role swap, and FO pin should be controlled by USB PD PHY. When a fast role swap event is detected by USB PD PHY, the FO pin should pull HIGH first, then enable the EN pin of NX5P3363/Q100 when the FRS is requested. Depending on the voltage on VBUS, there are two scenarios:

1. V(VBUS) > V(VIN): The switch enters RCP mode. Once the voltage on VBUS drops below VIN voltage, switch immediately turns on within 50 μS.
2. V(VBUS) ≤ V(VIN)
   The switch performs a fast turn ON as the FO is HIGH; the turn on time is 150 μS.

When fast role swap is finished and NX5P3363/Q100 is in all the other conditions, FO pin should remain LOW to limit the inrush current.

8.5 Undervoltage lockout

Independently of the logic level on the EN pin, the undervoltage lockout (UVLO) circuit disables the N-channel MOSFET and enters low power mode until the input voltage reaches the UVLO turn-on threshold VUVLO.

8.6 ILIM

The overcurrent protection circuit's (OCP) trigger value I_{OCP} can be set using an external resistor R_{ILIM} connected between ILIM pin and GND pin. When EN is set HIGH and the ILIM pin is grounded, the N-channel MOSFET is disabled. The I_{OCP} setting is given in Table 12.

8.7 Main power FET overcurrent protection (OCP)

The device offers overcurrent protection when enabled. The three possible overcurrent conditions that can occur are:

1. Overcurrent at startup: $I_{SW} > I_{OCP}$ when enabling the N-channel MOSFET.
2. Overcurrent when enabled: $I_{SW} > I_{OCP}$ when the N-channel MOSFET is enabled.
3. Short circuit when enabled: I_{SW} exceeds short circuit conditions

In the overcurrent condition, because the device clamps the output current rather than the switch, the power dissipation on the device might be increased which could lead to overtemperature protection (see Section 8.9).

8.7.1 Overcurrent at startup

If the device senses a VBUS short to GND or overcurrent while enabling the N-channel MOSFET, OCP is triggered. It limits the output current to I_{OCP} and after the deglitch time sets the $\overline{FLT}$ output LOW.

8.7.2 Overcurrent when enabled

If the device senses I_{SW} exceeds I_{OCP} when enabled, OCP is triggered. It limits the output current to I_{OCP} and after the deglitch time sets the $\overline{FLT}$ output LOW. As a consequence, limiting the output current reduces $V_{O(VBUS)}$.

8.7.3 Short circuit when enabled

If the current through switch exceeds 7.5 A (typical), the short circuit protection is triggered. That disables the N-channel MOSFET immediately. It then enables the N-channel MOSFET again; output current is limited to I_{OCP} and after the deglitch time the $\overline{FLT}$ output is set LOW. Thermal protection is triggered due to the big power consumption on the device.

In the customer specific application case, the short circuit protection ensures the VIN voltage stays above 4.5 V at the following short circuit testing.

- C_{IN} = 57 μF, VBUS short to GND directly by a metal tweezer; this means the short resistor to ground is typically 40 mΩ
- VIN connected to customer specified DC-DC

8.8 $\overline{FLT}$ output

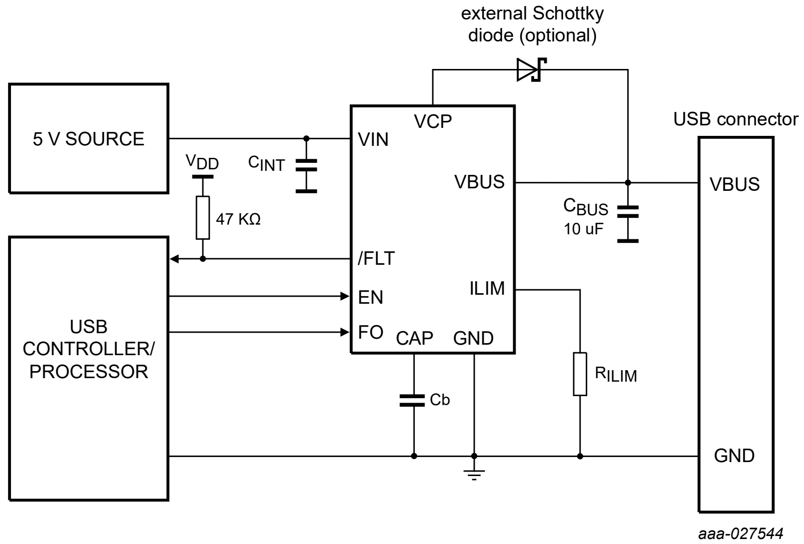
The $\overline{FLT}$ output is an open-drain output that requires an external pull-up resistor. The $\overline{FLT}$ output is set LOW to indicate an OCP or OTP condition has occurred. The $\overline{FLT}$ output returns to the high impedance state automatically once the fault condition is removed. An internal 8 ms deglitch circuit for the overcurrent protection is used when entering fault conditions. Overtemperature condition doesn't have deglitch time, and the $\overline{FLT}$ signal is asserted immediately. The RCP circuit won't trigger $\overline{FLT}$ signal.

8.9 Overtemperature protection

If the device temperature exceeds 140 °C when EN is set HIGH, the overtemperature protection (OTP) circuit disables the Power MOSFET and indicates a fault condition by setting the $\overline{FLT}$ pin LOW. Any transition on the EN pin has no effect. Once the device temperature decreases to below 115 °C the device returns to the defined state.

In the overcurrent limiting condition, the increased power dissipation on the device results in OTP, especially in the output-short-to-GND error.

9 Application diagram



A 0.1 µF ceramic capacitor (C_{INT}) is required for local decoupling. Higher capacitor values C_{INT} further reduce the voltage drop at the input. When driving inductive loads, a larger capacitance C_{INT} prevents voltage spikes from exceeding absolute maximum voltage of VIN. The CBUS capacitor should be placed as closer as possible to VBUS pin.

The recommended Cb is 1 nF with at least 16 V voltage tolerance.

The external Schottky diode is optional; NX5P3363/Q100 works well without it. To improve the lowest VBUS voltage during fast role swap, it is recommended to add a lower forward voltage diode, for example VF = 0.3 V.

Figure 4. Application diagram

10 Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_I	input voltage	VBUS	[1]	-0.5	+29	V
		VIN; VCP; ILIM; EN; FO	[1]	-0.5	+6	V
		CAP	[1]	-0.5	+12	V
	peak voltage tolerance	VBUS; 20 µs pulse width, 1 s interval	[1]	-0.5	+34	V
V_O	output voltage	$\overline{FLT}$	[1]	-0.5	+6	V
I_{IK}	input clamping current	input EN: $V_{I(EN)} < -0.5$ V		-50	-	mA
$I_{I(source)}$	input source current	input ILIM		-	1	mA
I_{SK}	switch clamping current	input VIN: $V_{I(VIN)} < -0.5$ V		-50	-	mA
		output VOUT: $V_{O(VBUS)} < -0.5$ V		-50	-	mA
I_{SW}	Main Power switch continuous current	$V_{SW} > -0.5$ V	[2]	-	3.6	A
$T_{j(max)}$	maximum junction temperature			-40	+125	°C
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation		[3]	-	1.7	W

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.
[2] Internally limited.
[3] The (absolute) maximum power dissipation depends on the junction temperature T_j. Higher power dissipation is allowed in conjunction with lower ambient temperatures. The conditions to determine the specified values are T_{amb} = 25 °C and the use of a two layer PCB.

11 Recommended operating conditions

Table 7. Recommended operating conditions

Symbol	Parameter	Conditions		Min	Max	Unit
V_I	input voltage	VIN		4.0	5.5	V
		EN; FO		0	5.5	V
		VBUS (OFF state)		0	23	V
V_O	Output voltage	VBUS; $\overline{FLT}$		0	5	V
I_{SW}	switch current	T_{amb} = -40 °C to +85 °C		0	3	A
$I_{O(sink)}$	output sink current	$\overline{FLT}$		0	10	mA
R_{ILIM}	current limit resistance	ILIM pin to GND		14.3	140	kΩ
C_{Bus}	VBUS output capacitance	VBUS to GND		10	100	µF
T_{amb}	ambient temperature			-40	+85	°C

12 Thermal characteristics

Table 8. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	58.4	K/W

[1] $R_{th(j-a)}$ is dependent upon board layout. To minimize $R_{th(j-a)}$, ensure all pins have a solid connection to larger copper layer areas. In multi-layer PCBs, the second layer should be used to create a large heat spreader area below the device. Avoid using solder-stop varnish under the device.

13 Static characteristics

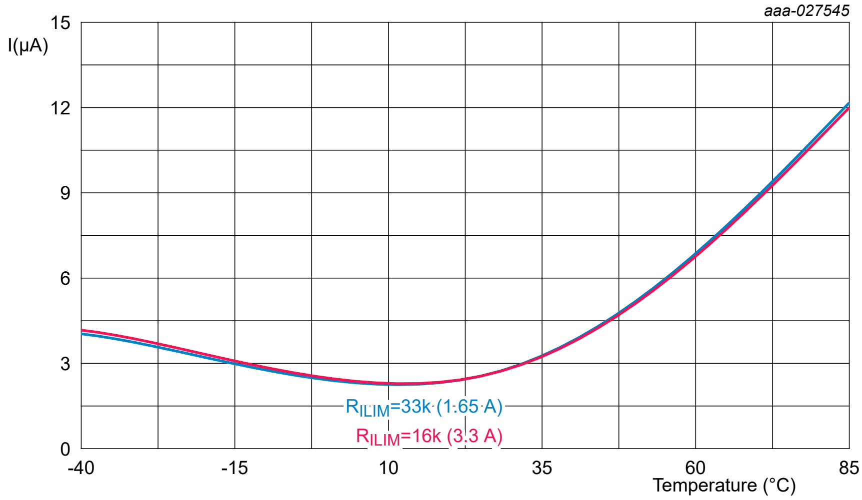
Table 9. Static characteristics

At recommended operating conditions; $V_{I(VIN)}$ = $V_{I(EN)}$, R_{FAULT} = 10 kΩ unless otherwise specified; Voltages are referenced to GND (ground = 0 V). See Figure 9

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{IH}	HIGH-level input voltage	EN; FO; $V_{I(VIN)}$ = 4.0 V to 5.5 V;		1.2	-	-	V
V_{IL}	LOW-level input voltage	EN; FO; $V_{I(VIN)}$ = 4.0 V to 5.5 V;		-	-	0.4	V
I_I	input leakage current	EN; FO; $V_{I(VIN)}$ = 5.0 V;		-	-	7	μA
$I_{(VIN)}$	supply current	VBUS open; $V_{I(VIN)}$ = 5.0 V					
		EN = GND (low power mode);		-	3	55	μA
		EN = $V_{I(VIN)}$; R_{ILIM} = 33 kΩ		-	1.3	1.7	mA
		EN = $V_{I(VIN)}$; R_{ILIM} = 16 kΩ		-	1.35	1.7	mA
$I_{S(OFF)}$	VBUS OFF-State leakage current	$V_{I(VIN)}$ = 5.0 V; $V_{I(VBUS)}$ = 0 V; EN = LOW	[2]	-5	-0.1	-	μA
	VIN OFF-state leakage current	$V_{I(VBUS)}$ = 5.0 V; $V_{I(VIN)}$ = 0 V; EN = LOW	[2]	-2	-0.1	-	μA
		$V_{I(VBUS)}$ = 20 V; $V_{I(VIN)}$ = 0 V; EN = LOW	[2]	-2	-0.1	-	μA
$I_{S(ON)}$	FET-B leakage current in RCP	$V_{I(VIN)}$ = 5 V; $V_{I(VBUS)}$ = 20 V; EN = 5 V	[2] [3]	-2	-0.1	-	μA
R_{pd}	Pull-down resistance	EN; FO; $V_{I(VIN)}$ = 5 V		-	1	-	MΩ
V_{UVLO}	under voltage lockout voltage	VIN pin		-	3.6	3.8	V
$V_{hys(UVLO)}$	under voltage lockout hysteresis voltage			-	100	-	mV
V_{OL}	LOW-level output voltage	$\overline{FLT}$; I_O = 4 mA		-	-	0.3	V
$C_{I(EN)}$	EN pin			-	3	-	pF
$C_{I(FO)}$	FO pin			-	4	-	pF

[1] Typical values are measured at T_j = 25 °C.
[2] Currents are defined with respect to conventional current flow into the respective terminal. Negative value means the current flows out of the respective terminal of the chip.
[3] Guaranteed by design

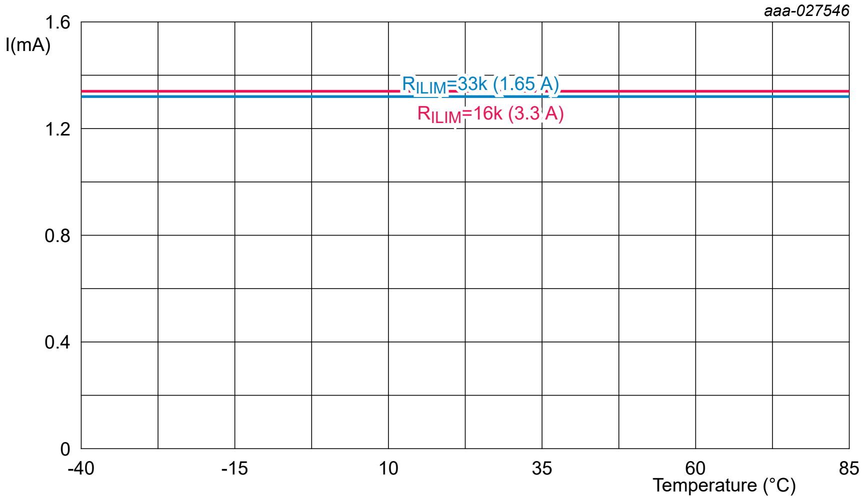
13.1 Graphs



$V_{I(EN)}$ = GND; $V_{I(VIN)}$ = 5.0 V

X = T_{amb}, Y = $I_{(VIN)}$

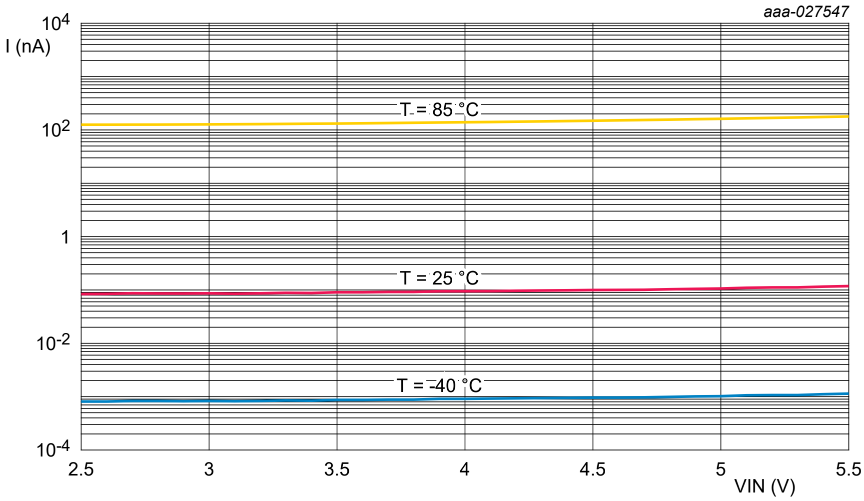
Figure 5. OFF state supply current versus temperature



$V_{I(EN)}$ = $V_{I(VIN)}$; $V_{I(VIN)}$ = 5.0 V

X = T_{amb}, Y = $I_{(VIN)}$

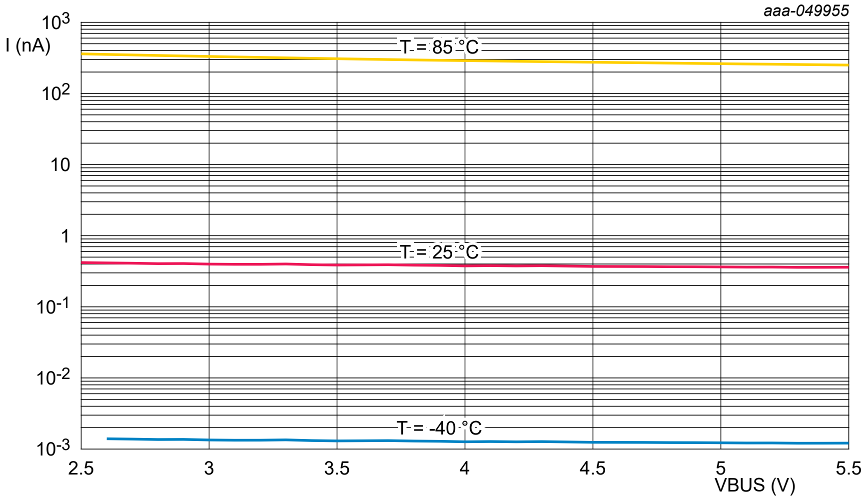
Figure 6. ON state supply current versus temperature



$V_{I(EN)}$ = GND; $V_{I(VBUS)}$ = 0 V; R_{ILIM} = 14.3 k (3.3 A)

X = $V_{I(VIN)}$ from 2.5 V to 5.5 V; Y = $-I_{(VBUS)}$

Figure 7. VBUS off state leakage versus temperature



$V_{I(EN)}$ = GND; $V_{I(VIN)}$ = 0 V; R_{ILIM} = 14.3 k (3.3 A)

X = $V_{I(VBUS)}$ from 2.5 V to 5.5 V; Y = $-I_{(VIN)}$

Figure 8. VIN off state leakage versus temperature

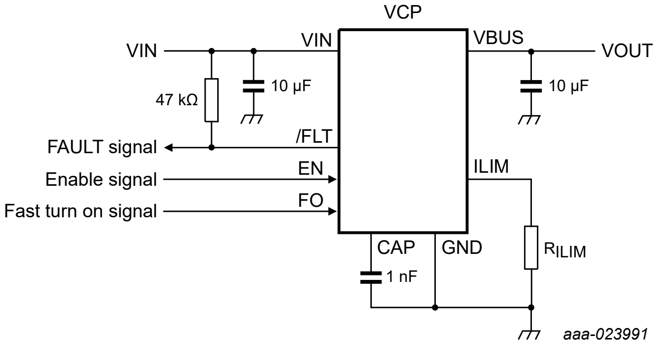


Figure 9. Typical characteristics reference schematic

13.2 Thermal shutdown

Table 10. Thermal shutdown

$V_{I(VIN)}$ = $V_{I(EN)}$, R_{FAULT} = 10 kΩ unless otherwise specified; Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{th(ots)}$	over temperature shutdown threshold temperature	$V_{I(VIN)}$ = 4.0 V to 5.5 V	-	140	-	°C
$T_{th(otp)hys}$	hysteresis of over temperature protection threshold temperature	$V_{I(VIN)}$ = 4.0 V to 5.5 V	-	25	-	°C

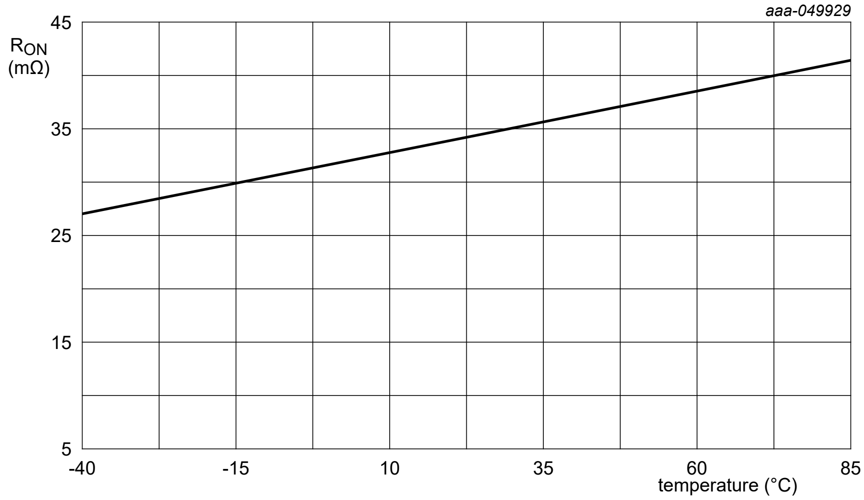
13.3 ON resistance

Table 11. ON resistance

$V_{I(VIN)}$ = $V_{I(EN)}$, R_{FAULT} = 10 kΩ unless otherwise specified; Voltages are referenced to GND (ground = 0 V). See Figure 9

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{ON}	ON resistance	R_{FETA} + R_{FETB}; $V_{I(VIN)}$ = 4.0 to 5.5 V; see Figure 10				
		T_{amb} = 25 °C	-	35	42	mΩ
		T_{amb} = -40 °C to +85 °C	-	-	49	mΩ

13.4 ON resistance graphs



X = T_{amb}, Y = Ron; $V_{I(VIN)}$ = 5.0 V

Figure 10. Typical ON resistance versus temperature

13.5 Current limit

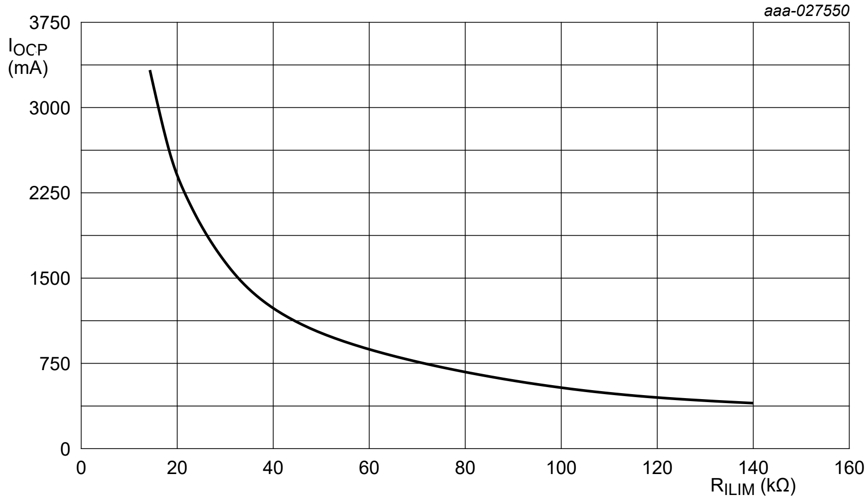
Table 12. Current limit

$V_{I(VIN)}$ = $V_{I(EN)}$, R_{FAULT} = 10 kΩ unless otherwise specified; Voltages are referenced to GND (ground = 0 V). See Figure 9

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
I_{OCP}	overcurrent protection current	$V_{I(VIN)}$ = 4.0 to 5.5 V; T_{amb} = -40 °C to +85 °C; see Figure 11,				
		R_{ILIM} = 140 kΩ	330	400	465	mA
		R_{ILIM} = 97.6kΩ	480	550	625	mA
		R_{ILIM} = 51 kΩ	915	1000	1107	mA
		R_{ILIM} = 30 kΩ	1505	1640	1780	mA
		R_{ILIM} = 22.1 kΩ	2024	2200	2398	mA
		R_{ILIM} = 18.2kΩ	2450	2640	2820	mA
		R_{ILIM} = 14.3 kΩ	3100	3300	3531	mA
		ILIM shorted to VIN	168	210	273	mA

[1] 1% tolerance resistor is recommend for R_{ILIM}

13.6 Current limit graphs



$V_{I(VIN)}$ = 5.0 V; X = R_{ILIM}, I_{OCP}= $39156R_{ILIM}^{-0.93}$

Figure 11. Typical overcurrent protection current versus external resistor value R_{ILIM}

14 Dynamic characteristics

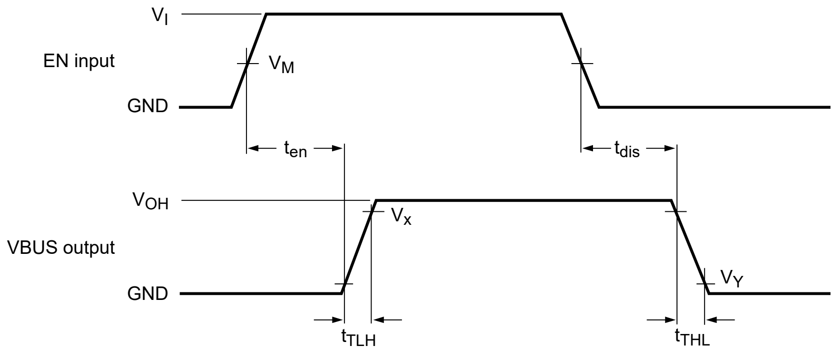
Table 13. Dynamic characteristics

At recommended operating conditions; $V_{I(VIN)} = V_{I(EN)}$*,* R_{FAULT} *= 10 kΩ unless otherwise specified; voltages are referenced to GND (ground = 0 V).*

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
t_{TLH}	LOW to HIGH output transition time	VBUS; $V_{I(VIN)}$ = 5.0 V; C_L = 10 µF; R_L = 100 Ω; see Figure 12 and Figure 13					
		$V_{I(FO)}$ = GND		-	1.5	-	ms
		$V_{I(FO)}$ = 5.0 V		-	50	100	µs
t_{THL}	HIGH to LOW output transition time	VOUT; C_L = 10 µF; R_L = 100 Ω; see Figure 12 and Figure 13					
		$V_{I(VIN)}$ = 5.0 V		-	2.2	-	ms
t_{en}	enable time	EN to VOUT; C_L = 10 µF; R_L = 100 Ω; seeFigure 14 and Figure 15					
		$V_{I(VIN)}$ = 5.0 V; $V_{I(FO)}$ = GND		-	0.75	-	ms
		$V_{I(VIN)}$ = 5.0 V; $V_{I(FO)}$ = 5.0 V		-	60	-	µs
t_{dis}	disable time	EN to VOUT; $V_{I(VIN)}$ = 5.0 V; C_L = 10 µF; R_L = 100Ω; see Figure 16 and Figure 17		-	90	-	µs
$t_{on(RCP)}$	RCP recovery time	$V_{I(VIN)}$ = 5.0 V; EN = HIGH; From VBUS drops below VIN to FET-B ON; C_L = 10 µF		-	15	50	µs
$t_{dis(RCP)}$	RCP turn off time	FET-B RCP turn OFF time	[2]	-	0.3	-	µs
t_{degl}	deglitch time	$\overline{FLT}$ in OCP; $V_{I(VIN)}$ = 5 V; see Figure 20 to Figure 21		-	8	-	ms
$t_{short(OCP)}$	OCP short circuit protection response time	$V_{I(VIN)}$ = 5.0 V; C_{BUS}=10 µF; Measure current at VBUS side		-	5	-	µs

[1] Typical values are measured at T_j = 25 °C.
[2] Guaranteed by design

14.1 Waveform and test circuits



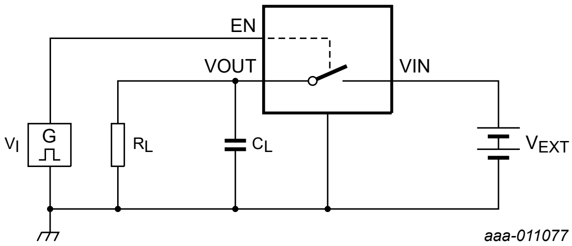
Measurement points are given in Table 14.

Logic level: V_{OH} is the typical output voltage that occurs with the output load.

Figure 12. Switching times and rise and fall times

Table 14. Measurement points

Supply voltage	EN Input	Output	
$V_{I(VIN)}$	V_M	V_X	V_Y
5.0 V	0.5 × $V_{I(EN)}$	0.9 × V_{OH}	0.1 × V_{OH}



Test data is given in Table 15.

Definitions test circuit:

R_L = Load resistance.

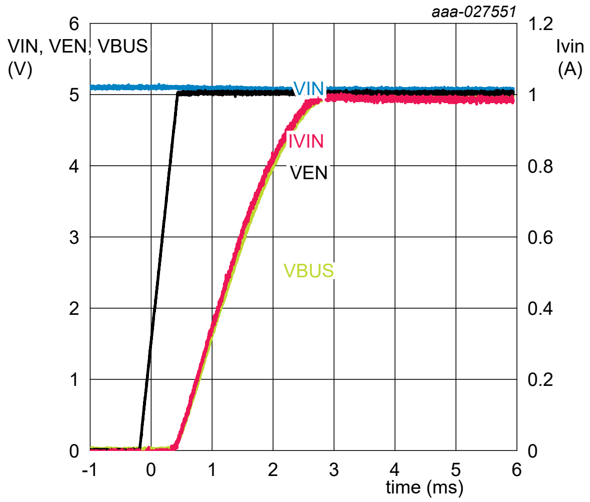
C_L = Load capacitance including jig and probe capacitance.

V_{EXT} = External voltage for measuring switching times.

Figure 13. Test circuit for measuring switching times

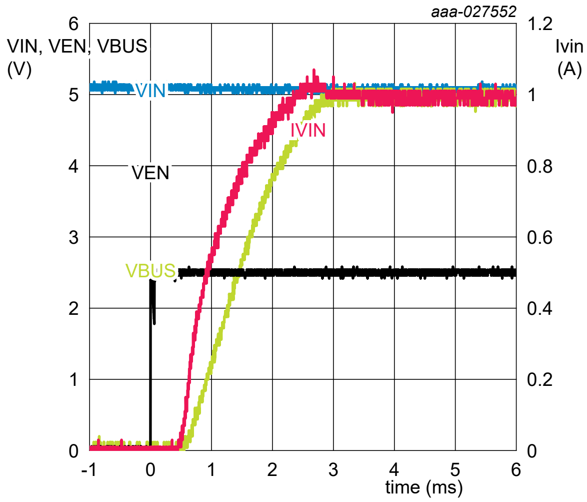
Table 15. Test data

Supply voltage	EN Input	Load	
V_{EXT}	$V_{I(EN)}$	C_L	R_L
5.0 V	0 to $V_{I(VIN)}$	10 µF	100 Ω



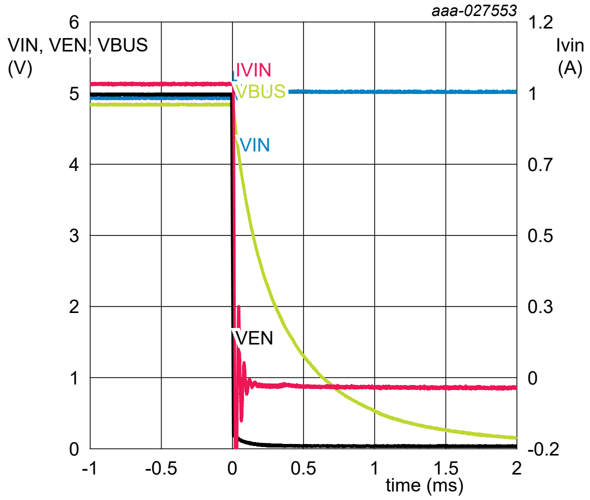
$V_{I(VIN)}$ = 5 V; R_L = 5 Ω; C_L = 10 µF; R_{ILIM} = 33 kΩ (1.5 A)

Figure 14. Typical 10 µF enable time versus inrush current



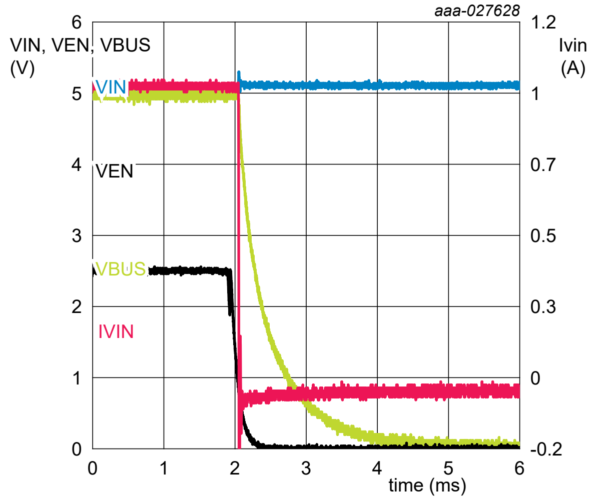
$V_{I(VIN)}$ = 5 V; R_L = 5 Ω; C_L = 100 µF; R_{ILIM} = 33 kΩ (1.5 A)

Figure 15. Typical 100 µF enable time versus inrush current



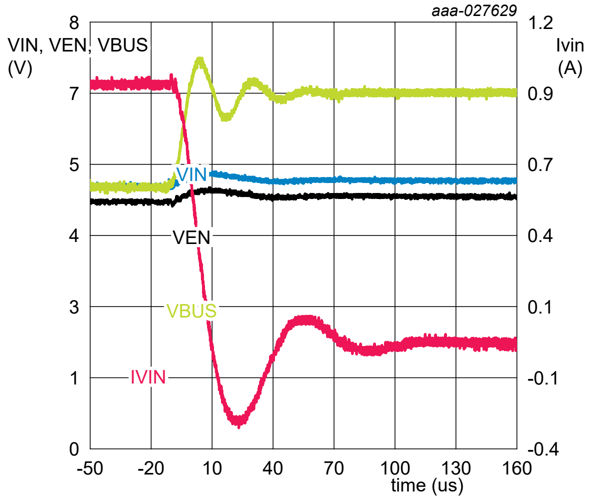
$V_{I(VIN)}$ = 5 V; R_L = 5 Ω; C_L = 10 µF; R_{ILIM} = 33 kΩ (1.5 A)

Figure 16. Typical 10 µF disable time



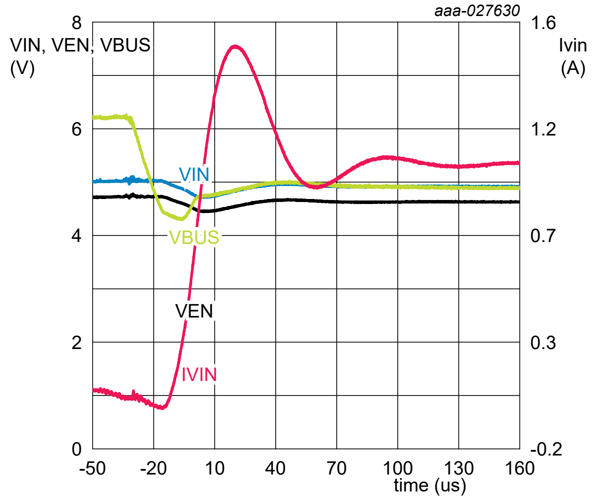
$V_{I(VIN)}$ = 5 V; R_L = 5 Ω; C_L = 100 µF; R_{ILIM} = 33 kΩ (1.5 A)

Figure 17. Typical 100 µF disable time



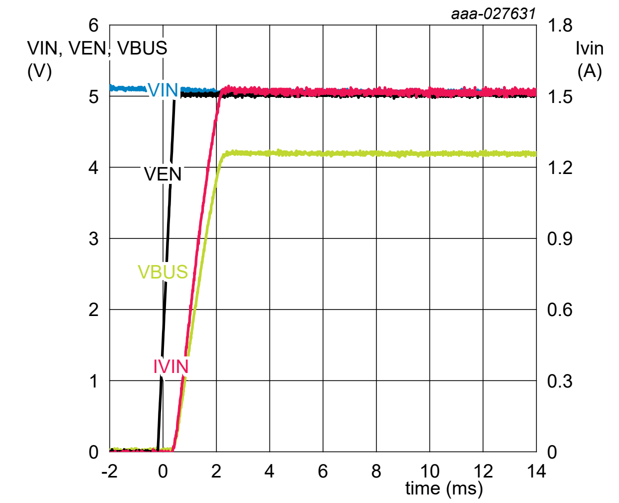
$V_{I(VIN)}$ = 5 V; R_{ILIM} = 33 kΩ

Figure 18. Reverse-current protection response



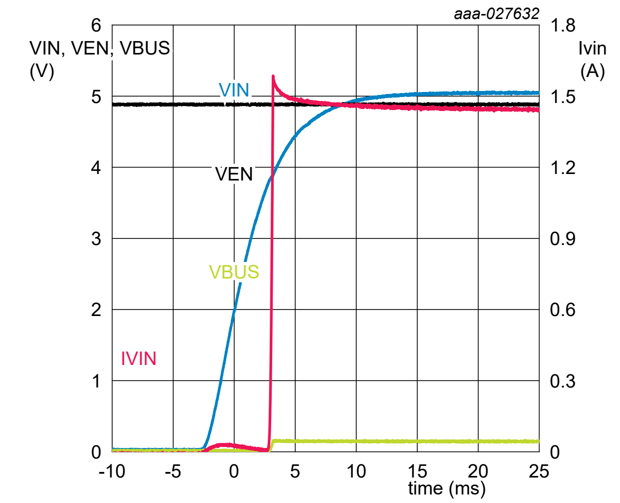
$V_{I(VIN)}$ = 5 V; R_{ILIM} = 33 kΩ

Figure 19. Reverse-current protection recovery



$V_{I(VIN)}$ = 5 V; R_{ILIM} = 33 kΩ (1.5 A)

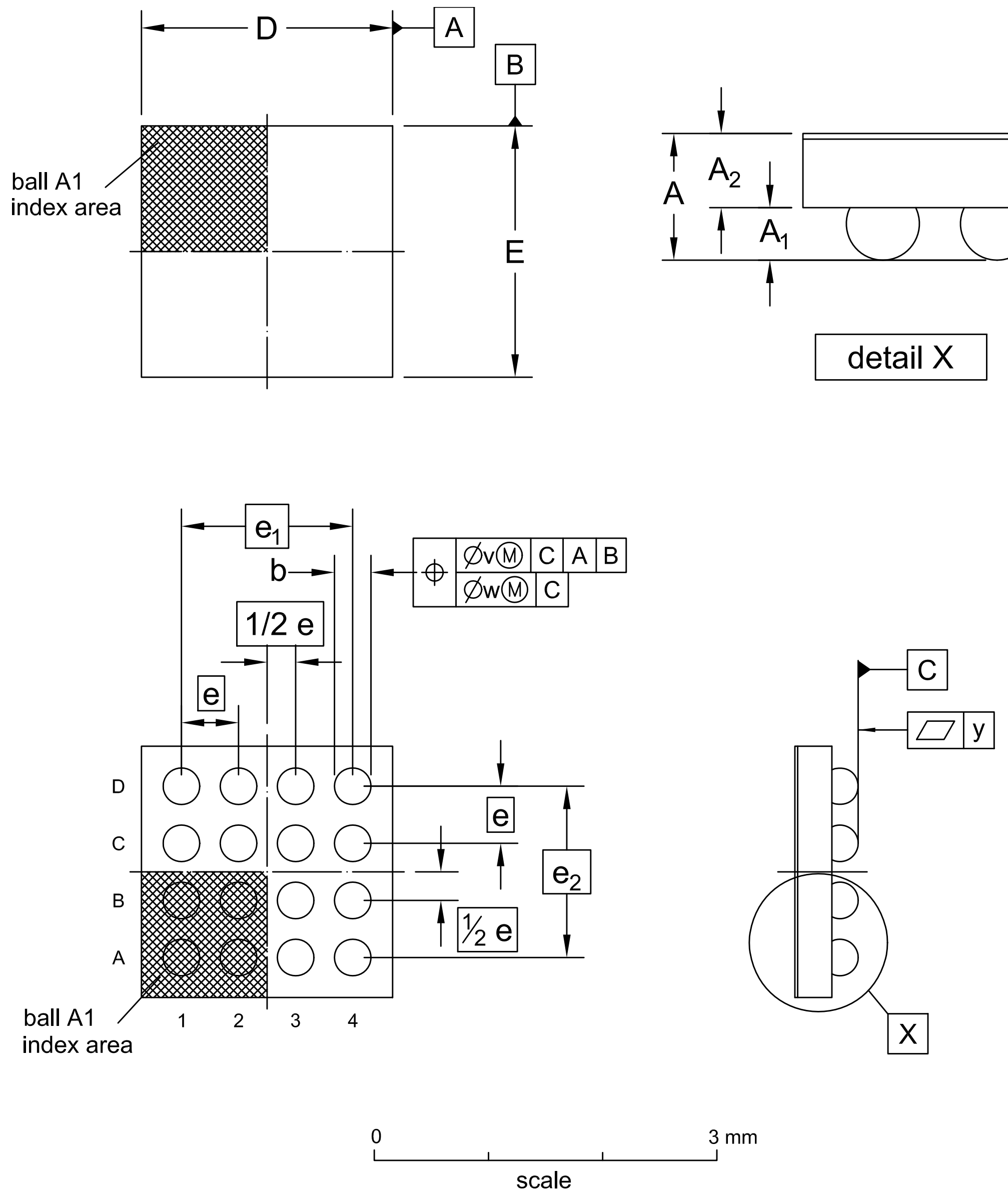
Figure 20. Device enabled into current limit mode



$V_{I(VIN)}$ = 5 V; R_{ILIM} = 33 kΩ (1.5 A)

Figure 21. Device start up in VBUS short to GND

15 Package outline



DIMENSIONS (mm are the original dimensions)

UNIT		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y
mm	MAX.	0.595	0.26	0.350	0.35	2.23	2.23	0.5	1.5	1.5	0.05	0.015	0.03
	NOM.	0.555	0.23	0.325	0.32	2.20	2.20						
	MIN.	0.515	0.20	0.300	0.29	2.17	2.17						

NOTE: Backside coating 25 um

Figure 22. Package outline SOT1394-3 (WLCSP16)

16 Abbreviations

Table 16. Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge
CDM	Charged Device Model
HBM	Human Body Model
USB	Universal Serial Bus

17 Revision history

Table 17. Revision history

Document ID	Release date	Description
NX5P3363_Q100 v.1.1	10 September 2024	• Changed Section 3
NX5P3363_Q100 v.1.0	31 May 2024	• Initial version

Legal information

Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL https://www.nxp.com.

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