

RF LDMOS Wideband Integrated Power Amplifiers

The MD8IC970N wideband integrated circuit is designed with on-chip prematching that makes it usable from 136 to 940 MHz. This multi-stage structure is rated for 26 to 32 Volt operation and covers all typical base station modulation formats. This device has a 2-stage design with off-chip matching for the input, interstage and output networks to cover the desired frequency sub-band.

- Typical Two-Tone Performance: $V_{DD1} = 28$ Volts, $V_{DD2} = 25$ Volts, $I_{DQ1(A+B)} = 60$ mA, $I_{DQ2(A+B)} = 550$ mA, $P_{out} = 35$ Watts Avg.

| Frequency | G _{ps} (dB) | PAE (%) | IMD (dBc) |
|-----------|----------------------|---------|-----------|
| 850 MHz | 30.6 | 40.1 | -30.5 |
| 900 MHz | 31.9 | 42.4 | -31.0 |
| 940 MHz | 32.6 | 42.1 | -31.3 |

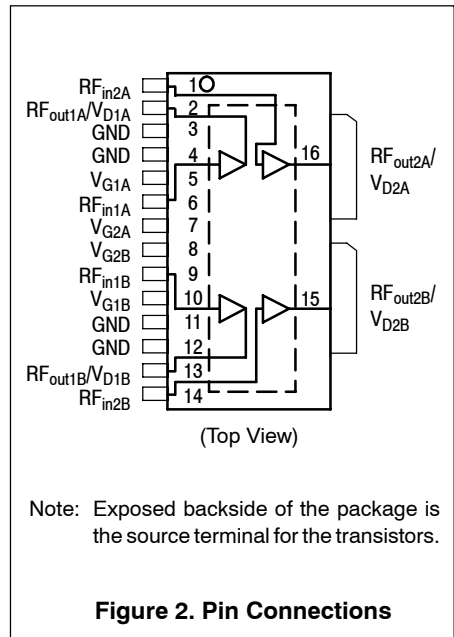
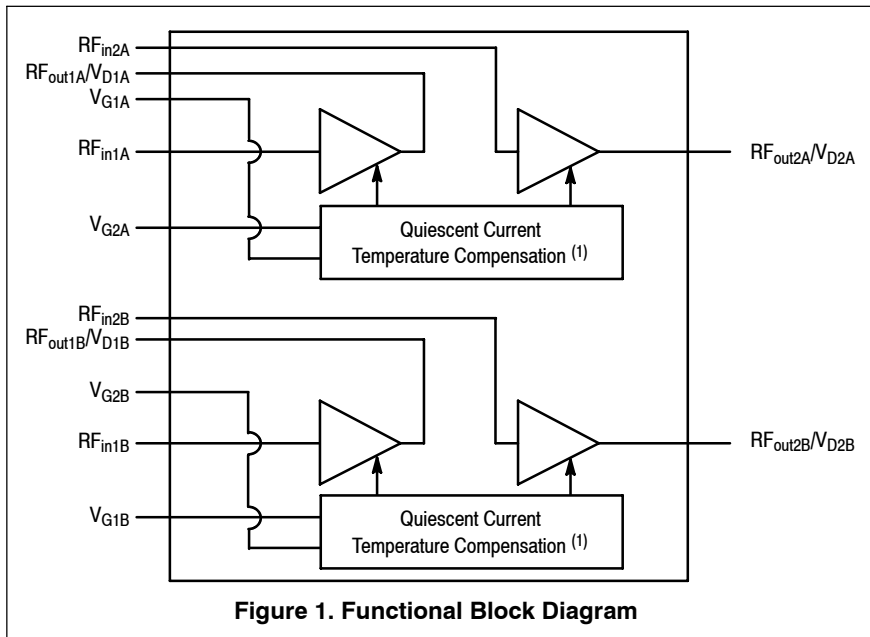
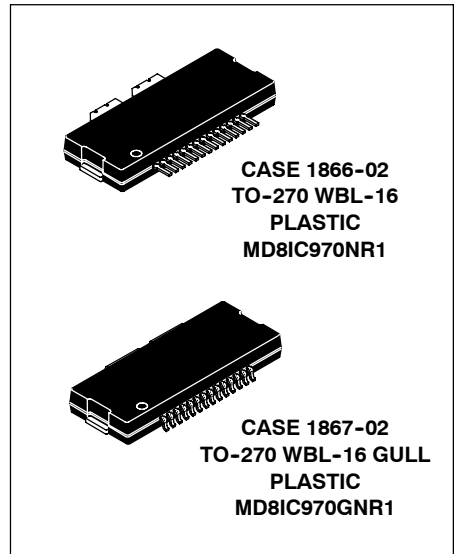
- Capable of Handling 10:1 VSWR, @ 32 Vdc, 940 MHz, 137 Watts CW Output Power (3 dB Input Overdrive from Rated P_{out}), Designed for Enhanced Ruggedness
- Typical P_{out} @ 1 dB Compression Point \approx 79 Watts CW

Features

- Characterized with Series Equivalent Large-Signal Impedance Parameters and Common Source S-Parameters
- On-Chip Prematching. On-Chip Stabilization.
- Integrated Quiescent Current Temperature Compensation with Enable/Disable Function (1)
- Integrated ESD Protection
- 225°C Capable Plastic Package
- RoHS Compliant
- In Tape and Reel. R1 Suffix = 500 Units, 44 mm Tape Width, 13 inch Reel.

MD8IC970NR1
MD8IC970GNR1

850-940 MHz, 35 W AVG., 28 V
RF LDMOS WIDEBAND
INTEGRATED POWER AMPLIFIERS



Note: Exposed backside of the package is the source terminal for the transistors.

1. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family* and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1977 or AN1987.

Table 1. Maximum Ratings

| Rating | Symbol | Value | Unit |
|--------------------------------------|-----------|-------------|------|
| Drain-Source Voltage | V_{DSS} | -0.5, +70 | Vdc |
| Gate-Source Voltage | V_{GS} | -0.5, +10 | Vdc |
| Operating Voltage | V_{DD} | 32, +0 | Vdc |
| Storage Temperature Range | T_{stg} | -65 to +150 | °C |
| Case Operating Temperature | T_C | 150 | °C |
| Operating Junction Temperature (1,2) | T_J | 225 | °C |
| Input Power | P_{in} | 30 | dBm |

Table 2. Thermal Characteristics

| Characteristic | Symbol | Value (2,3) | Unit |
|----------------|--------|-------------|------|
|----------------|--------|-------------|------|

Final Application

| | | | |
|--|-----------------|------------|------|
| Thermal Resistance, Junction to Case Case Temperature 80°C, 35 W Avg. Two-Tone Stage 1, 28 Vdc, $I_{DQ1(A+B)} = 60$ mA, $f_1 = 939.9$ MHz, $f_2 = 940.1$ MHz Stage 2, 25 Vdc, $I_{DQ2(A+B)} = 550$ mA, $f_1 = 939.9$ MHz, $f_2 = 940.1$ MHz | $R_{\theta JC}$ | 2.9 0.6 | °C/W |
|--|-----------------|------------|------|

Table 3. ESD Protection Characteristics

| Test Methodology | Class |
|---------------------------------------|--------------|
| Human Body Model (per JESD22-A114) | 1A (Minimum) |
| Machine Model (per EIA/JESD22-A115) | A (Minimum) |
| Charge Device Model (per JESD22-C101) | I (Minimum) |

Table 4. Moisture Sensitivity Level

| Test Methodology | Rating | Package Peak Temperature | Unit |
|--------------------------------------|--------|--------------------------|------|
| Per JESD22-A113, IPC/JEDEC J-STD-020 | 3 | 260 | °C |

Table 5. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|----------------|--------|-----|-----|-----|------|
|----------------|--------|-----|-----|-----|------|

Stage 1 — Off Characteristics (4)

| | | | | | |
|---|-----------|---|---|----|-----------------|
| Zero Gate Voltage Drain Leakage Current ($V_{DS} = 70$ Vdc, $V_{GS} = 0$ Vdc) | I_{DSS} | — | — | 10 | μAdc |
| Zero Gate Voltage Drain Leakage Current ($V_{DS} = 28$ Vdc, $V_{GS} = 0$ Vdc) | I_{DSS} | — | — | 1 | μAdc |
| Gate-Source Leakage Current ($V_{GS} = 1.5$ Vdc, $V_{DS} = 0$ Vdc) | I_{GSS} | — | — | 1 | μAdc |

Stage 1 — On Characteristics (4)

| | | | | | |
|--|--------------|-----|------|------|-----|
| Gate Threshold Voltage ($V_{DS} = 10$ Vdc, $I_D = 40$ μAdc) | $V_{GS(th)}$ | 1.2 | 2.0 | 2.7 | Vdc |
| Gate Quiescent Voltage ($V_{DS} = 28$ Vdc, $I_{DQ1(A+B)} = 60$ mAdc) | $V_{GS(Q)}$ | — | 3.1 | — | Vdc |
| Fixture Gate Quiescent Voltage ($V_{DD1} = 28$ Vdc, $I_{DQ1(A+B)} = 60$ mAdc, Measured in Functional Test) | $V_{GG(Q)}$ | 9.0 | 10.0 | 11.0 | Vdc |

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.
4. Side A and Side B are tied together for this measurement.

(continued)

Table 5. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted) (continued)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|-----------|-----|-----|-----|-----------------|
| Stage 2 — Off Characteristics (1) | | | | | |
| Zero Gate Voltage Drain Leakage Current ($V_{DS} = 70\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$) | I_{DSS} | — | — | 10 | μAdc |
| Zero Gate Voltage Drain Leakage Current ($V_{DS} = 28\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$) | I_{DSS} | — | — | 1 | μAdc |
| Gate-Source Leakage Current ($V_{GS} = 1.5\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$) | I_{GSS} | — | — | 1 | μAdc |

Stage 2 — On Characteristics (1)

| | | | | | |
|---|--------------|-----|------|-----|-----|
| Gate Threshold Voltage ($V_{DS} = 10\text{ Vdc}$, $I_D = 320\ \mu\text{Adc}$) | $V_{GS(th)}$ | 1.2 | 2.0 | 2.7 | Vdc |
| Gate Quiescent Voltage ($V_{DS} = 25\text{ Vdc}$, $I_{DQ2(A+B)} = 550\text{ mAdc}$) | $V_{GS(Q)}$ | — | 3.1 | — | Vdc |
| Fixture Gate Quiescent Voltage ($V_{DD2} = 25\text{ Vdc}$, $I_{DQ2(A+B)} = 550\text{ mAdc}$, Measured in Functional Test) | $V_{GG(Q)}$ | 7.6 | 8.6 | 9.6 | Vdc |
| Drain-Source On-Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 3.2\text{ Adc}$) | $V_{DS(on)}$ | 0.1 | 0.48 | 1.2 | Vdc |

Functional Tests (1,2) (In Freescale Test Fixture, 50 ohm system) $V_{DD1} = 28\text{ Vdc}$, $V_{DD2} = 25\text{ Vdc}$, $P_{out} = 35\text{ W Avg.}$, $I_{DQ1(A+B)} = 60\text{ mA}$, $I_{DQ2(A+B)} = 550\text{ mA}$, $f_1 = 939.9\text{ MHz}$, $f_2 = 940.1\text{ MHz}$

| | | | | | |
|----------------------------|----------|------|-------|-------|----|
| Power Gain | G_{ps} | 31.5 | 32.6 | 36.5 | dB |
| Power Added Efficiency | PAE | 40.5 | 42.1 | — | % |
| Intermodulation Distortion | IMD | — | -31.3 | -29.0 | dB |

Typical Broadband Performance (1) (In Freescale Test Fixture, 50 ohm system) $V_{DD1} = 28\text{ Vdc}$, $V_{DD2} = 25\text{ Vdc}$, $P_{out} = 35\text{ W Avg.}$, $I_{DQ1(A+B)} = 60\text{ mA}$, $I_{DQ2(A+B)} = 550\text{ mA}$

| Frequency | G_{ps} (dB) | PAE (%) | IMD (dBc) |
|-----------|------------------|------------|--------------|
| 850 MHz | 30.6 | 40.1 | -30.5 |
| 900 MHz | 31.9 | 42.4 | -31.0 |
| 940 MHz | 32.6 | 42.1 | -31.3 |

Typical Performances (1) (In Freescale Test Fixture, 50 ohm system) $V_{DD1} = 28\text{ Vdc}$, $V_{DD2} = 25\text{ Vdc}$, $I_{DQ1(A+B)} = 60\text{ mA}$, $I_{DQ2(A+B)} = 550\text{ mA}$, 850-940 MHz Bandwidth

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|------------------|-----|--------------|-----|-------|
| P_{out} @ 1 dB Compression Point, CW | P_{1dB} | — | 79 | — | W |
| IMD Symmetry @ 71 W PEP, P_{out} where IMD Third Order Intermodulation $\cong 30\text{ dBc}$ (Delta IMD Third Order Intermodulation between Upper and Lower Sidebands > 2 dB) | IMD_{sym} | — | 22 | — | MHz |
| VBW Resonance Point (IMD Third Order Intermodulation Inflection Point) | VBW_{res} | — | 50 | — | MHz |
| Quiescent Current Accuracy over Temperature with 8.25 k Ω Gate Feed Resistors (-30 to 85°C) (3) | ΔI_{QT} | — | 5.03 4.61 | — | % |
| Gain Flatness in 90 MHz Bandwidth @ $P_{out} = 35\text{ W Avg.}$ | G_F | — | 1.2 | — | dB |
| Gain Variation over Temperature (-30°C to +85°C) | ΔG | — | 0.03 | — | dB/°C |
| Output Power Variation over Temperature (-30°C to +85°C) | ΔP_{1dB} | — | 0.005 | — | dB/°C |

- Side A and Side B are tied together for this measurement.
- Part internally matched both on input and output.
- Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family* and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1977 or AN1987.

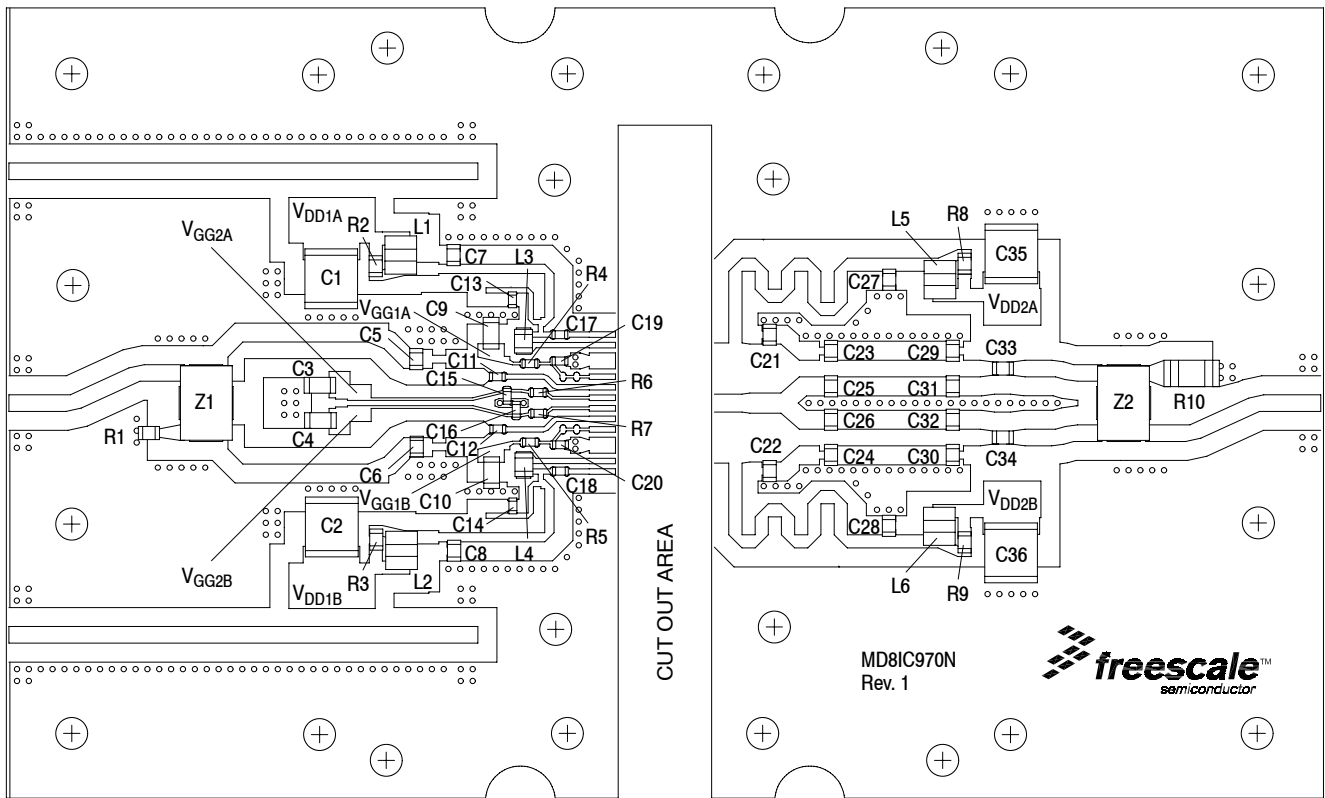


Figure 3. MD8IC970NR1(GNR1) Test Circuit Component Layout

Table 6. MD8IC970NR1(GNR1) Test Circuit Component Designations and Values

| Part | Description | Part Number | Manufacturer |
|----------------------------|--|--------------------|-----------------|
| C1, C2, C35, C36 | 10 μ F, 50 V Chip Capacitors | GRM55DR61H106KA88L | Murata |
| C3, C4, C9, C10 | 1 μ F, 50 V Chip Capacitors | GRM31MR71H105KA88L | Murata |
| C5, C6 | 3.3 pF Chip Capacitors | ATC600F3R3BT250XT | ATC |
| C7, C8, C27, C28, C33, C34 | 39 pF Chip Capacitors | ATC600F390JT250XT | ATC |
| C11, C12 | 47 pF Chip Capacitors | ATC600S470JT250XT | ATC |
| C13, C14 | 4.7 pF Chip Capacitors | ATC600S4R7JT250XT | ATC |
| C15, C16, C19, C20 | 0.1 μ F, 50 V Chip Capacitors | GRM188R71C104K01D | Murata |
| C17, C18 | 5.6 pF Chip Capacitors | ATC600S5R6JT250XT | ATC |
| C21, C22 | 15 pF Chip Capacitors | ATC600F150JT250XT | ATC |
| C23, C24, C25, C26 | 4.7 pF Chip Capacitors | ATC600F4R7BT250XT | ATC |
| C29, C30, C31, C32 | 2.7 pF Chip Capacitors | ATC600F2R7BT250XT | ATC |
| L1, L2, L5, L6 | 5.0 nH 2 Turn Inductors | A02TKLC | Coilcraft |
| L3, L4 | 2.8 nH Chip Inductors | 0805CS-020XJLC | Coilcraft |
| R1 | 51 Ω , 1/8 W Chip Resistor | SG73P2ATTD51R0F | KOA Speer |
| R2, R3, R8, R9 | 10 Ω , 1/8 W Chip Resistors | RK73H2ATTD10R0F | KOA Speer |
| R4, R5, R6, R7 | 8.25 k Ω , 1/10 W Chip Resistors | RK73H1JTTD8251F | KOA Speer |
| R10 | 50 Ω , 10 W SM Chip Power Resistor | 81A7031-50-5F | Florida RF Labs |
| Z1, Z2 | 900 MHz Band, 90°, 3 dB Chip Hybrid Couplers | GSC362-HYB0900 | Soshin |
| PCB | 0.030", $\epsilon_r = 3.66$ | RO4350B | Rogers |

TYPICAL CHARACTERISTICS

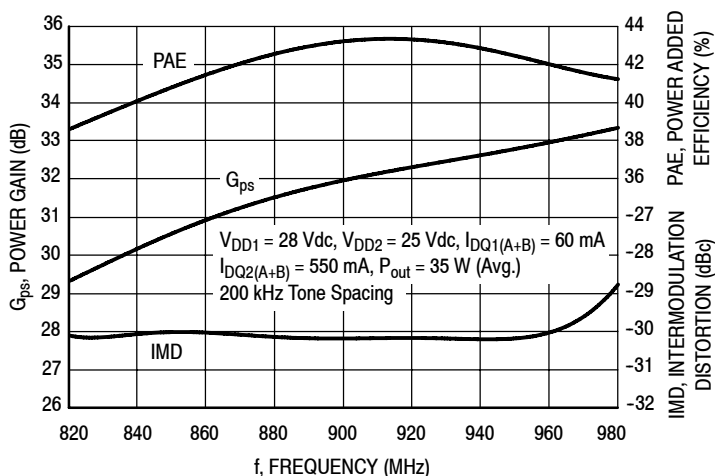


Figure 4. Two-Tone Broadband Performance @ $P_{out} = 35 \text{ Watts Avg.}$

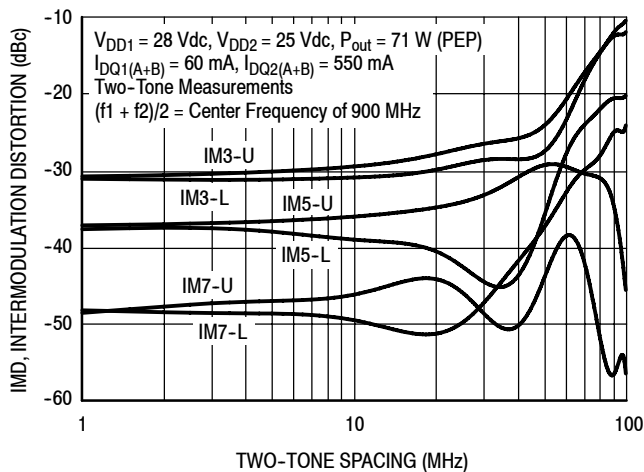


Figure 5. Intermodulation Distortion Products versus Two-Tone Spacing

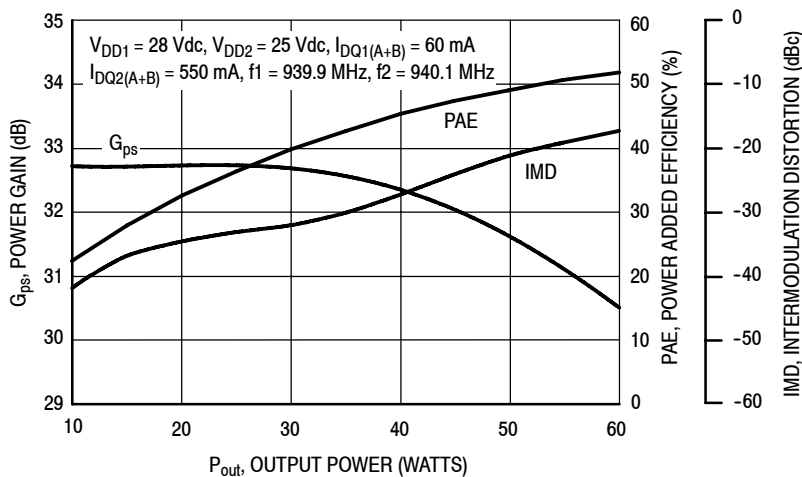


Figure 6. Power Gain, Power Added Efficiency and Intermodulation Distortion Products versus Average Output Power

TYPICAL CHARACTERISTICS

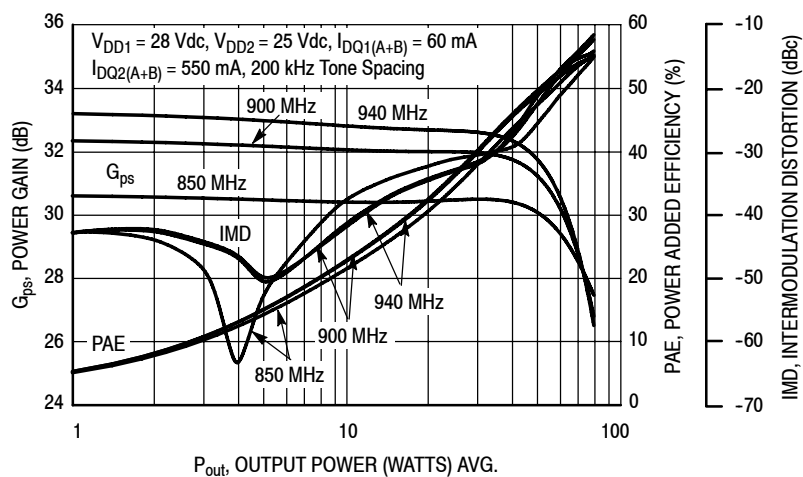


Figure 7. Power Gain, Power Added Efficiency and Intermodulation Distortion Products versus Output Power

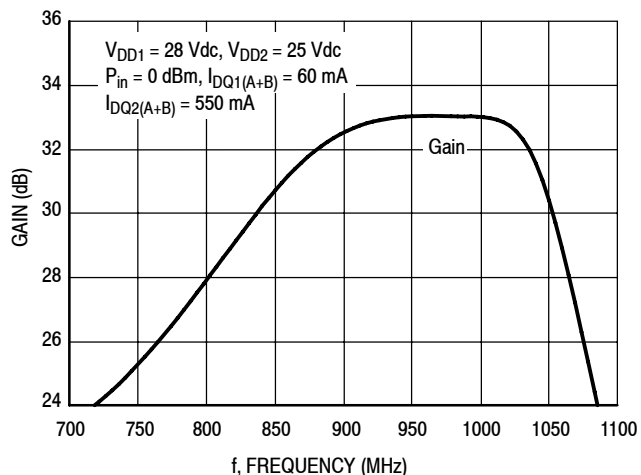


Figure 8. Broadband Frequency Response

$V_{DD1} = 28 \text{ Vdc}$, $I_{DQ1(A)} = 30 \text{ mA}$

| f MHz | Z_{in} Ω | Z_{load} Ω |
|----------|----------------------|------------------------|
| 820 | 18.4 - j13.0 | 11.3 + j20.0 |
| 840 | 18.8 - j12.7 | 11.7 + j21.9 |
| 860 | 19.1 - j12.9 | 12.1 + j23.4 |
| 880 | 19.1 - j13.2 | 12.5 + j24.5 |
| 900 | 18.7 - j13.6 | 12.7 + j25.1 |
| 920 | 18.0 - j13.9 | 12.5 + j25.6 |
| 940 | 17.2 - j14.2 | 11.8 + j26.0 |
| 960 | 16.1 - j14.3 | 10.9 + j26.6 |
| 980 | 14.6 - j14.3 | 9.6 + j27.4 |

Z_{in} = Device input impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

| f MHz | Z_{in} Ω | Z_{load} Ω |
|----------|----------------------|------------------------|
| 330 | 31.2 - j21.5 | 16.2 + j57.8 |
| 350 | 33.6 - j18.7 | 24.2 + j59.6 |
| 370 | 35.8 - j18.8 | 29.8 + j55.6 |
| 390 | 36.4 - j19.6 | 29.0 + j52.8 |
| 410 | 37.0 - j20.1 | 27.8 + j54.7 |
| 430 | 37.7 - j21.7 | 30.2 + j58.5 |
| 450 | 36.2 - j24.8 | 38.8 + j59.1 |

Z_{in} = Device input impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

| f MHz | Z_{in} Ω | Z_{load} Ω |
|----------|----------------------|------------------------|
| 120 | 42.7 - j27.4 | 47.3 + j80.0 |
| 130 | 40.0 - j22.5 | 61.4 + j93.3 |
| 140 | 40.2 - j16.0 | 84.0 + j104.2 |
| 150 | 43.8 - j13.3 | 114.5 + j107.2 |
| 160 | 47.8 - j10.0 | 147.2 + j98.5 |
| 170 | 51.5 - j10.0 | 179.4 + j81.3 |
| 180 | 54.9 - j10.6 | 215.9 + j53.3 |
| 190 | 58.2 - j12.9 | 256.6 - j7.6 |
| 200 | 59.6 - j16.9 | 233.3 - j109.9 |

Z_{in} = Device input impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

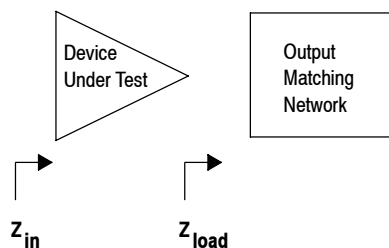


Figure 9. Series Equivalent Input and Load Impedance — Stage 1

NOTE: Measurement made on a per side basis.

$V_{DD2} = 25 \text{ Vdc}$, $I_{DQ2(A)} = 275 \text{ mA}$, $P_{out} = 17.5 \text{ Watts Avg.}$

| f MHz | Z_{in} Ω | Z_{load} Ω |
|----------|----------------------|------------------------|
| 820 | 9.49 + j10.2 | 3.19 + j1.99 |
| 840 | 10.3 + j10.3 | 3.29 + j2.11 |
| 860 | 11.2 + j10.2 | 3.39 + j2.18 |
| 880 | 12.2 + j9.89 | 3.45 + j2.20 |
| 900 | 13.1 + j9.34 | 3.46 + j2.16 |
| 920 | 14.0 + j8.53 | 3.40 + j2.08 |
| 940 | 14.6 + j7.51 | 3.24 + j2.00 |
| 960 | 15.1 + j6.28 | 2.98 + j1.96 |
| 980 | 15.2 + j4.87 | 2.66 + j1.99 |

Z_{in} = Device input impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

| f MHz | Z_{in} Ω | Z_{load} Ω |
|----------|----------------------|------------------------|
| 330 | 5.78 + j3.02 | 5.53 + j1.53 |
| 350 | 5.73 + j3.40 | 6.27 + j1.77 |
| 370 | 5.66 + j3.89 | 6.95 + j1.55 |
| 390 | 5.63 + j4.34 | 7.18 + j0.90 |
| 410 | 5.60 + j4.75 | 6.67 + j0.22 |
| 430 | 5.53 + j5.06 | 5.61 + j0.05 |
| 450 | 5.38 + j5.32 | 4.45 + j0.57 |

Z_{in} = Device input impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

| f MHz | Z_{in} Ω | Z_{load} Ω |
|----------|----------------------|------------------------|
| 120 | 5.47 - j0.60 | 5.74 + j2.70 |
| 130 | 5.46 - j0.36 | 6.36 + j1.97 |
| 140 | 5.47 - j0.13 | 6.21 + j1.37 |
| 150 | 5.47 + j0.11 | 5.95 + j1.37 |
| 160 | 5.46 + j0.35 | 6.09 + j1.63 |
| 170 | 5.43 + j0.56 | 6.59 + j1.58 |
| 180 | 5.42 + j0.75 | 6.70 + j0.92 |
| 190 | 5.49 + j0.93 | 5.73 + j0.82 |
| 200 | 5.42 + j1.05 | 4.83 + j2.57 |

Z_{in} = Device input impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

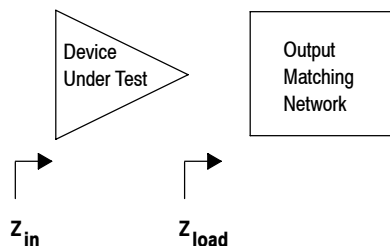


Figure 10. Series Equivalent Input and Load Impedance — Stage 2

NOTE: Measurement made on a per side basis.

ALTERNATIVE PEAK TUNE LOAD PULL CHARACTERISTICS — STAGE 2

$V_{DD2} = 25 \text{ Vdc}$, $I_{DQ2} = 300 \text{ mA}$, CW

| f MHz | Z_{source} Ω | $Z_{\text{load}}^{(1)}$ Ω | Max P_{out} | |
|----------|---------------------------------|-------------------------------------|----------------------|----|
| | | | P1dB | |
| | | | dBm | W |
| 850 | $10.9 + j10.2$ | $3.34 + j2.16$ | 47.1 | 51 |
| 940 | $14.6 + j7.51$ | $3.24 + j2.00$ | 46.8 | 48 |

(1) Load impedance for optimum P1dB power.

Z_{source} = Impedance as measured from gate contact to ground.

Z_{load} = Impedance as measured from drain contact to ground.

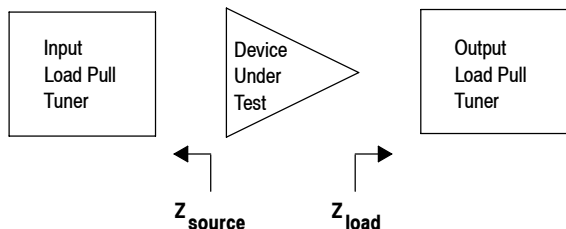


Figure 11. Single Side Load Pull Performance — Maximum P1dB Tuning

$V_{DD2} = 25 \text{ Vdc}$, $I_{DQ2} = 300 \text{ mA}$, CW

| f MHz | Z_{source} Ω | $Z_{\text{load}}^{(1)}$ Ω | Max Eff. |
|----------|---------------------------------|-------------------------------------|----------|
| | | | P1dB % |
| 850 | $10.9 + j10.2$ | $3.36 + j3.93$ | 66.2 |
| 940 | $14.6 + j7.51$ | $2.95 + j3.66$ | 62.1 |

(1) Load impedance for optimum P1dB efficiency.

Z_{source} = Impedance as measured from gate contact to ground.

Z_{load} = Impedance as measured from drain contact to ground.

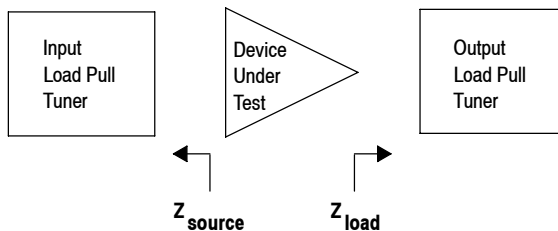


Figure 12. Single Side Load Pull Performance — Maximum Efficiency Tuning

$V_{DD2} = 25 \text{ Vdc}$, $I_{DQ2} = 300 \text{ mA}$, CW

| f MHz | Z_{source} Ω | $Z_{\text{load}}^{(1)}$ Ω | Max P_{out} | |
|----------|---------------------------------|-------------------------------------|----------------------|----|
| | | | P1dB | |
| | | | dBm | W |
| 430 | $5.53 + j5.06$ | $5.61 + j0.05$ | 46.8 | 48 |

(1) Load impedance for optimum P1dB power.

Z_{source} = Impedance as measured from gate contact to ground.

Z_{load} = Impedance as measured from drain contact to ground.

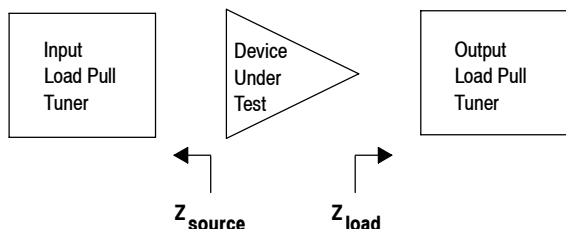


Figure 13. Single Side Load Pull Performance — Maximum P1dB Tuning

$V_{DD2} = 25 \text{ Vdc}$, $I_{DQ2} = 300 \text{ mA}$, CW

| f MHz | Z_{source} Ω | $Z_{\text{load}}^{(1)}$ Ω | Max Eff. |
|----------|---------------------------------|-------------------------------------|----------|
| | | | P1dB % |
| 430 | $5.53 + j5.06$ | $5.96 + j2.65$ | 66.1 |

(1) Load impedance for optimum P1dB efficiency.

Z_{source} = Impedance as measured from gate contact to ground.

Z_{load} = Impedance as measured from drain contact to ground.

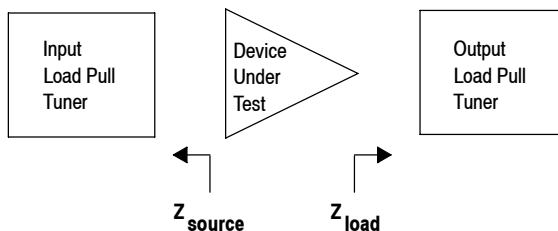
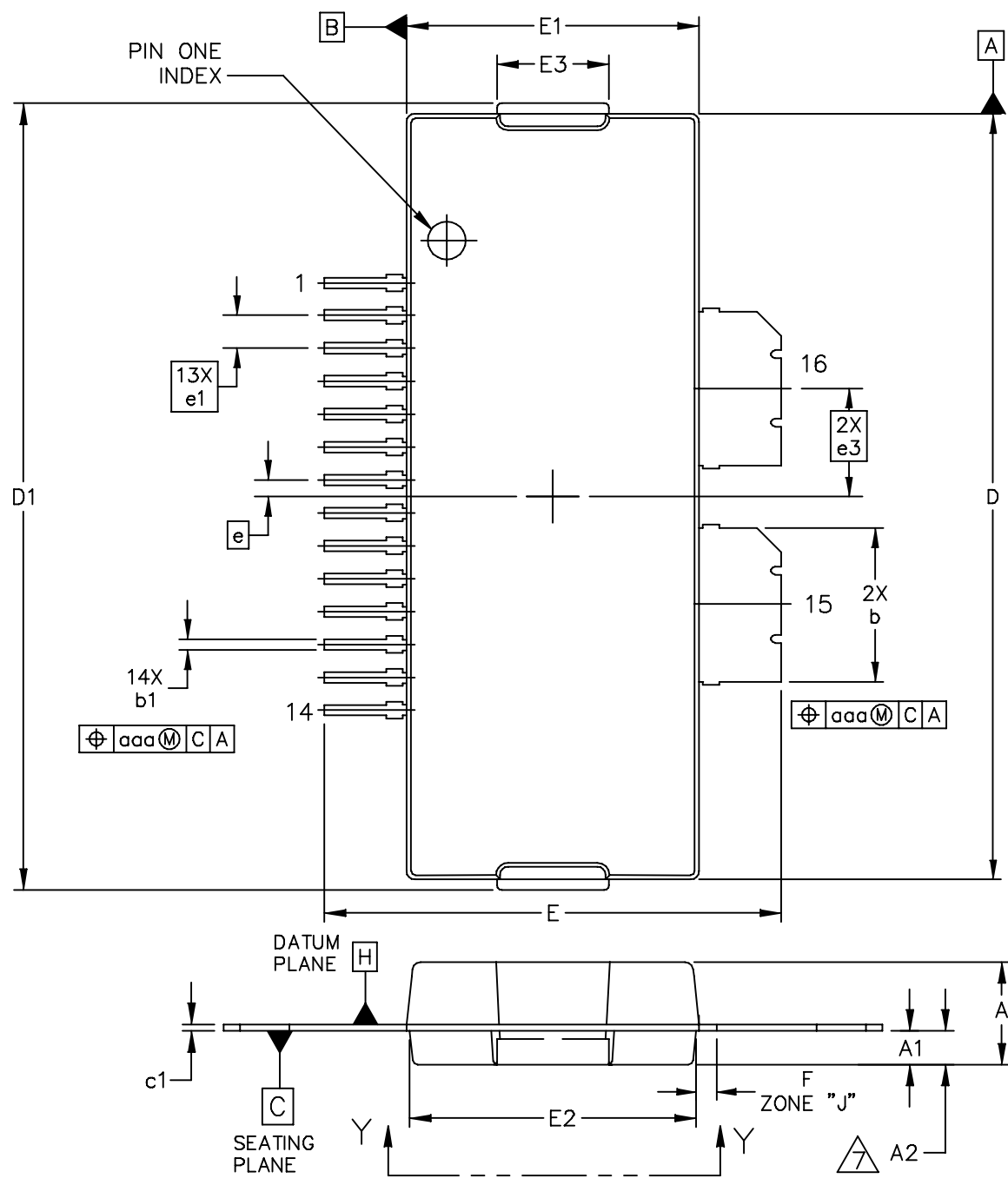
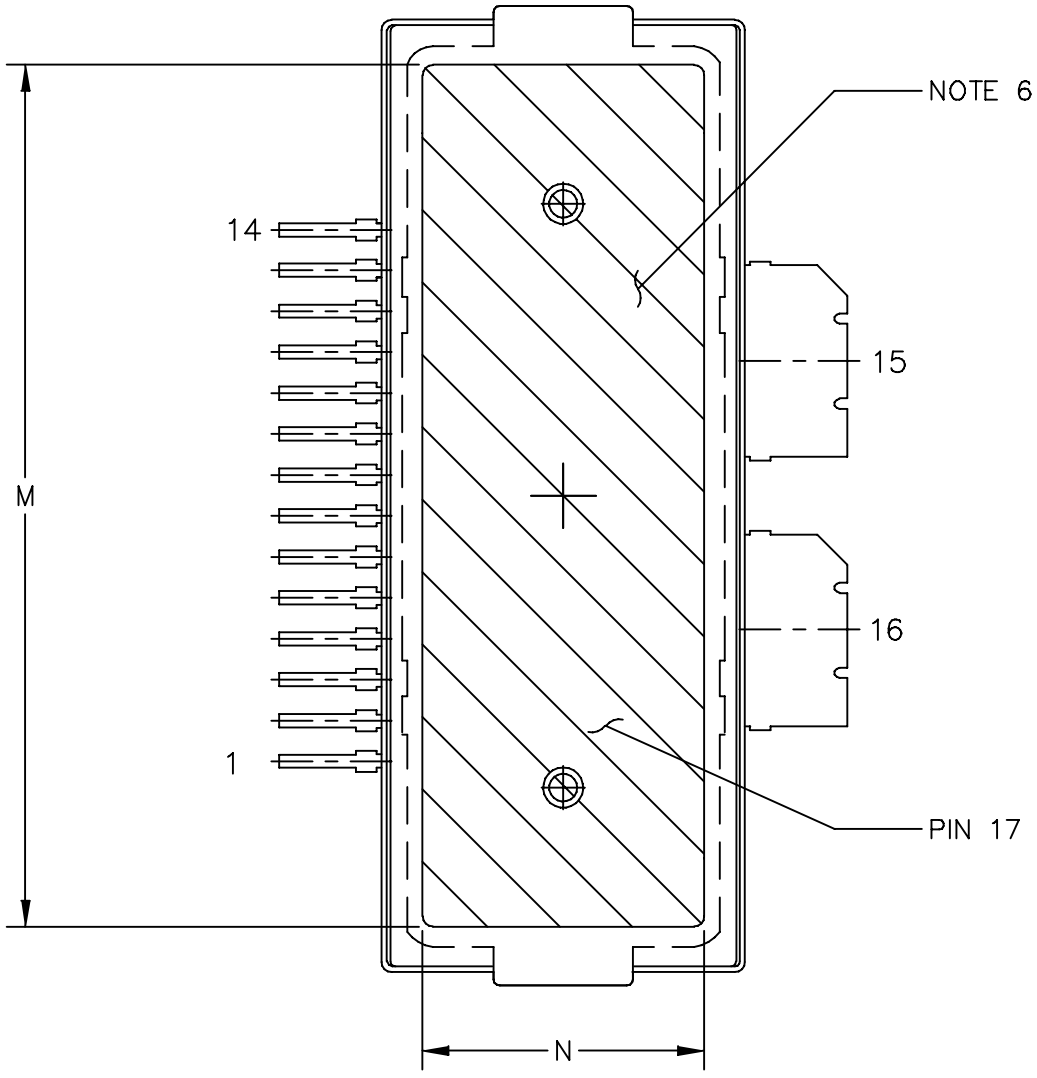


Figure 14. Single Side Load Pull Performance — Maximum Efficiency Tuning

PACKAGE DIMENSIONS



| | | |
|---|--------------------------|----------------------------|
| © FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED. | MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE |
| TITLE: TO-270 WIDE BODY LONG, 16 LEAD, PLASTIC | DOCUMENT NO: 98ASA10739D | REV: A |
| | CASE NUMBER: 1866-02 | 02 AUG 2007 |
| | STANDARD: NON-JEDEC | |



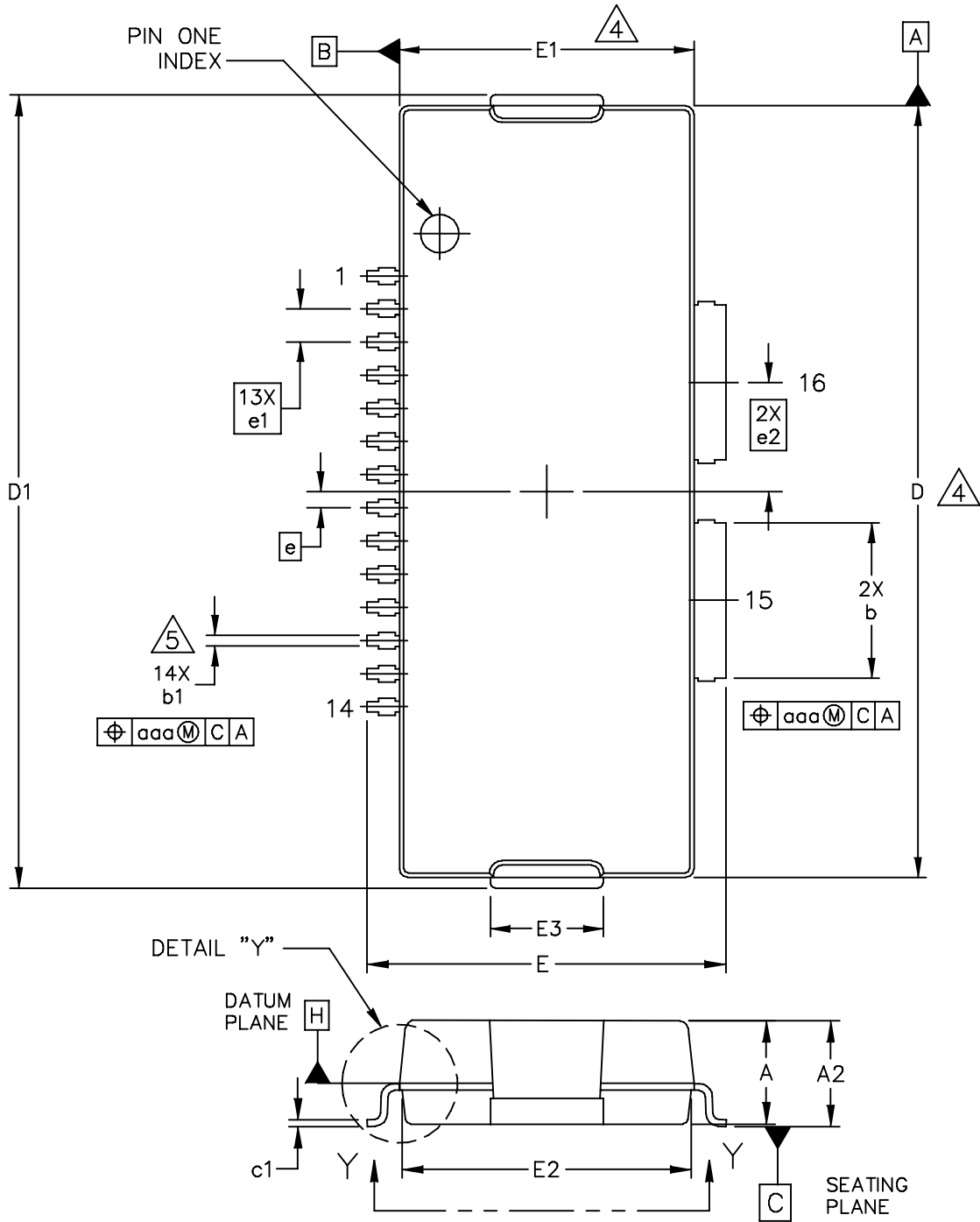
VIEW Y-Y

| | | | |
|---|--------------------------|----------------------------|--|
| © FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED. | MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE | |
| TITLE: TO-270 WIDE BODY LONG, 16 LEAD, PLASTIC | DOCUMENT NO: 98ASA10739D | REV: A | |
| | CASE NUMBER: 1866-02 | 02 AUG 2007 | |
| | STANDARD: NON-JEDEC | | |

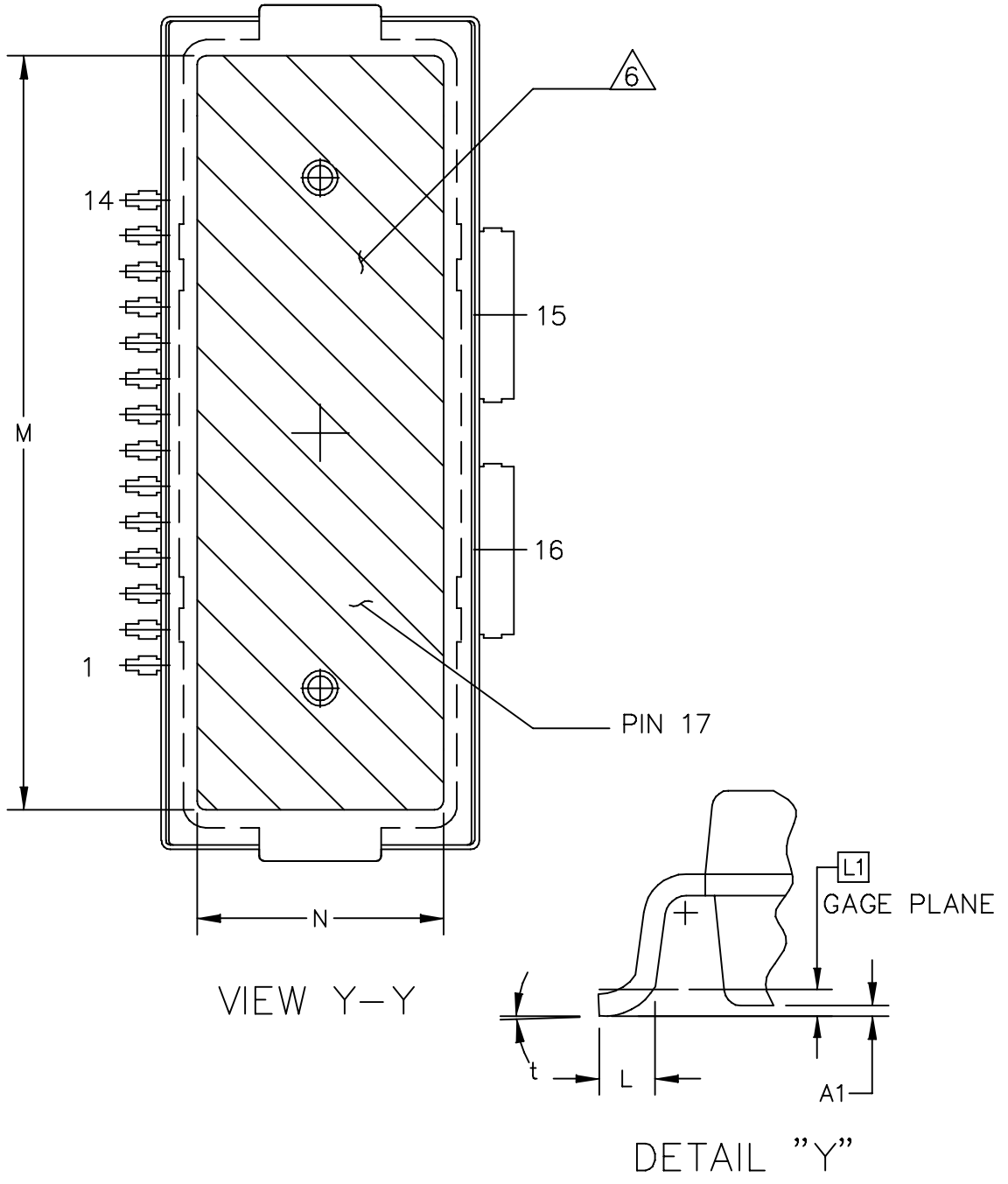
NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 (0.15) PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS "b" AND "b1" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b" AND "b1" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
6. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.
7. DIM A2 APPLIES WITHIN ZONE "J" ONLY.

| DIM | INCH | | MILLIMETER | | DIM | INCH | | MILLIMETER | |
|---|----------|------|--------------------|-------|--------------------------|----------------------------|------|-------------|------|
| | MIN | MAX | MIN | MAX | | MIN | MAX | MIN | MAX |
| A | .122 | .128 | 3.10 | 3.25 | M | .800 | ---- | 20.32 | ---- |
| A1 | .039 | .043 | 0.96 | 1.12 | N | .270 | ---- | 6.86 | ---- |
| A2 | .040 | .042 | 1.02 | 1.07 | b | .184 | .190 | 4.67 | 4.83 |
| D | .928 | .932 | 23.57 | 23.67 | b1 | .010 | .016 | 0.25 | 0.41 |
| D1 | .954 | .958 | 24.23 | 24.33 | c1 | .007 | .011 | 0.18 | 0.28 |
| E | .551 | .559 | 14.00 | 14.20 | e | .020 BSC | | 0.51 BSC | |
| E1 | .353 | .357 | 8.97 | 9.07 | e1 | .040 BSC | | 1.02 BSC | |
| E2 | .346 | .350 | 8.79 | 8.89 | e3 | .131 BSC | | 3.33 BSC | |
| E3 | .132 | .140 | 3.35 | 3.56 | | | | | |
| F | .025 BSC | | 0.64 BSC | | aaa | .004 | | 0.10 | |
| © FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED. | | | MECHANICAL OUTLINE | | | PRINT VERSION NOT TO SCALE | | | |
| TITLE: TO-270 WIDE BODY LONG, 16 LEAD, PLASTIC | | | | | DOCUMENT NO: 98ASA10739D | | | REV: A | |
| | | | | | CASE NUMBER: 1866-02 | | | 02 AUG 2007 | |
| | | | | | STANDARD: NON-JEDEC | | | | |



| | | | | | |
|--|--|--------------------------|--|----------------------------|--|
| © FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED. | | MECHANICAL OUTLINE | | PRINT VERSION NOT TO SCALE | |
| TITLE: TO-270 WIDE BODY LONG, 16 LEAD, GULL WING PLASTIC | | DOCUMENT NO: 98ASA10740D | | REV: C | |
| | | CASE NUMBER: 1867-02 | | 18 MAY 2010 | |
| | | STANDARD: NON-JEDEC | | | |



| | | | |
|--|--|--------------------------|----------------------------|
| © FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED. | | MECHANICAL OUTLINE | PRINT VERSION NOT TO SCALE |
| TITLE: TO-270 WIDE BODY LONG, 16 LEAD, GULL WING PLASTIC | | DOCUMENT NO: 98ASA10740D | REV: C |
| | | CASE NUMBER: 1867-02 | 18 MAY 2010 |
| | | STANDARD: NON-JEDEC | |

NOTES:

1. CONTROLLING DIMENSION: INCH
 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
 3. DATUM PLANE H IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

| DIM | INCH | | MILLIMETER | | DIM | INCH | | MILLIMETER | |
|-----|---------|------|------------|-------|-----|----------|------|------------|------|
| | MIN | MAX | MIN | MAX | | MIN | MAX | MIN | MAX |
| A | .122 | .128 | 3.10 | 3.25 | b | .184 | .190 | 4.67 | 4.83 |
| A1 | .001 | .004 | 0.02 | 0.10 | b1 | .010 | .016 | 0.25 | 0.41 |
| A2 | .125 | .131 | 3.18 | 3.33 | c1 | .007 | .011 | 0.18 | 0.28 |
| D | .928 | .932 | 23.57 | 23.67 | e | .020 BSC | | 0.51 BSC | |
| D1 | .954 | .958 | 24.23 | 24.33 | e1 | .040 BSC | | 1.02 BSC | |
| E | .429 | .437 | 10.9 | 11.1 | e2 | .131 BSC | | 3.33 BSC | |
| E1 | .353 | .357 | 8.97 | 9.07 | t | 2* | 8* | 2* | 8* |
| E2 | .346 | .350 | 8.79 | 8.89 | aaa | .004 | | 0.10 | |
| E3 | .132 | .140 | 3.35 | 3.56 | | | | | |
| L | .018 | .024 | 0.46 | 0.61 | | | | | |
| L1 | .01 BSC | | 0.25 BSC | | | | | | |
| M | .800 | ---- | 20.32 | ---- | | | | | |
| N | .270 | ---- | 6.86 | ---- | | | | | |

| | | | | | |
|---|--|--------------------|--------------------------|----------------------------|-------------|
| © FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED. | | MECHANICAL OUTLINE | | PRINT VERSION NOT TO SCALE | |
| TITLE: TO-270 WIDE BODY LONG, 16 LEAD, GULL WING PLASTIC | | | DOCUMENT NO: 98ASA10740D | | REV: C |
| | | | CASE NUMBER: 1867-02 | | 18 MAY 2010 |
| | | | STANDARD: NON-JEDEC | | |

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following documents, tools and software to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN1977: Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family
- AN1987: Quiescent Current Control for the RF Integrated Circuit Device Family

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

For Software and Tools, do a Part Number search at <http://www.freescale.com>, and select the "Part Number" link. Go to the Software & Tools tab on the part's Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

| Revision | Date | Description |
|----------|-----------|---|
| 0 | Feb. 2011 | • Initial Release of Data Sheet |
| 1 | Feb. 2011 | • Corrected output power from 35 W CW to 35 W Avg. Two-Tone, Table 2, Thermal Characteristics, p. 2 |
| 2 | May 2011 | • Added part number MD8IC970GNR1 (TO-270 WBL-16 Gull), p. 1 • Added 1867-02 (TO-270 WBL-16 Gull) package isometric, p. 1, and mechanical outline, p. 13-15 |

How to Reach Us:

Home Page:

www.freescale.com

Web Support:

<http://www.freescale.com/support>

USA/Europe or Locations Not Listed:

Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:

Freescale Semiconductor Literature Distribution Center
1-800-441-2447 or +1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc. 2011. All rights reserved.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[NXP:](#)

[MD8IC970GNR1](#) [MD8IC970NR1](#)