NXP Semiconductors
User Guide

Document identifier: KE17ZHDG
Rev. 0.1, 13 December 2021

KE17Z Hardware Developer's Guide

Contents

Chapter 1
Overview

This document provides board-level hardware design guidelines for the KE17Z family products (see table). The hardware design guidelines are similar for this product family. In this document, the MKE17Z256VLL7 device is used for demonstration purposes.

Table 1. KE17Z family

Product	Memory		Package		IO and ADC channel			HMI
Part number	Flash (KB)	SRAM (KB)	Pin count	Package	GPIOs	GPIOs (INT/HD) [1]	ADC channels	TSI
MKE17Z256VLL7	256	48	100	LQFP	89	89/8	16	50ch
MKE17Z256VLH7	256	48	64	LQFP	58	58/8	16	47ch
MKE17Z128VLL7	128	32	100	LQFP	89	89/8	16	50ch
MKE17Z128VLH7	128	32	64	LQFP	58	58/8	16	47ch
MKE13Z256VLL7	256	48	100	LQFP	89	89/8	16	25ch
MKE13Z256VLH7	256	48	64	LQFP	58	58/8	16	22ch
MKE13Z128VLL7	128	32	100	LQFP	89	89/8	16	25ch
MKE13Z128VLH7	128	32	64	LQFP	58	58/8	16	22ch
MKE12Z256VLL7	256	48	100	LQFP	89	89/8	16	-
MKE12Z256VLH7	256	48	64	LQFP	58	58/8	16	-
MKE12Z128VLL7	128	32	100	LQFP	89	89/8	16	-
MKE12Z128VLH7	128	32	64	LQFP	58	58/8	16	-

1. INT: interrupt pin numbers; HD: high drive pin numbers

KE17Z MCUs extend Kinetis E family to dual TSI performance and broader scalability. Robust and dual TSI provides high-level stability and accuracy to customer's HMI system. 1 Msps ADC and FlexTimer help build a perfect solution for a simple BLDC motor control system.

Following are the general features of the KE17Z series MCUs:

- Arm® Cortex®-M0+ core, supports up to 72 MHz frequency, with 2.35 CoreMark/MHz.
- Scalable memory up to 256 KB program flash and up to 48 KB SRAM
- 5 V power supply ranges from 2.7 V to 5.5 V.
- Dual capacitive touch sensing modules offer 2 x 25 ch touch sensing channels supporting both self-cap and mutual cap technologies.
- Precision mixed-signal capability with 1x high-speed on-chip analog comparator and 1× 12-bit analog-to-digital converter (ADC) with up to 16 channel analog inputs per module, up to 1 Msps.
- Flexible timers including 3 × Flex Timers (FTM) for PWM generation, offering up to 8 standard PWM channels

This document describes the following module and provides appropriate hardware design related recommendations:

- Power Supply
- Clock Module
- Reset Circuit

- Debugging and Programming Interface
- Touch Sensing interface (TSI)
- ADC Input Circuit
- Digital GPIO and unused pin
- General Board Layout Guidelines

A general schematic example is shown in the following figure.

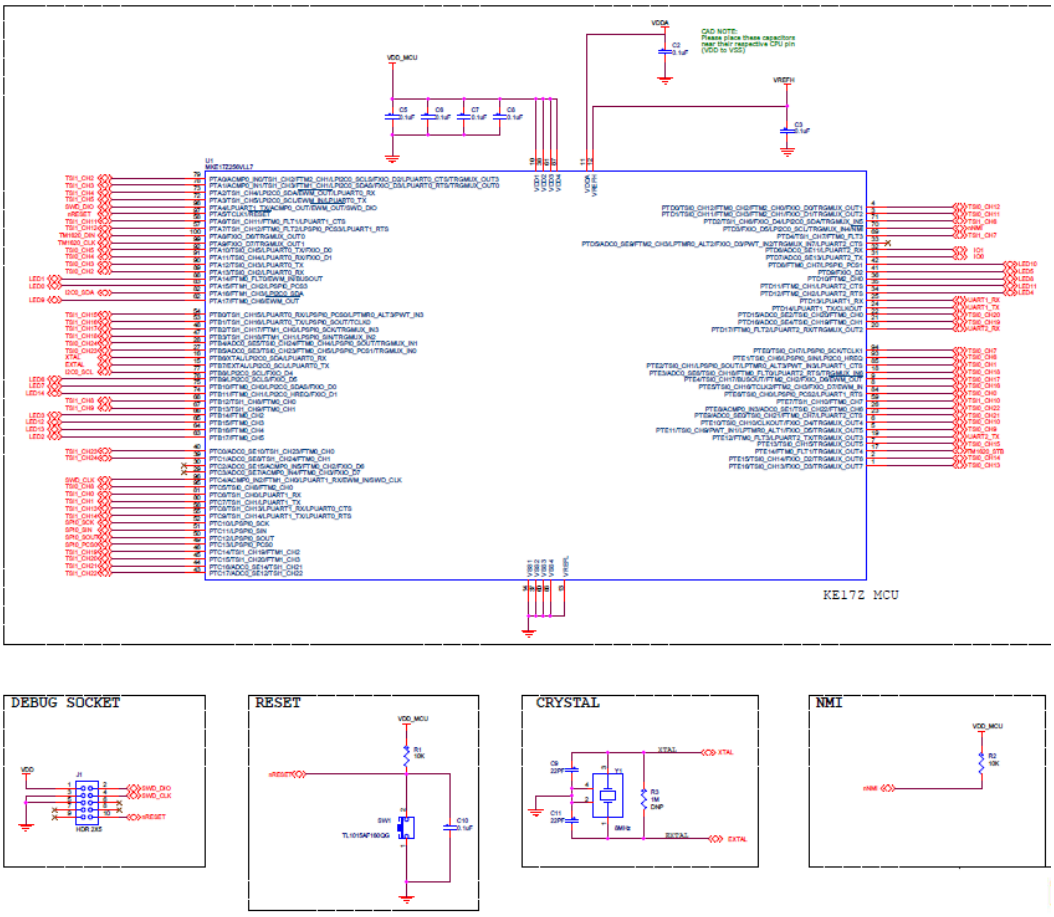


Figure 1. X-KE17Z-TSI-EVB schematic example

1.1 Related documentation

The table below lists and explains the additional documents and resources that you can refer to for more information on KE17Z MCUs. Some of the documents listed below may be available only under a non-disclosure agreement (NDA). To request access to these documents, contact your local field applications engineer (FAE) or sales representative.

Table 2. Related documentation

Document	Description	Link/how to access
Kinetis KE17Z/13Z/12Z with up to 256 KB Flash Reference Manual	Intended for system software and hardware developers and applications programmers who want to develop products with this device	KE1xZP100M72SF1RM

Table continues on the next page...

Table 2. Related documentation (continued)

Document	Description	Link/how to access
Kinetis KE17Z/13Z/12Z with up to 256 KB Flash Data Sheet	Provides information about electrical characteristics, hardware design considerations, and ordering information	KE1xZP100M72SF1
AN5426 Hardware Design Guidelines for S32K1xx Microcontrollers	Explains Hardware Design Guidelines for S32K1xx Microcontrollers	AN5426
KE15ZTSIUG KE15Z Touch Sensing Interface User Guide	Explains the new TSI (Touch Sensing Interface) measurement and how to develop the software and hardware board from the application point of view	KE15ZTSIUG

Chapter 2
Power Supply

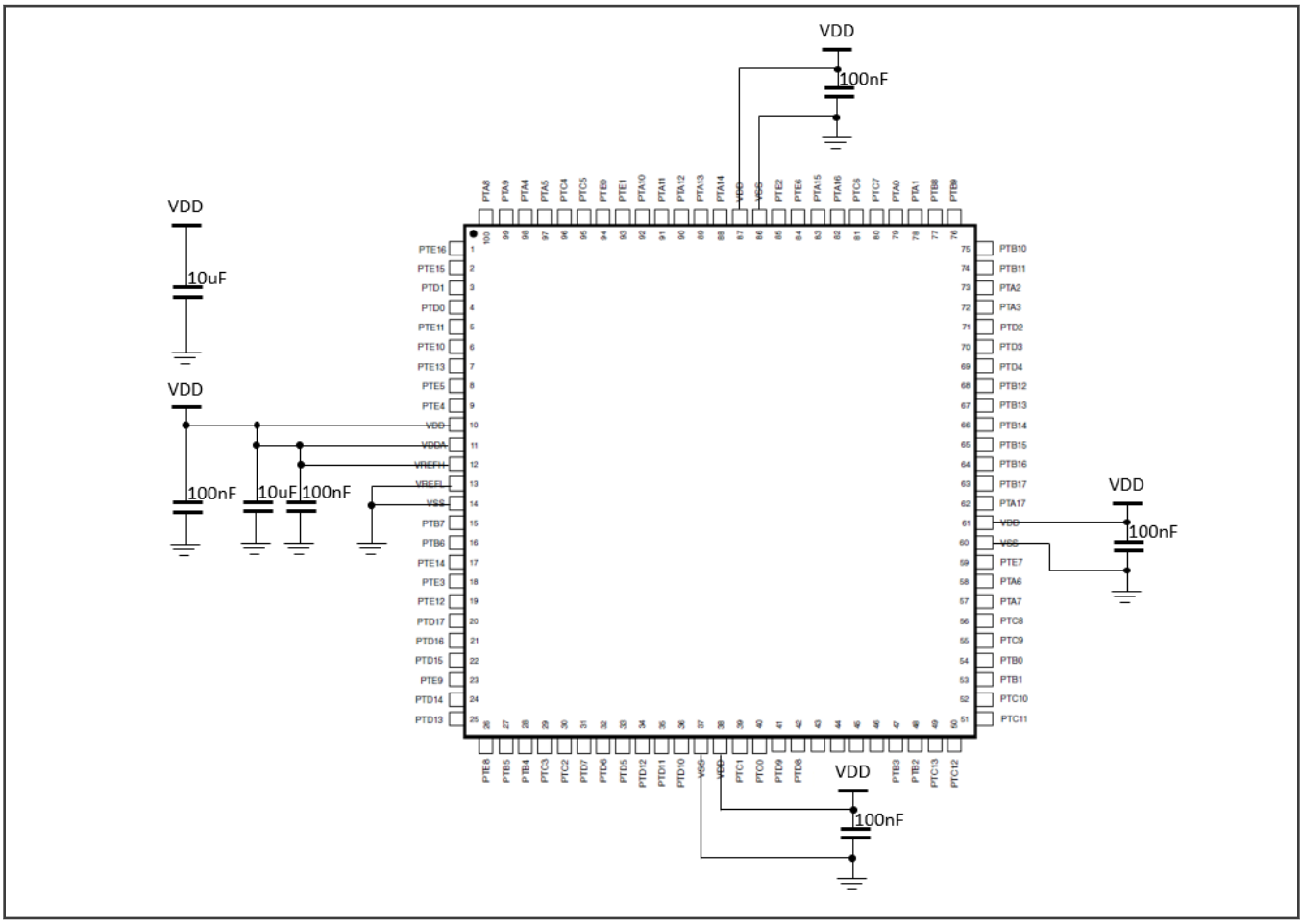
The power supply of KE17Z ranges from 2.7 V to 5.5 V, the detailed operating requirements are listed below. Note that the difference between VDD (digital power supply) and VDDA (analog power supply) cannot exceed 0.1 V, so it is recommended to connect VDD and VDDA directly in practice. Also, the power supply ramp up rate should be limited within 100 V/ms.

Table 3. Power supply

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	2.7	5.5	V	
V_{DDA}	Analog supply voltage	2.7	5.5	V	
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	– 0.1	0.1	V	
$V_{SS} – V_{SSA}$	V_{SS}-to-V_{SSA} differential voltage	– 0.1	0.1	V	

The decoupling capacitors (100 nF as shown in the figure below) are required to filter out the system noise. Figure below shows examples of decoupling capacitors on the schematic, at least one decoupling capacitor per power pin is recommended. On PCB layout level, all decoupling capacitors should be placed as close as possible to each of their respective power supply pin; the ground side of the decoupling capacitor should have a via to the pad which goes directly down to the ground plane. The decoupling capacitors should not route to the power plane through a long trace. The types and values of the decoupling capacitor depend on the noise level and frequency. The typical value is usually in the range of 0.01 µF to 0.1 µF.

The bulk capacitor (10 µF as shown in the figure below) acts as a local power supply to the power pin, its typical value is 10 µF.


VDD
100nF
VDD
10uF
VDD
100nF
10uF
100nF
VDD
100nF
VDD
100nF
PTA8
PTA9
PTA4
PTA5
PTC4
PTC5
PTE0
PTE1
PTA10
PTA11
PTA12
PTA13
PTA14
VDD
VSS
PTE2
PTE6
PTA15
PTA16
PTC6
PTC7
PTA0
PTA1
PTB8
PTB9
PTE16
PTE15
PTD1
PTD0
PTE11
PTE10
PTE13
PTE5
PTE4
VDD
VDDA
VREFH
VREFL
VSS
PTB7
PTB6
PTE14
PTE3
PTE12
PTD17
PTD16
PTD15
PTE9
PTD14
PTD13
PTB10
PTB11
PTA2
PTA3
PTD2
PTD3
PTD4
PTB12
PTB13
PTB14
PTB15
PTB16
PTB17
PTA17
VDD
VSS
PTE7
PTA6
PTA7
PTC8
PTC9
PTB0
PTB1
PTC10
PTC11
PTE8
PTB5
PTB4
PTC3
PTC2
PTD7
PTD6
PTD5
PTD12
PTD11
PTD10
VSS
VDD
PTC1
PTC0
PTD9
PTD8
PTB3
PTB2
PTC13
PTC12

Chapter 3
Clock Module

The KE17Z has the following clock sources:

- Fast internal reference clock (FIRC): 48 MHz high-accuracy (up to ±1%) fast internal reference clock (FIRC) for normal Run as the default system clock source after reset.
- Slow internal reference clock (SIRC): 8 MHz/2 MHz.
- LPFLL: Supports only up to 72 MHz
- LPO128K: 128 KHz always on internal low-power oscillator clock, for WDOG, LPTMR, EWM, PORT Control.
- External square wave input: Up to 60 MHz DC external square wave input clock
- External oscillator clock (OSC): high range 4 - 40 MHz (with low power or high gain mode) and low range 32 - 40 kHz (with high-gain mode only)

3.1 External oscillator circuit design

The EXTAL and XTAL pins provide the interface for a Crystal oscillator. EXTAL is the input to the crystal oscillator amplifier. XTAL is the output of the crystal oscillator amplifier. The pierce oscillator provides a robust, low-noise, and low-power external clock source. It is designed for optimal start-up margin with typical crystal oscillators. KE17Z supports two ranges of external oscillator:

- high-range: 4 - 40 MHz (with low-power or high-gain mode)

Table 4. External crystal/resonator connections

Oscillator mode	Oscillator mode
Low frequency (32.768 kHz), high gain	Diagram 3
High frequency (1-32 MHz), low power	Diagram 2
High frequency (1-32 MHz), high gain	Diagram 3

- low-range: 32 - 40 kHz (with high-gain mode only)

The typical circuit design of the external oscillator is shown in the figure below. For the low-power use case, the low-power oscillator mode is recommended, as shown in Diagram 2, thus the 1 Mohm R_F (feedback resistor) is not needed in this case. For noise use case, the high-gain oscillator is preferred as shown in Diagram 3. The user needs to add 1 Mohm R_F (feedback resistor), also the use needs to double check with the crystal vendor about the exact value of R_S (series resistor). The load capacitors of C1 and C2 must be provided by external capacitors and their load capacitance depends on the crystal or resonator manufacturers' recommendation. Check the crystal datasheet for the recommended values. And, also consider the parasitic capacitance of package and board.

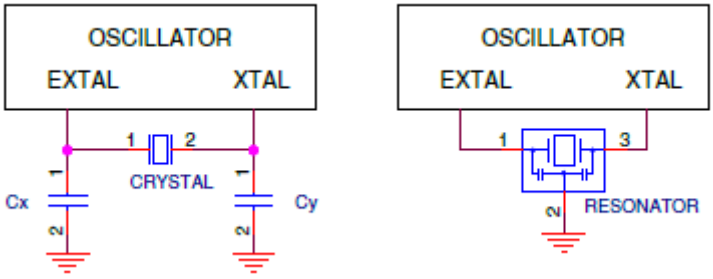


Figure 2. Crystal circuit design – Diagram 2

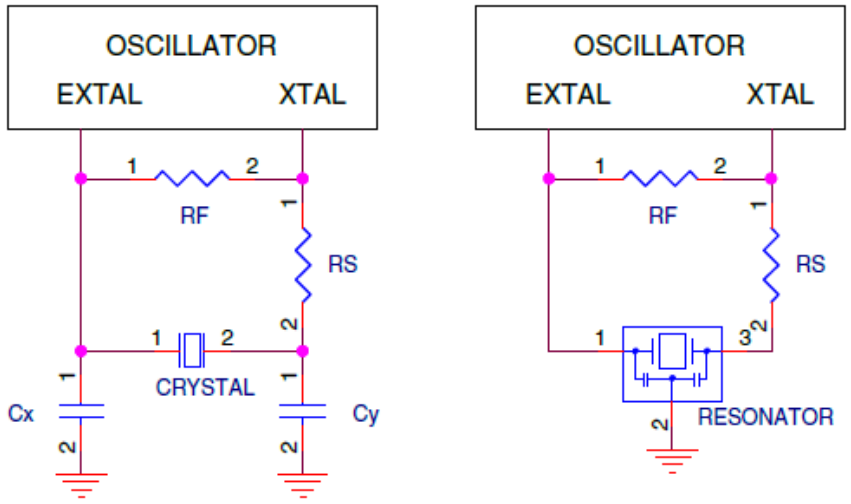


Figure 3. Crystal circuit design – Diagram 3

3.2 EMC considerations

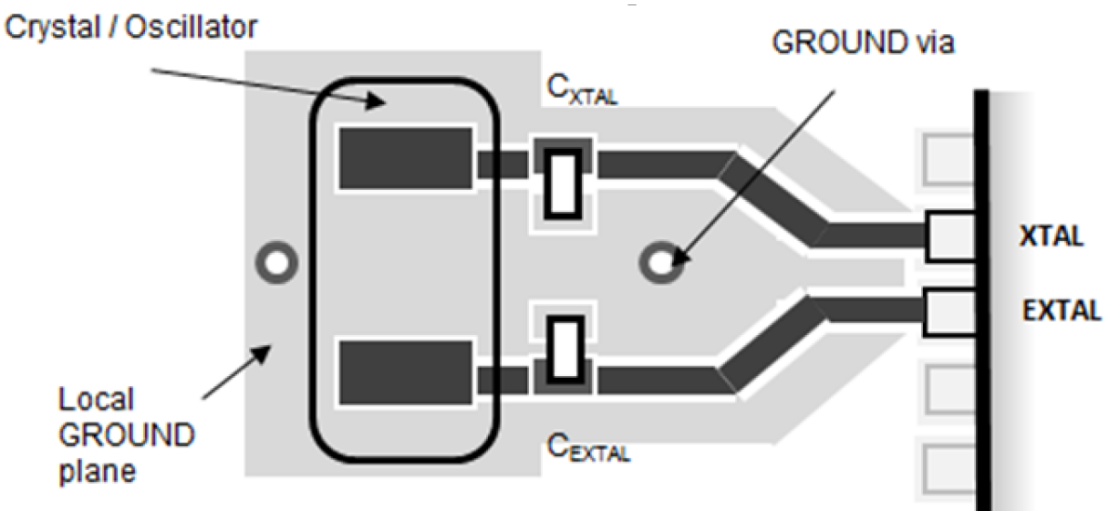
As the clock circuit is very sensitive to the noise, you need to pay attention to the following guidelines on PCB layout:

Avoid placing any signal traces close to the clock circuit.

Place the external crystal to the EXTAL/XTAL pins as close as possible.

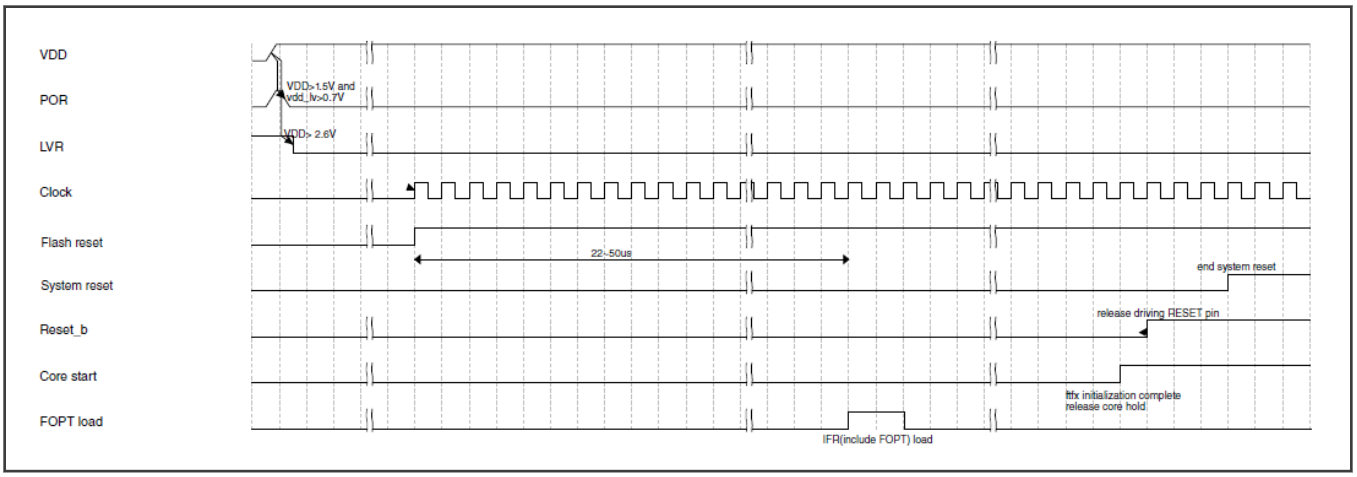
A ground area should be placed under the crystal oscillator area. This ground guard ring must be clean ground. This means that no current from and to other devices should be flowing through the guard ring. This guard ring should be connected to VSS with a short trace. Never connect the ground guard ring to any other ground signal on the board. Also avoid implementing ground loops.

The following figure shows the recommended placement and routing for the oscillator layout.

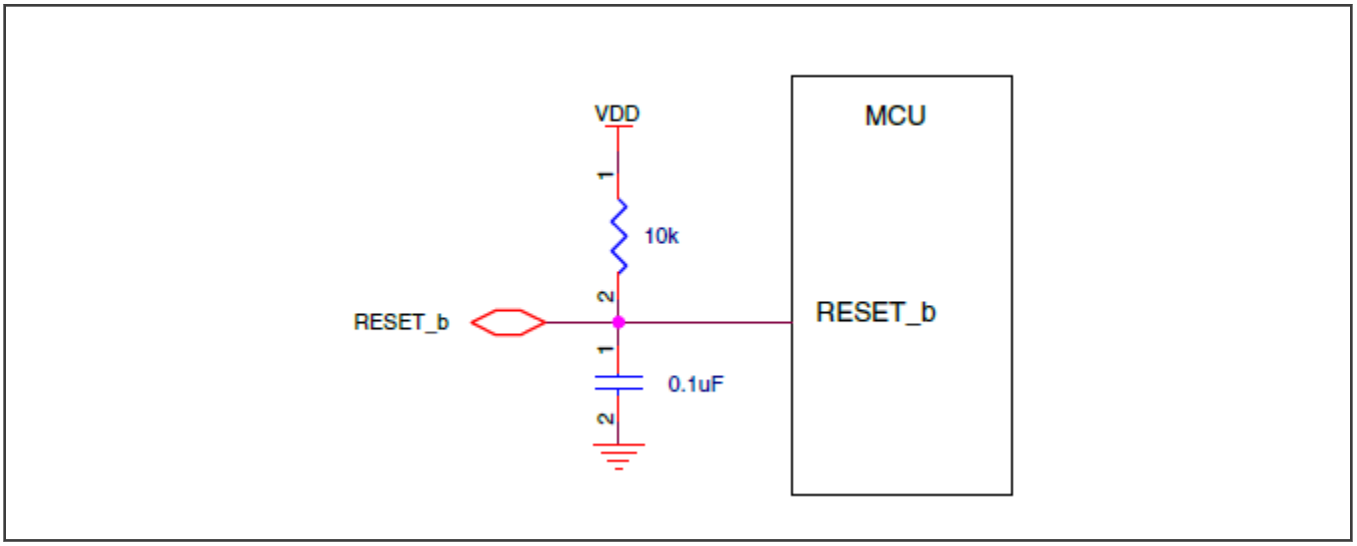


Chapter 4
Reset Circuit

Resetting the MCU provides a way to start processing from a known set of initial conditions. System reset begins with the on-chip regulator in full regulation and system clocking generation from an internal reference.



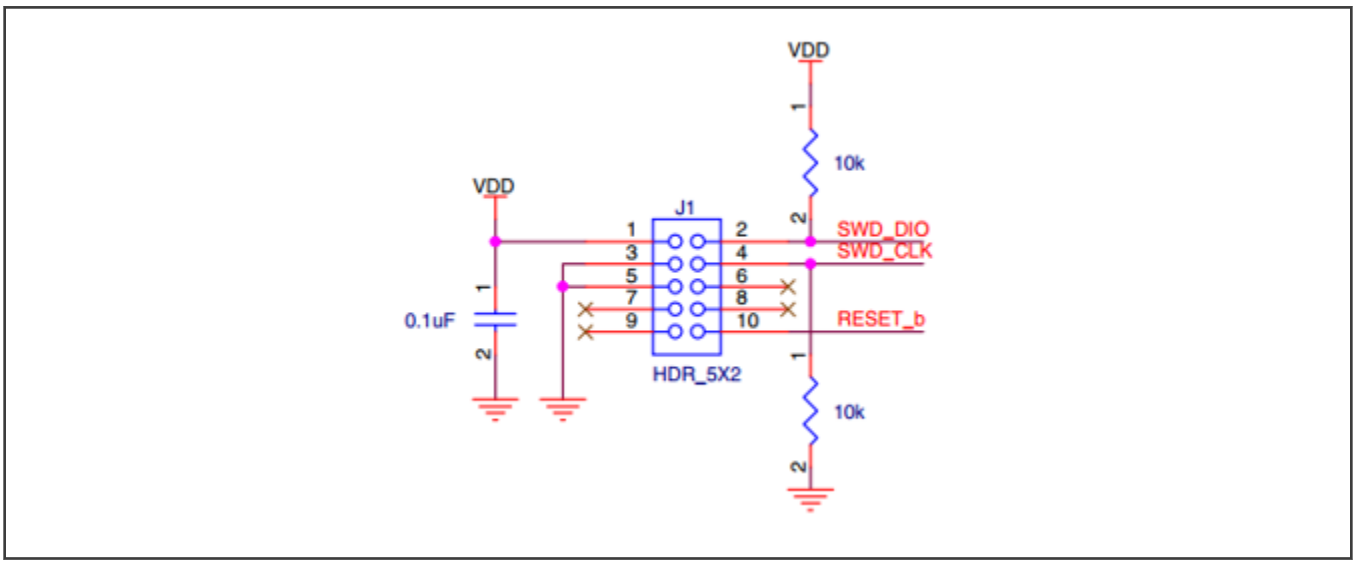
For all reset sources, the RESET_B pin is driven low by the MCU for at least 128 bus clock cycles and until the flash memory initialization is completed. After flash memory initialization completes, the RESET_B pin is released and the internal chip reset is deasserted. Keeping the RESET_B pin asserted externally delays the negation of the internal chip reset. The detailed boot sequence is shown in the figure above.



As shown in the schematic example figure, the reset circuit consists of an external pullup resistor added between reset pin to power supply, a capacitor between the reset pin to ground, and an optional reset button.

Chapter 5
Debug and Programming Interface

This MCU uses the standard Arm SWD interface protocol as shown in the following figure. While pull-up or pull-down resistors are not required (`SWD_DIO` has an internal pull-up and `SWD_CLK` has an internal pull-down), external 10 kΩ pull resistors are recommended for system robustness. The `RESET_b` pin recommendations mentioned above must also be considered.



Chapter 6
Touch Sensing Input

Touch sensing input (TSI) provides touch sensing detection on capacitive touch sensors. The external capacitive touch sensor is typically formed on PCB and the sensor electrodes are connected to TSI input channels through the I/O pins in the device.

KE17Z TSI supports dual TSI modules and each TSI module supports two kinds of touch sensing method, the self-capacitive mode and the mutual-capacitive mode.

6.1 TSI self-capacitive mode design considerations

The self-capacitive mode requires single pin for each touch sensor and measures the capacitance on an electrode connected to a single TSI channel. It then converts the capacitance into a digital count by driving average current on the electrode and measuring the charge/discharge times.

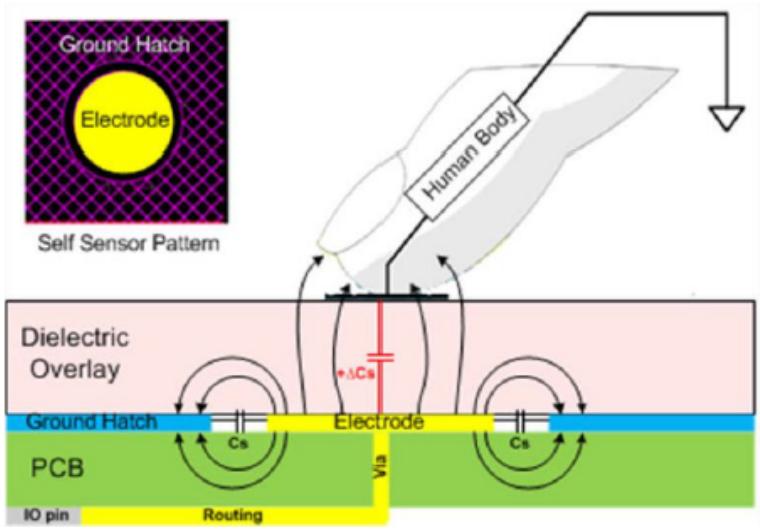
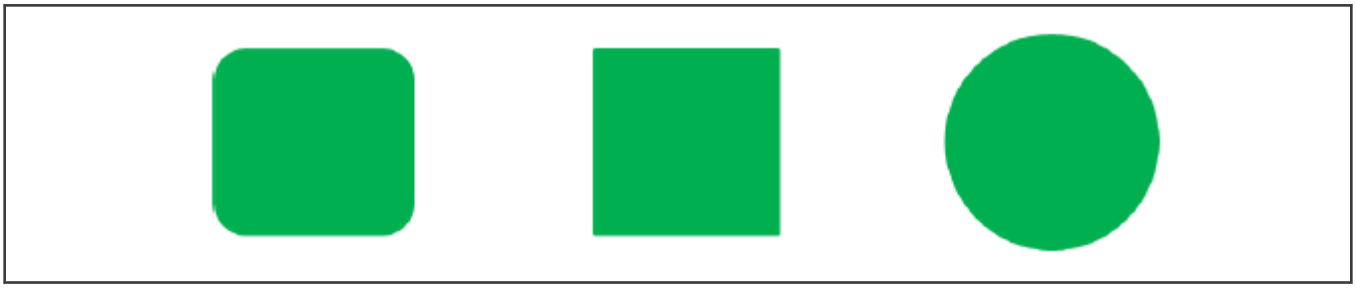


Figure 4. PCB layout of the electrode shapes for TSI self-capacitive mode

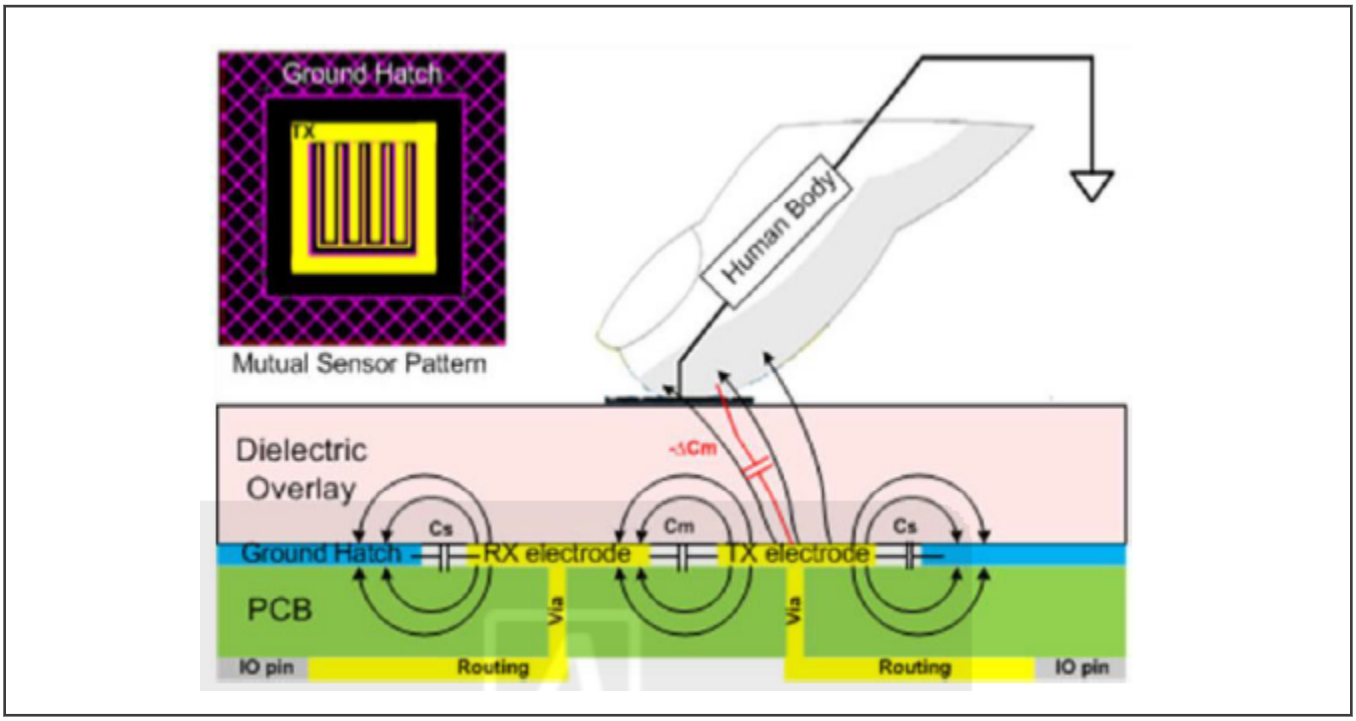
To maximize the electrodes area from the capacitor plates, it is recommended that the size of the electrode is similar to a human finger (10×10 mm is considered a good size).



6.2 TSI mutual capacitive mode design considerations

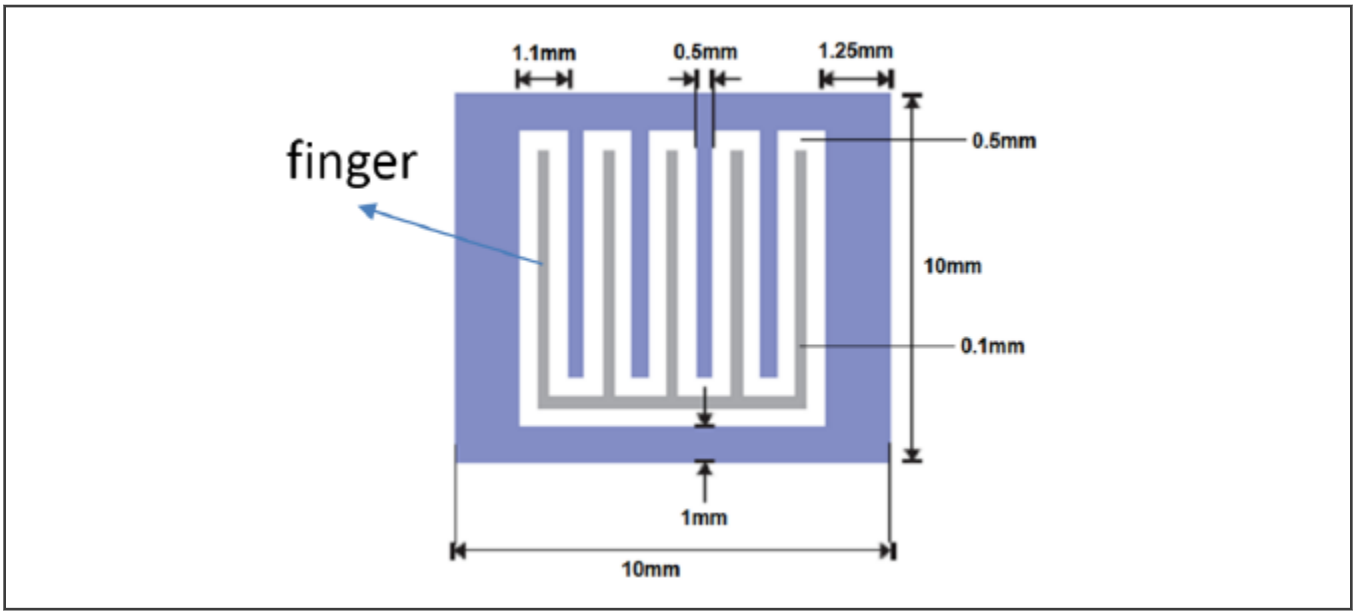
Mutual capacitive mode measures the capacitance between two electrodes connected to two TSI channels. One of the TSI channels is used as transmit (TX) channel and the other one is used as receive (RX) channel.

Figure below shows the connections of TSI channel in mutual-capacitive mode.



6.3 PCB layout of the electrode shapes for TSI mutual capacitive mode

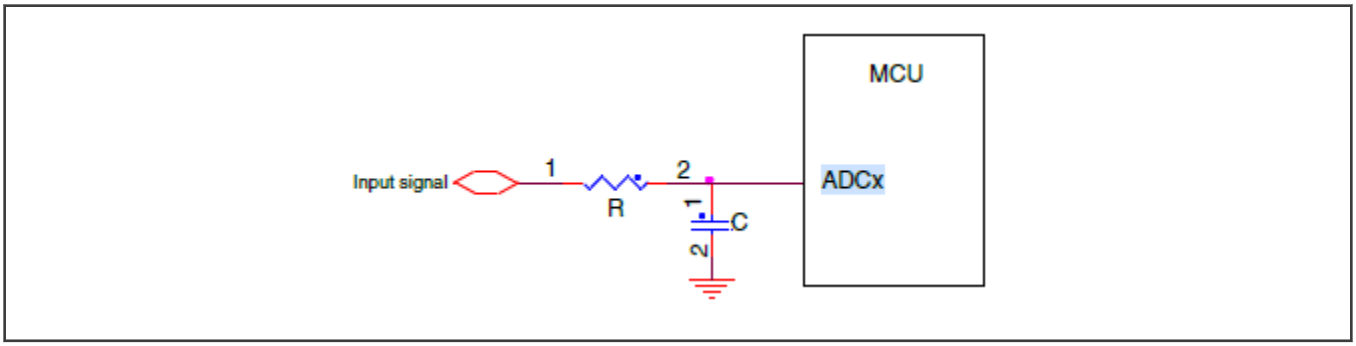
The following figure is the recommended mutual key shape. Note that the number of fingers has much impact on the touch sensitivity. In general, more fingers result in stronger noise immunity but less touch sensitivity. Customer should select the right finger numbers for the thickness of touch overlay. For example, if the touch overlay is 3 mm in thickness, 4 fingers is the best choice. If the touch overlay is 2 mm in thickness, 5 fingers are ok.



For the detailed TSI design guide, see KE15ZTSIUG, KE15Z Touch Sensing Interface User Guide.

Chapter 7
ADC Input Circuit

Each ADC input must have an RC filter as shown in the following figure. The maximum value of the resistor must be less than R_S (maximum 5 kohm as shown in the table below) if fast sampling and high resolution are required. The value of C must be chosen to ensure that the RC time constant is very small compared to the sample period. For example, the typical filter resistor is 100 ohm, together with the 220 pF capacitor, the low-pass cutoff frequency is 7.238 MHz.



The specifications of ADC input impedance and operating conditions are shown below for your reference.

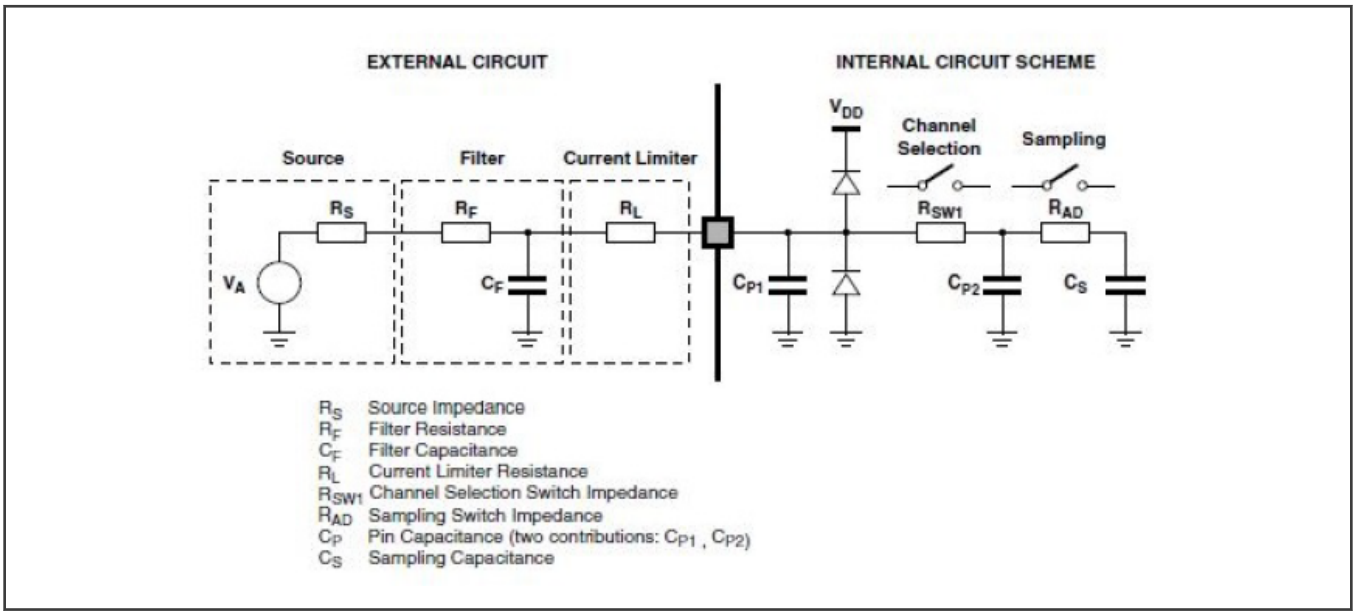


Table 5. 12-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	2.7	—	5.5	V	
ΔV_{DDA}	Supply voltage	Delta to V_{DD} (V_{DD} – V_{DDA})	-100	0	+100	mV	[2]
ΔV_{SSA}	Ground voltage	Delta to V_{SS} (V_{SS} – V_{SSA})	-100	0	+100	mV	[2]

Table continues on the next page...

Table 5. 12-bit ADC operating conditions (continued)

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{REFH}	ADC reference voltage high		2.5	V_{DDA}	V_{DDA} + 100m	V	[3]
V_{REFL}	ADC reference voltage low		− 100	0	100	mV	[3]
V_{ADIN}	Input voltage		V_{REFL}	—	V_{REFH}	V	
R_S	Source impedendance	f_{ADCK} < 4 MHz	—	—	5	kΩ	
R_{SW1}	Channel Selection Switch Impedance		—	0.5	1.2	kΩ	
R_{AD}	Sampling Switch Impedance		—	2	5	kΩ	
C_{P1}	Pin Capacitance		—	3	—	pF	
C_{P2}	Analog Bus Capacitance		—	—	5	pF	
C_S	Sampling capacitance		—	4	5	pF	
f_{ADCK}	ADC conversion clock frequency		2	40	50	MHz	[4,5]
C_{rate}	ADC conversion rate	No ADC hardware averaging[6] Continuous conversions enabled, subsequent conversion time	20	—	1200	Ksps	[7]

1. Typical values assume V_{DDA} = 5 V, Temp = 25 °C, f_{ADCK} = 40 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. For packages without dedicated V_{REFH} and V_{REFL} pins, V_{REFH} is internally tied to V_{DDA}, and V_{REFL} is internally tied to V_{SSA}.
4. Clock and compare cycle need to be set according the guidelines in the block guide.
5. ADC conversion will become less reliable above maximum frequency.
6. When using ADC hardware averaging, refer to the device *Reference Manual* to determine the most appropriate setting for AVGS.
7. Max ADC conversion rate of 1200 Ksps is with 10-bit mode

Chapter 8
Digital GPIO and Unused Pin

For the detailed IO pin mux functions and pinout, see "Section 4 Pinouts" in KE1xZP100M72SF1, Kinetis KE17Z/13Z/12Z with up to 256 KB Flash Data Sheet.

Regarding IO drive strength, there are 8 high drive pins with 20 mA drive strength. These high drive pins are: PTD0, PTD1, PTD15, PTD16, PTB4, PTB5, PTE0, and PTE1. In practice, keep the total output current for all ports under 100 mA as specified in Data Sheet.

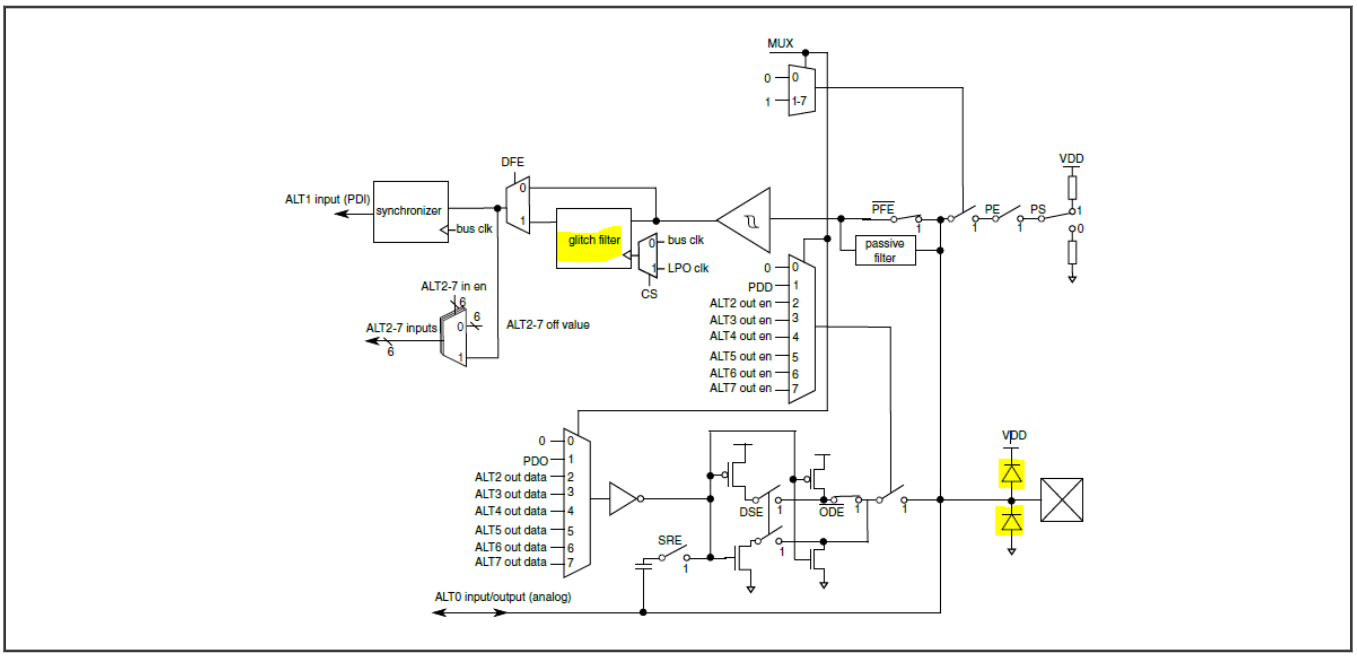
Regarding the switching terms, the minimum positive voltage applied to the input which will be accepted by the device as a logic high (V_{IH}) is 0.7*VDD, and the maximum positive voltage applied to the input which will be accepted by the device as a logic low (V_{IL}) is 0.3*VDD. They are also listed in the Data Sheet.

On reset, the most digital GPIOs (excepting debugging pins) are Disabled/Hi-z by default.

8.1 EMC considerations

The general IO block diagram is shown below. As port E supports the glitch filter feature, it's recommended to use port E pins as the digital input pins, with better noise immunity by enabling the glitch filter feature.

There is a pair of ESD protecting diodes on each IO pin, so the user doesn't need to add the extra ESD diode.



8.2 NMI pin considerations

After reset, the default function of PTD3 pin is NMI (no mask interrupt, low active). The software can configure the pin as other functions only after the reset completes and begins to execute the application code. Therefore, note that the NMI pin cannot be low level at reset, otherwise the code will be stuck in NMI interrupt service routine. In practice, keep the NMI pin unused and unconnected (or pull up with 4.7 kohm resistor) if there is enough pin to use.

8.3 Unused pin considerations

In order to improve EMC noise immunity and reduce the current consumption, the used pins are suggested to keep unconnected and the software should configure these unused pins as DISABLED, which is the default pin status after reset.

Chapter 9
General Board Layout Guidelines

For the detailed general board layout guidelines, see "Chapter 10" in AN5426, Hardware Design Guidelines for S32K1xx Microcontrollers.

Appendix A
Revision History

The table below summarizes the revisions to this document.

Table 6. Revision history

Revision	Date	Topic cross-reference	Change description
0.1	13 December 2021	Overview	Fixed cross-references
0	9 December 2021		Initial public release

How To Reach Us

Home Page:

nxp.com

Web Support:

nxp.com/support

Limited warranty and liability — Information in this document is provided solely to enable system and software implementers to use NXP products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document. NXP reserves the right to make changes without further notice to any products herein.

NXP makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does NXP assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. “Typical” parameters that may be provided in NXP data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including “typicals,” must be validated for each customer application by customer's technical experts. NXP does not convey any license under its patent rights nor the rights of others. NXP sells products pursuant to standard terms and conditions of sale, which can be found at the following address: nxp.com/SalesTermsandConditions.

Right to make changes - NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Security — Customer understands that all NXP products may be subject to unidentified or documented vulnerabilities. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer’s applications and products. Customer’s responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer’s applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately. Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

For more information, please visit: http://www.nxp.com

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 13 December 2021

Document identifier: KE17ZHDG

arm

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

NXP:

FRDM-KE17Z