

# BMI7018

## 18-cell battery-cell controller IC

Rev. 1.0 — 23 September 2024

Product data sheet

## 1 General description

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The BMI7018 is a lithium-ion battery-cell controller IC. It can be used in industrial applications, such as energy storage systems (ESS) and uninterruptible power supply (UPS) systems.

The BMI7018 offers transport protocol link (TPL3 - proprietary isolated daisy chain protocol of NXP) and Serial Peripheral Interface (SPI) for communication with the host microcontroller unit (MCU).

These devices support high precision cell voltage and temperature measurements along with various cell voltage balancing strategies. Aside from a SPI interface to enable direct communication with the host MCU, they provide alternatively a daisy chain communication interface which supports capacitive and inductive isolation between nodes.



## 2 Features and benefits

- Ambient temperature range: from  $-20^{\circ}\text{C}$  to  $+60^{\circ}\text{C}$
- Support for cell-voltage and cell-temperature measurements from the host MCU to the cell
- Cell voltage measurement
  - 4 to 18 cells per device
  - Operating voltage range from 9 V to 90 V
  - Supports bus bars voltage measurement with -3 V to +5 V input voltage
  - 16-bit resolution and up to  $\pm 0.8$  mV typical measurement accuracy with ultra low long-term drift
  - Integrated configurable digital filter
- External temperature and auxiliary voltage measurements
  - One analog input for absolute measurement, 5 V input range
  - Eight analog inputs configurable as absolute or ratiometric, 5 V input range
  - 16-bit resolution and  $\pm 5$  mV typical measurement accuracy
  - Integrated configurable digital filter
- Internal measurement
  - Two redundant internal temperature sensors
  - Supply voltages
  - External transistor current
- Cell voltage balancing
  - 18 internal balancing field effect transistors (FET), up to 360 mA peak with  $0.5\ \Omega\ R_{\text{DSon}}$  per channel (typ.)
  - Support for simultaneous passive balancing of all channels with automatic odd/even sequence
  - Global balancing timeout timer
  - Timer controlled balancing with individual timers with 10 s resolution and up to 45 h duration
  - Voltage controlled balancing with global and individual undervoltage thresholds
  - Temperature controlled balancing; if balancing resistors or the IC are in overtemperature, balancing is interrupted
  - Configurable pulse width modulation (PWM) duty cycle balancing
  - Automatic pause of balancing during measurement with configurable filter settling time
  - Configurable delay of the start of balancing after transition to sleep
  - Automatic discharge of the battery pack (emergency discharge)
  - Constant current cell balancing to compensate the balancing current variation due to cell voltage variation
- I<sup>2</sup>C-bus leader interface to control external devices, for example, EEPROMs and security ICs
- Configurable alarm output
- Cyclic wake-up to monitor the pack and the balancing function during sleep.
- Capability to wake up the host MCU via daisy chain in case of a fault event.
- Host interface supporting SPI or isolated daisy chain communication (TPL3)
  - 2 Mbit/s data rate for TPL interface
  - 4 Mbit/s data rate for SPI interface
- TPL3 daisy chain communication supports
  - Two-wire daisy chain with capacitive or inductive isolation
  - Protocol supporting up to six daisy chains and 62 nodes per chain
- Unique device ID with dynamic addressing
- Operation modes
  - Active mode FP (12 mA typ.)
  - Sleep mode LP (60  $\mu\text{A}$  typ.)
  - Deep Sleep mode ULP (15  $\mu\text{A}$  typ.)

### 3 Applications

#### 3.1 Industrial

- Energy storage systems (ESS)
- Uninterruptible power supply (UPS)

### 4 Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
MBMI7018	LQFP64	Plastic, thermal enhanced low profile quad flat package; 64 terminals; 0.50 mm pitch; 10 x 10 x 1.4 mm body	SOT1510-2

#### 4.1 Ordering options

Table 2. Part numbers

Type number	Description
MBMI7018TA1AE	TPL interface
MBMI7018SA1AE	SPI interface

5 Block diagram

Figure 1 shows the general architecture of the BMI7018.

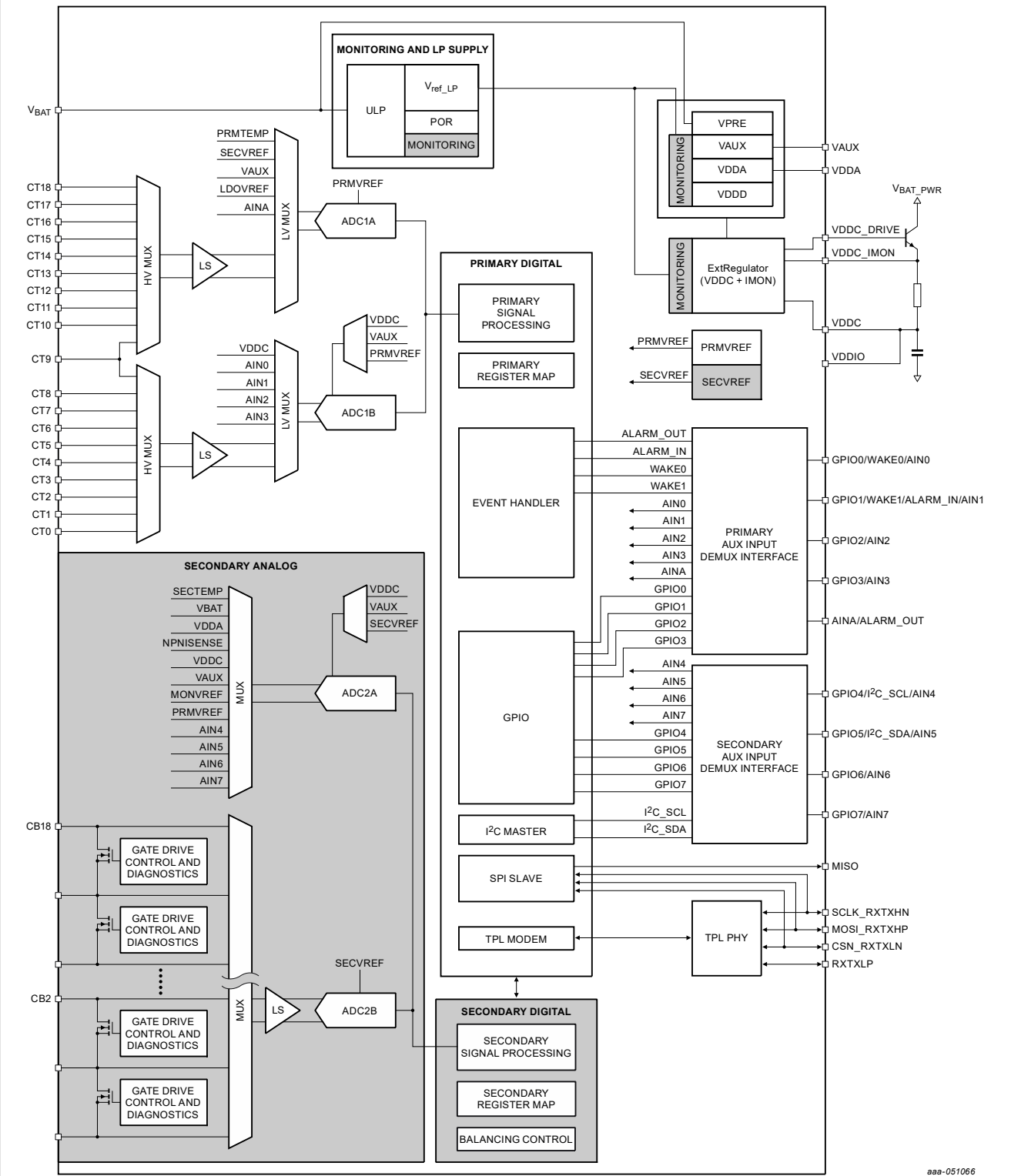
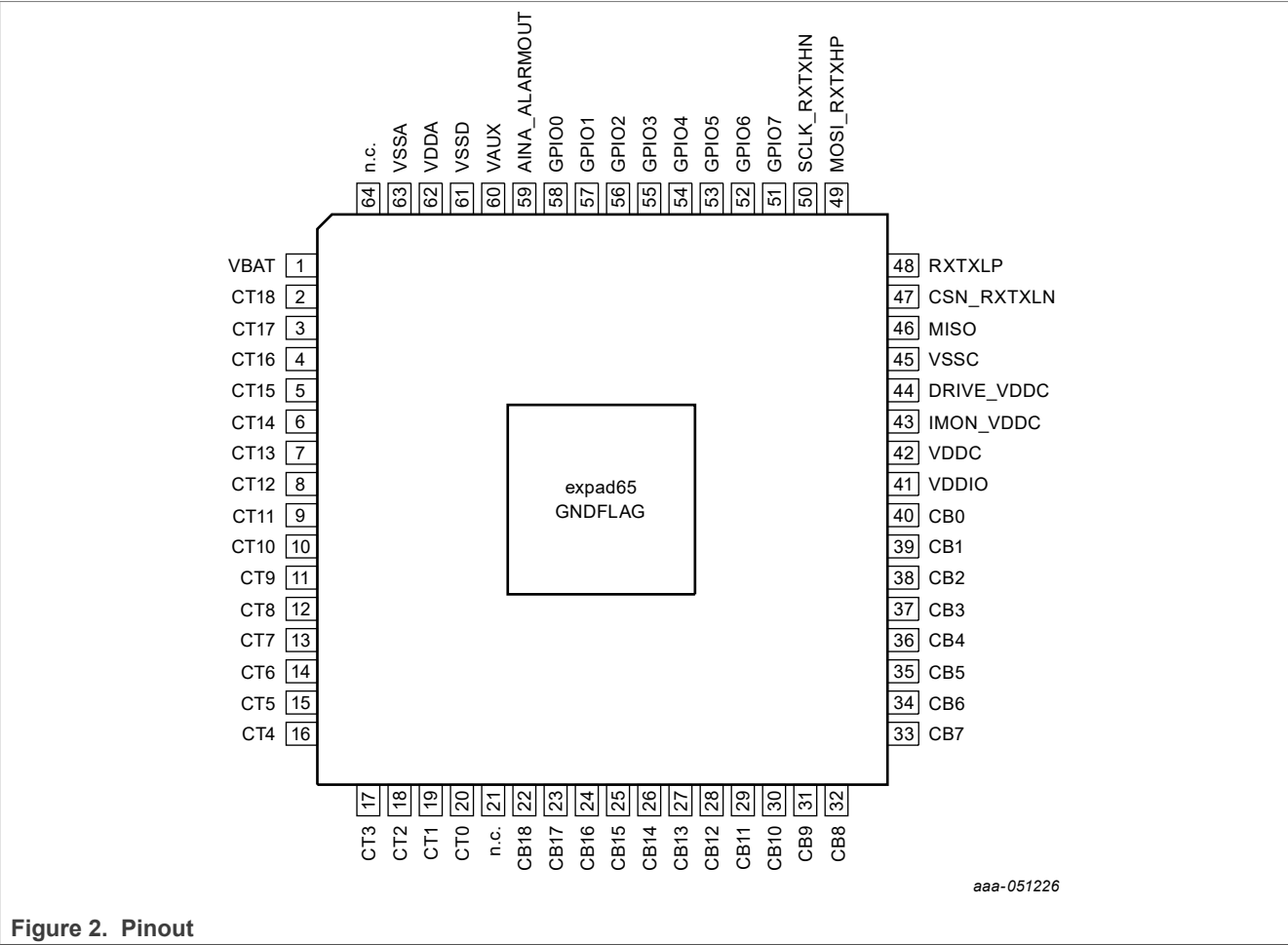


Figure 1. Simplified internal block diagram

6 Pinning information

6.1 Pinout diagram



6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
VBAT	1	Supply input of the product.
CT18	2	Cell terminal 18 input.
CT17	3	Cell terminal 17 input.
CT16	4	Cell terminal 16 input.
CT15	5	Cell terminal 15 input.
CT14	6	Cell terminal 14 input.
CT13	7	Cell terminal 13 input.
CT12	8	Cell terminal 12 input.
CT11	9	Cell terminal 11 input.
CT10	10	Cell terminal 10 input.

Table 3. Pin description...continued

Symbol	Pin	Description
CT9	11	Cell terminal 9 input.
CT8	12	Cell terminal 8 input.
CT7	13	Cell terminal 7 input.
CT6	14	Cell terminal 6 input.
CT5	15	Cell terminal 5 input.
CT4	16	Cell terminal 4 input.
CT3	17	Cell terminal 3 input.
CT2	18	Cell terminal 2 input.
CT1	19	Cell terminal 1 input.
CT0	20	Cell terminal 0 input.
n.c.	21	Not connected.
CB18	22	Secondary cell terminal 18 input 1. High input for cell 17 balancing
CB17	23	1. Secondary cell terminal 17 input 2. Low input for cell 17 balancing 3. High input for cell 16 balancing
CB16	24	1. Secondary cell terminal 16 input 2. Low input for cell 16 balancing 3. High input for cell 15 balancing
CB15	25	1. Secondary cell terminal 15 input 2. Low input for cell 15 balancing 3. High input for cell 14 balancing
CB14	26	1. Secondary cell terminal 14 input 2. Low input for cell 14 balancing 3. High input for cell 13 balancing
CB13	27	1. Secondary cell terminal 13 input 2. Low input for cell 13 balancing 3. High input for cell 12 balancing
CB12	28	1. Secondary cell terminal 12 input 2. Low input for cell 12 balancing 3. High input for cell 11 balancing
CB11	29	1. Secondary cell terminal 11 input 2. Low input for cell 11 balancing 3. High input for cell 10 balancing
CB10	30	1. Secondary cell terminal 10 input 2. Low input for cell 10 balancing 3. High input for cell 9 balancing
CB9	31	1. Secondary cell terminal 9 input 2. Low input for cell 9 balancing 3. High input for cell 8 balancing
CB8	32	1. Secondary cell terminal 8 input 2. Low input for cell 8 balancing 3. High input for cell 7 balancing
CB7	33	1. Secondary cell terminal 7 input 2. Low input for cell 7 balancing 3. High input for cell 6 balancing

Table 3. Pin description...continued

Symbol	Pin	Description
CB6	34	<ol style="list-style-type: none"> <li>1. Secondary cell terminal 6 input</li> <li>2. Low input for cell 6 balancing</li> <li>3. High input for cell 5 balancing</li> </ol>
CB5	35	<ol style="list-style-type: none"> <li>1. Secondary cell terminal 5 input</li> <li>2. Low input for cell 5 balancing</li> <li>3. High input for cell 4 balancing</li> </ol>
CB4	36	<ol style="list-style-type: none"> <li>1. Secondary cell terminal 4 input</li> <li>2. Low input for cell 4 balancing</li> <li>3. High input for cell 3 balancing</li> </ol>
CB3	37	<ol style="list-style-type: none"> <li>1. Secondary cell terminal 3 input</li> <li>2. Low input for cell 3 balancing</li> <li>3. High input for cell 2 balancing</li> </ol>
CB2	38	<ol style="list-style-type: none"> <li>1. Secondary cell terminal 2 input</li> <li>2. Low input for cell 2 balancing</li> <li>3. High input for cell 1 balancing</li> </ol>
CB1	39	<ol style="list-style-type: none"> <li>1. Secondary cell terminal 1 input</li> <li>2. Low input for cell 1 balancing</li> <li>3. High input for cell 0 balancing</li> </ol>
CB0	40	<ol style="list-style-type: none"> <li>1. Secondary cell terminal 0 input</li> <li>2. Low input for cell 0 balancing</li> </ol>
VDDIO	41	External VDDIO supply input.
VDDC	42	External VDDC supply input.
IMON_VDDC	43	External NPN monitoring input.
DRIVE_VDDC	44	External NPN base output.
VSSC	45	VDDIO and VDDC ground reference.
MISO	46	SPI follower data output to leader.
CSN_RXTXLN	47	<ol style="list-style-type: none"> <li>1. SPI chip select input from leader</li> <li>2. TPLRX negative input from lower node</li> <li>3. TPLTX negative output to lower node if not used to be tied to GND through a pulldown resistor</li> </ol>
RXTXLP	48	<ol style="list-style-type: none"> <li>1. TPLRX positive input from lower node</li> <li>2. TPLTX positive output to lower node if not used to be tied to GND through a pulldown resistor</li> </ol>
MOSI_RXTXHP	49	<ol style="list-style-type: none"> <li>1. SPI follower data input from leader</li> <li>2. TPLRX positive input from upper node</li> <li>3. TPLTX positive output to upper node if not used to be tied to GND through a pulldown resistor</li> </ol>
SCLK_RXTXHN	50	<ol style="list-style-type: none"> <li>1. SPI clock input from leader</li> <li>2. TPLRX negative input from upper node</li> <li>3. TPLTX negative output to upper node if not used to be tied to GND through a pulldown resistor</li> </ol>
GPIO7	51	<ol style="list-style-type: none"> <li>1. Analog input AIN7 for ratiometric measurement to VAUX/VDDC</li> <li>2. Analog input AIN7 for absolute measurement</li> <li>3. General-purpose input 7</li> <li>4. General-purpose output 7 if not used to be tied to GND</li> </ol>

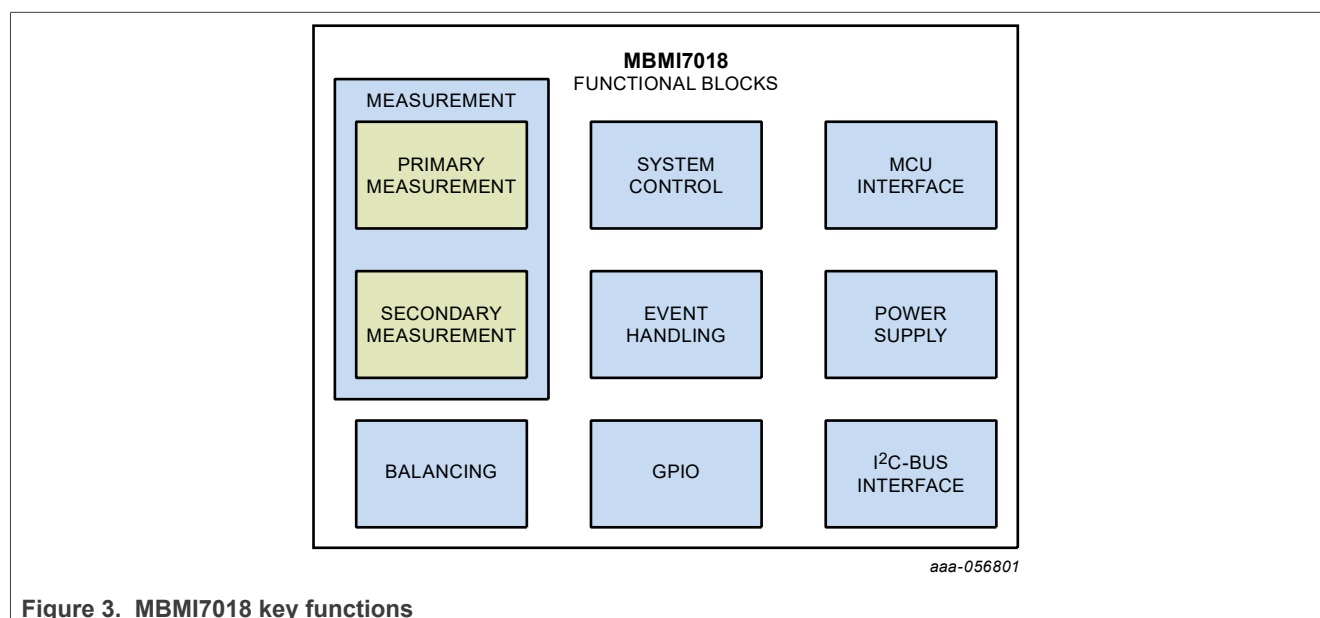
Table 3. Pin description...continued

Symbol	Pin	Description
GPIO6	52	<ol style="list-style-type: none"> <li>1. Analog input AIN6 for ratiometric measurement to VAUX / VDDC</li> <li>2. Analog input AIN6 for absolute measurement</li> <li>3. General-purpose input 6</li> <li>4. General-purpose output 6 if not used to be tied to GND</li> </ol>
GPIO5	53	<ol style="list-style-type: none"> <li>1. Analog input AIN5 for ratiometric measurement to VAUX/VDDC</li> <li>2. Analog input AIN5 for absolute measurement</li> <li>3. General-purpose input 5</li> <li>4. General-purpose output 5</li> <li>5. I2CSDA if not used to be tied to GND</li> </ol>
GPIO4	54	<ol style="list-style-type: none"> <li>1. Analog input AIN4 for ratiometric measurement to VAUX/VDDC</li> <li>2. Analog input AIN4 for absolute measurement</li> <li>3. General-purpose input 4</li> <li>4. General-purpose output 4</li> <li>5. I2CSCL if not used to be tied to GND</li> </ol>
GPIO3	55	<ol style="list-style-type: none"> <li>1. Analog input AIN3 for ratiometric measurement to VAUX/VDDC</li> <li>2. Analog input AIN3 for absolute measurement</li> <li>3. General-purpose input 3</li> <li>4. General-purpose output 3 if not used to be tied to GND</li> </ol>
GPIO2	56	<ol style="list-style-type: none"> <li>1. Analog input AIN2 for ratiometric measurement to VAUX/VDDC</li> <li>2. Analog input AIN2 for absolute measurement</li> <li>3. General-purpose input 2</li> <li>4. General-purpose output 2 if not used to be tied to GND</li> </ol>
GPIO1	57	<ol style="list-style-type: none"> <li>1. Analog input AIN1 for ratiometric measurement to VAUX/VDDC</li> <li>2. Analog input AIN1 for absolute measurement</li> <li>3. General-purpose input 1</li> <li>4. General-purpose output 1</li> <li>5. Wake-up input 1</li> <li>6. Alarm input if not used to be tied to GND</li> </ol>
GPIO0	58	<ol style="list-style-type: none"> <li>1. Analog input AIN0 for ratiometric measurement to VAUX/VDDC</li> <li>2. Analog input AIN0 for absolute measurement</li> <li>3. General-purpose input 0</li> <li>4. General-purpose output 0 if not used to be tied to GND</li> <li>5. Wake-up input 0</li> </ol>
AINA_ALARMOUT	59	<ol style="list-style-type: none"> <li>1. Analog input AINA for absolute measurement</li> <li>2. Alarm output if not used to be tied to GND</li> </ol>
VAUX	60	Supply output for external sensors.
VSSD	61	Digital ground.
VDDA	62	Internal analog supply. Should be connected to a 100nF capacitor. Should not be used for application.
VSSA	63	Analog ground.
n.c.	64	Not connected.
GNDFLAG	Expad 65	Grounded exposed pad.



## 7 Functional description

The BMI7018 is a lithium-ion battery-cell controller IC designed for industrial applications. The key functions of the BMI7018 are shown in [Figure 3](#).



The [System control](#) block defines the operational state and the basic configuration of the device.

The [Event handling](#) block configures the behavior of the device as response to events such as faults, wake-up, and alarms.

The [Power supply](#) section contains information about the power supply of the IC and the external supplies the BMI7018 offers.

The BMI7018 can measure and balance up to 18 battery cells. The measurement block, containing the primary and secondary measurements, is described in [Section 7.4 "Measurement"](#). [Section 7.5 "Cell balancing"](#) contains information about the cell balancing functionality.

The BMI7018 provides eight general-purpose input/output (GPIO) pins. The GPIO ports can be used for several purposes, such as interrupt pins or to implement an I<sup>2</sup>C-bus interface. See [Section 7.6 "GPIO pins"](#) for details about the GPIO pins and [Section 7.8 "I<sup>2</sup>C-bus interface"](#) for details on the I<sup>2</sup>C-bus interface.

Communication between the superior control unit and the BMI7018 is established via TPL or SPI by the [microcontroller interface](#).

### 7.1 System control

The system control function block controls the operating modes of the device and, along with the operation mode, the availability of the various supply voltages described in [Section 7.3](#).

#### 7.1.1 Operation modes

The device offers four different operation modes.

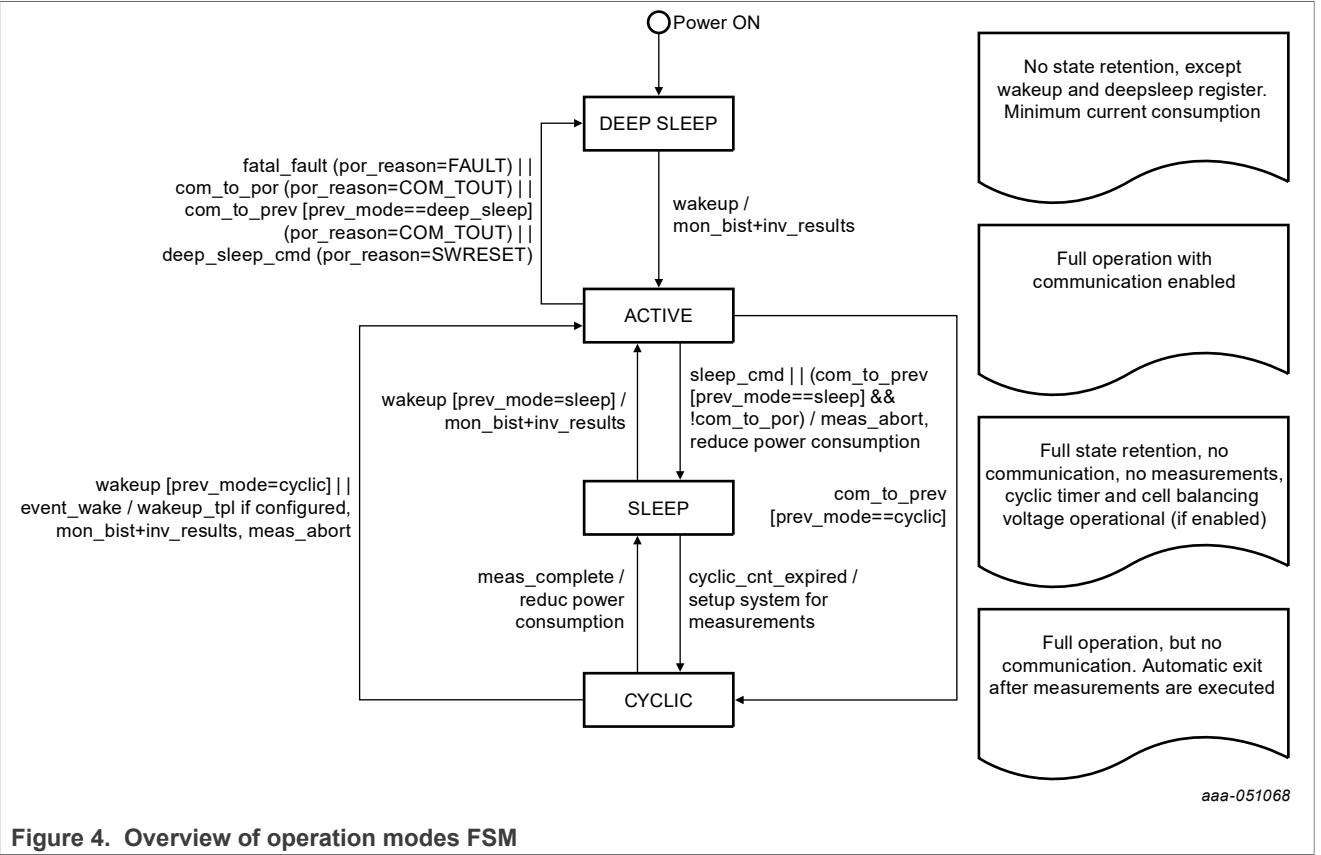


Figure 4. Overview of operation modes FSM

Table 4. Explanation of symbols

Name	Documentation
meas_abort	Abort measurement if currently ongoing.
wakeup_tpl	Send TPL wake-up frame.
reset	Reset and initialize IC.
mon_bist + inv_results	Run supply monitor BIST and set all measurement result registers to invalid.
com_to_por	Communication timeout occurred and timeout reaction is configured to POR.
com_to_prev	Communication timeout occurred and timeout reaction is configured to transition back to previous mode.
cyclic_cnt_expired	Cyclic wake-up counter has expired.
event_wake	An event configured for wake-up occurred: internal events configurable for wake-up, i.e., OV/UV events, or configurable external wake-up sources, i.e., GPIO wake-up pin.
fatal_fault	A fatal internal fault occurred or an internal event that is configured to trigger a POR occurred.
sleep_cmd	SW command to transition to sleep (SYS_MODE register).
deep_sleep_cmd	SW command to transition to deep sleep (SYS_MODE register).
wakeup	Wake-up event on the MCU interface detected.
prev_mode	Previous mode before transition.
por_reason	FEH_POR_REASON register.
meas_complete	Measurement cycle completed.

Each operation mode has different features and power consumptions associated with it.

Table 5. Operation modes

Operation mode	Behavior	Application usage
Deep sleep (ULP)	Device is off; activation possible only via communication.	Storage mode and default mode after reset.
Sleep (LP)	Low-power operation mode.	Inactive mode, for example, parking of the vehicle; cell balancing possible.
Active	All functions enabled; full performance of device.	Monitoring of the battery.
Cyclic	Device switches automatically between Sleep mode and Active mode.	Balancing while parking of a vehicle.

### 7.1.1.1 Deep Sleep mode

In Deep Sleep mode, the device is offering the lowest current consumption. Deep Sleep mode is entered automatically after a power-on reset. The device remains in Deep Sleep mode until it detects bus activity. Other wake-up sources are disabled. The deep sleep storage data registers (SYS\_DS\_STORAGE0 and SYS\_DS\_STORAGE1) retain their current information. The register FEH\_POR\_REASON contains the information about the reason for entering Deep Sleep mode. All other registers are reset.

Setting the bit field SYS\_MODE.TARGETMODE to DEEPSLEEP (14h) initiates the transition to Deep Sleep mode. This bit field must be set with a message that accesses only the SYS\_MODE.TARGETMODE register.

**Note:** Single-register access is achieved by setting DATALEN to 00b. See [Section 7.9.1.1 "TPL3 message structure"](#) for details.

### 7.1.1.2 Sleep mode

In Sleep mode, the current consumption is very low. The device monitors the wake-up sources, but does not perform ADC conversions. Balancing is possible in Sleep mode. The register content of the [cell balancing registers](#), the [system control registers](#), the [event handling registers](#), and the [primary measurement register](#) remain valid. All other registers are reset. With the SYS\_CYC\_WAKEUP\_CFG register set to 0000h, the BMI7018 remains in Sleep mode until a transition to Active mode is initiated. With SYS\_CYC\_WAKEUP\_CFG register set to a value other than 0000h the device automatically changes between Sleep and Cyclic modes.

The sequence to enter Sleep mode in a controlled way is:

1. Read undervoltage and overvoltage status bits to confirm system integrity.
2. Disable the measurement (measurement results are invalidated).
3. Read undervoltage and overvoltage status bits and discard the results.
4. Read FEH\_WAKEUP\_REASON to ensure no wake-up events are pending.
5. Send go-to-sleep command.

Setting the bit field SYS\_MODE.TARGETMODE to SLEEP (0Ah) initiates the transition to Sleep mode. This bit field must be set with a message that accesses only the SYS\_MODE.TARGETMODE register.

**Note:** Single-register access is achieved by setting DATALEN to 00b. See [Section 7.9.1.1 "TPL3 message structure"](#) for details.

### 7.1.1.3 Active mode

In Active mode, the device is fully operational. When entering Active mode, all measurement results are invalidated. A [BIST](#) is executed when entering into Active mode to check the integrity of the device.

#### 7.1.1.4 Cyclic mode

Cyclic mode is entered via Sleep mode with SYS\_CYC\_WAKEUP\_CFG register set to a value other than 0000h. The device automatically transitions between cyclic and sleep states. In the cyclic state, BMI7018 executes one periodic measurement ([Section 7.4.3.1 "Periodic measurement"](#)) and evaluates the results for undervoltage and overvoltage conditions. After the evaluation, it either returns to Sleep mode or wakes up if any of the configured wake-up events ([Section 7.2.2 "Events"](#)) has been detected. The bit field SYS\_CYC\_WAKEUP\_CFG.PERIOD configures the cycle time.

**Note:** The BMI7018 manages the MEASEN bit in Cyclic mode automatically.

### 7.1.2 System control features

#### 7.1.2.1 System configuration CRC

The BMI7018 contains many configuration registers. All of these registers can be read to verify the device configuration. The BMI7018 calculates a cyclic redundancy check (CRC) across the content of the configuration registers. The MCU can use this CRC value to validate the integrity of the configuration. The CRC is recalculated whenever a register covered by the CRC is written or the CRC value is read.

The system configuration CRC covers the SYS\_COM\_CFG, SYS\_COM\_TO\_CFG, SYS\_SUPPLY\_CFG, SYS\_CYC\_WAKEUP\_CFG, and SYS\_TPL\_CFG register.

The used polynomial is:  $D175h (+1) = X^{16} + X^{15} + X^{13} + X^9 + X^7 + X^6 + X^5 + X^3 + X^1 + 1$ .

**Notes:**

- The CRC value depends on the configuration of the device and is therefore application dependent.
- The polynomial used here is different to the polynomial used for communication.

Application usage: Check integrity of the system configuration.

#### 7.1.2.2 Communication, communication timeout configuration, and TPL configuration

The register SYS\_COM\_CFG contains the daisy chain and device address of the device, as well as the overall number of devices in the daisy chain.

The register SYS\_COM\_TO\_CFG configures the communication timeout of the device.

The register SYS\_TPL\_CFG configures the wake-up compatibility, termination, and response properties of the TPL ports.

The configuration applied here is used by the microcontroller interface. For a detailed description, see [Section 7.9 "Microcontroller interface"](#).

#### 7.1.2.3 Supply configuration

VDDC and VAUX are intended to supply the GPIO ports and sensor networks. The bits VDDCCYC and VAUXCYC in the SYS\_SUPPLY\_CFG register control the state of the VDDC and VAUX supplies in Cyclic mode. The bit VAUXACT controls the state of VAUX in Active mode.

The bit CURMATCH enables the supply current matching feature of the BMI7018. When the feature is enabled, the current consumption of the BMI7018 is within  $\Delta I_{BAT(FP)}$ .

#### 7.1.2.4 System mode and interval for cyclic measurements

The registers SYS\_MODE and SYS\_CYC\_WAKEUP\_CFG control the operation mode of the device and the interval for the cyclic measurements.

Application usage: State control and monitoring of the system voltages, for example, during balancing in Sleep mode.

7.1.2.5 Clock synchronization

With the register SYNCCNT, it is possible to adjust the internal clock of the BMI7018.

Application usage: Synchronize measurement timing between multiple BMI7018 devices.

7.1.2.6 System version

The SYS\_VERSION register provides information about the revision of the silicon.

Table 6. System version identification

TYPE	FREV	MREV	Product version
03h	9h	1h	BMI7018
Others			Reserved for future usage

Application usage: Identification of silicon revision.

7.1.2.7 Software interface information

The BMI7018 does not contain software, but provides some information about the compatibility between the register definitions of different product variants. The SYS\_PROD\_VER register allows a fast assessment whether software generated for a specific product version can be used for other product versions.

Table 7. Software interface information

Major	Minor	Patch	Silicon state
2h	0h	0h	

7.1.2.8 Unique device ID

The registers SYS\_UID\_LOW, SYS\_UID\_MID, and SYS\_UID\_HIGH provide together a unique identification value for each BMI7018.

Application usage: Identification of ICs for system integrity checks and tracking.

7.1.2.9 Deep sleep storage data

The registers SYS\_DS\_STORAGE0 and SYS\_DS\_STORAGE1 provide 32-bit data storage. The bits are not used by the BMI7018 and are free to be used in the overall application. The BMI7018 never clears the content of these registers. However, when the supply voltage for the BMI7018 is removed, the content of the register is lost. The register is not initialized at restart of the IC and may show any value.

Application usage: Storage of tracking data; storage of current class for contactor relays.

7.1.3 System control registers

All registers related to the system control are listed here. Details to the registers and the bit fields are explained in the register map section.

Table 8. Register overview: System\_Control\_Registers

Address	Name	Access	Reset	Description
0h	<a href="#">SYS_CFG_CRC</a>	R	0h	system configuration CRC
1h	<a href="#">SYS_COM_CFG</a>	R/W	200h	communication initialization
2h	<a href="#">SYS_COM_TO_CFG</a>	R/W	1Eh	system communication timeout
3h	<a href="#">SYS_SUPPLY_CFG</a>	R/W	8003h	supply configuration
4h	<a href="#">SYS_MODE</a>	R/W	1400h	system mode
5h	<a href="#">SYS_CYC_WAKEUP_CFG</a>	R/W	0h	interval for cyclic measurements
6h	<a href="#">SYS_TPL_CFG</a>	R/W	10h	TPL configuration
8h	<a href="#">SYS_CLK_SYNC_CTRL</a>	R/W	0h	clock Synchronization
10h	<a href="#">SYS_VERSION</a>	R	320h	device silicon identifier
11h	<a href="#">SYS_UID_LOW</a>	R	0h	unique device ID lower part
12h	<a href="#">SYS_UID_MID</a>	R	0h	unique device ID middle part
13h	<a href="#">SYS_UID_HIGH</a>	R	0h	unique device ID higher part
14h	<a href="#">SYS_PROD_VER</a>	R	200h	software interface related version of the product
80h	<a href="#">SYS_DS_STORAGE0</a>	R/W	0h	deep sleep storage data 0; the value is stored in the ULP domain
81h	<a href="#">SYS_DS_STORAGE1</a>	R/W	0h	deep sleep storage data 1; the value is stored in the ULP domain

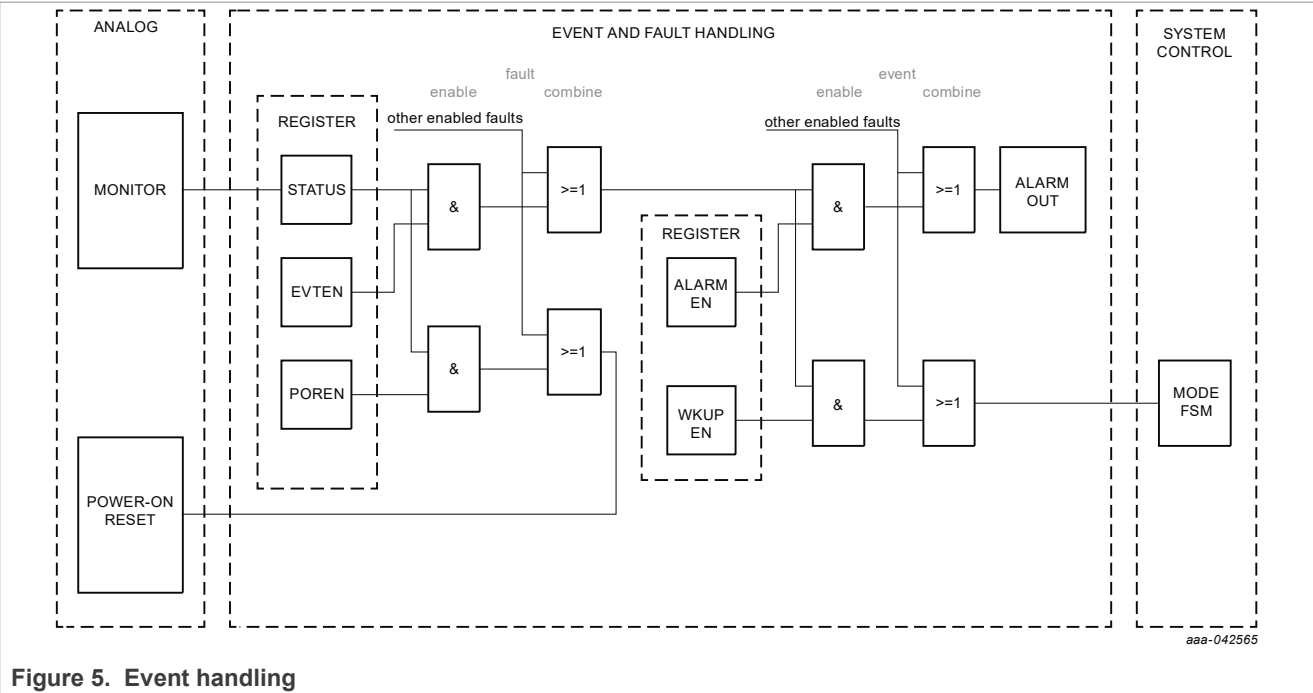
## 7.2 Event handling

The event handling block configures the reaction of the device when events or faults occur.

During regular operation of the device, events can occur. Events are items, such as wake-up or alarm signals. Events can cause a wake-up and/or an activation of the alarm output.

The term "fault" is used for events that should not occur during regular operation. Faults indicate a malfunction of the system, such as missing supply voltages. For faults, it can be selected to create a power-on reset (POR) or create a fault event. If nothing is selected, the fault is only reported.

Figure 5 shows the principle structure of the fault and event handling in the system.



7.2.1 Faults

The BMI7018 monitors the system for faults. The monitoring is done via dedicated hardware instances and independent of the measurement block. Some faults are critical for the correct operation of the device. These faults (VDDDLPPERMOV, VBATUV, VDDCOC, VDDDOV, VDDDUV, VDDDLPUV, OTEMPSHUTDOWN, PRMCLK, SECCLK, SLEEPOSC, and LOGICERR) trigger a POR.

Once a fault is detected, the corresponding fault bit is set. Individual faults are grouped into supply, analog, communication, and measurement-related faults allowing a quick overview. Register FEH\_GRP\_FLT\_STAT provides the overview based on the fault group. The fault registers (FEH\_SUPPLY\_FLT\_STAT0, FEH\_SUPPLY\_FLT\_STAT1, FEH\_ANA\_FLT\_STAT, FEH\_COM\_FLT\_STAT, and FEH\_MEAS\_FLT\_STAT) signal the specific fault. For each fault, it can be selected that the BMI7018 directly issues a POR, and/or generates a system [fault event \(SYSFLTEVT\)](#). If nothing is selected, the device reports the fault and continues operation.

Table 9. Overview of faults

Faults	Fault description	Forced POR	Fault group	Monitoring condition	Covered by BIST	Effects and comments
VDDDLPPERMOV	Undervoltage on internal supply for low-power operation.	Yes	SUPPLYFLT	All modes	No	
VBATOV	Overvoltage condition on pin VBAT (external supply for IC).	Selectable	SUPPLYFLT	Active and Cyclic modes	Start-up BIST	<ul style="list-style-type: none"><li>Disabling of balancing</li><li>Incorrect ADC results for VBAT</li><li>Disables AFECPUV leading to AFECPUV</li><li>Invalidation of SYNC measurement results in SECM</li></ul>
VBATLV	Low-voltage condition on pin VBAT (external supply for IC).	Yes, in case automatic discharge is on; selectable in case automatic discharge is off	SUPPLYFLT	Active and Cyclic modes; Sleep mode if balancing is enabled	No	Generates wake event in case balancing is Active and FEH_WAKEUP_CFG0.SYSFLTEV is set

Table 9. Overview of faults...continued

Faults	Fault description	Forced POR	Fault group	Monitoring condition	Covered by BIST	Effects and comments
VBATUV	Undervoltage condition on pin VBAT (external supply for IC).	Yes	SUPPLYFLT		No	
VDDCOV	Overvoltage condition on VDDC (supply for GPIO pins and TPL interface).	Selectable	SUPPLYFLT	Active mode and Cyclic mode when VDDCCYC = 1	Manual BIST	Invalidation of APP results in case VDDC is used for ratiometric results
VDDCUV	Undervoltage condition on VDDC (supply for GPIO pins and TPL interface).	Selectable	SUPPLYFLT	Active mode and Cyclic mode when VDDCCYC = 1	Manual BIST	Invalidation of APP results in case VDDC is used for ratiometric results
VDDCOC	Overcurrent condition on VDDC.	Yes	SUPPLYFLT	Active mode and Cyclic mode when VDDCCYC = 1	No	
VDDCHC	High current condition on VDDC.	Selectable	SUPPLYFLT	Active mode and Cyclic mode when VDDCCYC = 1	No	
VAUXOV	Overvoltage condition on VAUX (supply for external circuit).	Selectable	SUPPLYFLT	Active mode when VAUXACT = 1 and Cyclic mode when VAUXCYC = 1	Manual BIST	Invalidation of APP results in case VAUX is used for ratiometric results
VAUXUV	Undervoltage condition on VAUX (supply for external circuit).	Selectable	SUPPLYFLT	Active mode when VAUXACT = 1 and Cyclic mode when VAUXCYC = 1	Manual BIST	Invalidation of APP results in case VAUX is used for ratiometric results
VDDIOOV	Overvoltage condition on VDDIO (supply for SPI and I2C-bus).	Selectable	SUPPLYFLT	Active and Cyclic modes	No	
VDDIOUV	Undervoltage condition on VDDIO (supply for SPI and I2C-bus).	Selectable	SUPPLYFLT	Active and Cyclic modes	No	
VDDDOV	Overvoltage condition on VDDD (internal digital supply).	Yes	SUPPLYFLT	Active and Cyclic modes	No	
VDDDUV	Undervoltage condition on VDDD (internal digital supply).	Yes	SUPPLYFLT	Active and Cyclic modes	No	
VDDDLPUV	Undervoltage on internal supply for low-power operation.	Yes	SUPPLYFLT	Active, Cyclic, and Sleep modes	No	
VDDAOV	Overvoltage condition on VDDA (internal analog supply).	Selectable	SUPPLYFLT	Active and Cyclic modes	Start-up BIST and manual BIST	Invalidation of SYNC measurement results in SECM
VDDAUV	Undervoltage condition on VDDA.	Selectable	SUPPLYFLT	Active and Cyclic modes	Start-up BIST and manual BIST	Invalidation of SYNC measurement results in SECM
VPREOV	Overvoltage condition on VPRES (supply of the IC).	Selectable	SUPPLYFLT	Active and Cyclic modes	No	
VPREUV	Undervoltage condition on VPRES (supply of the IC).	Selectable	SUPPLYFLT	Active and Cyclic modes	No	



Table 9. Overview of faults...continued

Faults	Fault description	Forced POR	Fault group	Monitoring condition	Covered by BIST	Effects and comments
VPREREFSOV	Overvoltage condition on VPR EREFS (supply for IC reference).	Selectable	SUPPLYFLT	Active and Cyclic modes	No	
VPREREFSUV	Undervoltage condition on VPR EREFS (supply for IC reference).	Selectable	SUPPLYFLT	Active and Cyclic modes	Start-up BIST and manual BIST	
VANAOV	Overvoltage condition on VANA.	Selectable	SUPPLYFLT	Active and Cyclic modes	Start-up BIST and manual BIST	Invalidation of SYNC measurement results in SECM
VANAUUV	Undervoltage condition on VANA.	Selectable	SUPPLYFLT	Active and Cyclic modes	Start-up BIST and manual BIST	Invalidation of SYNC measurement results in SECM
AFECPOV	Overvoltage condition on AFECF.	Selectable	SUPPLYFLT	Active and Cyclic modes	Start-up BIST and manual BIST	Invalidation of SYNC measurement results in SECM
AFECPUV	Undervoltage condition on AFECF.	Selectable	SUPPLYFLT	Active and Cyclic modes	Start-up BIST and manual BIST	<ul style="list-style-type: none"> <li>Invalidation of SYNC measurement results in SECM</li> <li>AFECPUV can only be cleared if VBATOV is cleared.</li> </ul>
OTEMPSHUTDOWN	Too high junction temperature.	Yes	ANAFLT	Active and Cyclic modes	No	
MONBIST	BIST monitor failure.	No	ANAFLT	On entering Active mode; during manual BIST		
PRMCLK	Primary clock monitor failure.	Yes	ANAFLT	Active and Cyclic modes	No	Invalidation of SYNC measurement results in SECM
SECCLK	Secondary clock monitor failure.	Yes	ANAFLT	Active mode when SECM_CFG.MEASEN = 1	No	Invalidation of SYNC measurement results in SECM
SLEEPOSC	Low frequency oscillator failure.	Yes	ANAFLT	Active, Cyclic, and Sleep modes	No	
FUSEERR	Corrected single bit error in fuses.	No	ANAFLT	Active, Cyclic, and Sleep modes	No	
BALERR	Balancing switch fault.	No	ANAFLT	Active and Cyclic; in Sleep mode, BALERR is detected but wake is only issued in Cyclic and Active mode	No	
FRAMEERR	Communication frame error.	No	COMFLT	Active mode	No	
CRCERR	Communication CRC error.	No	COMFLT	Active mode	No	
COMTO	Communication timeout.	Selectable	COMFLT	Active mode	No	
COMERRORS	> 255 communication errors.	Selectable	COMFLT	Active mode	No	
PRIMCALCRCFLT	Primary calibration CRC error.	No	MEASFLT	On entering Active or Cyclic mode; start of a synchronous measurement	No	Invalidation of SYNC measurement results in SECM

Table 9. Overview of faults...continued

Faults	Fault description	Forced POR	Fault group	Monitoring condition	Covered by BIST	Effects and comments
SECCALCCRCFLT	Secondary calibration CRC error.	No	MEASFLT	On entering Active or Cyclic mode; start of a synchronous measurement	No	Invalidation of SYNC measurement results in SECM
LOGICERR	EDC error.	Yes	MEASFLT	Active, Cyclic, and Sleep modes	No	
SYNCMEASFLT	Synchronous measurement error.	No	MEASFLT	During synchronous measurements	No	Invalidation of SYNC measurement results in SECM

Application usage: Check for faults in the system.

7.2.2 Events

Events are situations that occur during the normal operation of the product. Events include various system faults, balancing ready, voltage checks based on measured data, and so on. Events can be used to trigger a wake-up or can be output via the alarm output signal.

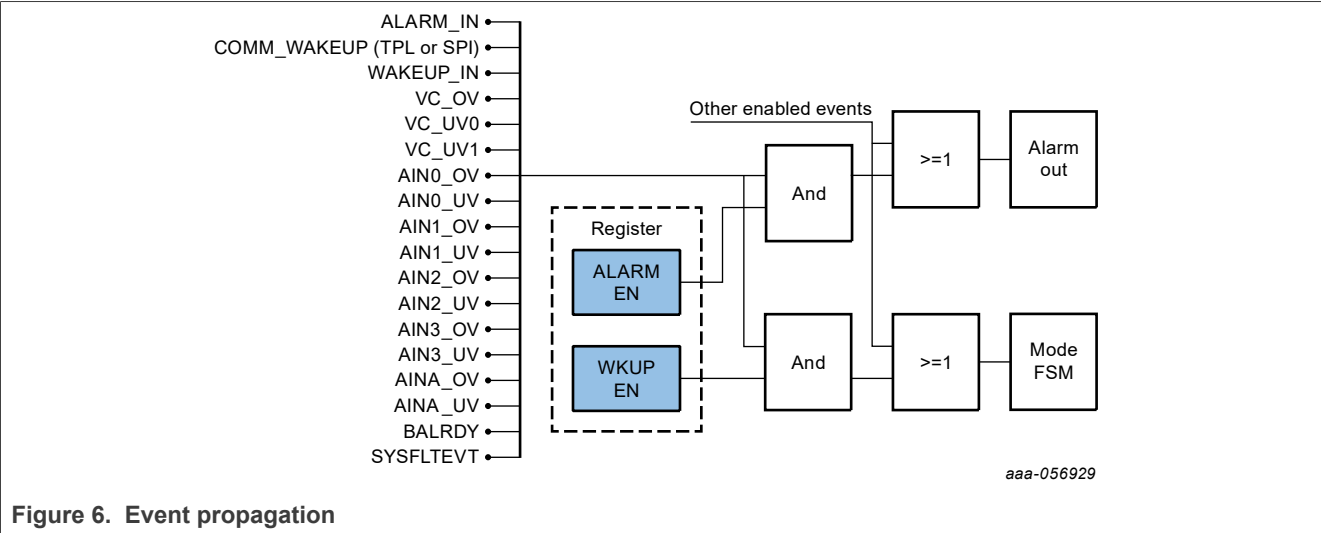


Figure 6. Event propagation

The register FEH\_ALARM\_CFG (Section 12.1.17) configures which events generate an alarm. Registers FEH\_WAKEUP\_CFG0 and FEH\_WAKEUP\_CFG1 (Section 12.1.22) do configure which events generate a wake-up. The wake-up initiates state transition as described in operation modes and initiates wake-up commands as described in Section 7.9.2.

Table 10. Overview of events

Events	Event description
ALARM_IN	Alarm detection on alarm input pins
COMM_WAKEUP (TPL or SPI)	Wake-up via communication
WAKEUP_IN	Wake-up via wake-up input
VC_OV	Cell voltage on one of the cells enabled in PRMM_VC_OV_UV_CFG measured to be higher than PRMM_VC_OV_TH_CFG
VC_UV0	Cell voltage on one of the cells enabled in PRMM_VC_OV_UV_CFG measured to be lower than PRMM_VC_UV0_TH_CFG
VC_UV1	Cell voltage on one of the cells enabled in PRMM_VC_OV_UV_CFG measured to be lower than PRMM_VC_UV1_TH_CFG
AIN0_OV	Voltage at pin AIN0 measured to be above PRMM_AIN0_OV_TH_CFG
AIN0_UV	Voltage at pin AIN0 measured to be below PRMM_AIN0_UV_TH_CFG

Table 10. Overview of events...continued

Events	Event description
AIN1_OV	Voltage at pin AIN1 measured to be above PRMM_AIN1_OV_TH_CFG
AIN1_UV	Voltage at pin AIN1 measured to be below PRMM_AIN1_UV_TH_CFG
AIN2_OV	Voltage at pin AIN2 measured to be above PRMM_AIN2_OV_TH_CFG
AIN2_UV	Voltage at pin AIN2 measured to be below PRMM_AIN2_UV_TH_CFG
AIN3_OV	Voltage at pin AIN3 measured to be above PRMM_AIN3_OV_TH_CFG
AIN3_UV	Voltage at pin AIN3 measured to be below PRMM_AIN3_UV_TH_CFG
AINA_OV	Voltage at pin AINA measured to be below PRMM_AINA_OV_TH_CFG
AINA_UV	Voltage at pin AINA measured to be below PRMM_AINA_UV_TH_CFG
BALRDY	Balancing activity finished; bit BALRDY is set
SYSAULT	Occurrence of a fault (see <a href="#">Table 9</a> ) that: <ol style="list-style-type: none"> <li>Does not result in a POR.</li> <li>Is enabled.</li> </ol>

Application usage: Notification of MCU about events.

### 7.2.3 Alarm output

The BMI7018 offers an alarm output on AINA\_ALARMOUT pin. The alarm output is only available in Active mode. The register [FEH\\_ALARM\\_CFG](#) defines the configuration. The configuration options are Active HIGH, Active LOW, or Heartbeat mode. In Heartbeat mode, the BMI7018 provides a pattern with a fixed high time and a selectable low time.

Application usage: Notification of MCU about events. Heartbeat mode is also used for checking of integrity of the alarm line.

### 7.2.4 Alarm input

The BMI7018 offers an alarm input on GPIO1 pin. The register [FEH\\_ALARM\\_CFG](#) defines the configuration. The configuration options are Active HIGH, Active LOW, or Heartbeat mode. In Heartbeat mode, the BMI7018 expects a pattern with a fixed high time and a selectable low time. The bit [FEH\\_ALARM\\_CFG.ALARMINHBINV](#) allows inverting the expected pattern. The device is then expecting a fixed low time and a selectable high time.

Application usage: Forwarding of events. Heartbeat mode is also used for checking of integrity of the alarm line.

### 7.2.5 Built-in self-test (BIST)

The BMI7018 has two BIST methods implemented. The start-up BIST is executed automatically each time the device is entering into Active mode. The manual BIST is started when the bit [FEH\\_MON\\_BIST\\_CTRL.STARTBIST](#) is set. [FEH\\_MON\\_BIST\\_CTRL.BISTCRC](#) reflects the CRC result of the last BIST. This information shows a completion of the BIST. The individual results of the BIST can be read in the register [FEH\\_MON\\_BIST\\_RES](#). The covered faults of the BIST are shown in [Table 9](#).

**Note:** Execution of the BIST is manipulating the inputs to the measurements of the BMI7018. The execution of the BIST results in erratic measurements and triggers system faults. During the execution of the start-up BIST, the system faults are masked. No masking is applied during the manual BIST. The BMI7018 reacts to the faults introduced during the manual BIST in the same way as in normal operation. As per the configuration of the device, invalidation of the measurement result, an activation of the fault and alarm outputs, or a POR is initiated. Measurement results that have been acquired while the BIST was Active must be discarded.

Application usage: Functionality check of monitoring instances.

### 7.2.6 Event handling configuration CRC

The BMI7018 contains many configuration registers. For validation of the correctness of the configuration of the device, all configuration registers can be read. The BMI7018 is calculating a CRC across the content of the configuration registers. The MCU can use this CRC value to validate the integrity of the configuration. The CRC is recalculated whenever a register covered by the CRC is written or the CRC value is read.

The event handling CRC covers the FEH\_ALARM\_CFG, FEH\_ALARM\_OUT\_CFG0, FEH\_ALARM\_OUT\_CFG1, FEH\_WAKEUP\_CFG0, FEH\_WAKEUP\_CFG1, FEH\_SUPPLY\_FLT\_POR\_CFG0, FEH\_SUPPLY\_FLT\_POR\_CFG1, FEH\_ANA\_FLT\_POR\_CFG, FEH\_COM\_FLT\_POR\_CFG, FEH\_SUPPLY\_FLT\_EVT\_CFG0, FEH\_SUPPLY\_FLT\_EVT\_CFG1, FEH\_ANA\_FLT\_EVT\_CFG, FEH\_COM\_FLT\_EVT\_CFG, and FEH\_MEAS\_FLT\_EVT\_CFG register.

The used polynomial is:  $D175h (+1) = X^{16} + X^{15} + X^{13} + X^9 + X^7 + X^6 + X^5 + X^3 + X^1 + 1$ .

#### Notes:

- The CRC value depends on the configuration of the device and is therefore application dependent.
- The polynomial used here is different to the polynomial used for communication.

Application usage: Check of integrity of the system configuration.

### 7.2.7 Last POR reason

The register FEH\_POR\_REASON provides information about the reason of the last POR. The error code for the various reasons is listed in the [FEH\\_POR\\_REASON](#) register.

A POR may not always be initiated by a single source, but by an event that causes multiple reasons to occur simultaneously. In case supplies are affected, the integrity of the FEH\_POR\_REASON may also be affected. Because of this reason, the content of the FEH\_POR\_REASON should only be considered as an indication and so used only for debugging purposes.

Application usage: Debugging information.

### 7.2.8 Event handling registers

All registers related to the event handling are listed here. Details of registers and the bit fields are explained in the register map section.

Table 11. Register overview: Event\_Handling\_Registers

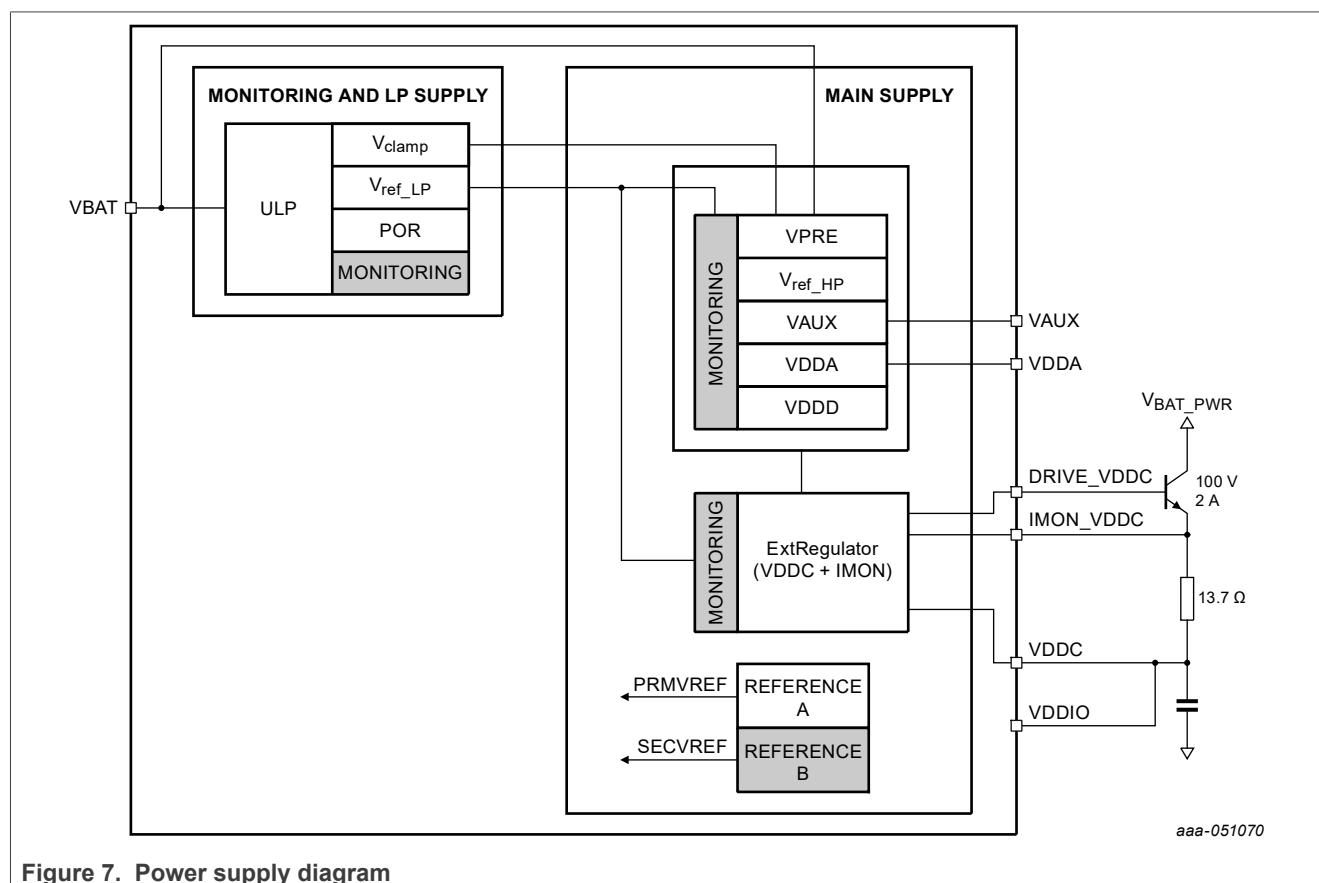
Address	Name	Access	Reset	Description
400h	<a href="#">FEH_CFG_CRC</a>	R	0h	configuration CRC
401h	<a href="#">FEH_ALARM_CFG</a>	R/W	0h	general alarm configuration
402h	<a href="#">FEH_ALARM_OUT_CFG0</a>	R/W	0h	alarm output source selection
403h	<a href="#">FEH_ALARM_OUT_CFG1</a>	R/W	0h	alarm output source selection
404h	<a href="#">FEH_ALARM_OUT_REASON0</a>	R	0h	alarm output reason
405h	<a href="#">FEH_ALARM_OUT_REASON1</a>	R	0h	alarm output reason
408h	<a href="#">FEH_WAKEUP_CFG0</a>	R/W	0h	wake up source configuration
409h	<a href="#">FEH_WAKEUP_CFG1</a>	R/W	0h	wake up source configuration
40Ah	<a href="#">FEH_WAKEUP_REASON0</a>	R	0h	wake up reason register
40Bh	<a href="#">FEH_WAKEUP_REASON1</a>	R	0h	wake up reason register
410h	<a href="#">FEH_MON_BIST_CTRL</a>	R/W	0h	monitor BIST control register
411h	<a href="#">FEH_MON_BIST_RES</a>	R	FFh	monitor BIST result register; value changes at start-up, if everything is fine to 0000h

Table 11. Register overview: Event\_Handling\_Registers...continued

Address	Name	Access	Reset	Description
41Eh	<a href="#">FEH_ACC_ERR</a>	R	0h	access error status register
41Fh	<a href="#">FEH_GRP_FLT_STAT</a>	R	0h	main system fault status register; this register holds one bit per fault group. For each fault group a separate status register exists. The bit here is cleared if all its sources are cleared.
420h	<a href="#">FEH_SUPPLY_FLT_STAT0</a>	R/W	0h	supply fault status register 0 (these monitors are part of the BIST)
421h	<a href="#">FEH_SUPPLY_FLT_STAT1</a>	R/W	0h	supply fault status register 1 (these monitors are not part of the BIST)
422h	<a href="#">FEH_ANA_FLT_STAT</a>	R/W	0h	analog fault status register
423h	<a href="#">FEH_COM_FLT_STAT</a>	R/W	0h	communication fault status register
424h	<a href="#">FEH_MEAS_FLT_STAT</a>	R/W	0h	other fault status register
428h	<a href="#">FEH_SUPPLY_FLT_POR_CFG0</a>	R/W	0h	supply fault POR selection 0
429h	<a href="#">FEH_SUPPLY_FLT_POR_CFG1</a>	R/W	0h	supply fault POR selection 1
42Ah	reserved	R	0h	analog fault POR selection
42Bh	<a href="#">FEH_COM_FLT_POR_CFG</a>	R/W	8h	communication fault POR enable register
430h	<a href="#">FEH_SUPPLY_FLT_EVT_CFG0</a>	R/W	0h	supply fault event selection register 0
431h	<a href="#">FEH_SUPPLY_FLT_EVT_CFG1</a>	R/W	0h	supply fault event selection register 1
432h	<a href="#">FEH_ANA_FLT_EVT_CFG</a>	R/W	0h	analog fault event enable register
433h	<a href="#">FEH_COM_FLT_EVT_CFG</a>	R/W	0h	communication fault event enable register
434h	<a href="#">FEH_MEAS_FLT_EVT_CFG</a>	R/W	0h	measurement fault event enable register
480h	<a href="#">FEH_POR_REASON</a>	R	0h	power-on reset reason. The value is stored in the ULP domain.

### 7.3 Power supply

The power supply block provides all voltages that are required internally, as well as the voltages provided externally. In addition, it monitors the voltages for overvoltage and undervoltage.



**Figure 7. Power supply diagram**

### 7.3.1 Overview

[Table 12](#) gives an overview of the supplies, the intended usage, the source, and the diagnostic information for this supply.

### Table 12. Supply overview

Supply	Intended usage	Source	Diagnostics
VBAT	External supply for IC	External	<ol style="list-style-type: none"> <li>1. Overvoltage and undervoltage</li> <li>2. Analog voltage measurement</li> </ol>
VPRE	Supply of the IC	VBAT	Overvoltage
VPREF	Supply for IC references	VBAT	Undervoltage and overvoltage
VAUX	Supply for external circuits	VPRE	<ol style="list-style-type: none"> <li>1. Undervoltage and overvoltage</li> <li>2. Analog voltage measurement</li> </ol>
VDDC	Supply for GPIO pins and TPL interface	External	<ol style="list-style-type: none"> <li>1. Undervoltage and overvoltage</li> <li>2. Analog current measurement</li> <li>3. High current and overcurrent</li> <li>4. Analog voltage measurement</li> </ol>

Table 12. Supply overview...continued

Supply	Intended usage	Source	Diagnostics
VDDIO	Supply for SPI and I <sup>2</sup> C-bus	External or VDDC	Undervoltage and overvoltage
Internal: RevLDO	Reference for supplies	VPRE	Analog voltage measurement
Internal: VDDA	Internal analog supply	VPRE	1. Undervoltage and overvoltage 2. Analog voltage measurement
Internal: VDDD	Internal digital supply	VPRE	Undervoltage and overvoltage (forces power-on reset, info can be read in FEH_POR_REASON.SOURCE)
Internal: RefA	Reference voltage for ADC1	VPRE REF	Analog voltage measurement
Internal: RefB	Reference voltage for ADC2	VPRE REF	Analog voltage measurement
Internal: RevMON	Supply monitoring	VPRE REF	Analog voltage measurement
Internal: VANA	Internal analog supply	VPRE	Undervoltage and overvoltage
Internal: IBIAS	Internal reference current	VPRE	Undercurrent and overcurrent
Internal: AFE charge pump	Internal analog supply	VPRE	Undervoltage and overvoltage

[Table 13](#) gives an overview of the availability of the supplies in the various operation modes.

Table 13. Availability of supplies vs. operation modes

Supply	Active mode	Cyclic mode	Sleep mode	Deep sleep mode
VDDC	Available	Available if VDDCCYC = 1	Off	Off
VAUX	Available if VAUXACT = 1	Available if VAUXCYC = 1	Off	Off

### 7.3.2 VPRE

VPRE is a preregulated supply voltage. VPRE is generated out of the VBAT voltage. Most of the supply voltages, reference voltages, and reference currents are derived from VPRE. A detailed overview is given in [Table 12](#).

### 7.3.3 VAUX

VAUX is intended to supply external analog circuits, such as resistor and negative temperature coefficient (NTC) networks.

VAUX can also be used as reference voltage for the ADC converter in case ratiometric measurements are needed. See [Section 7.4](#) for more details.

### 7.3.4 VDDC

VDDC is used for the GPIO pins and the TPL communication. VDDC can also be used as supply for VDDIO and external analog circuits, and as reference voltage for the ADC converter in case ratiometric measurements are needed. To limit the power dissipation inside the IC, VDDC is generated via an external transistor. See [Section 7.4](#) for more details.

### 7.3.5 VDDIO

VDDIO is an input voltage of the BMI7018. VDDIO can be supplied by a 5 V supply, such as VDDC, or via an external 3.3 V regulator. VDDIO is used for SPI and I<sup>2</sup>C-bus interface.

### 7.3.6 VDDA

VDDA is an internal supply. On pin VDDA, an external capacitor must be connected to buffer the supply, see [Section 11.1.1.1](#). No other circuit is allowed to be attached.

### 7.3.7 Others

VDDD, RefA, RefB, VANA, IBIAS, and analog front-end (AFE) are internal voltages or currents. They do not have a direct connection to a pin of the IC.

## 7.4 Measurement

The BMI7018 offers a primary and a secondary measurement chain. The two chains are independent from each other. The measurement operations of the two measurement chains can be synchronized.

### 7.4.1 Functional diagram

[Figure 8](#) and [Figure 9](#) show the functional diagrams of the measurement blocks.

#### 7.4.1.1 Primary measurement

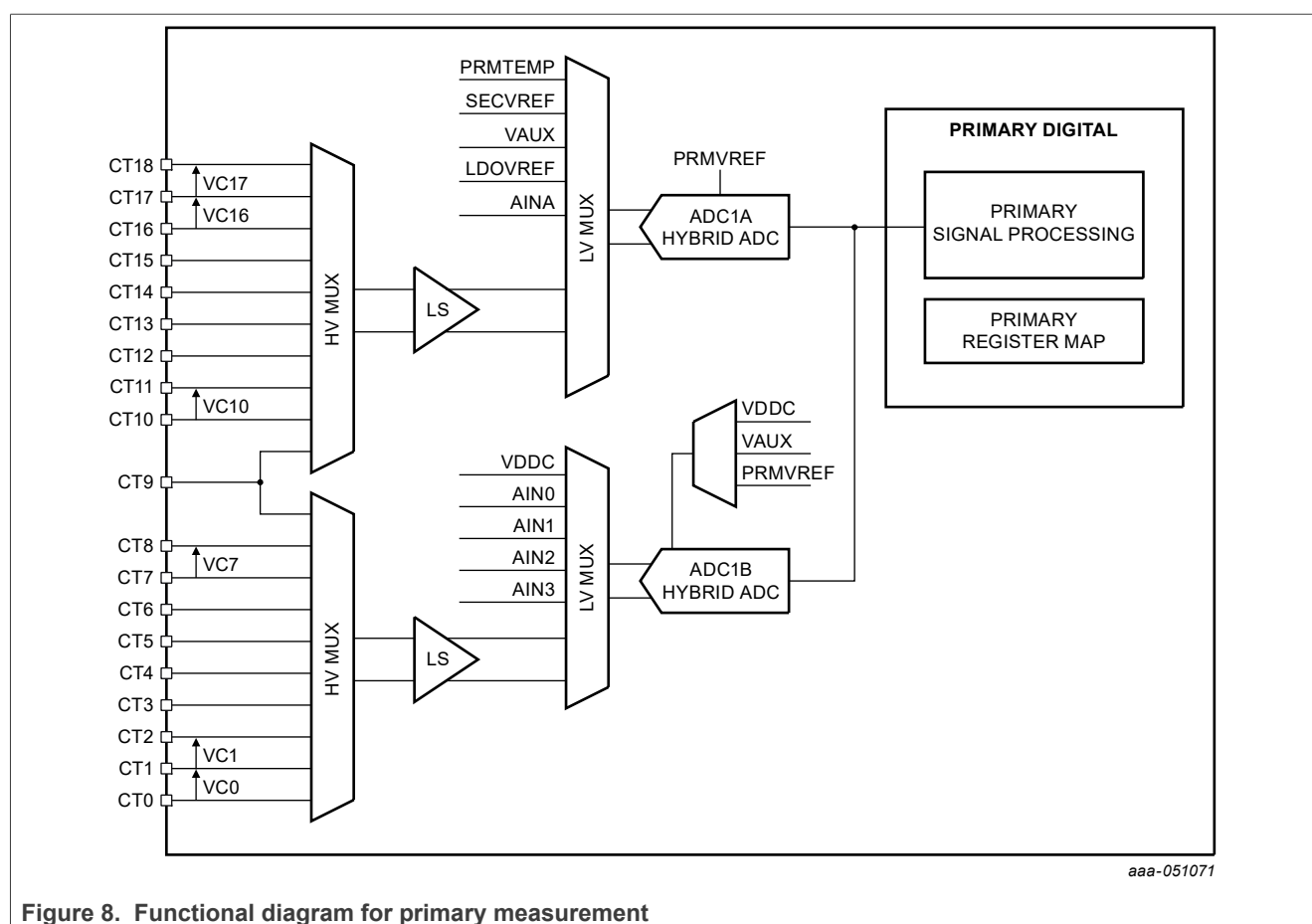
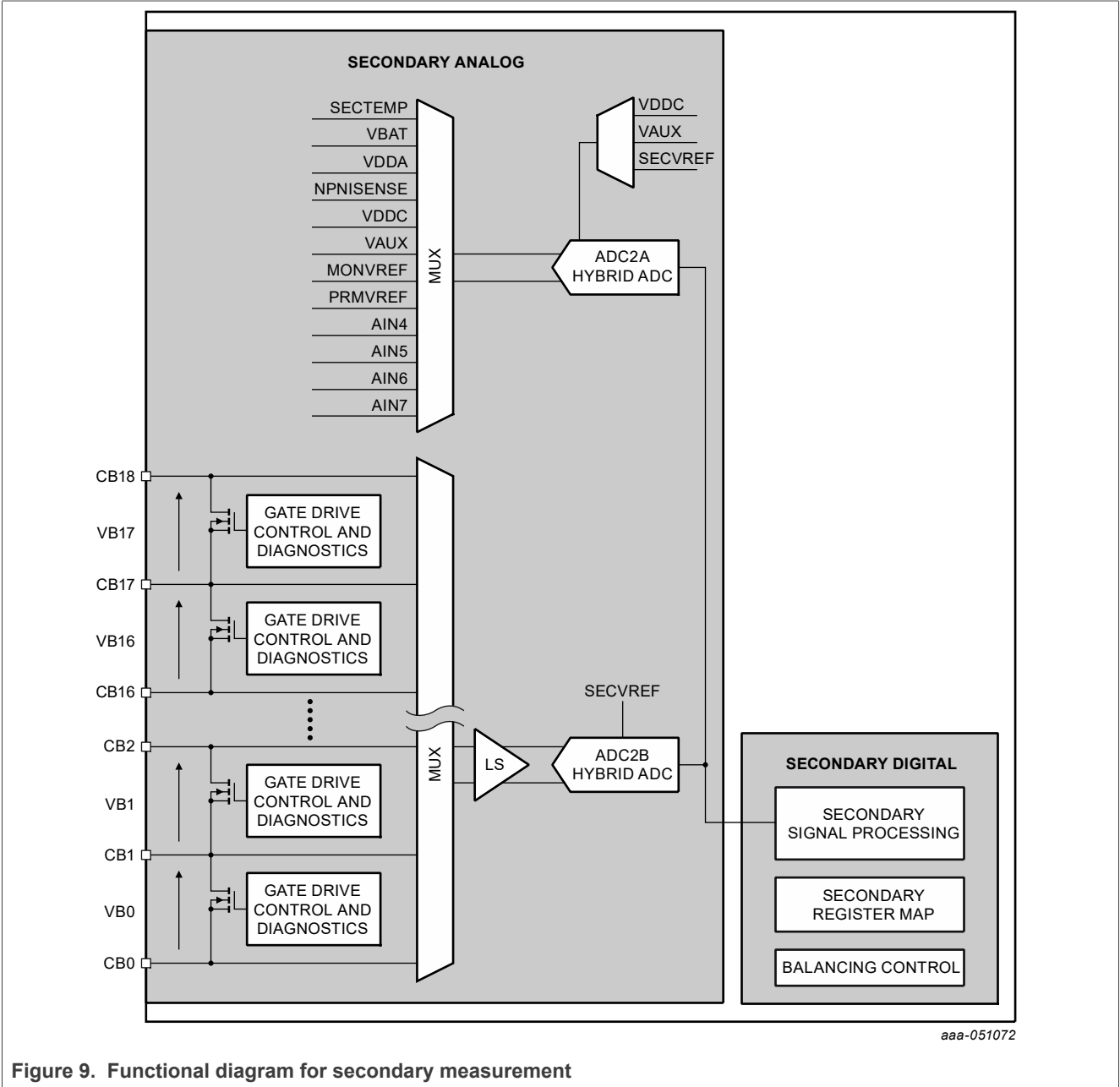


Figure 8. Functional diagram for primary measurement



7.4.1.2 Secondary measurement



7.4.2 Functional description

The BMI7018 offers a primary and a secondary measurement chain. The primary measurement chain is using the registers listed in the [Primary Measurement Registers](#) block. The secondary measurement chain is using the registers listed in the [Secondary Measurement Registers](#) block. The two register blocks are independent of each other. The two chains are independent from each other.

The event handling block monitors the synchronicity between the primary and secondary measurements. See [Section 7.2](#) for details on the event handling block.

The registers block [All Measurement Registers](#) is writing simultaneously into the primary and the secondary measurement registers. This mechanism provides a comfortable way of ensuring the measurement configuration registers are set simultaneously for the primary and secondary measurement chain. A read back of the All Measurement Registers is not possible. The BMI7018 returns 0000h as data in case one of the All Measurement Registers is read.

#### 7.4.2.1 Measurement sequence

To achieve a high sampling rate, the primary measurement chain has two ADCs.

ADC1A measures:

- The primary IC temperature (PRMTEMP)
- The cell voltages 9 to 17 (VC9 to VC17)
- The auxiliary supply (VAUX)
- The voltage reference for the secondary measurement chain (SECVREF)
- The analog input AINA
- The voltage reference for the internal power supplies (LDOVREF)

ADC1B measures:

- The supply voltage for GPIO and the TPL interface (VDDC)
- The cell voltages 0 to 8 (VC0 to VC8)
- The analog inputs 0 to 3 (AIN0 to AIN3)

The primary measurement chain measures all signals cyclically. Once an ADC conversion is completed, the next signal is measured. After all 14 signals are measured once, the scan is completed and the next measurement cycle starts ([Figure 10](#)).

The secondary measurement chain has two ADCs.

ADC2A measures:

- The secondary IC temperature (SECTEMP)
- The battery supply (VBAT)
- The analog supply voltage (VDDA)
- The current in the external NPN (NPNISENSE)
- The supply voltage for GPIO and the TPL interface (VDDC)
- The auxiliary supply (VAUX)
- The reference for the primary measurement chain (PRMVREF)
- The reference (MONVREF)
- The analog inputs 4 to 7 (AIN4 to AIN7)

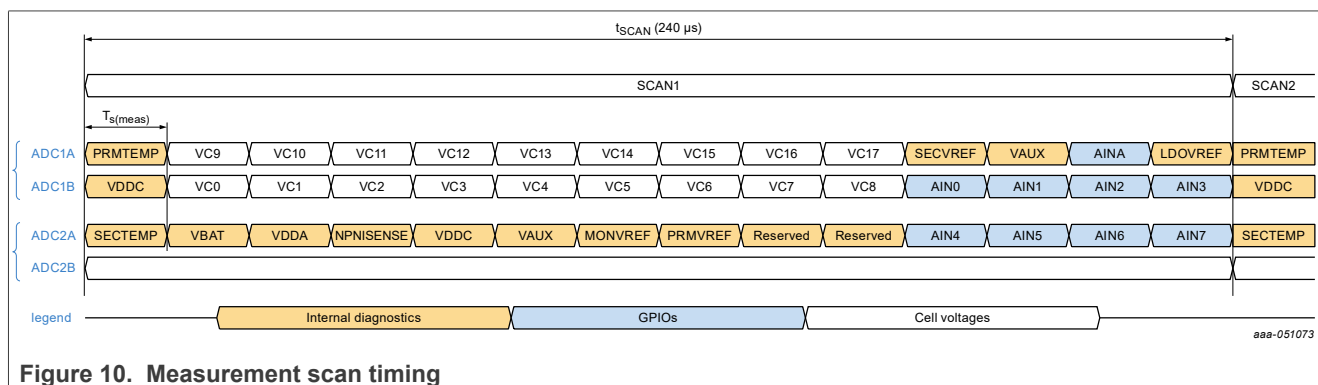
ADC2A measures cyclically, similar to ADC1A and ADC1B. After all 14 channels are measured once, the scan is completed and the next cycle starts.

ADC2B measures the cell voltages via the balancing pins (VB0 to VB17). As the cell balancing pins do not have an external antialiasing filter, ADC2B uses an internal antialiasing filter. The sampling scheme of the BMI7018 implements appropriate settling times for the internal antialiasing filter. ADC2B measures one signal several times before it switches to the next signal. In a synchronous measurement cycle, the signal is measured for  $\text{SECM\_PER\_CTRL.PERLEN} \times 14 \times t_{s(\text{meas})}$ . In a fast VB measurement cycle, each signal is measured for  $28 \times t_{s(\text{meas})}$ .

Disabling measurements has no influence on the sequence for ADC1A, ADC1B, and ADC2A. ADC2B skips cells that are disabled.

**Notes:**

- *PRMM\_PER\_CTRL.PERLEN and SECM\_PER\_CTRL.PERLEN must be set to the same value.*
- *SECVREF is available when secondary measurement is enabled. PRMVREF is available when primary measurement is enabled.*

**Figure 10. Measurement scan timing**

The result of a single scan cycle as shown in [Figure 10](#) is not directly available. The BMI7018 makes the averaged value over multiple scan cycles available.

**7.4.2.2 Measurement configuration**

The registers PRMM\_VC\_CFG, PRMM\_AIN\_CFG, PRMM\_VBUF\_CFG, SECM\_VBUF\_CFG, SECM\_VB\_CFG, and SECM\_AIN\_CFG configure the measurements that are enabled. Disabling signals measured by ADC1A, ADC1B, or ADC2A does not influence the measurement timing. Signals measured by ADC2B are only measured when enabled. Disabled channels are skipped.

The registers PRMM\_AIN\_CFG and SECM\_AIN\_CFG contain the bitfields RATIOMETRICAIN0 to RATIOMETRICAIN7. These bits configure the measurement of the pins AIN0 to AIN7. Options are:

- Absolute regarding SECVREF or PRMVREF.
- Ratiometric to VAUX.
- Ratiometric to VDDC.

The bits FLTAPPINV in PRMM\_AIN\_CFG and SECM\_AIN\_CFG force an automatic invalidation of the application timed measurement results once a measurement fault (see [Section 7.4.4](#)) is detected.

**7.4.2.3 Measurement configuration CRC**

The BMI7018 contains many configuration registers. For validation of the correctness of the configuration of the device, all configuration registers can be read. The BMI7018 calculates a CRC across the content of the configuration registers. The MCU can use this CRC value to validate the integrity of the configuration. The CRC is recalculated whenever a register covered by the CRC is written or the CRC value is read.

PRMM\_CFG\_CRC contains the CRC value for the registers PRMM\_CFG, PRMM\_PER\_CTRL, PRMM\_VC\_CFG0, PRMM\_VC\_CFG1, PRMM\_AIN\_CFG, PRMM\_VBUF\_CFG, PRMM\_VC\_OV\_UV\_CFG0, PRMM\_VC\_OV\_UV\_CFG1, PRMM\_VC\_OV\_TH\_CFG, PRMM\_VC\_UV0\_TH\_CFG, PRMM\_VC\_UV1\_TH\_CFG, PRMM\_AIN0\_OV\_TH\_CFG, PRMM\_AIN1\_OV\_TH\_CFG, PRMM\_AIN2\_OV\_TH\_CFG, PRMM\_AIN3\_OV\_TH\_CFG, PRMM\_AINA\_OV\_TH\_CFG, PRMM\_AIN0\_UV\_TH\_CFG, PRMM\_AIN1\_UV\_TH\_CFG, PRMM\_AIN2\_UV\_TH\_CFG, PRMM\_AIN3\_UV\_TH\_CFG, PRMM\_AINA\_UV\_TH\_CFG.

SECM\_CFG\_CRC contains the CRC value of the registers SECM\_CFG, SECM\_PER\_CTRL, SECM\_VB\_CFG, SECM\_AIN\_CFG, and SECM\_VBUF\_CFG.

The used polynomial is:  $D175h (+1) = X^{16} + X^{15} + X^{13} + X^9 + X^7 + X^6 + X^5 + X^3 + X^1 + 1$ .

#### Notes:

- The CRC value depends on the configuration of the device and is therefore application dependent.
- The polynomial used here is different to the polynomial used for communication.

Application usage: Check of integrity of the system configuration.

#### 7.4.2.4 Undervoltage and overvoltage checks

The BMI7018 performs an undervoltage and overvoltage check after each periodic measurement. For the cell terminals voltages, this check is optional. Register PRMM\_VC\_OV\_UV\_CFG configures which of the cell voltages take part in the undervoltage and overvoltage comparison. The register PRMM\_VC\_OV\_TH\_CFG contains the overvoltage threshold to be used for the comparison. The results of the comparisons are available in the PRMM\_VC\_OV\_FLT\_STAT register.

The register PRMM\_VC\_UV0\_TH\_CFG contains the threshold used for cell undervoltage-based balancing as described in the [Cell undervoltage based balancing](#). The results of the comparison can be read in the PRMM\_VC\_UV0\_FLT\_STAT register.

The register PRMM\_VC\_UV1\_TH\_CFG contains the threshold used for global undervoltage-based balancing as described in the [Global undervoltage based balancing](#). The results of the comparison can be read in the PRMM\_VC\_UV1\_FLT\_STAT register.

The registers PRMM\_AIN0\_OV\_TH\_CFG to PRMM\_AIN3\_OV\_TH\_CFG and PRMM\_AINA\_OV\_TH\_CFG and PRMM\_AIN0\_UV\_TH\_CFG to PRMM\_AIN3\_UV\_TH\_CFG and PRMM\_AINA\_UV\_TH\_CFG contain the undervoltage and overvoltage thresholds for AIN0 to AIN3 and AINA. The results of the comparison can be read in the PRMM\_AIN\_OV\_FLT\_STAT and PRMM\_AIN\_UV\_FLT\_STAT registers. The thresholds set by these registers are also used for the [Temperature-modulated balancing](#).

The BMI7018 performs the undervoltage and overvoltage comparison together. In some cases, it can be of interest to compare only to one of the thresholds. Configuring not used thresholds to the invalid code (8000h) prevents setting the corresponding undervoltage or overvoltage bits.

#### 7.4.2.5 Measurement data format

The BMI7018 provides the measurement results as 16-bit two's complement. Code 8000h represents invalid data (see [Section 7.4.4](#)). Clamping is signaled when the measured value is out of the measurement range of the BMI7018. Code 7FFFh indicates the value is clamped positively. Code 8001h indicates a negative clamping.

Measurements that have only a positive measurement range, for instance all GPIO measurements, are still provided as 16-bit two's complement.

Table 14. Measurement data representation

Code	Value	Example for PRMM_APP_VC0
7FFFh	Positive clamped value	Positive clamping occurred; cell voltage above measurement range
7FFEh	maximum positive value = 32766 <sup>[1]</sup>	$32766 \times \text{LSB} \times V_{\text{meas(res)}} = 5.05 \text{ V}$
0001h	+1	$+1 \text{ LSB} \times V_{\text{meas(res)}} = 154 \mu\text{V}$
0000h	0	0 V
FFFFh	-1	$-1 \text{ LSB} \times V_{\text{meas(res)}} = -154 \mu\text{V}$
8002h	Maximum negative value = -32766 <sup>[1]</sup>	$-32766 \times \text{LSB} \times V_{\text{meas(res)}} = -5.05 \text{ V}$

Table 14. Measurement data representation...continued

Code	Value	Example for PRMM_APP_VC0
8001h	Negative clamped value	Negative clamping occurred; cell voltage below measurement range
8000h	Invalid	Measurement is invalidated, for example, fewer than 16 scans

[1] Saturation may occur before maximum value is reached (see [Section 7.4.2.6](#)).

7.4.2.6 Measurement saturation, resolution, and references

[Table 15](#) lists the measurement location and the reference potential for the individual measurements of the BMI7018. The table also lists the resolution of the measurements and, when applicable, the saturation values. If a single ADC conversion is outside the saturation limits, the measurement result register for this measurement indicates clamping. If the value is below the lower saturation limit, the negative clamping value (8001h) is used. If the value is above the upper saturation limit, the positive clamping value (7FFFh) is used.

Table 15. Measurements and references

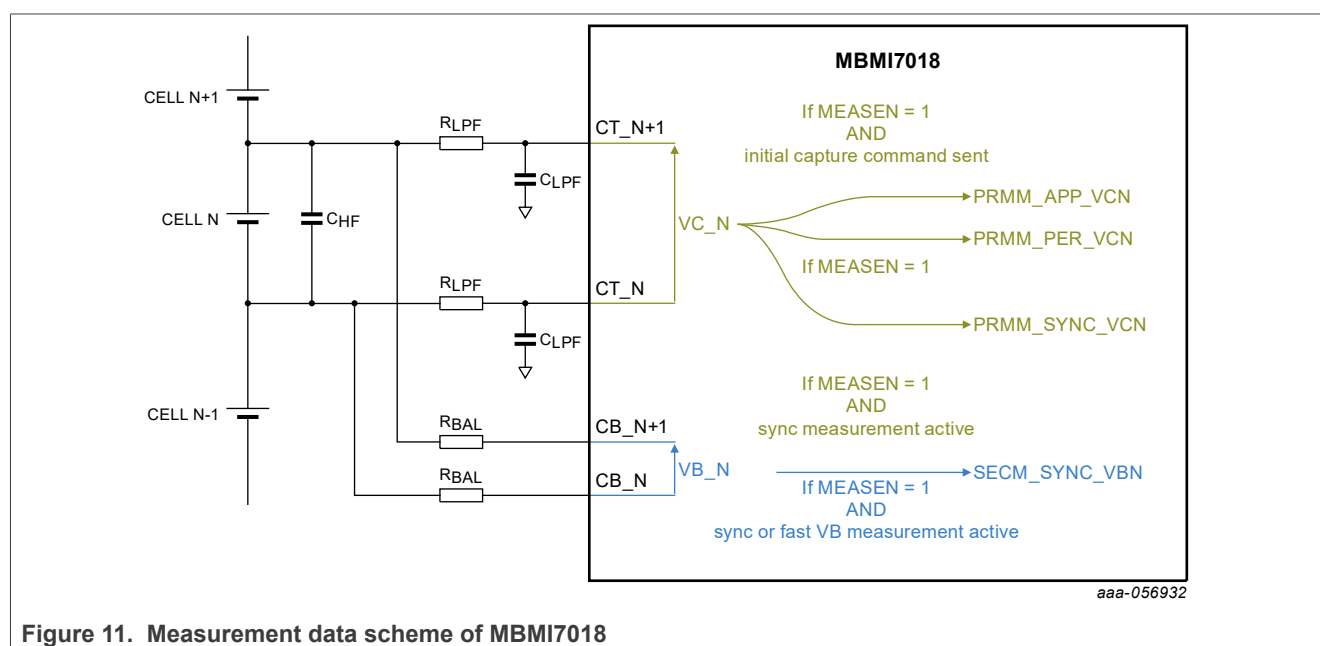
Measurement	Measurement location	Reference potential	Conversion formula (typ.)	Saturation
Cell terminal measurement VC(X); X = 0 to 17	CT(X+1)	CT(X)	154 $\mu$ V $\times$ result register value	Positive saturation at 7FF7h Negative saturation at 8008h
Cell voltage at balancing pins VB(X); X = 0 to 17	CB(X+1)	CB(X)	154 $\mu$ V $\times$ result register value	Positive saturation at 7FF7h negative saturation at B2D9h
AIN(X); X = 0 to 7, A	AIN(X)	AINX_VSSA	154 $\mu$ V $\times$ result register value (for absolute measurement) 3.05176 m% $\times$ result register value (for ratiometric measurement)	positive saturation at 7FF7h Negative saturation at FEEh
VDDA	VDDA	VSSA	154 $\mu$ V $\times$ result register value	Not applicable
VBAT	VBAT	VSSA	3.128 mV $\times$ result register value	Not applicable
PRMTEMP	Internal	Internal	32.4 mK $\times$ result register value (to get result in Kelvin) 32.4 mK $\times$ result register value - 273.15 (to get result in $^{\circ}$ C)	Not applicable
SECTEMP	Internal	Internal	32.4 mK $\times$ result register value (to get result in Kelvin) 32.4 mK $\times$ result register value - 273.15 (to get result in $^{\circ}$ C)	Not applicable
VAUX	VAUX	ADC1A: AINX_GND ADC2A: VSSA	308 $\mu$ V $\times$ result register value (for absolute measurement)	Not applicable
VDDC	VDDC	ADC1A: AINX_GND ADC2A: VSSA	308 $\mu$ V $\times$ result register value	Not applicable
NPNISENSE	VDDC_IMON	VDDC	7.69 $\mu$ V $\times$ result register value	Not applicable
PRMVREF	Internal	Internal	38.452 $\mu$ V $\times$ result register value	Not applicable
SECVREF	Internal	Internal	38.452 $\mu$ V $\times$ result register value-	Not applicable

7.4.3 Measurement modes

The BMI7018 allows four main measurement modes:

- Periodic measurements
- Application timed continuous measurements
- Synchronized measurements of VC and VB terminals
- Fast VB measurements

The synchronized and fast VB measurements are mutually exclusive, all measurements can run in parallel with each other. When measurements run in parallel, one ADC conversion result is used for all active measurement modes. [Figure 11](#) shows the measurement location for the cell voltages and the result registers where the cell voltage data are stored. [Figure 11](#) also shows the conditions that trigger the storing of the ADC result to the result register sets. Based on this, one ADC conversion result for a cell terminal voltage can be used for the periodic, the application and the synchronous measurements. Not all inputs have all register sets. For instance the cell balancing voltages have only a set for the synchronous results.



[Table 16](#) shows the key characteristics of the measurement modes.

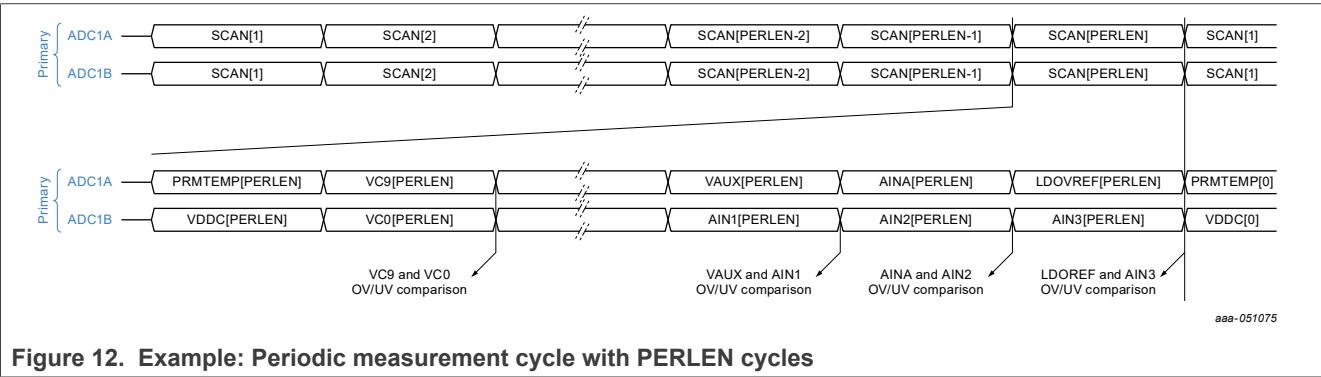
**Table 16. Overview of measurement modes**

Measurement	Measurement frequency	Averaging interval	Result update	Start condition	Applies to
Periodic	$f_{\text{PER}} = \frac{1}{14 \times t_{\text{s(meas)}}} = \text{approx. 4.2 kHz}$	defined by bit field PERLEN (primary: 16 to 511 measurements)	periodically depending on PERCTRL	continuous measurement (as soon as MEASEN is set 1)	ADC1A, ADC1B, and ADC2A
Application timed continuous	$f_{\text{APP}} = \frac{1}{14 \times t_{\text{s(meas)}}} = \text{approx. 4.2 kHz}$	defined by capture command (16 to 65535 measurements)	after capture command (PRMM_APP_CTRL[5:0] and SECM_APP_CTRL[9:6])	continuous measurement (as soon as MEASEN is set 1 and first capture command for the signal is received)	ADC1A, ADC1B, and ADC2A
Synchronized	$f_{\text{SYNC_PRMM}} = \frac{1}{14 \times t_{\text{s(meas)}}} = \text{approx. 4.2 kHz}$ $f_{\text{SYNC_SECM}} = \frac{1}{t_{\text{s(meas)}}} = \text{approx. 59 kHz}$	defined by bit field PERLEN (primary: 16 to 511 measurements) (secondary: must use same time interval as primary)	after measurement is finished	start of a synchronous measurement cycle <sup>[1]</sup>	ADC1A, ADC1B, ADC2A, and ADC2B
Fast VB	$f_{\text{fast VB}} = \frac{1}{t_{\text{s(meas)}}} = \text{approx. 59 kHz}$	$28 \times t_{\text{s(meas)}}$	after measurement is finished	start of a fast VB measurement (SECM_SYNC_CTRL.FASTFB)	ADC2B

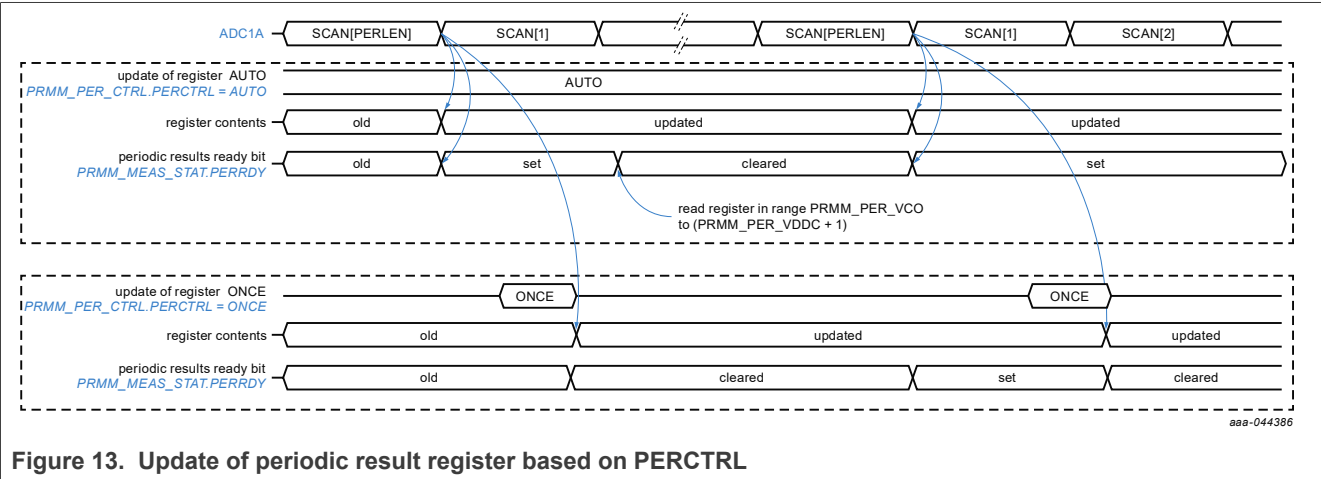
[1] Set PRMM\_SYNC\_CTRL.SYNCCYC and SECM\_SYNC\_CTRL.SYNCCYC simultaneously via writing to ALLM\_SYNC\_CTRL.SYNCCYC.

7.4.3.1 Periodic measurement

In Periodic Measurement mode, a configurable number of samples is taken and an averaged result is stored. The number of measurement cycles is defined in PRMM\_PER\_CTRL.PERLEN and SECM\_PER\_CTRL.PERLEN. Once the device has performed the configured number of measurements for a signal, the result is checked for undervoltage or overvoltage conditions (see [Undervoltage and overvoltage checks](#)). Once the device has completed the configured number of the measurements for all signals, the averaged results are stored in the periodic measurement result registers. Based on this implementation, the undervoltage and overvoltage flags are updated before the measurement results are available.



The update of the periodic result registers (PRMM\_PER\_NUM to PRMM\_PER\_LDORF and SECM\_PER\_NUM to SECM\_PER\_NPNISENSE) is done based on the bit field PRMM\_PER\_CTRL.PERCTRL and SECM\_PER\_CTRL.PERCTRL. When PERCTRL is set to auto, the result registers contain the latest generated results. Setting PERCTRL to ONCE initiates one update. After the update, the result registers are frozen. This mechanism allows reading of time aligned measurement data across multiple devices. PRMM\_PER\_NUM and SECM\_PER\_NUM contain the number of the periodic cycle in which the primary periodic results have been created, the other registers contain the measurement results.



Application usage: Measurement over a fixed time period; used for all undervoltage and overvoltage checks.

**Note:** PRMM\_PER\_CTRL and SECM\_PER\_CTRL must have the same setting. ALLM\_PER\_CTRL sets PRMM\_PER\_CTRL and SECM\_PER\_CTRL simultaneously.



### 7.4.3.2 Application timed measurement

The application timed measurement averages the measurement results between two capture commands. The time between the capture commands is up to the application, but must allow minimum 16 scan cycles and maximum 65534 scan cycles. If a capture is shorter than 16 measurements or longer than 65535 measurements, the results registers are set to invalid. A capture command means writing of PRMM\_APP\_CTRL[5:0] and/or SECM\_APP\_CTRL[9:6] with logic 1. The measurement results are made available in the application result registers (PRMM\_APP\_VC\_CNT to PRMM\_APP\_AIN3 and SECM\_APP\_AIN4 to SECM\_APP\_AIN7). Register PRMM\_APP\_VC\_CNT contains the number of cell voltage measurements performed within the last VC capture cycle. The other register contains the measured voltages. Bits PRMM\_MEAS\_STAT[5:0] and SECM\_MEAS\_STAT[3:0] signal that more than 16 measurements have been performed, which indicates that a new capture can be initiated.

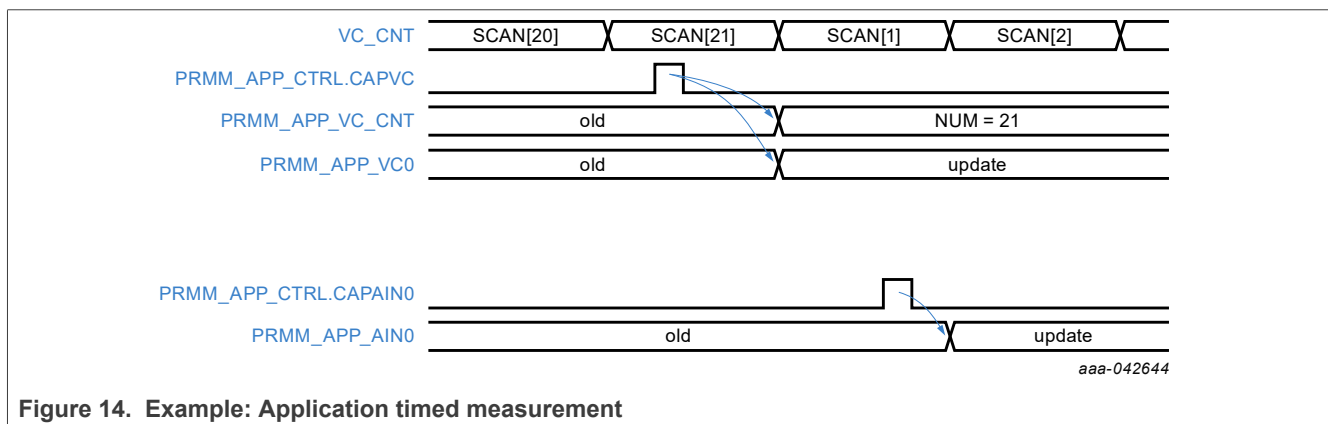


Figure 14. Example: Application timed measurement

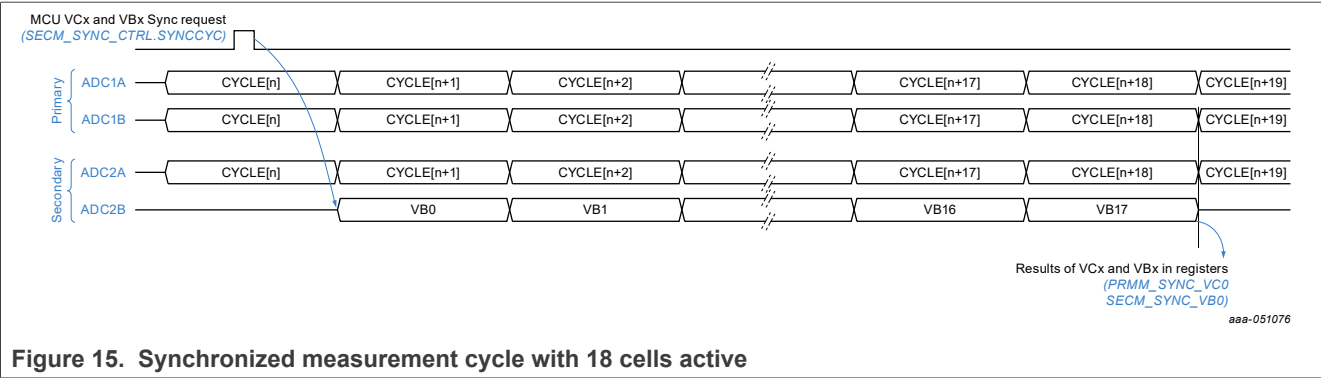
Application usage: Measurement over an MCU controlled time period.

### 7.4.3.3 Synchronized measurement

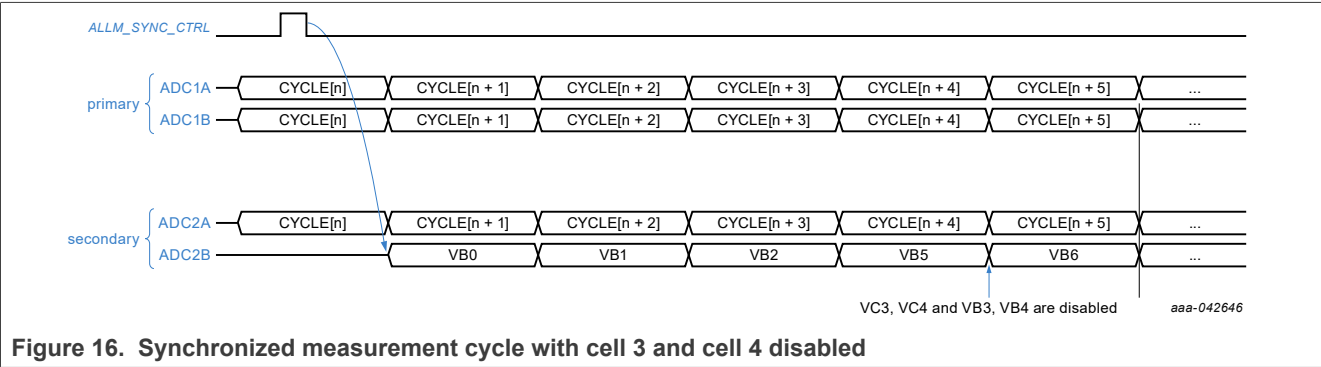
The synchronized measurement is a measurement of the primary and secondary voltages. The synchronized measurement is initiated by setting the bits PRMM\_SYNC\_CTRL.SYNCCYC and SECM\_SYNC\_CTRL.SYNCCYC. To ensure synchronous measurements, the bits must be set simultaneously. The bit ALLM\_SYNC\_CTRL.SYNCCYC can be used to set the PRMM\_SYNC\_CTRL.SYNCCYC and SECM\_SYNC\_CTRL.SYNCCYC simultaneously.

The synchronous measurement cycle starts with the next periodic measurement. ADC2B measures the cells continuously until the number of samples for one period is reached. ADC1A and ADC1B operate as usual. When ADC2B has completed the measurement for VB17, all the synchronous measurement result registers are updated. The secondary measurement registers are populated with the average results of ADC2B for the individual cells. The primary measurement registers are populated with the average results of ADC1A/ADC1B while ADC2B has measured the same cell. The bits PRMM\_MEAS\_STAT.SYNCRDY and SECM\_MEAS\_STAT.SYNCRDY signal the completion of the measurement.

The results of the synchronized measurement are available in the registers PRMM\_SYNC\_NUM to PRMM\_SYNC\_VC17 and SECM\_SYNC\_NUM to SECM\_SYNC\_VB17. PRMM\_SYNC\_NUM and SECM\_SYNC\_NUM contain the number of the synchronous cycle in which the synchronous results have been created, the other registers contain the measured voltages.



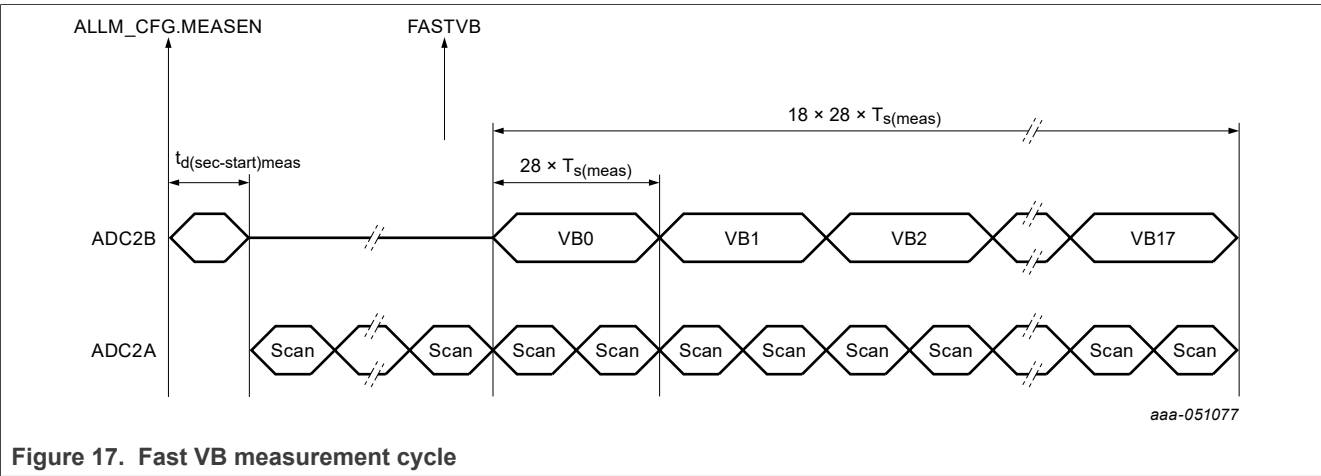
ADC2B skips cells that are disabled during a synchronized or fast VB measurement.



Application usage: Independent time synchronized measurement of the cell voltage.

7.4.3.4 Fast VB measurement

The fast VB measurement is a measurement of the VBx voltages. The fast VB measurement is initiated by setting the bit SECM\_SYNC\_CTRL.FASTVB. ADC2B measures each enabled VBx voltage for  $28 \times t_{s(meas)}$ . A fast VB measurement is started latest with the second scan cycle after the bit ALLM\_SYNC\_CTRL.FASTVB is set. The bit SECM\_MEAS\_STAT.FASTVBRDY signals the completion of the measurement. The averaged results for each channel are available in the registers SECM\_SYNC\_VB0 to SECM\_SYNC\_VB17.



Application usage: Check of the connectivity of VB terminals and open load detection.

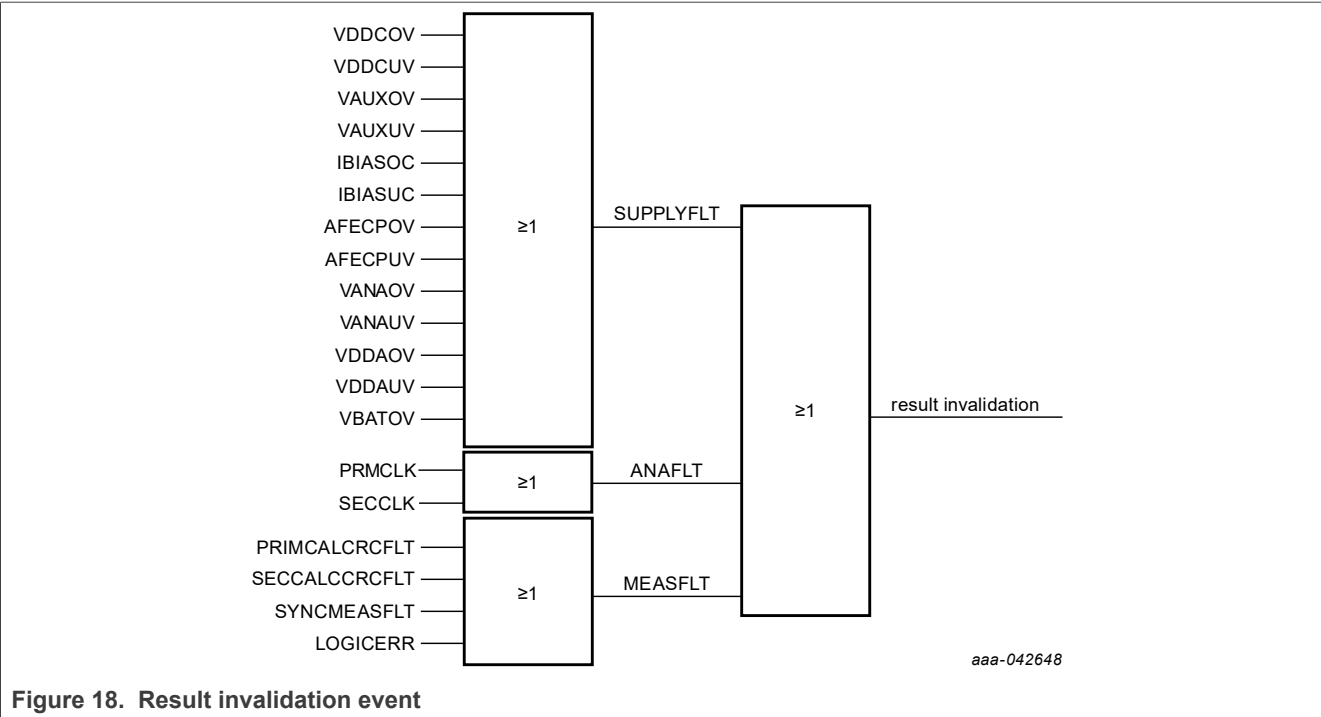
7.4.4 Invalidation of measurement results

The BMI7018 invalidates the measurement results in order to avoid usage of old or corrupted data. The code 8000h represents invalid data (see [Measurement data format](#)). [Table 17](#) gives an overview of the events and the result registers that are invalidated.

Table 17. Invalidation of measurement results

Event	Invalidated results	Comment
Transition into Active mode.	Primary and secondary measurement results.	
Read of a measurement register.	Register that was read.	The result is always invalidated, independently, of the communication success of the register to the MCU.
<a href="#">Faults leading to result invalidation</a>	Secondary synchronous measurement results (registers SECM_SYNC_VB0 to SECM_SYNC_VB17).	All primary results, the secondary periodic, and secondary application results are not invalidated.
<a href="#">Faults leading to result invalidation</a> with PRMM_AIN_CFG.FLTAPPINV set to 1.	Application measurement results of AIN0 to AIN3 and AINA (registers PRMM_APP_AIN0 to PRMM_APP_AIN3 and PRMM_APP_AINA).	Periodic results are not invalidated.
<a href="#">Faults leading to result invalidation</a> with SECM_AIN_CFG.FLTAPPINV set to 1.	Application measurement results of AIN4 to AIN7 (registers SECM_APP_AIN4 to SECM_APP_AIN7).	Periodic results are not invalidated.
Receiving of a capture command before 16 scans are performed.	Application measurements with fewer than 16 scans.	PRMM_APP_VC_CNT shows the actual number of scans performed.
Receiving of a capture command after 65535 scans are performed.	Application measurements with more than 65535 scans.	PRMM_APP_VC_CNT shows FFFFh.
Disabling of the measurement.	Primary and secondary measurement results.	

There are various sources that can lead to an erratic measurement. The fault events leading to a result invalidation are shown in [Figure 18](#).



**Note:** Figure 18 shows only the supply faults that can cause an invalidation of the results. All faults leading to a supply fault are shown in Table 9.

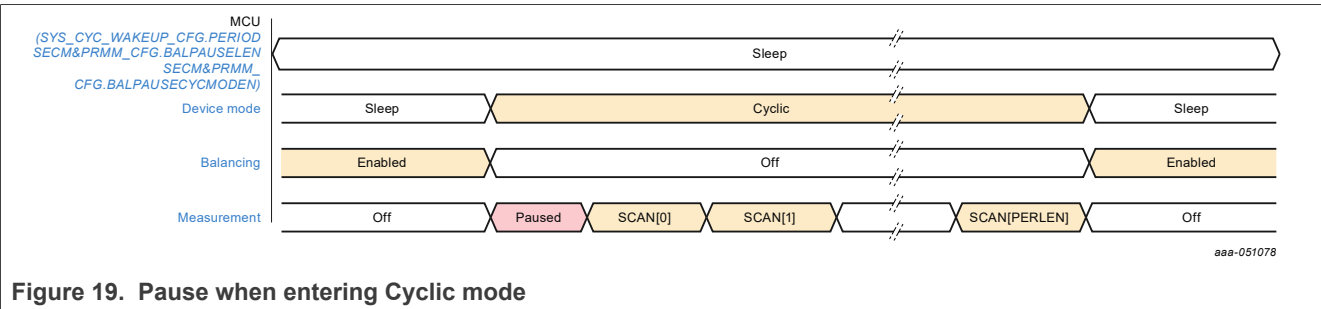
**Note:** VAUXUV, VAUXOV, VDDCUV, and VDDCOV only cause an invalidation of the results if they are used as references for the measurement.

7.4.5 Pausing of balancing

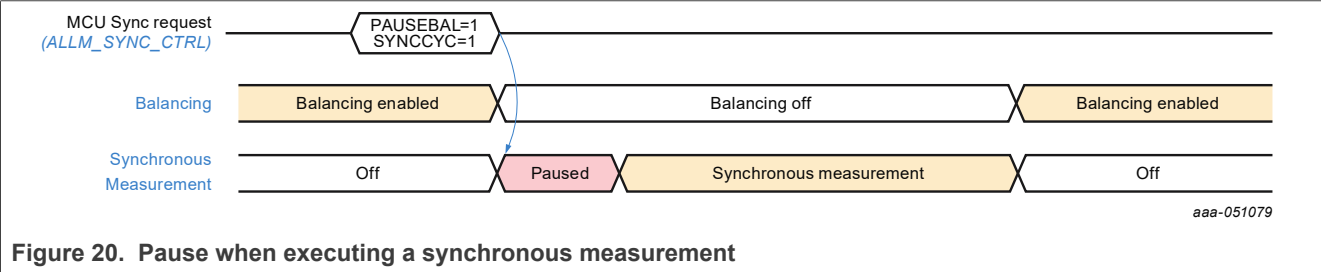
In a typical battery management system (BMS), each battery cell terminal is connected with a single wire to the application circuit of the BMI7018 (see Figure 55). An active cell balancing leads to voltage drop at the connectors and wirings. The voltage drop creates an undesired offset in the voltages measured by the BMI7018. To allow an accurate measurement, the BMI7018 provides the option to pause the balancing. To allow the external filters to settle to their steady state value, the measurement after start of a pause can be delayed.

The bit fields PRMM\_CFG.BALPAUSELEN and SECM\_CFG.BALPAUSELEN control the length of the pause before the measurement is started. In order to avoid generation of a SYNCMEASFLT, PRMM\_CFG.BALPAUSELEN, and SECM\_CFG.BALPAUSELEN must be set to the same value.

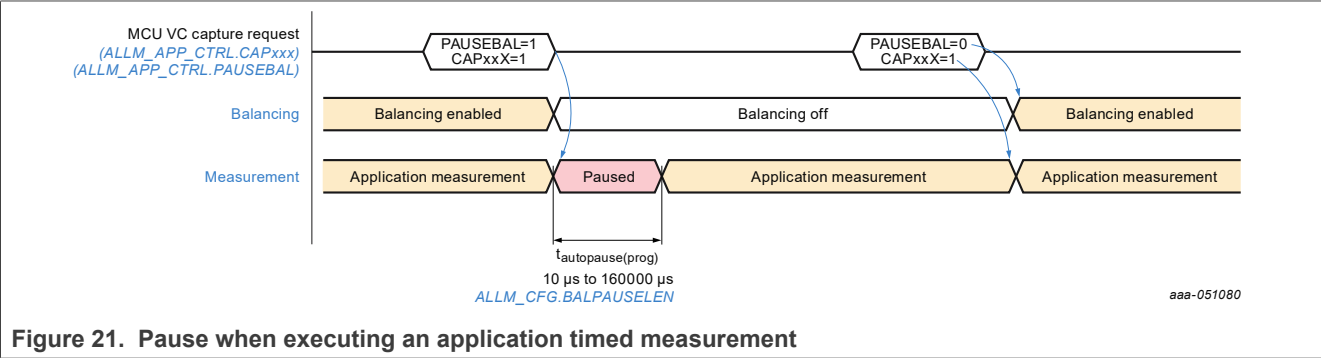
The bits PRMM\_CFG.BALPAUSECYCMODEN and SECM\_CFG.BALPAUSECYCMODEN force a balancing pause during the measurement and a pause after transitioning from Sleep to Cyclic mode and the start of the first measurement in Cyclic mode.



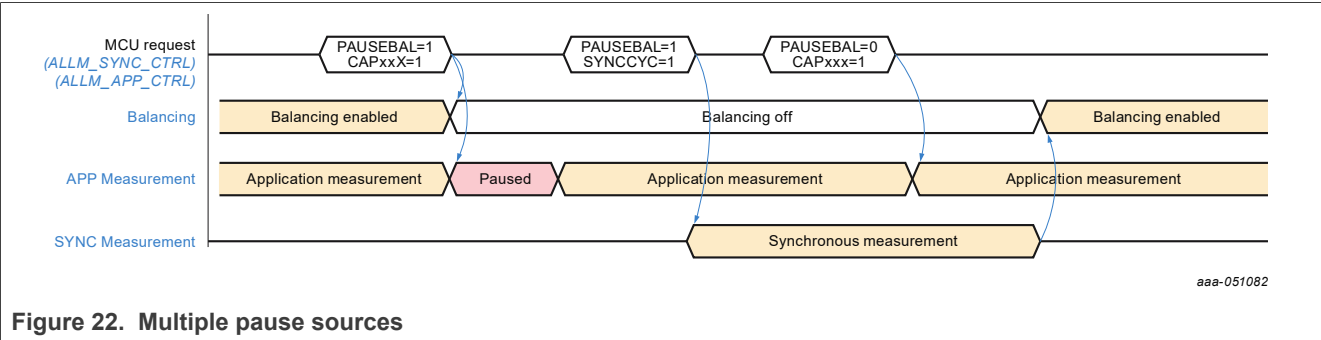
The bits PRMM\_SYNC\_CTRL.PAUSEBAL and SECM\_SYNC\_CTRL.PAUSEBAL allow forcing a pause for a synchronized measurement (Section 7.4.3.3) or a Fast VB measurement (Section 7.4.3.4).



The bits PRMM\_APP\_CTRL.PAUSEBAL and SECM\_SYNC\_APP\_CTRL.PAUSEBAL allow forcing a pause for an application timed measurement (Section 7.4.3.2).



In case one or more measurements with balancing are triggered, the IC keeps the balancing paused until the last measurement sequence is completed. If a different measurement pauses the balancing already, the new measurement is directly started without a pause.



**Note:** Keep the configuration for primary and secondary measurements identical to avoid triggering a SYNCMEASFLT. The usage of the ALLM\_xxx registers ensures primary and secondary measurements are set identical.

7.4.6 Registers for primary measurement

All registers related to the primary measurement are listed here. Details to the registers and the bitfields are explained in the register map section.

Table 18. Register overview: Primary\_Measurement\_Registers

Address	Name	Access	Reset	Description
1800h	<a href="#">PRMM_CFG</a>	R/W	0h	general measurement control
1801h	<a href="#">PRMM_APP_CTRL</a>	R/W	7C00h	application measurement control
1802h	<a href="#">PRMM_PER_CTRL</a>	R/W	10h	periodic measurement control
1803h	<a href="#">PRMM_SYNC_CTRL</a>	W	0h	synchronous measurement control
1808h	<a href="#">PRMM_VC_CFG0</a>	R/W	0h	cell voltage measurement enable
1809h	<a href="#">PRMM_VC_CFG1</a>	R/W	0h	cell voltage measurement enable
180Ah	<a href="#">PRMM_AIN_CFG</a>	R/W	20h	AINx measurement enables
180Bh	<a href="#">PRMM_AIN_OL_CFG</a>	R/W	0h	AINx open-load detection enable
180Ch	<a href="#">PRMM_VBUF_CFG</a>	R/W	3h	voltage buffer enable
1810h	<a href="#">PRMM_VC_OV_UV_CFG0</a>	R/W	0h	cell voltage overvoltage and undervoltage check enable
1811h	<a href="#">PRMM_VC_OV_UV_CFG1</a>	R/W	0h	cell voltage overvoltage and undervoltage check enable
1812h	<a href="#">PRMM_VC_OV_TH_CFG</a>	R/W	7FFFh	upper comparator limit for VC0 to VC17
1813h	<a href="#">PRMM_VC_UV0_TH_CFG</a>	R/W	0h	lower comparator limit 0 for VC0 to VC17
1814h	<a href="#">PRMM_VC_UV1_TH_CFG</a>	R/W	0h	lower comparator limit 1 for VC0 to VC17
1815h	<a href="#">PRMM_AIN0_OV_TH_CFG</a>	R/W	7FFFh	upper comparator limit for AIN0
1816h	<a href="#">PRMM_AIN1_OV_TH_CFG</a>	R/W	7FFFh	upper comparator limit for AIN1
1817h	<a href="#">PRMM_AIN2_OV_TH_CFG</a>	R/W	7FFFh	upper comparator limit for AIN2
1818h	<a href="#">PRMM_AIN3_OV_TH_CFG</a>	R/W	7FFFh	upper comparator limit for AIN3
1819h	<a href="#">PRMM_AINA_OV_TH_CFG</a>	R/W	7FFFh	upper comparator limit for AINA
181Ah	<a href="#">PRMM_AIN0_UV_TH_CFG</a>	R/W	8001h	lower comparator limit for AIN0
181Bh	<a href="#">PRMM_AIN1_UV_TH_CFG</a>	R/W	8001h	lower comparator limit for AIN1
181Ch	<a href="#">PRMM_AIN2_UV_TH_CFG</a>	R/W	8001h	lower comparator limit for AIN2
181Dh	<a href="#">PRMM_AIN3_UV_TH_CFG</a>	R/W	8001h	lower comparator limit for AIN3
181Eh	<a href="#">PRMM_AINA_UV_TH_CFG</a>	R/W	8001h	lower comparator limit for AINA
1820h	<a href="#">PRMM_CAL_CRC</a>	R/W	0h	CRC over calibration data
1821h	<a href="#">PRMM_CFG_CRC</a>	R	0h	CRC over configuration values
1822h	<a href="#">PRMM_VC_OV_FLT_STAT0</a>	R	0h	cell voltage overvoltage status
1823h	<a href="#">PRMM_VC_OV_FLT_STAT1</a>	R	0h	cell voltage overvoltage status
1824h	<a href="#">PRMM_VC_UV0_FLT_STAT0</a>	R	0h	cell voltage undervoltage status regarding limit 0
1825h	<a href="#">PRMM_VC_UV0_FLT_STAT1</a>	R	0h	cell voltage undervoltage status regarding limit 0
1826h	<a href="#">PRMM_VC_UV1_FLT_STAT0</a>	R	0h	cell voltage undervoltage status regarding limit 1
1827h	<a href="#">PRMM_VC_UV1_FLT_STAT1</a>	R	0h	cell voltage under-voltage status regarding limit 1
1828h	<a href="#">PRMM_AIN_OV_FLT_STAT</a>	R	0h	AINx overvoltage status
1829h	<a href="#">PRMM_AIN_UV_FLT_STAT</a>	R	0h	AINx undervoltage status
183Eh	<a href="#">PRMM_MEAS_STAT</a>	R	0h	measurement status
183Fh	<a href="#">PRMM_APP_VC_CNT</a>	R	0h	application measurement VC sample count number
1840h	<a href="#">PRMM_APP_VC0</a>	R	8000h	application measurement result cell 0
1841h	<a href="#">PRMM_APP_VC1</a>	R	8000h	application measurement result cell 1
1842h	<a href="#">PRMM_APP_VC2</a>	R	8000h	application measurement result cell 2
1843h	<a href="#">PRMM_APP_VC3</a>	R	8000h	application measurement result cell 3

Table 18. Register overview: Primary\_Measurement\_Registers...continued

Address	Name	Access	Reset	Description
1844h	<a href="#">PRMM_APP_VC4</a>	R	8000h	application measurement result cell 4
1845h	<a href="#">PRMM_APP_VC5</a>	R	8000h	application measurement result cell 5
1846h	<a href="#">PRMM_APP_VC6</a>	R	8000h	application measurement result cell 6
1847h	<a href="#">PRMM_APP_VC7</a>	R	8000h	application measurement result cell 7
1848h	<a href="#">PRMM_APP_VC8</a>	R	8000h	application measurement result cell 8
1849h	<a href="#">PRMM_APP_VC9</a>	R	8000h	application measurement result cell 9
184Ah	<a href="#">PRMM_APP_VC10</a>	R	8000h	application measurement result cell 10
184Bh	<a href="#">PRMM_APP_VC11</a>	R	8000h	application measurement result cell 11
184Ch	<a href="#">PRMM_APP_VC12</a>	R	8000h	application measurement result cell 12
184Dh	<a href="#">PRMM_APP_VC13</a>	R	8000h	application measurement result cell 13
184Eh	<a href="#">PRMM_APP_VC14</a>	R	8000h	application measurement result cell 14
184Fh	<a href="#">PRMM_APP_VC15</a>	R	8000h	application measurement result cell 15
1850h	<a href="#">PRMM_APP_VC16</a>	R	8000h	application measurement result cell 16
1851h	<a href="#">PRMM_APP_VC17</a>	R	8000h	application measurement result cell 17
1852h	<a href="#">PRMM_APP_AINA</a>	R	8000h	application measurement result AINA
1853h	<a href="#">PRMM_APP_AIN0</a>	R	8000h	application measurement result AIN0
1854h	<a href="#">PRMM_APP_AIN1</a>	R	8000h	application measurement result AIN1
1855h	<a href="#">PRMM_APP_AIN2</a>	R	8000h	application measurement result AIN2
1856h	<a href="#">PRMM_APP_AIN3</a>	R	8000h	application measurement result AIN3
185Fh	<a href="#">PRMM_PER_NUM</a>	R	0h	measurement period number of the primary periodic results
1860h	<a href="#">PRMM_PER_VC0</a>	R	8000h	periodic measurement result cell 0
1861h	<a href="#">PRMM_PER_VC1</a>	R	8000h	periodic measurement result cell 1
1862h	<a href="#">PRMM_PER_VC2</a>	R	8000h	periodic measurement result cell 2
1863h	<a href="#">PRMM_PER_VC3</a>	R	8000h	periodic measurement result cell 3
1864h	<a href="#">PRMM_PER_VC4</a>	R	8000h	periodic measurement result cell 4
1865h	<a href="#">PRMM_PER_VC5</a>	R	8000h	periodic measurement result cell 5
1866h	<a href="#">PRMM_PER_VC6</a>	R	8000h	periodic measurement result cell 6
1867h	<a href="#">PRMM_PER_VC7</a>	R	8000h	periodic measurement result cell 7
1868h	<a href="#">PRMM_PER_VC8</a>	R	8000h	periodic measurement result cell 8
1869h	<a href="#">PRMM_PER_VC9</a>	R	8000h	periodic measurement result cell 9
186Ah	<a href="#">PRMM_PER_VC10</a>	R	8000h	periodic measurement result cell 10
186Bh	<a href="#">PRMM_PER_VC11</a>	R	8000h	periodic measurement result cell 11
186Ch	<a href="#">PRMM_PER_VC12</a>	R	8000h	periodic measurement result cell 12
186Dh	<a href="#">PRMM_PER_VC13</a>	R	8000h	periodic measurement result cell 13
186Eh	<a href="#">PRMM_PER_VC14</a>	R	8000h	periodic measurement result cell 14
186Fh	<a href="#">PRMM_PER_VC15</a>	R	8000h	periodic measurement result cell 15
1870h	<a href="#">PRMM_PER_VC16</a>	R	8000h	periodic measurement result cell 16
1871h	<a href="#">PRMM_PER_VC17</a>	R	8000h	periodic measurement result cell 17
1872h	<a href="#">PRMM_PER_AINA</a>	R	8000h	periodic measurement result AINA
1873h	<a href="#">PRMM_PER_AIN0</a>	R	8000h	periodic measurement result AIN0

Table 18. Register overview: Primary\_Measurement\_Registers...continued

Address	Name	Access	Reset	Description
1874h	<a href="#">PRMM_PER_AIN1</a>	R	8000h	periodic measurement result AIN1
1875h	<a href="#">PRMM_PER_AIN2</a>	R	8000h	periodic measurement result AIN2
1876h	<a href="#">PRMM_PER_AIN3</a>	R	8000h	periodic measurement result AIN3
1877h	<a href="#">PRMM_PER_PRMTEMP</a>	R	8000h	periodic measurement result primary device temperature
1878h	<a href="#">PRMM_PER_SECVREF</a>	R	8000h	periodic measurement result secondary voltage reference
1879h	<a href="#">PRMM_PER_VAUX</a>	R	8000h	periodic measurement result auxiliary supply voltage
187Ah	<a href="#">PRMM_PER_VDDC</a>	R	8000h	periodic measurement result VDDC
187Fh	<a href="#">PRMM_SYNC_NUM</a>	R	0h	measurement period number of the synchronous results.
1880h	<a href="#">PRMM_SYNC_VC0</a>	R	8000h	synchronous measurement result cell 0
1881h	<a href="#">PRMM_SYNC_VC1</a>	R	8000h	synchronous measurement result cell 1
1882h	<a href="#">PRMM_SYNC_VC2</a>	R	8000h	synchronous measurement result cell 2
1883h	<a href="#">PRMM_SYNC_VC3</a>	R	8000h	synchronous measurement result cell 3
1884h	<a href="#">PRMM_SYNC_VC4</a>	R	8000h	synchronous measurement result cell 4
1885h	<a href="#">PRMM_SYNC_VC5</a>	R	8000h	synchronous measurement result cell 5
1886h	<a href="#">PRMM_SYNC_VC6</a>	R	8000h	synchronous measurement result cell 6
1887h	<a href="#">PRMM_SYNC_VC7</a>	R	8000h	synchronous measurement result cell 7
1888h	<a href="#">PRMM_SYNC_VC8</a>	R	8000h	synchronous measurement result cell 8
1889h	<a href="#">PRMM_SYNC_VC9</a>	R	8000h	synchronous measurement result cell 9
188Ah	<a href="#">PRMM_SYNC_VC10</a>	R	8000h	synchronous measurement result cell 10
188Bh	<a href="#">PRMM_SYNC_VC11</a>	R	8000h	synchronous measurement result cell 11
188Ch	<a href="#">PRMM_SYNC_VC12</a>	R	8000h	synchronous measurement result cell 12
188Dh	<a href="#">PRMM_SYNC_VC13</a>	R	8000h	synchronous measurement result cell 13
188Eh	<a href="#">PRMM_SYNC_VC14</a>	R	8000h	synchronous measurement result cell 14
188Fh	<a href="#">PRMM_SYNC_VC15</a>	R	8000h	synchronous measurement result cell 15
1890h	<a href="#">PRMM_SYNC_VC16</a>	R	8000h	synchronous measurement result cell 16
1891h	<a href="#">PRMM_SYNC_VC17</a>	R	8000h	synchronous measurement result cell 17



### 7.4.7 Registers for secondary measurement

All registers related to the secondary measurement are listed here. Details to the registers and the bitfields are explained in the register map section.

**Table 19. Register overview: Secondary\_Measurement\_Registers**

Address	Name	Access	Reset	Description
1C00h	<a href="#">SECM_CFG</a>	R/W	0h	general measurement control
1C01h	<a href="#">SECM_APP_CTRL</a>	W	0h	application measurement control
1C02h	<a href="#">SECM_PER_CTRL</a>	R/W	10h	periodic measurement control
1C03h	<a href="#">SECM_SYNC_CTRL</a>	R/W	7C00h	synchronous measurement control
1C08h	<a href="#">SECM_VB_CFG0</a>	R/W	0h	balance voltage measurement enable
1C09h	<a href="#">SECM_VB_CFG1</a>	R/W	0h	balance voltage measurement enable
1C0Ah	<a href="#">SECM_AIN_CFG</a>	R/W	80h	measurement enables for extra channel
1C0Bh	<a href="#">SECM_AIN_OL_CFG</a>	R/W	0h	AINx open-load detection enable
1C0Ch	<a href="#">SECM_VBUF_CFG</a>	R/W	3h	voltage buffer enable
1C20h	<a href="#">SECM_CAL_CRC</a>	R/W	0h	CRC over calibration data
1C21h	<a href="#">SECM_CFG_CRC</a>	R	0h	CRC over configuration values
1C3Eh	<a href="#">SECM_MEAS_STAT</a>	R	0h	measurement status
1C53h	<a href="#">SECM_APP_AIN4</a>	R	8000h	application measurement result AIN4
1C54h	<a href="#">SECM_APP_AIN5</a>	R	8000h	application measurement result AIN5
1C55h	<a href="#">SECM_APP_AIN6</a>	R	8000h	application measurement result AIN6
1C56h	<a href="#">SECM_APP_AIN7</a>	R	8000h	application measurement result AIN7
1C5Fh	<a href="#">SECM_PER_NUM</a>	R	0h	measurement period number of the secondary periodic results
1C73h	<a href="#">SECM_PER_AIN4</a>	R	8000h	periodic measurement result AIN4
1C74h	<a href="#">SECM_PER_AIN5</a>	R	8000h	periodic measurement result AIN5
1C75h	<a href="#">SECM_PER_AIN6</a>	R	8000h	periodic measurement result AIN6
1C76h	<a href="#">SECM_PER_AIN7</a>	R	8000h	periodic measurement result AIN7
1C77h	<a href="#">SECM_PER_SECTEMP</a>	R	8000h	periodic measurement result secondary device temperature
1C78h	<a href="#">SECM_PER_PRMVREF</a>	R	8000h	periodic measurement result primary voltage reference
1C79h	<a href="#">SECM_PER_VAUX</a>	R	8000h	periodic measurement result auxiliary supply voltage
1C7Ah	<a href="#">SECM_PER_VBAT</a>	R	8000h	periodic measurement result VBAT
1C7Bh	<a href="#">SECM_PER_VDDA</a>	R	8000h	periodic measurement result VDDA
1C7Ch	<a href="#">SECM_PER_VDDC</a>	R	8000h	periodic measurement result VDDC
1C7Eh	<a href="#">SECM_PER_NPNISENSE</a>	R	8000h	periodic measurement result NPN current sensor
1C7Fh	<a href="#">SECM_SYNC_NUM</a>	R	0h	measurement number of the secondary synchronous results
1C80h	<a href="#">SECM_SYNC_VB0</a>	R	8000h	synchronous measurement result from balancing pins cell 0.
1C81h	<a href="#">SECM_SYNC_VB1</a>	R	8000h	synchronous measurement result from balancing pins cell 1
1C82h	<a href="#">SECM_SYNC_VB2</a>	R	8000h	synchronous measurement result from balancing pins cell 2
1C83h	<a href="#">SECM_SYNC_VB3</a>	R	8000h	synchronous measurement result from balancing pins cell 3
1C84h	<a href="#">SECM_SYNC_VB4</a>	R	8000h	synchronous measurement result from balancing pins cell 4
1C85h	<a href="#">SECM_SYNC_VB5</a>	R	8000h	synchronous measurement result from balancing pins cell 5
1C86h	<a href="#">SECM_SYNC_VB6</a>	R	8000h	synchronous measurement result from balancing pins cell 6

Table 19. Register overview: Secondary\_Measurement\_Registers...continued

Address	Name	Access	Reset	Description
1C87h	<a href="#">SECM_SYNC_VB7</a>	R	8000h	synchronous measurement result from balancing pins cell 7
1C88h	<a href="#">SECM_SYNC_VB8</a>	R	8000h	synchronous measurement result from balancing pins cell 8
1C89h	<a href="#">SECM_SYNC_VB9</a>	R	8000h	synchronous measurement result from balancing pins cell 9
1C8Ah	<a href="#">SECM_SYNC_VB10</a>	R	8000h	synchronous measurement result from balancing pins cell 10
1C8Bh	<a href="#">SECM_SYNC_VB11</a>	R	8000h	synchronous measurement result from balancing pins cell 11
1C8Ch	<a href="#">SECM_SYNC_VB12</a>	R	8000h	synchronous measurement result from balancing pins cell 12
1C8Dh	<a href="#">SECM_SYNC_VB13</a>	R	8000h	synchronous measurement result from balancing pins cell 13
1C8Eh	<a href="#">SECM_SYNC_VB14</a>	R	8000h	synchronous measurement result from balancing pins cell 14
1C8Fh	<a href="#">SECM_SYNC_VB15</a>	R	8000h	synchronous measurement result from balancing pins cell 15
1C90h	<a href="#">SECM_SYNC_VB16</a>	R	8000h	synchronous measurement result from balancing pins cell 16
1C91h	<a href="#">SECM_SYNC_VB17</a>	R	8000h	synchronous measurement result from balancing pins cell 17

### 7.4.8 Registers for all measurement

The registers block [All Measurement Registers](#) is writing simultaneously into the primary and the secondary measurement registers. This mechanism provides a comfortable way of ensuring the measurement configuration registers are set simultaneously for the primary and secondary measurement chain. A read back of the All Measurement Registers is not possible. The BMI7018 returns 0000h as data in case one of the All Measurement Registers is read.

Table 20. Register overview: All\_Measurement\_Registers

Address	Name	Access	Reset	Description
1400h	<a href="#">ALLM_CFG</a>	W	0h	general measurement control
1401h	<a href="#">ALLM_APP_CTRL</a>	W	7C00h	application measurement control
1402h	<a href="#">ALLM_PER_CTRL</a>	W	10h	periodic measurement control
1403h	<a href="#">ALLM_SYNC_CTRL</a>	W	7C00h	synchronous measurement control
1408h	<a href="#">ALLM_VCVB_CFG0</a>	W	0h	cell voltage measurement enable
1409h	<a href="#">ALLM_VCVB_CFG1</a>	W	0h	cell voltage measurement enable

## 7.5 Cell balancing

The cell voltage-balancing function allows discharging individual cells based on external resistors and PWM modulated currents controlled by the BMI7018. A constant current mode-balancing feature permits to limit the current variation due to the cell voltage. Because of the balancing structure, the balancing switches are enabled alternatively depending of their position on the module (odd/even). Different PWM duty cycle can be used to define the average current. The internal switches can be controlled by individual balancing timers and/or by the cell voltage. Additionally, the balancing process can be interrupted based on an external temperature sensor in order to manage the heat dissipation of the balancing resistors.

### 7.5.1 Functions

The BMI7018 allows two main balancing modes:

- Timer-based balancing
- Cell voltage-based balancing

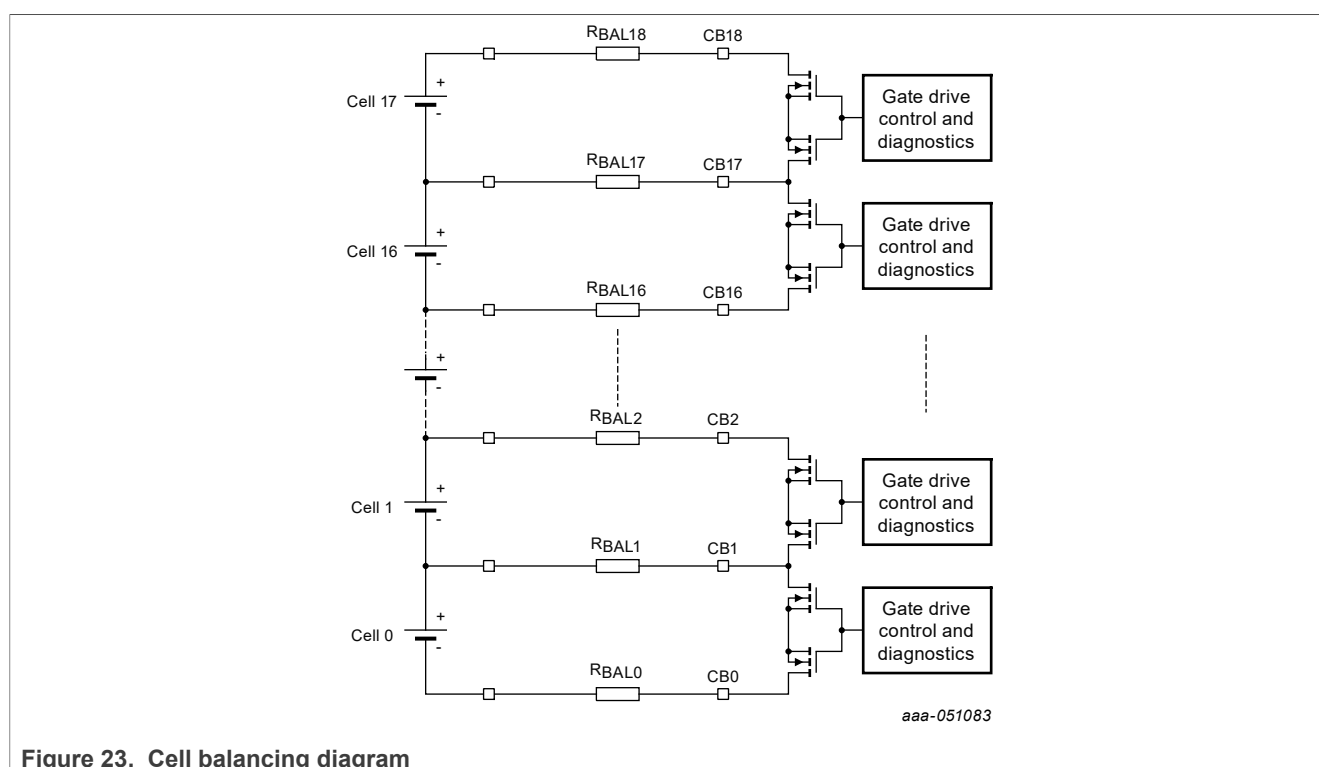
Combining of balancing modes is possible.

Other balancing functions enhance the balancing functionality.

- Global balancing timeout
- Global cell undervoltage-based balancing
- Temperature modulated balancing
- Junction temperature balancing protection
- Constant current balancing
- prebalancing timer
- PWM
- Auto pause
- Emergency discharge
- Analog switch monitoring

### 7.5.1.1 Cell balancing diagram

The cell-balancing circuit uses two back-to-back MOSFET transistors for each cell to support negative cell voltages.



### 7.5.2 Functional diagram

[Figure 24](#) shows the functional diagram of the balancing functionality.

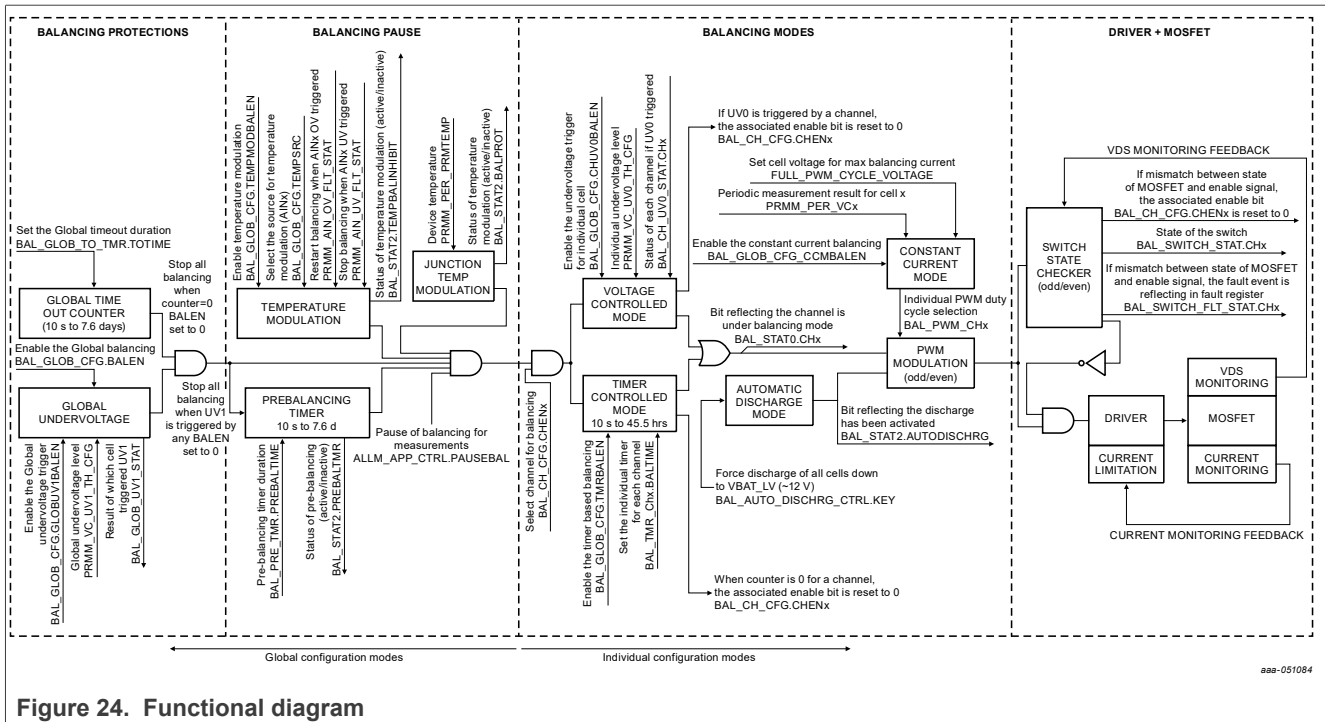


Figure 24. Functional diagram

## 7.5.3 Functional description

During balancing, odd and even balance MOSFET banks are alternatively enabled at the fixed frequency  $f_{\text{PWM}(\text{bal})}$ . The following are descriptions of the different balancing modes.

### 7.5.3.1 Timer-based balancing

The timer-based balancing allows a time-controlled discharge of the cells. The discharge time for the cells can be set individually for the channels. Individual discharge time is set by writing into the registers `BAL_TMR_CH0` to `BAL_TMR_CH17`. Writing into `BAL_TMR_CH_ALL` sets all registers `BAL_TMR_CH0` to `BAL_TMR_CH17` simultaneously. If the timer-based balancing is active, the balancing timer counter counts down every 10 seconds. Once the timer for a cell expires, the balancing action for this cell stops.

To enable timer-based balancing, the bits `BAL_GLOB_CFG.BALEN` and `BAL_GLOB_CFG.TMRBALEN` must be logic 1. `BAL_GLOB_TO_TMR.TOTIME` must be non-zero.

The timer-based balancing can be combined with the other balancing functions. The other enabled balancing functions can cause an interruption of the balancing activity. During the interruption, the balancing timer of the affected channel does not decrement.

**Note:** Even if timer-based balancing is not enabled `BAL_GLOB_CFG.TMRBALEN = 0`, writing 0 in any `BAL_TMR_CHx` register will stop the balancing of the corresponding channel and will be reported in the corresponding `BAL_CH_CFG` register (`CHENx` bit set to 0). Writing any other value will have no effect on the balancing.

Application usage: Timer-based balancing is a state-of-the-art way for cell balancing.

### 7.5.3.2 Cell undervoltage based balancing

The cell voltage-balancing function allows discharging of a cell until the cell reaches the undervoltage threshold set in `PRMM_VC_UV0_TH_CFG`. For the monitoring of the cell voltage, the primary measurement chain is used.

To enable cell undervoltage-based balancing, the bits `BAL_GLOB_CFG.BALEN` and `BAL_GLOB_CFG.CHUV0BALEN` must be logic 1. `BAL_GLOB_TO_TMR.TOTIME` must be non-zero.

The cell undervoltage-based balancing can be combined with the other balancing functions. Other enabled balancing functions can cause an interruption or complete stop of the balancing activity.

Application usage: Cell undervoltage-based balancing is a new way for cell balancing. It discharges the cells to the `PRMM_VC_UV0_TH_CFG` threshold.

**Note:** *The cyclic measurement must be active to allow cell voltage-measurement updates. If cyclic measurements are disabled, the balancing continues until the global balancing timeout function stops the discharge.*

### 7.5.3.3 Global undervoltage based balancing

The global undervoltage-balancing function allows discharging of a cell until one cell reaches the undervoltage threshold `PRMM_VC_UV1_TH_CFG`. For the monitoring of the cell voltages, the primary measurement chain is used.

To enable global undervoltage-based balancing, the bits `BAL_GLOB_CFG.BALEN` and `BAL_GLOB_CFG.GLOBUV1BALEN` must be logic 1. `BAL_GLOB_TO_TMR.TOTIME` must be non-zero.

The global undervoltage-based balancing can be combined with the other balancing functions. Other enabled balancing functions can cause an interruption or complete stop of the balancing activity.

Application usage: Global undervoltage-based balancing is a protection feature to avoid deep discharge of cells because of current consumption of the IC during balancing.

**Note:** *The cyclic measurement must be active to allow cell voltage-measurement updates. If cyclic measurements are disabled, the balancing continues until the global balancing timeout function stops the discharge.*

### 7.5.3.4 Global balancing timeout

The global-balancing timeout timer is used to configure the maximum balancing time for all balancing activities. The counter counts down every 10 seconds as soon as its value is non-zero, independent of any other conditions. Once the timer expires, the balancing switches are switched OFF. The bit `BAL_GLOB_CFG.BALEN` is set to logic 0. The global-balancing timeout timer and the balancing timers for the individual channels use independent clock sources. In case balancing actions are intended, the global-balancing timeout should be set long enough to allow the needed balancing activities.

Application usage: Global timeout is protection feature to avoid deep discharge.

### 7.5.3.5 prebalancing timer

The prebalancing timer `BAL_PRE_TMR` allows delaying or pausing of the balancing activity. The counter decrements as soon as bit `BAL_GLOB_CFG.BALEN` is set logic 1. Once the counter is expired, the balancing activity is enabled. The prebalancing timer holds the timers for the timer-based balancing. The prebalancing timer has no impact on the global balancing timeout.

Application usage: The prebalancing timer can be set to allow a cooldown of the system before the balancing activity is started.

### 7.5.3.6 Temperature-modulated balancing

The temperature-modulated balancing is an add-on to the other balancing functions. It cannot be used standalone. This mode is activated when `BAL_GLOB_CFG.TEMPMODBALEN` is set to 1. The source of the temperature-modulated balancing can be selected with `BAL_GLOB_CFG.TEMPSRC`. Only AIN0 to AIN3 can

be used. The temperature-modulated balancing works with a two-point approach. The balancing is stopped once the selected analog-input pin falls below the lower comparator limit (register [PRMM\\_AIN0\\_UV\\_TH\\_CFG](#) to [PRMM\\_AIN3\\_UV\\_TH\\_CFG](#)). If timer-based balancing is active, the balancing timers are on hold as well. The global balancing timeout timer continues. Once the selected analog input pin exceeds the upper comparator limit (register [PRMM\\_AIN0\\_OV\\_TH\\_CFG](#) to [PRMM\\_AIN3\\_OV\\_TH\\_CFG](#)), the balancing activity is started again. The cell balancing timers decrement again.

Application usage: Temperature-modulated balancing allows thermal management during balancing.

**Note:** *The cyclic measurement must be active to allow updates of the AIN pin measurements. If cyclic measurements are disabled, the balancing is not modulated.*

### 7.5.3.7 PWM for balancing

The PWM for balancing allows operating the activated analog balancing switch in PWM mode. The PWM duty cycle is controlled with registers BAL\_PWM\_CH0 to BAL\_PWM\_CH17 and can be set from 0 to 100 % by 0.39 % step.

Application usage: PWM for balancing allows thermal management during balancing.

### 7.5.3.8 Constant current cell balancing

The Constant Current Cell Balancing mode allows to balance with a constant current based on a fixed balancing resistor and a changing cell voltage. The Constant Current mode balancing feature permits to have less variation of the balancing current versus cell voltage. It adapts automatically the PWM duty cycle of the activated balancing channels based on their primary periodic measurement results. This mode is activated when BAL\_GLOB\_CFG.CCMBALLEN is set to 1.

As the balancing current depends on the external balancing resistor, to keep a constant balancing current, a configurable full PWM cycle voltage register (register [FULL\\_PWM\\_CYCLE\\_VOLTAGE](#)) sets the minimum cell voltage on which the balancing is operating at the maximum current (100 % ON in respective odd or even sequence). The PWM duty cycle can be calculated from the following equation

$$[\text{PWM}] \text{ _DutyCycle} = V_{\text{(Cell\_min)}} / V_{\text{Cell}}.$$

BAL\_PWM\_CH0 to BAL\_PWM\_CH17 registers are automatically updated with the last duty cycle calculated by the device.

Application usage: PWM for balancing allows constant current during balancing.

### 7.5.3.9 Analog balancing switch monitoring

The analog balancing switch does the actual switching of the balancing current. It is implemented for each channel. Each switch has a current limitation circuit. Each switch is monitored for the correct status when the switch is enabled for monitoring (BAL\_SWITCH\_MON\_CFG) and the balancing is enabled (BAL\_GLOB\_CFG.BALEN = 1).

A violation of the status is detected when the voltage across the corresponding CB pins is:

- Above the output fault detection voltage threshold, when the switch shall be closed
- Below the output fault detection voltage threshold, when the switch shall be open

**Note:** *Connectivity of the CB pins is checked via the cell balancing terminal pulldown resistors in the measurement block (see [Section 7.7.2](#)).*

Application usage: Execution and monitoring of balancing activities.

### 7.5.3.10 Junction temperature balancing protection

The Junction Temperature Balancing mode is an additional protection to avoid the risk of over temperature on the die during balancing sequence. It cannot be deactivated. It is enabled when balancing operation is enabled.

Balancing of all cells are interrupted when the internal IC primary junction temperature measurement is above the junction temperature upper threshold for cell balancing thermal protection. If timer-based balancing is active, the balancing timers are on hold as well. The individual balancing timers will resume automatically when the internal IC primary junction temperature measurement has decreased by the junction temperature hysteresis for cell balancing thermal protection and the cell balancing timers decrement again.

The pause does not affect the global balancing timeout timer.

### 7.5.3.11 Auto pause

The auto pause feature is implemented as part of the measurement function. The cell balancing function receives the pause signal, which temporarily inhibits the cell balancing. The balancing function holds the individual balancing timer. The pause does not influence the global timeout timer.

Application usage: The auto pause feature is used to avoid influence of the balancing activity on the secondary cell voltage measurement.

### 7.5.3.12 Automatic discharge

The automatic discharge functionality allows an emergency discharge of the cells. The discharge is started by writing the enable key (DEADh) into register BAL\_AUTO\_DISCHRG\_CTRL. Once the automatic discharge is enabled, the balancing switches are turned on with 100 % duty cycle. The discharge is stopped by writing the disable key (2152h) into register BAL\_AUTO\_DISCHRG\_CTRL or when a supply low-voltage condition occurs.

The automatic discharge is the only balancing feature that can be active in case the BAL\_GLOB\_CFG.BALEN is logic 0. Automatic discharge is independent of the temperature modulation. The global balancing timeout has no influence on the automatic discharge, but when the automatic discharge is active, the global balancing timeout timer is on hold. In case an overvoltage condition on VBAT is present during auto discharge, the automatic discharge is put on hold. The global balancing timeout timer is resuming from hold. Clearing of the overvoltage error flag (FEH\_SUPPLY\_FLT\_STAT0.VBATOV) enables the auto discharge again. The global balancing timeout timer is again put on hold.

In case a switch error on a balancing switch is detected, the affected channel is turned off.

## 7.5.4 Cell balancing process

### 7.5.4.1 Start of balancing

The bit BAL\_GLOB\_CFG.BALEN is the global enabling bit for the balancing circuit. All balancing related functions, including diagnostics are only active if the bit is set to logic 1.

### 7.5.4.2 Balancing operation

During balancing in Active mode, the BMI7018 is operating the same way as without balancing. Once the balancing activity of a channel is completed, the individual balancing enable bit BAL\_CH\_CFG.CHEN0 to CHEN17 for this channel is cleared.

When the cyclic wake-up function is used, the BMI7018 enters into Cyclic mode at the selected set time interval. In Cyclic mode, one periodic measurement is performed. The measurement results are used for the voltage- and temperature-based balancing functionality.



### 7.5.4.3 Completion of balancing

When all individual balancing enable bits BAL\_CH\_CFG.CHEN0 to BAL\_CH\_CFG.CHEN17 are cleared, the balancing activity is finished. The bit BAL\_GLOB\_CFG.BALEN is reset and the bit BAL\_STAT1.RDY is set to logic 1.

The following conditions clear the balancing enable bits:

- Global balancing timer is expired
- Timer-based balancing is activated and all activated individual balancing timers are expired
- Global undervoltage based balancing is activated and one activated cell has reached the global undervoltage threshold
- Cell undervoltage based balancing is activated and all activated cells have reached the undervoltage threshold

**Note:** The BMI7018 does not report the reason for clearing the individual enable bits.

### 7.5.5 Cell balancing diagnostics

The BMI7018 provides diagnostic to monitor the integrity of the balancing operation. Connectivity of the CB pins is checked via the cell balancing terminal pulldown resistors in the measurement block (see [Section 7.7.2](#)).

#### 7.5.5.1 Switch status monitoring

Registers BAL\_SWITCH\_STAT0 and BAL\_SWITCH\_STAT1 provide for each switch the status (open or closed).

#### 7.5.5.2 Analog balancing switch monitoring

The analog balancing switch monitoring does the monitoring of each individual switch. Registers BAL\_SWITCH\_FLT\_STAT0 and BAL\_SWITCH\_FLT\_STAT1 provide, for each switch, a fault indication. Any deviation of the physical state of the balancing circuit from the intended one is considered as a fault.

Each switch is monitored for the correct status, overcurrent, and open-load detection circuit with a separate enable.

Application usage: Execution and monitoring of balancing activities.

### 7.5.6 Cell balancing registers

All registers related to the cell balancing are listed here. Details on the registers and the bit fields are explained in the register map section.

**Table 21. Register overview: Balancing\_Registers**

Address	Name	Access	Reset	Description
1000h	<a href="#">BAL_GLOB_CFG</a>	R/W	0h	The global balancing configuration register is used to configure the balancing modes.
1001h	<a href="#">BAL_GLOB_TO_TMR</a>	R/W	0h	The Global Balancing timeout timer register is used to configure the maximum balancing time for all balancing activities to make sure that in case of fault the balancing switches are switched OFF.
1002h	<a href="#">BAL_CH_CFG0</a>	R/W	0h	balancing channel individual enable channel 0 - 15
1003h	<a href="#">BAL_CH_CFG1</a>	R/W	0h	balancing channel individual enable channel 16 - 17
1004h	<a href="#">BAL_PRE_TMR</a>	R/W	0h	prebalancing timer
1005h	<a href="#">BAL_AUTO_DISCHRG_CTRL</a>	R/W	2152h	emergency discharge enable



Table 21. Register overview: Balancing\_Registers...continued

Address	Name	Access	Reset	Description
1006h	<a href="#">BAL_SWITCH_MON_CFG0</a>	R/W	FFFFh	balancing switch monitoring enable
1007h	<a href="#">BAL_SWITCH_MON_CFG1</a>	R/W	3h	balancing switch monitoring enable
1008h	<a href="#">FULL_PWM_CYCLE_VOLTAGE</a>	R/W	0h	full PWM cycle voltage
1009h	<a href="#">BAL_CH_UV0_STAT0</a>	R	0h	channel undervoltage balancing status channel 0 - 15
100Ah	<a href="#">BAL_CH_UV0_STAT1</a>	R	0h	channel undervoltage balancing status channel 16 - 17
100Bh	<a href="#">BAL_GLOB_UV1_STAT0</a>	R	0h	global undervoltage balancing status channel 0 - 15
100Ch	<a href="#">BAL_GLOB_UV1_STAT1</a>	R	0h	global undervoltage balancing status channel 16 - 17
100Dh	<a href="#">BAL_STAT0</a>	R	0h	logical balancing channel status channel 0 - 15
100Eh	<a href="#">BAL_STAT1</a>	R	0h	logical balancing channel status channel 16 - 17
100Fh	<a href="#">BAL_STAT2</a>	R	0h	balancing status
1010h	<a href="#">BAL_SWITCH_STAT0</a>	R	0h	physical balancing channel status channel 0 - 15
1011h	<a href="#">BAL_SWITCH_STAT1</a>	R	0h	physical balancing channel status channel 16 - 17
1012h	<a href="#">BAL_SWITCH_FLT_STAT0</a>	R	0h	balancing switch fault channel 0 - 15
1013h	<a href="#">BAL_SWITCH_FLT_STAT1</a>	R	0h	balancing switch fault channel 16 - 17
101Fh	<a href="#">BAL_TMR_CH_ALL</a>	W	0h	virtual register, writes in parallel into BAL_TMR_CH0 up to BAL_TMR_CH17
1020h	<a href="#">BAL_TMR_CH0</a>	R/W	0h	balancing timer channel 0
1021h	<a href="#">BAL_TMR_CH1</a>	R/W	0h	balancing timer channel 1
1022h	<a href="#">BAL_TMR_CH2</a>	R/W	0h	balancing timer channel 2
1023h	<a href="#">BAL_TMR_CH3</a>	R/W	0h	balancing timer channel 3
1024h	<a href="#">BAL_TMR_CH4</a>	R/W	0h	balancing timer channel 4
1025h	<a href="#">BAL_TMR_CH5</a>	R/W	0h	balancing timer channel 5
1026h	<a href="#">BAL_TMR_CH6</a>	R/W	0h	balancing timer channel 6
1027h	<a href="#">BAL_TMR_CH7</a>	R/W	0h	balancing timer channel 7
1028h	<a href="#">BAL_TMR_CH8</a>	R/W	0h	balancing timer channel 8
1029h	<a href="#">BAL_TMR_CH9</a>	R/W	0h	balancing timer channel 9
102Ah	<a href="#">BAL_TMR_CH10</a>	R/W	0h	balancing timer channel 10
102Bh	<a href="#">BAL_TMR_CH11</a>	R/W	0h	balancing timer channel 11
102Ch	<a href="#">BAL_TMR_CH12</a>	R/W	0h	balancing timer channel 12
102Dh	<a href="#">BAL_TMR_CH13</a>	R/W	0h	balancing timer channel 13
102Eh	<a href="#">BAL_TMR_CH14</a>	R/W	0h	balancing timer channel 14
102Fh	<a href="#">BAL_TMR_CH15</a>	R/W	0h	balancing timer channel 15
1030h	<a href="#">BAL_TMR_CH16</a>	R/W	0h	balancing timer channel 16
1031h	<a href="#">BAL_TMR_CH17</a>	R/W	0h	balancing timer channel 17
1032h	<a href="#">BAL_PWM_CH_ALL</a>	W	FFh	virtual register, writes in parallel into BAL_PWM_CH0 up to BAL_PWM_CH17
1033h	<a href="#">BAL_PWM_CH0</a>	R/W	FFh	balancing PWM channel 0
1034h	<a href="#">BAL_PWM_CH1</a>	R/W	FFh	balancing PWM channel 1
1035h	<a href="#">BAL_PWM_CH2</a>	R/W	FFh	balancing PWM channel 2
1036h	<a href="#">BAL_PWM_CH3</a>	R/W	FFh	balancing PWM channel 3

Table 21. Register overview: Balancing\_Registers...continued

Address	Name	Access	Reset	Description
1037h	<a href="#">BAL_PWM_CH4</a>	R/W	FFh	balancing PWM channel 4
1038h	<a href="#">BAL_PWM_CH5</a>	R/W	FFh	balancing PWM channel 5
1039h	<a href="#">BAL_PWM_CH6</a>	R/W	FFh	balancing PWM channel 6
103Ah	<a href="#">BAL_PWM_CH7</a>	R/W	FFh	balancing PWM channel 7
103Bh	<a href="#">BAL_PWM_CH8</a>	R/W	FFh	balancing PWM channel 8
103Ch	<a href="#">BAL_PWM_CH9</a>	R/W	FFh	balancing PWM channel 9
103Dh	<a href="#">BAL_PWM_CH10</a>	R/W	FFh	balancing PWM channel 10
103Eh	<a href="#">BAL_PWM_CH11</a>	R/W	FFh	balancing PWM channel 11
103Fh	<a href="#">BAL_PWM_CH12</a>	R/W	FFh	balancing PWM channel 12
1040h	<a href="#">BAL_PWM_CH13</a>	R/W	FFh	balancing PWM channel 13
1041h	<a href="#">BAL_PWM_CH14</a>	R/W	FFh	balancing PWM channel 14
1042h	<a href="#">BAL_PWM_CH15</a>	R/W	FFh	balancing PWM channel 15
1043h	<a href="#">BAL_PWM_CH16</a>	R/W	FFh	balancing PWM channel 16
1044h	<a href="#">BAL_PWM_CH17</a>	R/W	FFh	balancing PWM channel 17

### 7.5.7 Balancing related registers

The most important registers related to the balancing function and the related content are shown in [Table 22](#).

Table 22. Balancing related registers

Register	Content
PRMM_AIN0_OV_TH_CFG ( <a href="#">Section 12.1.147</a> )	upper comparator limit for AIN0
PRMM_AIN1_OV_TH_CFG ( <a href="#">Section 12.1.148</a> )	upper comparator limit for AIN1
PRMM_AIN2_OV_TH_CFG ( <a href="#">Section 12.1.149</a> )	upper comparator limit for AIN2
PRMM_AIN3_OV_TH_CFG ( <a href="#">Section 12.1.150</a> )	upper comparator limit for AIN3
PRMM_AIN0_UV_TH_CFG ( <a href="#">Section 12.1.152</a> )	lower comparator limit for AIN0
PRMM_AIN1_UV_TH_CFG ( <a href="#">Section 12.1.153</a> )	lower comparator limit for AIN1
PRMM_AIN2_UV_TH_CFG ( <a href="#">Section 12.1.154</a> )	lower comparator limit for AIN2
PRMM_AIN3_UV_TH_CFG ( <a href="#">Section 12.1.155</a> )	lower comparator limit for AIN3
PRMM_VC_UV1_TH_CFG ( <a href="#">Section 12.1.146</a> )	lower comparator limit 1 for VC0 to VC17
PRMM_VC_UV0_TH_CFG ( <a href="#">Section 12.1.145</a> )	lower comparator limit 0 for VC0 to VC17

## 7.6 GPIO pins

The GPIO pins allow a flexible usage for specific application functions. The functionalities offered by the GPIOs are:

- Analog input for auxiliary (ratiometric) measurements (all GPIO pins)
- Analog input for auxiliary (absolute) measurements (all GPIO pins and AINA pin)
- General-purpose inputs (all GPIO pins)
- General-purpose outputs (all GPIO pins)
- Wake input (GPIO0 and GPIO1)
- Alarm input (GPIO1)

- Alarm output (AINA)
- I<sup>2</sup>C-bus leader interface (GPIO4 and GPIO5)

Each pin offers several functionalities. [Table 23](#) shows an overview of the pins and the functions.

**Table 23. GPIO functions**

Pin	Function
GPIO0	<ol style="list-style-type: none"> <li>1. Analog input AIN0 for ratiometric measurement to VAUX or VDDC</li> <li>2. Analog input AIN0 for absolute measurement</li> <li>3. General-purpose input 0</li> <li>4. General-purpose output 0</li> <li>5. Wake-up input 0</li> </ol>
GPIO1	<ol style="list-style-type: none"> <li>1. Analog input AIN1 for ratiometric measurement to VAUX or VDDC</li> <li>2. Analog input AIN1 for absolute measurement</li> <li>3. General-purpose input 1</li> <li>4. General-purpose output 1</li> <li>5. Wake-up input 1</li> <li>6. Alarm input</li> </ol>
GPIO2	<ol style="list-style-type: none"> <li>1. Analog input AIN2 for ratiometric measurement to VAUX or VDDC</li> <li>2. Analog input AIN2 for absolute measurement</li> <li>3. General-purpose input 2</li> <li>4. General-purpose output 2</li> </ol>
GPIO3	<ol style="list-style-type: none"> <li>1. Analog input AIN3 for ratiometric measurement to VAUX or VDDC</li> <li>2. Analog input AIN3 for absolute measurement</li> <li>3. General-purpose input 3</li> <li>4. General-purpose output 3</li> </ol>
GPIO4	<ol style="list-style-type: none"> <li>1. Analog input AIN4 for ratiometric measurement to VAUX or VDDC</li> <li>2. Analog input AIN4 for absolute measurement</li> <li>3. General-purpose input 4</li> <li>4. General-purpose output 4</li> <li>5. I<sup>2</sup>C-bus SCL</li> </ol>
GPIO5	<ol style="list-style-type: none"> <li>1. Analog input AIN5 for ratiometric measurement to VAUX or VDDC</li> <li>2. Analog input AIN5 for absolute measurement</li> <li>3. General-purpose input 5</li> <li>4. General-purpose output 5</li> <li>5. I<sup>2</sup>C-bus SDA</li> </ol>
GPIO6	<ol style="list-style-type: none"> <li>1. Analog input AIN6 for ratiometric measurement to VAUX or VDDC</li> <li>2. Analog input AIN6 for absolute measurement</li> <li>3. General-purpose input 6</li> <li>4. General-purpose output 6</li> </ol>
GPIO7	<ol style="list-style-type: none"> <li>1. Analog input AIN7 for ratiometric measurement to VAUX or VDDC</li> <li>2. Analog input AIN7 for absolute measurement</li> <li>3. General-purpose input 7</li> <li>4. General-purpose output 7</li> </ol>
AINA	<ol style="list-style-type: none"> <li>1. Analog input AINA for absolute measurement</li> <li>2. Alarm output</li> </ol>

Configuring a special function (wake, alarm, I<sup>2</sup>C-bus) sets the configuration of the GPIO pin automatically for this functionality. More than one function can be selected.

When a pin is configured as analog input, an external low-pass filter is mandatory. If no external low-pass filter is present, the analog measurement functionality must be disabled. Configuring I<sup>2</sup>C-bus functionality and general-purpose output functionality results in I<sup>2</sup>C-bus functionality. General-purpose output settings are ignored in this case.

### 7.6.1 Analog input

The primary measurement chain measures the voltage at GPIO0 to GPIO3 and AINA.

The secondary measurement chain measures the voltage at GPIO4 to GPIO7.

**Note:** During cyclic measurement of the BMI7018, only the primary measurement chain is active. GPIO4 to GPIO7 cannot be monitored in cyclic mode.

**Note:** The leakage current of  $I_{L(GPIO)}$  is for GPIO2 to GPIO7 only guaranteed if VDDC is available. If GPIO2 and GPIO3 shall be measured in cyclic mode, VDDC must be enabled (set bit `SYS_SUPPLY_CFG.VDDCCYC` to logic 1).

Details on the measurement functionality are in the [measurement section](#).

Application usage: Analog voltage measurements for various functions, such as temperature-based balancing (GPIO0 to GPIO3), voltage measurements, and independent voltage measurements.

### 7.6.2 I<sup>2</sup>C-bus leader interface

GPIO4 and GPIO5 offer an I<sup>2</sup>C-bus leader interface.

Details on the I<sup>2</sup>C-bus leader interface functionality are in the [I<sup>2</sup>C-bus interface section](#).

Application usage: Communication to other components, i.e., external EEPROM, near-field communication (NFC).

### 7.6.3 General-purpose input

All GPIO pins offer a general-purpose input functionality.

The bits `GPIO_CFG0.INPEN0` to `GPIO_CFG0.INPEN7` enable the pin for input. The bits `GPIO_IN.IN0` to `GPIO_IN.IN7` reflect the status of the pin. The bits `GPIO_IN.HIGHDET0` to `GPIO_IN.HIGHDET7` provide the info whether a high level was present at the pin since the last read command.

Application usage: Reading of digital input signals.

### 7.6.4 General-purpose output

All GPIO pins offer a general-purpose output functionality.

The bits `GPIO_CFG0.OUTEN0` to `GPIO_CFG0.OUTEN7` enable the pin for output. The bits `GPIO_CFG1.ODEN0` to `GPIO_CFG1.ODEN7` configure the output pin for open-drain configuration. The bits `GPIO_OUT.OUT0` to `GPIO_OUT.OUT7` set the state for the output.

Application usage: Driving of digital outputs signals.

### 7.6.5 Wake input

GPIO0 and GPIO1 offer a wake-up input functionality. `FEH_WAKEUP_CFG0.WAKEUPIN` configures GPIO0 as wake-up input. `FEH_WAKEUP_CFG0.ALARMIN` configures GPIO1 as wake-up input.

**Note:** GPIO0 expects an active HIGH signal. GPIO1 can be configured for acting on active HIGH, active LOW, or heartbeat signals.

Application usage: Wake-up of the system on external triggers.

7.6.6 Alarm input

GPIO1 offers an alarm input functionality. FEH\_ALARM\_CFG.ALARMIN configures GPIO1 as alarm input. See [Section 7.2](#) on how to use the alarm input event.

**Note:** An alarm reported in FEH\_ALARM\_OUT\_REASON0.ALARMIN should be re-checked by the pack controller. To such purpose, the pack controller may clear the flag (set it to 0) to check if the error is reconfirmed.

Application usage: Wake-up of the system by alarms.

7.6.7 GPIO registers

All registers related to the GPIOs are listed here. Details to the registers and the bit fields are explained in the register map section.

Table 24. Register overview: GPIO\_Registers

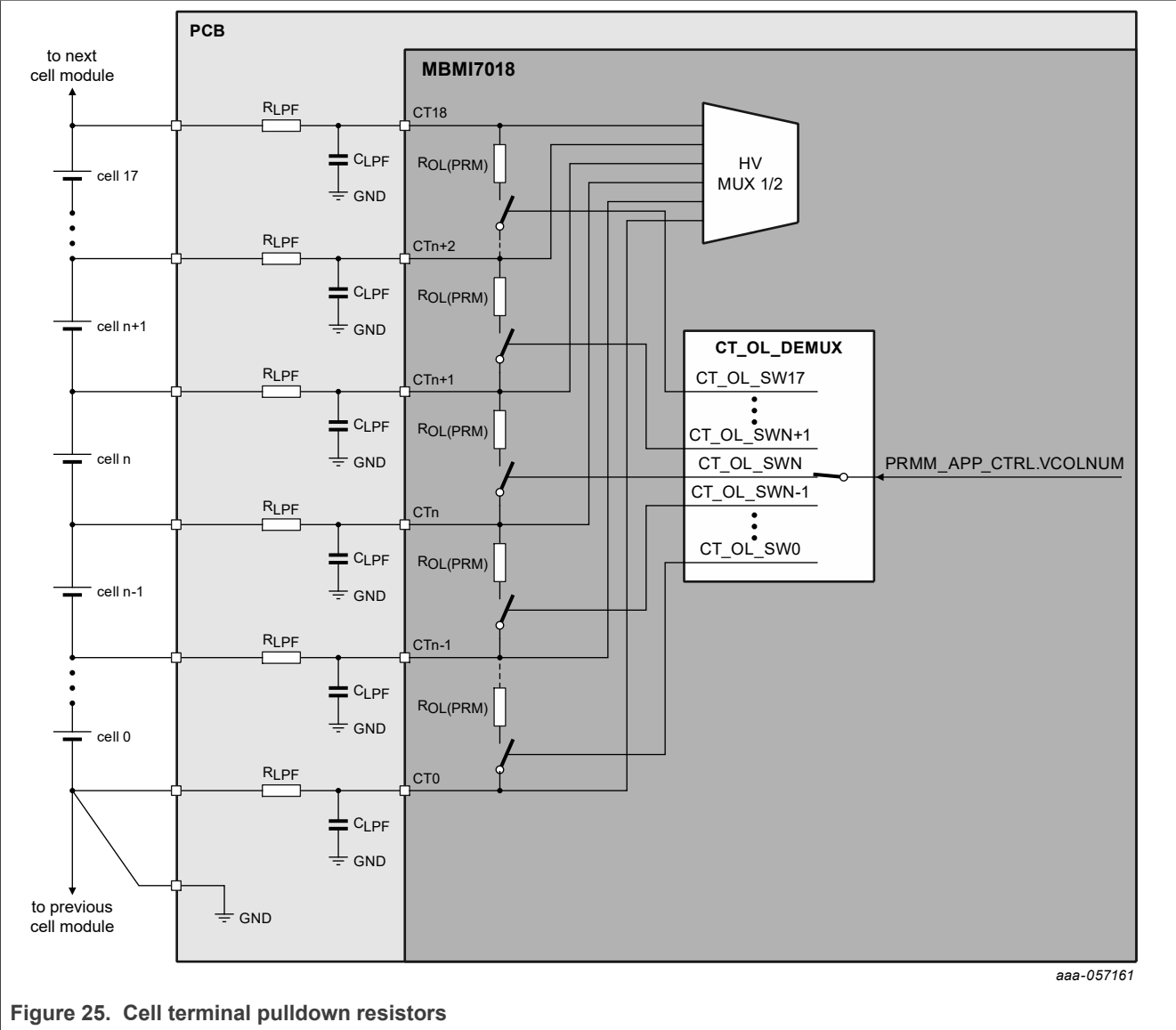
Address	Name	Access	Reset	Description
800h	<a href="#">GPIO_CFG0</a>	R/W	0h	GPIO configuration 0
801h	<a href="#">GPIO_CFG1</a>	R/W	0h	GPIO configuration 1
802h	<a href="#">GPIO_OUT</a>	R/W	0h	GPIO output
804h	<a href="#">GPIO_IN</a>	R	0h	GPIO input

7.7 Diagnostics

The BMI7018 provides diagnostic options to validate the integrity of the measurement chain.

7.7.1 Cell-terminal pulldown resistors (CTx pins)

The BMI7018 allows turning on a pulldown resistor between two adjacent cell terminal pins.



PRMM\_APP\_CTRL.VCOLNUM selects which switch is closed. Maximum one switch closes at one moment in time.

Application usage: Monitoring of the cell terminal connectivity and testing of the multiplexer functionality.

7.7.2 Cell-balancing terminal pulldown resistors (CBx pins)

The BMI7018 allows turning on a pulldown resistor network between two adjacent cell-balancing terminal pins.

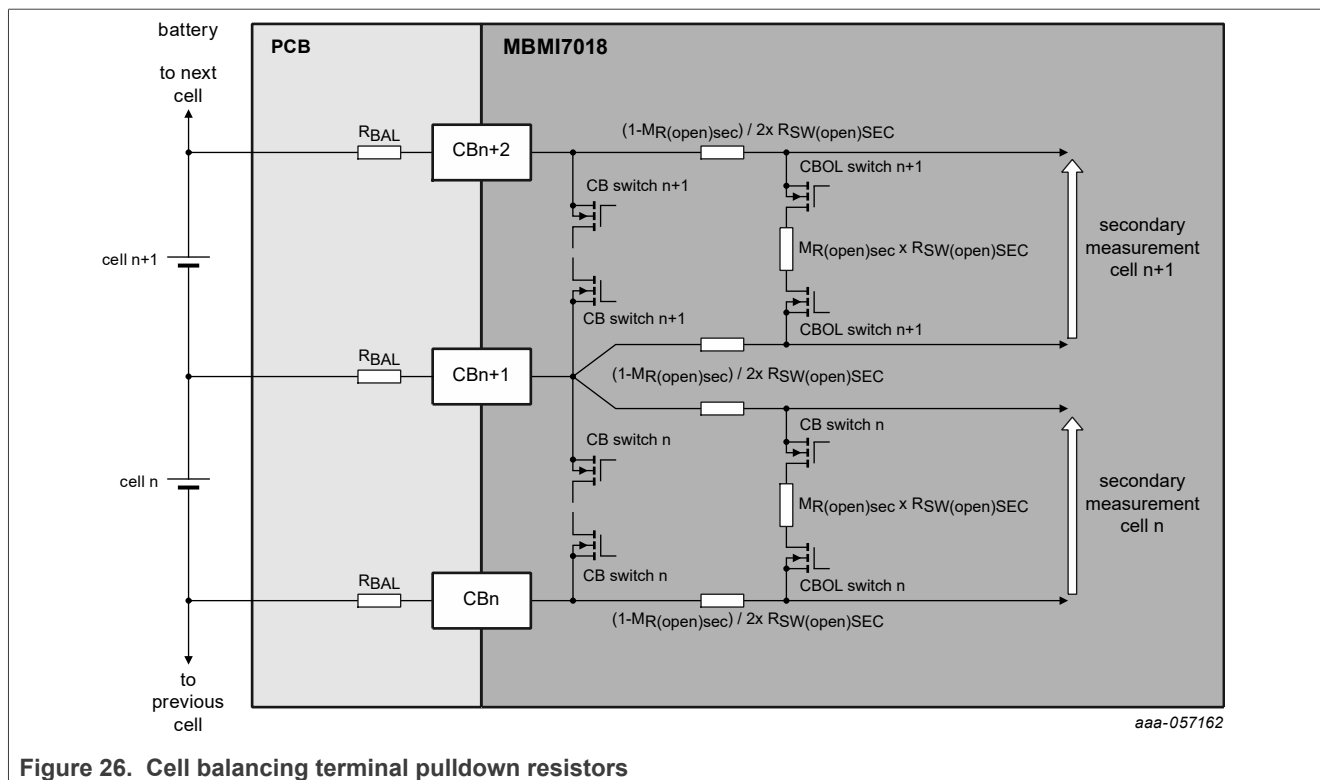


Figure 26. Cell balancing terminal pulldown resistors

SECM\_SYNC\_CTRL.VBOLNUM selects which switch is closed. Possible options are:

- One selected switch is closed (SECM\_SYNC\_CTRL.VBOLNUM is set to 0d to 17d)
- The BMI7018 closes the switch for the channel ADC2B is measuring (SECM\_SYNC\_CTRL.VBOLNUM is set to 30d = 1Eh)
- No switch is closed (SECM\_SYNC\_CTRL.VBOLNUM is set to 1Fh)

Maximum one switch closes at one moment in time.

Application usage: Monitoring of the cell balancing terminal connectivity and testing of the multiplexer functionality.

### 7.7.3 AINx terminal pulldown resistors (AINx pins)

The BMI7018 allows turning on a pulldown resistor for each individual analog input pin to GND.

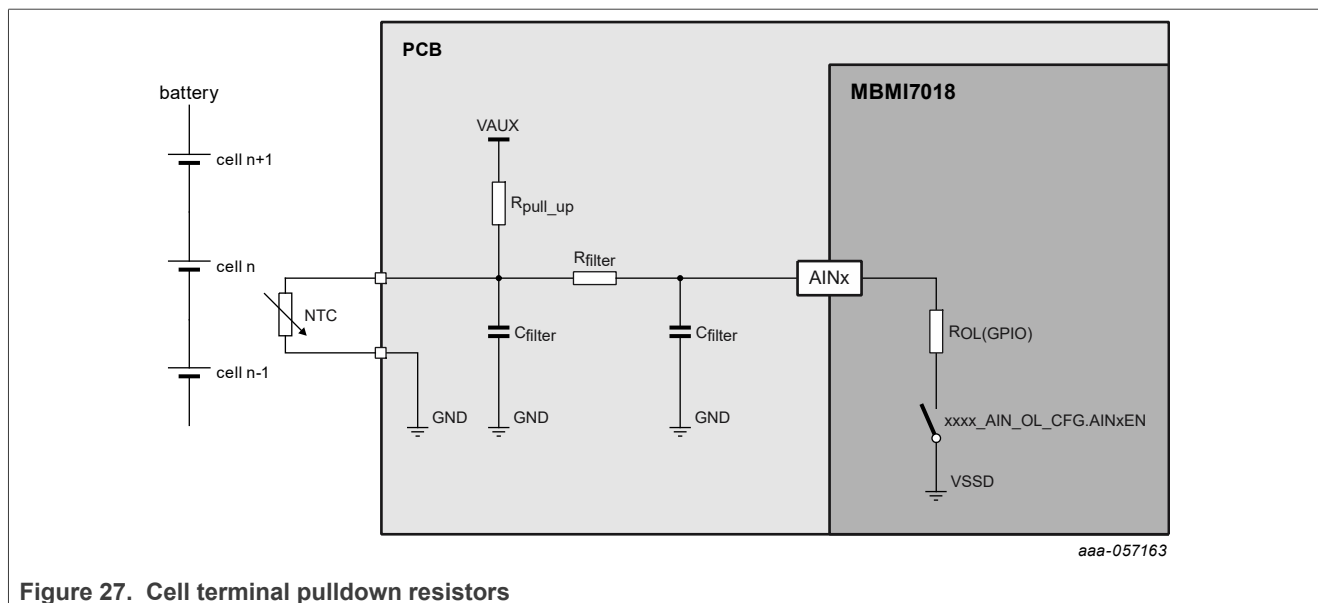


Figure 27. Cell terminal pulldown resistors

PRMM\_AIN\_OL\_CFG.AIN0EN to PRMM\_AIN\_OL\_CFG.AIN3EN and PRMM\_AIN\_OL\_CFG\_AINAEN control the OL\_DETECT\_SW for AIN0 to AIN3 and AINA.

SECM\_AIN\_OL\_CFG.AIN4EN to SECM\_AIN\_OL\_CFG.AIN7EN control the OL\_DETECT\_SW for AIN4 to AIN7.

Application usage: Monitoring of the connectivity of the AIN pins and testing of the multiplexer functionality.

#### 7.7.4 Calibration CRCs

The BMI7018 is calibrated at the end of the device production line. The calibration data is protected by a CRC. In case the register PRMM\_CAL\_CRC or SECM\_CAL\_CRC contains the value BEEFh, the calibration data is intact. If a different value is returned, the calibration data may be corrupted. Performance of devices with corrupted calibration data must not be trusted. The bit PRIMCALCRCFLT is signaling that a fault on the primary calibration data is detected. The bit SECCALCRCFLT is signaling a fault on the secondary calibration data. Both error bits result in a result invalidation trigger ([Figure 18](#)).

**Note:** Even when the BMI7018 provides error bits for the calibration CRC faults, the MCU must check the PRMM\_CAL\_CRC and SECM\_CAL\_CRC register content as well.

Application usage: Check of integrity of the calibration.

#### 7.7.5 Measurement status bits

The registers PRMM\_MEAS\_STAT and SECM\_MEAS\_STAT contain several status bits. The bits MEASFLT, ANAFLT, and SUPPLYFLT signal faults that lead to invalidation of the measurement results (see [Section 7.4.4](#)). The bit COMFLT has no direct influence on the measurement, but is included in the registers as important diagnostic information.

The bits SYNCRDY and PERRDY signal that the new synchronized measurement results (see [Section 7.4.4](#)) or the new periodic measurement results (see [Section 7.4.3.3](#)) are available. The bits APPRDYVC, APPRDYAIN0 to APPRDYAIN7, and APPRDYAINA signal that new application timed measurement results can be requested (see [Section 7.4.3.1](#)).

Application usage: Monitoring of the measurement chains.



### 7.7.6 Synchronization monitoring

The purpose of a synchronous measurement is to measure with the primary and secondary measurement chain the same input at the same moment in time. To ensure that the measurements are performed at the same moment in time, the BMI7018 monitors the synchronicity of the measurement chains during a synchronous measurement cycle. In case a deviation is detected, the bit SYNCMEASFLT is set. Reasons for deviations could be that the values of PRMM\_PER\_CTRL.PERLEN and SECM\_PER\_CTRL.PERLEN are unequal, the PRMM\_SYNC\_CTRL.SYNCCYC and SECM\_SYNC\_CTRL.SYNCCYC are not set simultaneously. Also differences in the enabled cells in the PRMM\_VC\_CFG and SECM\_VB\_CFG result in a SYNCMEASFLT.

Application usage: Ensure synchronicity of the measurement chains during a synchronous measurement cycle.

### 7.8 I<sup>2</sup>C-bus interface

The I<sup>2</sup>C-bus block allows communication to other components on the printed-circuit board (PCB), i.e., EEPROM, NFC. The device acts as I<sup>2</sup>C-bus leader. The I<sup>2</sup>C-bus leader module creates I<sup>2</sup>C-bus transactions as configured via the microcontroller interface. The BMI7018 executes the I<sup>2</sup>C-bus transaction autonomously. An ongoing transaction has no impact on other blocks and can be executed parallel to any other task of the BMI7018.

The I<sup>2</sup>C-bus interface is compliant to NXP [UM10204](#) for I<sup>2</sup>C-bus operation in Standard mode. The interface also supports Fast mode and Fast mode plus.

Transactions with a length below 14 bytes (including the device address) can be set up in one communication frame. If longer transactions are needed, the I<sup>2</sup>C-bus is held until the next part of the transaction has been set up. The I<sup>2</sup>C-bus offers various diagnostic information to allow a monitoring of the I<sup>2</sup>C-bus from the application microcontroller.

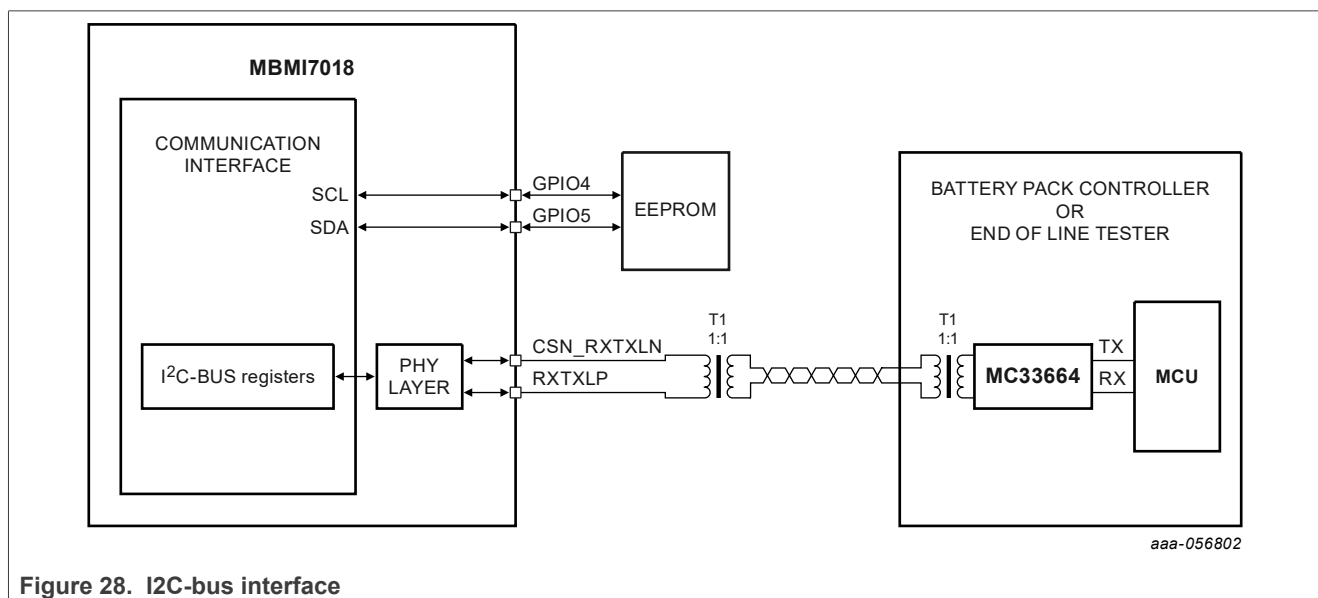


Figure 28. I<sup>2</sup>C-bus interface

Register I2C\_CFG allows enabling and disabling of the interface and setting the I<sup>2</sup>C-bus clock frequency. Register I2C\_CTRL initiates I<sup>2</sup>C-bus communication. Register I2C\_STAT provides the status information of the interface. The data registers (I2C\_DATA0 to I2C\_DATA17) contain the actual data to be transmitted. After a read operation, the data read on the I<sup>2</sup>C-bus is stored in the data registers.

To ensure that all I<sup>2</sup>C-bus transitions are correct, it must be avoid sending the BMI7018 to Sleep mode while a transaction is pending.

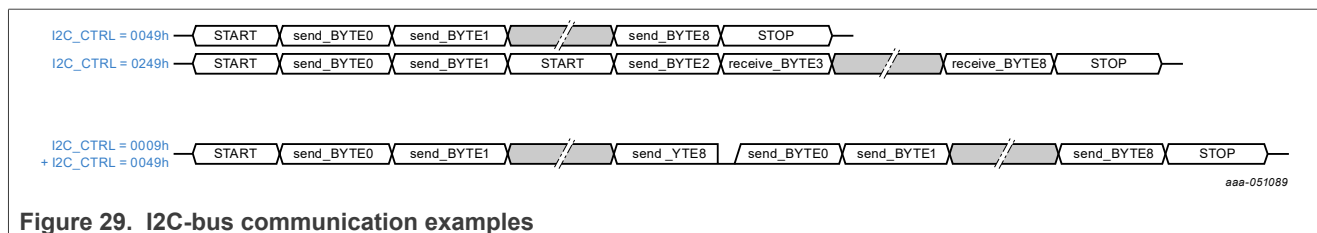


Figure 29 shows some possible I<sup>2</sup>C-bus transactions. The first line is a write command. The second line is a write with a switch to read. The third transaction shows a long sequence using two I<sup>2</sup>C-bus transactions. Direct read commands, without using the switch to read function, are supported, as well. NXP [UM10204](#) provides details about the I<sup>2</sup>C-bus.

### 7.8.1 I<sup>2</sup>C-bus registers

All registers related to the I<sup>2</sup>C-bus interface are listed here. Details to the registers and the bitfields are explained in the register map section.

Table 25. Register overview: I2C\_Registers

Address	Name	Access	Reset	Description
C00h	<a href="#">I2C_CFG</a>	R/W	0h	I2C configuration
C01h	<a href="#">I2C_CTRL</a>	R/W	0h	I2C control
C02h	<a href="#">I2C_STAT</a>	R	0h	I2C status
C04h	<a href="#">I2C_DATA0</a>	R/W	0h	I2C data register 0
C05h	<a href="#">I2C_DATA1</a>	R/W	0h	I2C data register 1
C06h	<a href="#">I2C_DATA2</a>	R/W	0h	I2C data register 2
C07h	<a href="#">I2C_DATA3</a>	R/W	0h	I2C data register 3
C08h	<a href="#">I2C_DATA4</a>	R/W	0h	I2C data register 4
C09h	<a href="#">I2C_DATA5</a>	R/W	0h	I2C data register 5
C0Ah	<a href="#">I2C_DATA6</a>	R/W	0h	I2C data register 6
C0Bh	<a href="#">I2C_DATA7</a>	R/W	0h	I2C data register 7
C0Ch	<a href="#">I2C_DATA8</a>	R/W	0h	I2C data register 8
C0Dh	<a href="#">I2C_DATA9</a>	R/W	0h	I2C data register 9
C0Eh	<a href="#">I2C_DATA10</a>	R/W	0h	I2C data register 10
C0Fh	<a href="#">I2C_DATA11</a>	R/W	0h	I2C data register 11
C10h	<a href="#">I2C_DATA12</a>	R/W	0h	I2C data register 12
C11h	<a href="#">I2C_DATA13</a>	R/W	0h	I2C data register 13
C12h	<a href="#">I2C_DATA14</a>	R/W	0h	I2C data register 14
C13h	<a href="#">I2C_DATA15</a>	R/W	0h	I2C data register 15
C14h	<a href="#">I2C_DATA16</a>	R/W	0h	I2C data register 16
C15h	<a href="#">I2C_DATA17</a>	R/W	0h	I2C data register 17

## 7.9 Microcontroller interface

The microcontroller interface facilitates the communication between the microcontroller and the BMI7018. The interface is based on registers and exchanges data, i.e., the voltage measurements and GPIO pin status information.

The microcontroller interface features:

- Single leader - multiple follower communication
- Flexible or fixed frame length options (64-, 80-, 96-, and 112-bit frames)

Communication is done via SPI or TPL. The frame format for SPI and TPL communication is equivalent.

### 7.9.1 TPL3 message format

Command and response frames are exchanged primarily between a single leader and a single follower. Broadcast commands can be transmitted from one leader to multiple followers. The purpose of the command and response transactions is to read and write to registers within the BMI7018 register map.

The BMI7018 uses TPL3 protocol, which supports messages with a length of 64 bits, 80 bits, 96 bits, and 112 bits. The dynamic message-length feature reduces the number of transactions for read/write of consecutive registers.

The BMI7018 defines a set of fields that constitute the message format.

#### 7.9.1.1 TPL3 message structure

The device supports dynamic message length.

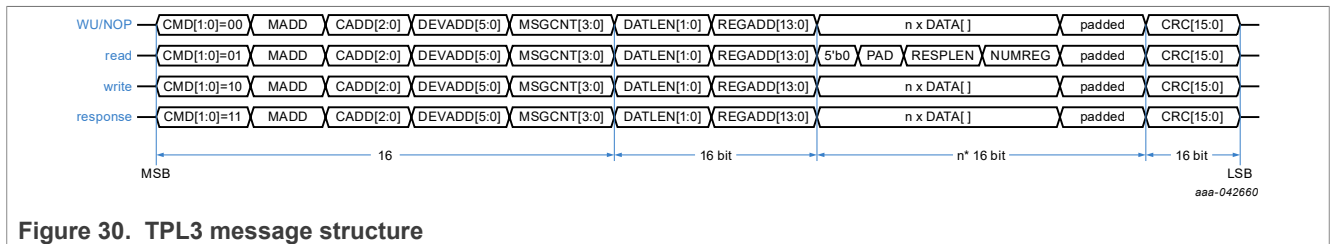


Figure 30. TPL3 message structure

The symbols used in the messages are listed in [Table 26](#).

Because of the padding option, the number of register data provided in the data fields do not have to match with the message length. The data used for padding is used for CRC calculation, but has otherwise no effect. If a message contains fewer data fields than specified by DATALEN[1:0], the communication frame is discarded.

Table 26. Symbol description

Symbol	Value	Description
CMD[1:0]		Operation to be performed
	00	Wake-up message or no operation (NOP) <sup>[1]</sup>
	01	Read request message
	10	Write request message
MADD		Indicates the address of the leader transmitting
	0	leader 0 (also used by BMI7018 in all response messages)
	1	leader 1
CADD[2:0]		Daisy chain address
	0	Reserved for future usage
	1	Daisy chain 1
	2	Daisy chain 2
	3	Daisy chain 3

Table 26. Symbol description...continued

Symbol	Value	Description
	4	Daisy chain 4
	5	Daisy chain 5
	6	Daisy chain 6
	7	All daisy chains
DEVADD[5:0]		Device address in the daisy chain
	0	Unenumerated device
	1 to 62	Device address
	63	All devices
MSGCNT[3:0]		Each BMI7018 has a local message counter which is incremented after a message was sent. The counter rolls over to 0.
	0 to 15	Response message: current message counter value other messages: ignored by the BMI7018
DATLEN[1:0] <sup>[2]</sup>		Number of valid data fields in the message
	0	DATA0 is valid
	1	DATA0 and DATA 1 are valid
	2	DATA0, and DATA1 and DATA2 are valid
	3	All four data fields are valid
REGADD[13:0]		Indicates the start address of the register access
	0 to 16383	Register addressed
0 0000b reserved (only for read commands)		This field is reserved and must have the value 0.
PAD <sup>[3]</sup> (only for read commands)	0	No padding used in response frames
	1	Padding is used in response frames
RESPLEN[1:0] (only for read commands)		Number of registers to be transferred in one response frame. If RESPLEN is greater than the number of registers to be transmitted, the device adapts the response length to fit the number of registers.
	0	Response length is one register
	1	Response length is two registers
	2	Response length is three registers
	3	Response length is four registers
NUMREG[7:0] (only for read commands)		Number of total registers requested
	0	One register
	1 to 255	Number of total registers requested = NUMREG + 1
DATA0[15:0]		Data to be transferred
DATA1[15:0]		Data to be transferred
DATA2[15:0]		Data to be transferred
DATA3[15:0]		Data to be transferred
Padded	0000h	Optional padding of message
CRC[15:0]		CRC value

[1] Differentiation for wake-up message and NOP messages is described in [Section 7.9.1.4.1](#).

[2] Read commands with DATALEN ≠ 0 are accepted, but only DATA0 is used.

[3] See [Section 7.9.1.3](#).

### 7.9.1.2 Message CRC generation

The leader and followers calculate a 16-bit CRC on the entire message using the processes detailed in this section. The CRC is calculated using the polynomial  $X^{16} + X^{13} + X^{12} + X^{11} + X^{10} + X^8 + X^6 + X^5 + X^2 + 1$  (identified by 3D65h - MSB first notation) with a seed value of 0000h. The seed value represents the initial status of the CRC calculation.

**Note:** In Koopman notation, the polynomial corresponds to 9EB2h.

Table 27. CRC parameters

Description	Value
CRC result width	16 bits
Polynomial (MSB-first notation)	3D65h
Polynomial (Koopman notation)	9EB2h
Seed	0000h

#### Procedure for CRC encoding (transmission)

The part of the message being encoded are bits from MSB to bit 16, bits 15 to 0 are reserved for CRC result.

1. Calculate the CRC over the message bits MSB to bit 16 using the given polynomial, and the seed as initial value.
2. Once the CRC is calculated, append it at the end of the message, and the message can be transmitted.

Table 28. CRC calculation examples

Message bits MSB to 16	CRC, 16 bit	Frame
1FFF FFFF FFEEh	7EF4h	1FFF FFFF FFEE 7EF4h
9FF0 1403 7C01h	D0C2h	9FF0 1403 7C01 D0C2h
4410 187F 070Eh	9434h	4410 187F 070E 9434h

#### Procedure for CRC check (reception)

Calculate the CRC over all bits of the received message (including CRC) using the given polynomial, and the seed as initial value.

- If the result is 00h, the CRC is correct. The BMI7018 processes the message.
- If the result is different than 00h, the CRC is incorrect. The BMI7018 discards the message, sets the CRCERR fault bit in the FEH\_COM\_FLT\_STAT register, and increments the COMERRCNT.

**Note:** The bit COMFLT signals the occurrence of communication faults, as well.

Table 29. CRC check examples

Frame	CRC check result, 16 bit
01FF 0000 FFEE 948Eh	0000h
9FF0 1403 7C01 D0C2h	0000h
4410 187F 070E 9434h	0000h
C418 9009 0000 0000 0000 10F9h	0000h

### 7.9.1.3 Multiread responses with padding

The TPL3 protocol offers the option to request multiple consecutive registers with one read request message. The symbol RESPLEN[1:0] defines the number of registers to be transferred in one message. The symbol NUMREG[7:0] defines the number of registers that are requested. To transfer the requested number of

registers, the BMI7018 sends as many messages with  $\text{DATALEN}[1:0] = \text{RESPLEN}[1:0]$  as needed. If the last message has less data to transfer than specified in  $\text{RESPLEN}[1:0]$ , the device sends in the last message only the remaining register data.

The symbol PAD configures the length of this last message. With PAD set to logic 0, the length of the last message is adapted to match the number of registers to be transferred. With PAD set to logic 1, the last message is padded with 0000h to match the requested message length (as indicated by RESPLEN). If the message is a response to an access error, the padding is done with 8000h instead.

**Note:** DATALEN is indicating the length of the message including the padded data.

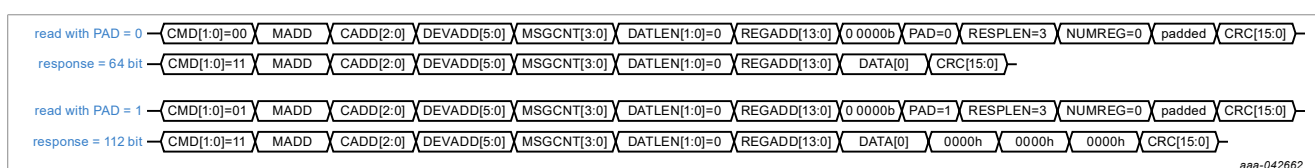


Figure 31. TPL3 response with and without padding

### 7.9.1.4 TPL wake-up commands

The BMI7018 wakes up by any kind of bus activity; a dedicated wake message is needed. In order to wake all TPL3 devices connected, the TPL3 communication features a special command to wake up the system. In order to allow compatibility with TPL2 devices such as MC33664, the BMI7018 can also be configured to initiate an MC33664-compatible wake command.

#### 7.9.1.4.1 TPL3 wake-up message

NOP messages do not cause a reaction of the BMI7018. The only exception to this behavior is the wake-up message. The wake-up message is a 64-bit NOP message with  $\text{DATA}[0] = \text{FEEh}$  sent to all devices ( $\text{DEVADD}[5:0] = 11\ 1111\text{b}$ ). The daisy chain address ( $\text{CADD}[2:0]$ ), leader address ( $\text{MADD}$ ), data length ( $\text{DATLEN}$ ), and the message counter ( $\text{MSGCNT}[3:0]$ ) are ignored.



Figure 32. Wake-up message for BMI7018

Once the device receives the wake-up message as explained above, the device initiates a wake-up of the system. For details of the system wake-up, see [Section 7.9.2.3](#).

**Note:** The system wake-up is initiated only once after entering active mode. The second wake-up message after entering active mode is treated as a regular NOP command.

The wake-up message sent by the BMI7018 is shown in [Figure 33](#).

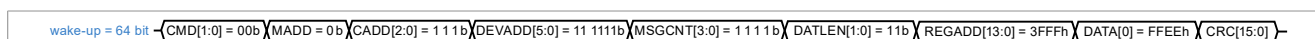


Figure 33. Wake-up message sent by BMI7018 (WAKEUPCOMP = MBMI7018)

#### 7.9.1.4.2 Wake-up compatibility for MC33664

The MC33664 uses a different wake-up message than the BMI7018. To ensure compatibility with the MC33664, the BMI7018 supports the generation of MC33664-compatible wake-up messages. The bits  $\text{SYS\_TPL\_CFG.WAKEUPCOMP}[1:0]$  set the wake-up message type for each TPL port. One port can be configured to MC33664 compatibility.

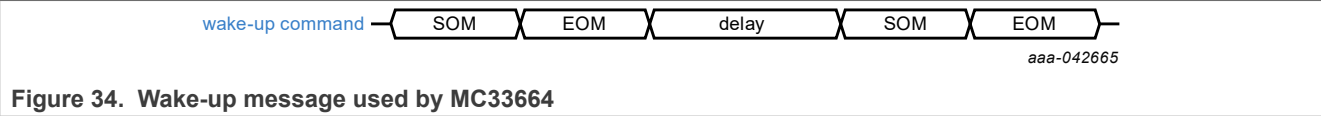


Figure 34 shows the sequence sent by the BMI7018. The sequence consists of a two messages: a start of message (SOM) symbol and an end of message (EOM) symbol. The messages are separated by a delay.

7.9.2 TPL3 interface

High-speed differential isolated communication is achieved by using transformers or capacitors. The BMI7018 offers two TPL ports to allow a daisy-chain communication of multiple devices. In one daisy chain, up to 62 nodes can be logically addressed via the device address. Device address 0d (DADD[5:0] or DEVADD[5:0] = 00 0000b) is reserved for network initialization. Device address 63d (DADD[5:0] or DEVADD[5:0]= 11 1111b) is reserved for broadcast messages.

7.9.2.1 TPL communication symbols

The TPL uses four pulse-encoded symbols for communication. The four symbols are shown in Figure 35 to Figure 38. The transformer driver generates SOM and EOM symbols. They always occur at the start and end of the communication message, respectively. Data pulses are used to transfer the actual information.

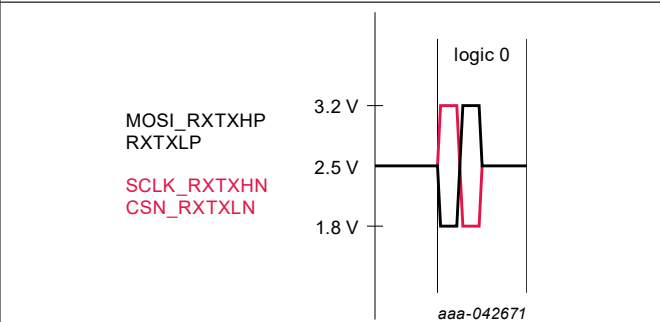
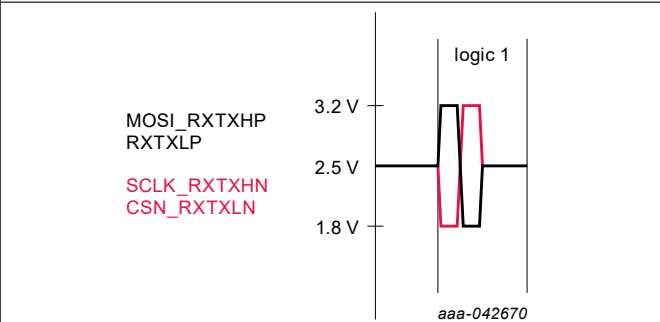
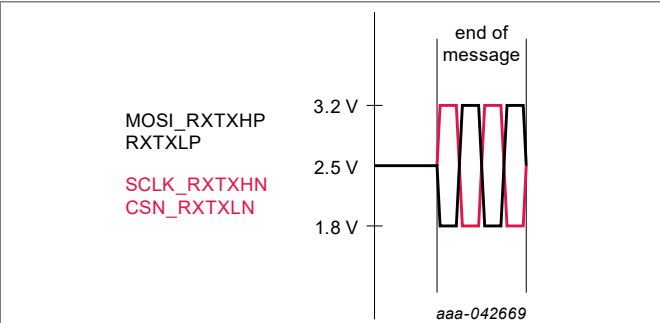
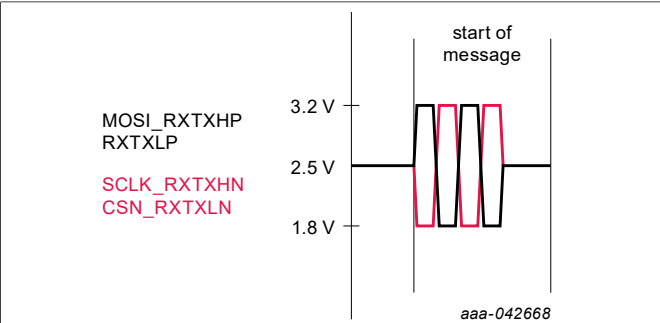


Figure 39 shows a typical TPL communication frame.

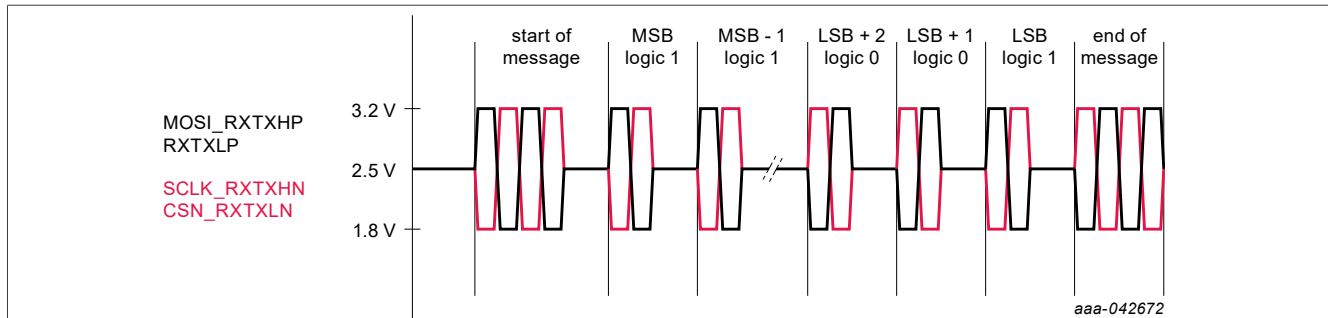


Figure 39. Example frame with content 11 to 001

### 7.9.2.2 TPL daisy-chain communication

The TPL communication is done in a daisy-chain configuration.

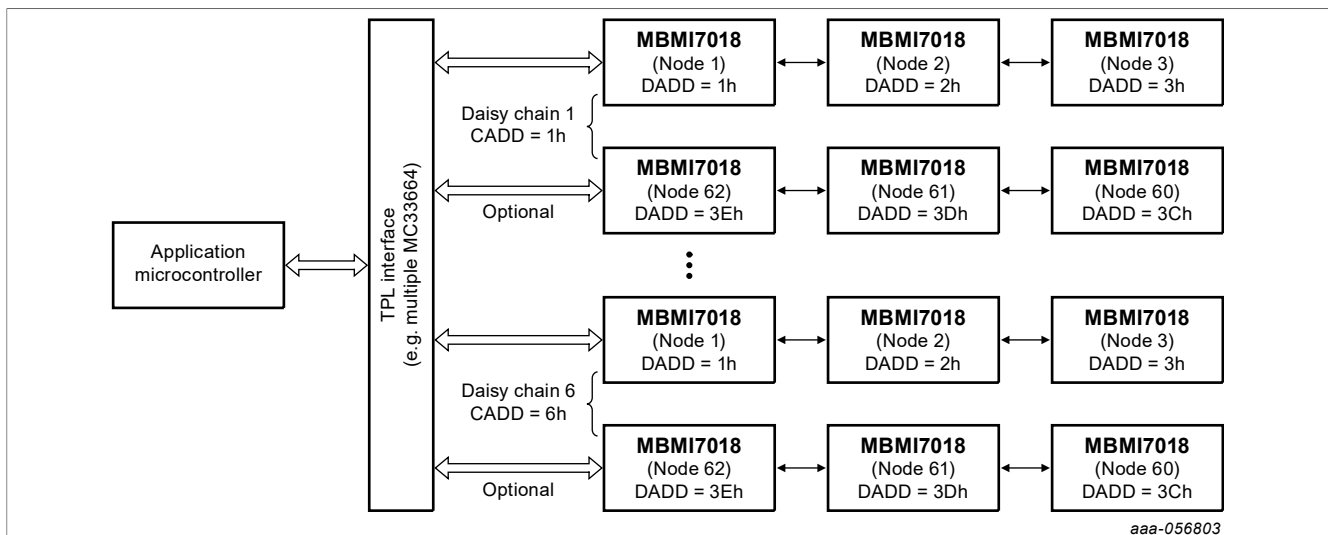


Figure 40. Setup for multiple TPL daisy chains

During communication, each device is checking the device address field in the communication messages. Devices react only to commands that are addressed to them (DEVADD of message is equal to DADD of the device, or broadcast messages). The BMI7018 is not decoding the CADD field, but uses the CADD in all response messages. CADD = 0h must be reserved for future usage.

#### 7.9.2.2.1 Communication methodology

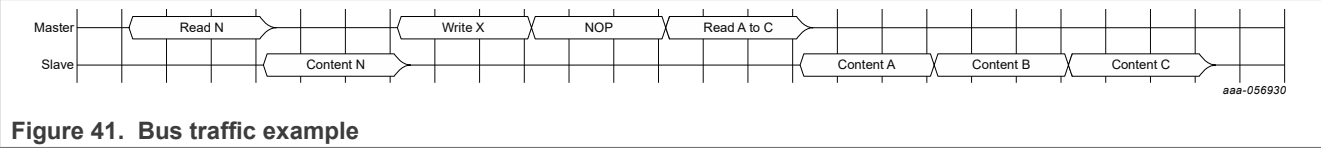
The TPL communication physical layer does not offer any collision avoidance mechanism. On the higher communication layers, some mechanisms are implemented.

- The BMI7018 ignores read commands to all devices (DEVADD[5:0] = 63), because the responses would cause bus collisions
- The BMI7018 delays the start of sending of response messages in case the bus is busy. Messages received while a response is pending are ignored.

Otherwise, it is the task of the communication leader to ensure that no collisions happen. If collisions occur, it is the task of the communication leader to re-establish proper communication.



Write commands to the BMI7018 do not generate a response message. Read commands sent by the leader may generate a single response or multiple responses depending on the parameters used in the read request. The message size and start register are identified in the read command sent by the leader.



### 7.9.2.2.2 Message processing and compensation of forward delays

Each message received by the BMI7018 is checked for integrity after reception. Valid messages for an individual device (DEVADD[5:0] = 0 to 3Eh) are executed within the delay time between two messages ( $t_{d(req)MCU}$ ). The execution of write messages for all devices (DEVADD[5:0] = 3Fh) is delayed. The delay is calculated based on:

- The device address (SYS\_COM\_CFG.DADD)
- The number of nodes in the daisy chain (SYS\_COM\_CFG.NUMNODES)
- The direction of the communication (MADD of the communication message)
- The average forward delay

Table 30. Equation used for delay if MADD = 0

$$t_{delay} = (NUMNODES - DADD) \times t_{d(Fd)}$$

Table 31. Equation used for delay if MADD = 1

$$t_{delay} = (DADD - 1) \times t_{d(Fd)}$$

**Note:** Read messages for all devices are ignored as they would cause bus collisions.

Compensating the forward delays allows all devices to execute global write commands at nearly the same moment in time.

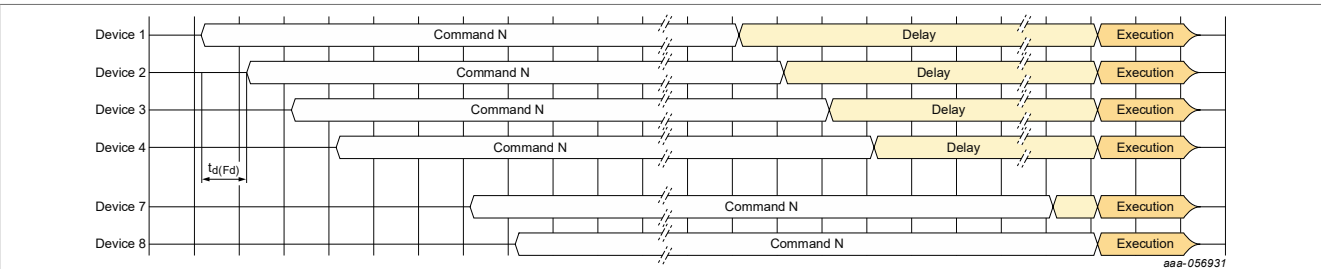


Figure 42. Compensation of forward delays with MADD = 0 and NUMNODES = 8

**Notes:** For proper operation of the forward delay compensation:

- For proper operation of the forward delay compensation:
  - The SYS\_COM\_CFG.NUMNODES must be set correctly in all devices
  - If NUMNODES - DADD < 0, then the device considers  $t_{delay} = 0$
  - The devices must be enumerated in incrementing order when MADD = 0 is used and in decrementing order when MADD = 1 is used
- During the delay time, it is forbidden to send new messages to the BMI7018.

Application usage: Synchronized start and end of measurements.

7.9.2.2.3 Device address and enumeration of devices

After power-up or Deep Sleep mode, the BMI7018 starts with DADD = 0. To allow forwarding of messages and therefore enable communication toward a complete daisy chain, the DADD has to be assigned. This process is called *enumeration*.

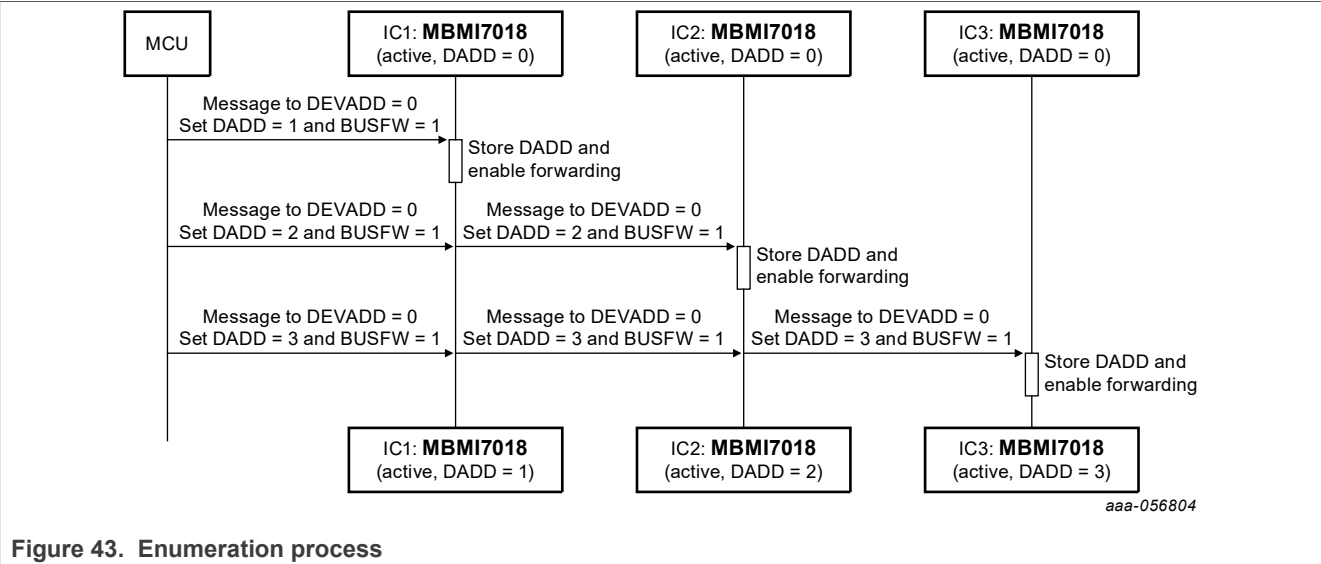


Figure 43. Enumeration process

An unenumerated device (DADD = 0) does not forward any communication. This behavior allows setting the device address for each device in the daisy chain based on the position in the daisy chain. An enumerated device (DADD ≠ 0) with enabled bus forwarding (bit SYS\_COM\_CFG.BUSFW) forwards any communication received on one TPL port to the other TPL port. This behavior allows communication from upper nodes to lower nodes and lower nodes to upper nodes. All devices in a daisy chain receive any communication sent by the application microcontroller.

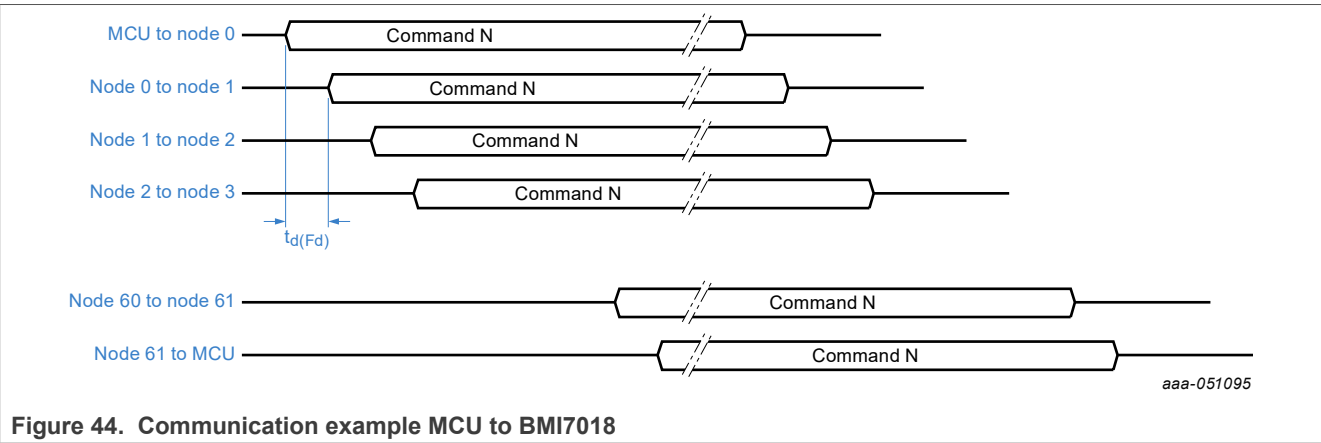
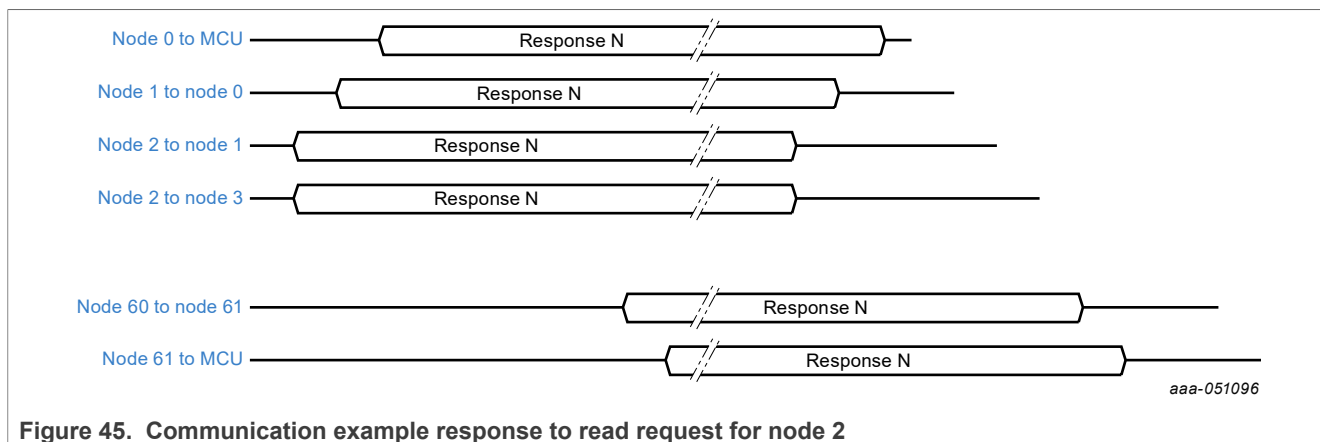


Figure 44. Communication example MCU to BMI7018

Responses to read commands are transmitted at both TPL interfaces. [Figure 45](#) shows a response assuming that command N in [Figure 44](#) was a read command for node 2.



### 7.9.2.3 Wake-up by TPL communication

The BMI7018 contains bus wake-up capability. An BMI7018 can wake up other devices, and other devices can wake up the BMI7018. If the BMI7018 detects a wake-up condition and the wake-up is enabled, the device initiates a wake-up pulse sequence on the bus.

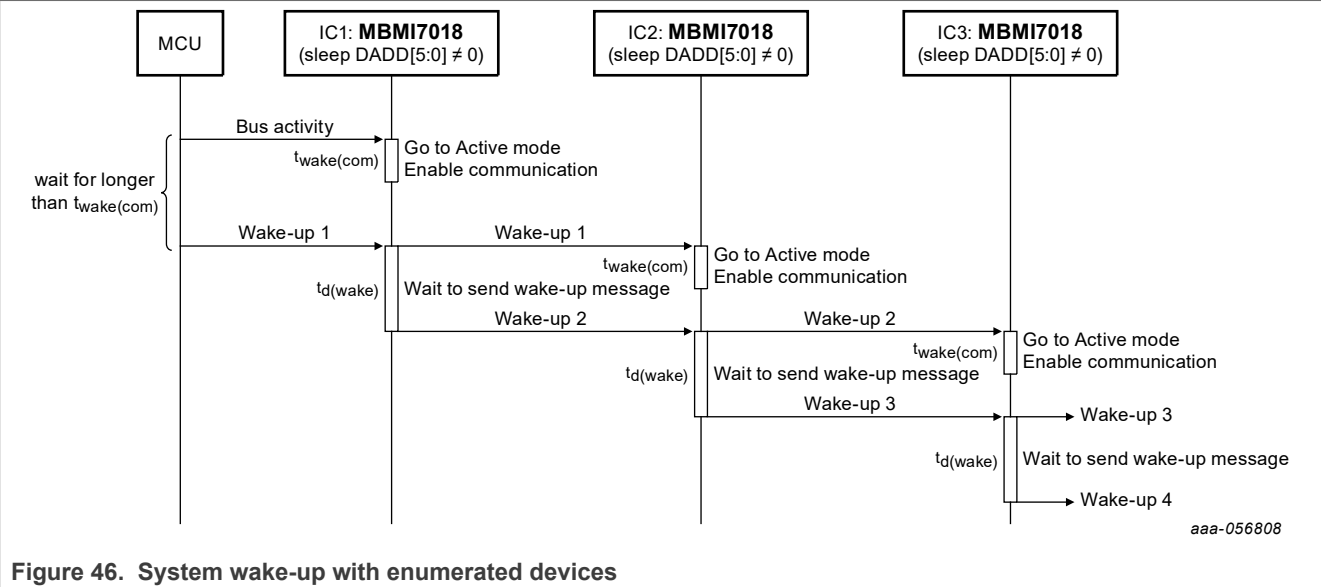
#### 7.9.2.3.1 Wake-up of BMI7018

The BMI7018 wakes up once there is any communication on the TPL bus.

##### 7.9.2.3.1.1 Wake-up with enumerated devices ( $DADD[5:0] \neq 0$ and $BUSFW = 1$ ) using device wake-up messages

The first wake-up message or bus activity initiates a transition to Active mode. In Active mode, an enumerated BMI7018 with  $BUSFW = 1$  forwards any message. The second wake-up message transmitted by the MCU is forwarded to the next BMI7018 in the daisy chain. The first BMI7018 has now received two wake-up messages. It automatically sends one additional wake-up message toward the second BMI7018.

The second BMI7018 in the daisy chain receives one forwarded wake-up message plus the generated message and acts in the same way as the first BMI7018. This behavior wakes the entire daisy chain. Figure 46 illustrates this behavior.



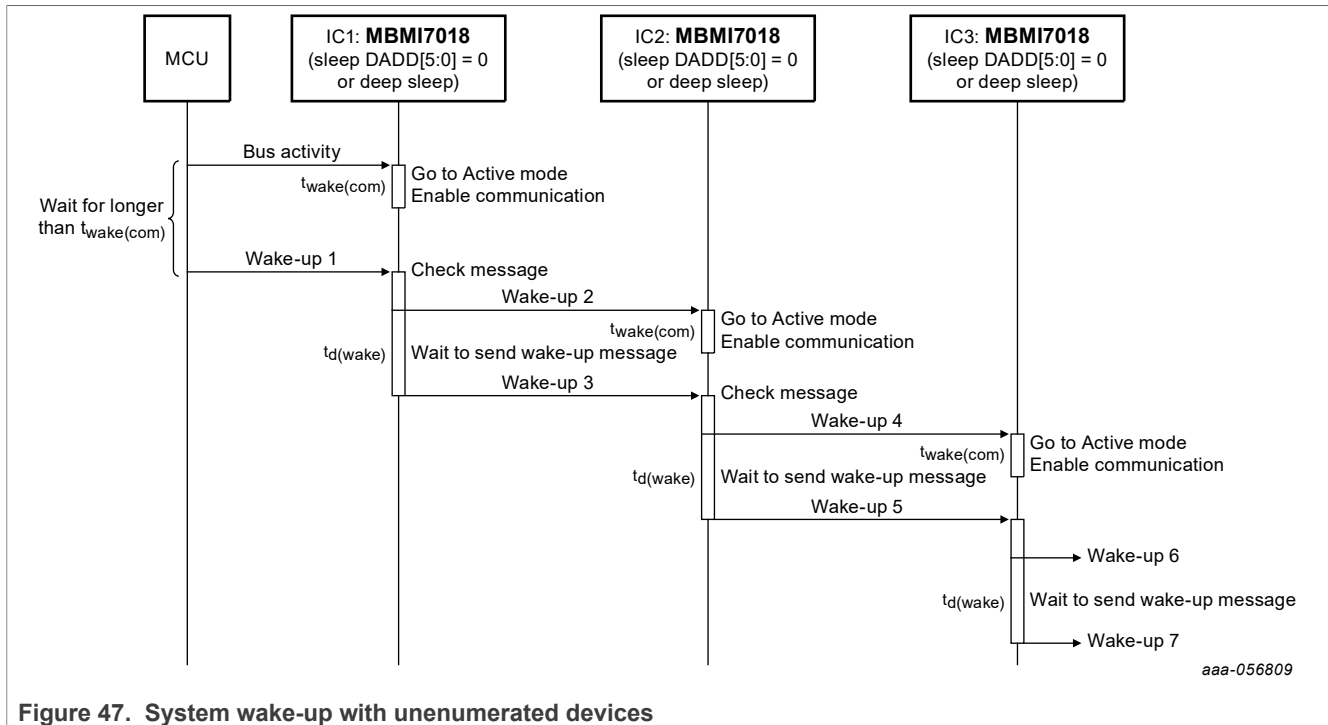
Notes:

- The wake-up message used here is the one defined in [Section 7.9.1.4.1](#).
- Reception of a valid message during the wait time between the wake-up messages ( $t_{d(wake)}$ ) stops the wake-up process.

7.9.2.3.1.2 Wake-up with unenumerated devices (DADD[5:0] = 0) using device wake-up messages

An unenumerated BMI7018 does not forward communication. The microcontroller can communicate only with the physically first IC of the daisy chain. Assigning a daisy chain address (DADD  $\neq$  0) and enabling the bus forwarding (BUSFW = 1) enables communication with the first and second IC. Continuing this process allows assigning unique addresses to all devices in the daisy chain based on their physical position in the daisy chain.

The first wake-up message or bus activity initiates a transition to Active mode. In Active mode, an unenumerated BMI7018 does not forward messages. The second wake-up message transmitted by the MCU is not forwarded to the next BMI7018 in the daisy chain. To wake up the entire daisy chain, the unenumerated BMI7018 automatically sends two wake-up messages toward the second BMI7018.



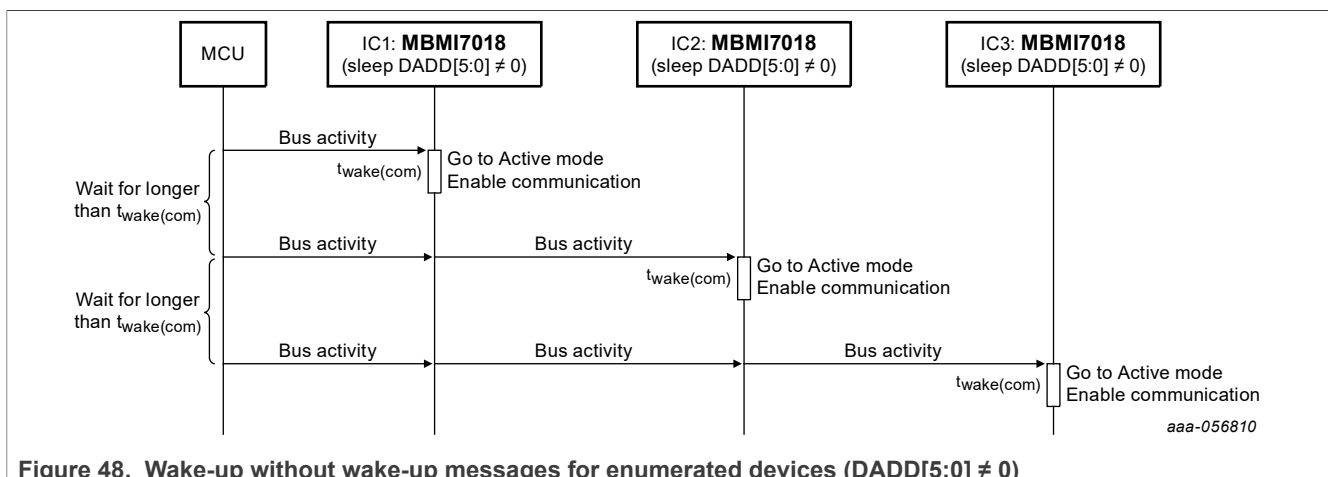
**Notes:**

- The wake-up message used here is the one defined in [Section 7.9.1.4.1](#).
- Reception of a valid message during the wait time between the wake-up messages ( $t_{d(wake)}$ ) stops the wake-up process.

### 7.9.2.3.1.3 Wake-up with regular communication

The usage of wake-up messages as described in [Section 7.9.2.3.1.1](#) and [Section 7.9.2.3.1.2](#) automatically ensures the wake-up of the whole daisy chain. It is also possible to wake the system without usage of dedicated wake-up messages.

With start of bus activity, the first device in the chain starts to wake up. Once the device has completed the transition to Active mode, the device can receive and send messages. If the device is enumerated and the bus forwarding is enabled, the device forwards the communication. The resulting bus activity wakes up the next device in the daisy chain.



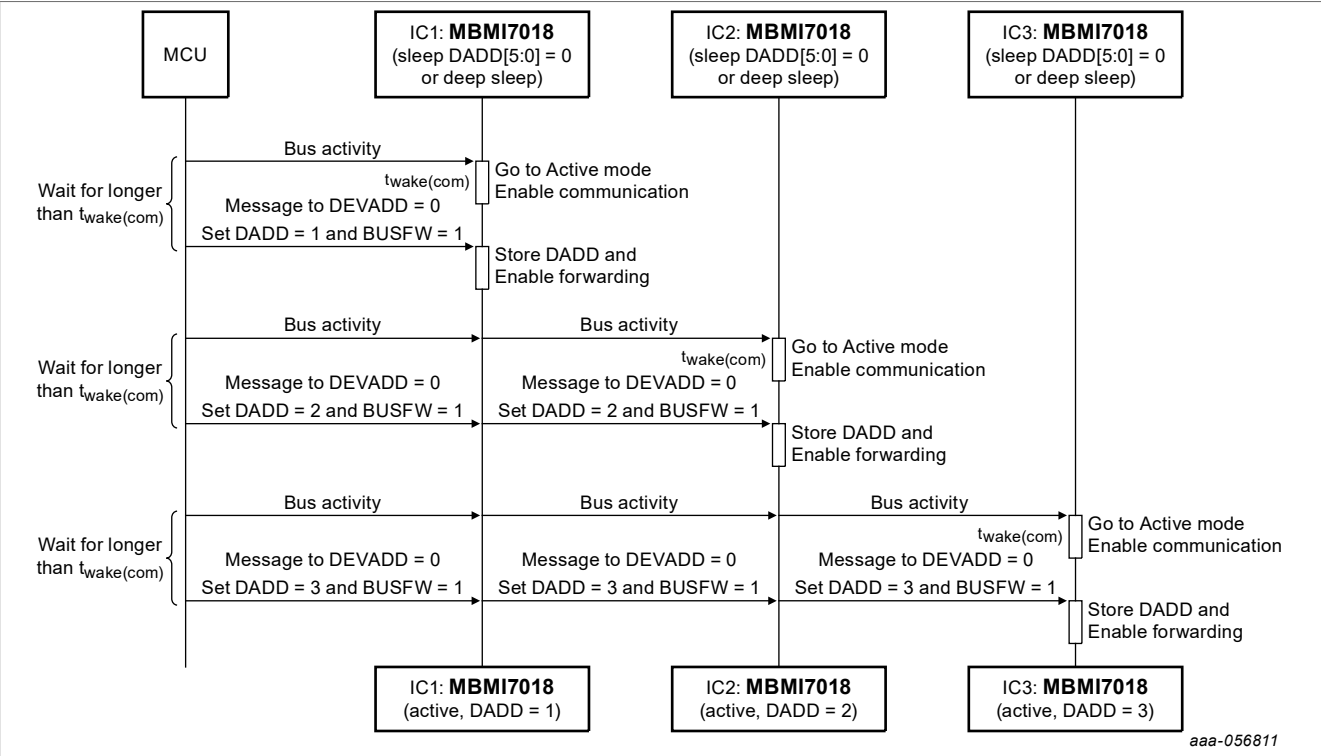


Figure 49. Wake-up and enumeration without wake-up messages for unenumerated devices (DADD[5:0] = 0)

### 7.9.3 SPI interface

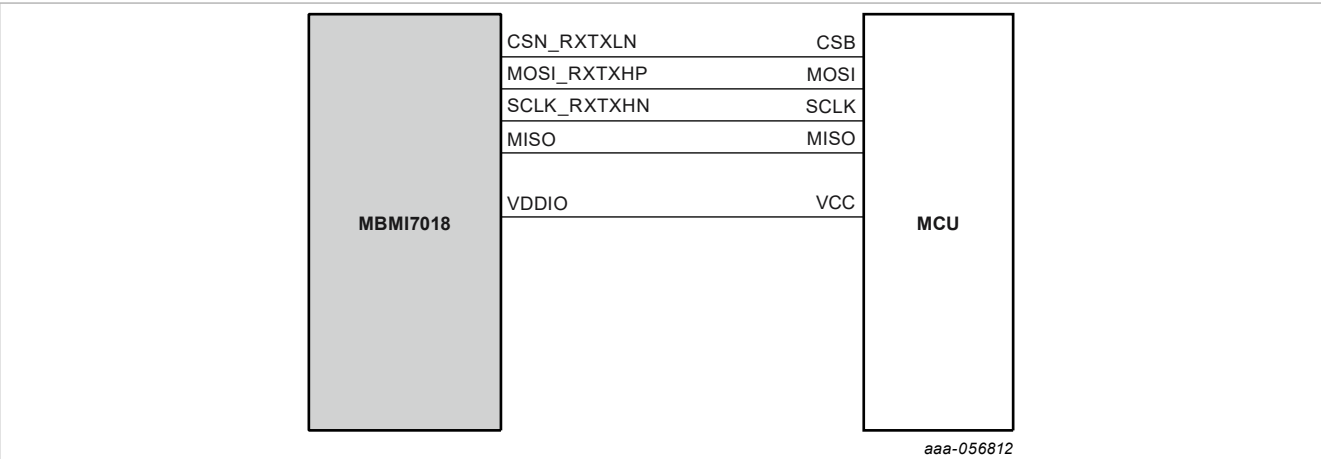


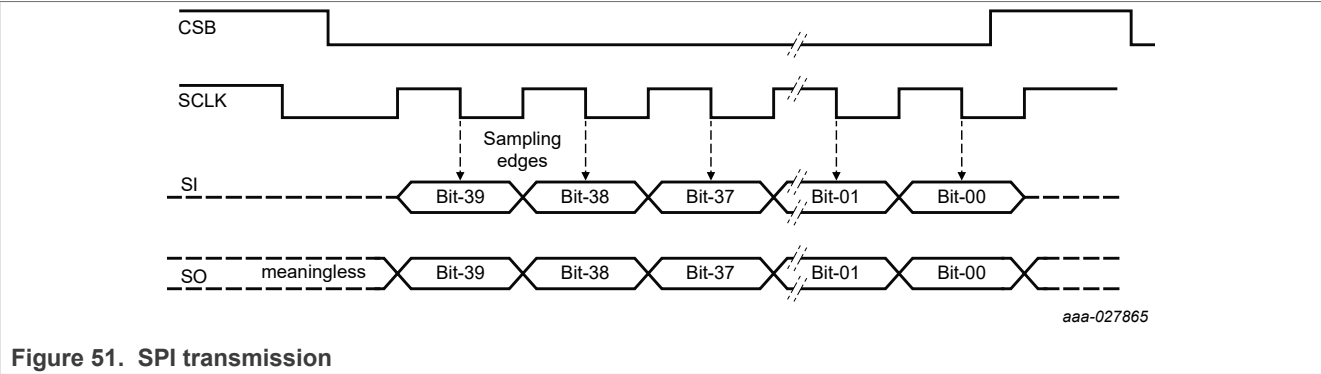
Figure 50. SPI connection

The SPI input signal levels to the BMI7018 operate at 5.0 V logic levels but are 3.3 V compatible.

The VDDIO pin can be connected to the VDDC pin to get 5.0 V SPI output signal levels. To get 3.3 V SPI output signal levels, the VDDIO pin should be connected to an external 3.3 V supply.

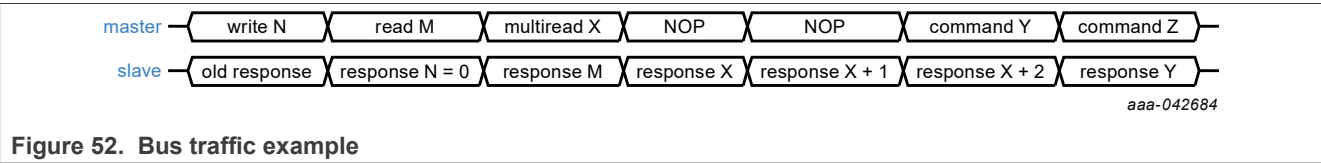
The BMI7018 SPI is a standard SPI with a chip select (CSN\_RXTXLN), clock (SCLK\_RXTXHN), leader input follower output (MISO), and leader output follower input (MOSI) (MOSI\_RXTXHP). The shifting of the data

follows a first in first out (FIFO) order, with both input and output words transferring the most significant bit (MSB) first. The microcontroller controls all SPI communication to the BMI7018.



The BMI7018 decodes the SPI message with the rising edge of the chip select (CSN\_RXTXLN) pin. The clock polarity is active HIGH (idles LOW). The rising edge on SCLK changes data bits, with the falling edge data bits are sampled (valid). The BMI7018 responds to a received command with the next transmission.

The BMI7018 accepts read requests for more registers than the actual data length. NOP messages allow the device to send pending data. If the device has no data anymore to send, it responds with all remaining bits logic 0. Other commands than NOP commands cancel the transmission of pending data. To write commands, the device responds with all bits logic 0.



Change of the data length of the SPI frames is allowed. However, the user must ensure that pending responses fit the SPI frame length. Otherwise, a response frame error is generated.

7.9.4 Microcontroller interface monitoring

The microcontroller interface facilitates several diagnostics and monitoring functionalities. They are explained in the following sections.

7.9.4.1 Communication error counter

If any communication issue (FRAMEERR, CRCERR, RSPLENERR) is detected, the communication error counter FEH\_COM\_FLT\_STAT.COMERRCNT increases by one. A write to the FEH\_COM\_FLT\_STAT.COMERRCNT with any data unequal to 00h resets the counter.

7.9.4.2 Error counter overflow

In case the communication error counter is maxed out, the communication error counter stays at the maximum value, and the bit FEH\_COM\_FLT\_STAT.ERRCNTOF is set. A write to the bit with logic 1 clears the FEH\_COM\_FLT\_STAT.ERRCNTOF bit.

Application usage: An error counter overflow can be used to trigger a power-on reset of the device.

7.9.4.3 Response errors

Response errors can only occur when the BMI7018 is used with SPI communication. In case the length of an SPI frame does not match the length of the response frame to be transmitted, the CRC bit field is

not at the end of the message. This error is signaled with the bit FEH\_COM\_FLT\_STAT.RSPLENERR and FEH\_COM\_FLT\_STAT.COMERRCNT is increased. A write to the bit with logic 1 clears the FEH\_COM\_FLT\_STAT.RSPLENERR bit.

7.9.4.4 Communication timeout

In case the device does not receive or transmit a valid message for a time longer than set in SYS\_COM\_TO\_CFG.COMTO a communication timeout error is generated. The bit FEH\_COM\_FLT\_STAT.COMTO is set and FEH\_COM\_FLT\_STAT.COMERRCNT is increased. The further reaction of the BMI7018 depends on the configuration in the [event handling](#). A write to the bit with logic 1 clears the FEH\_COM\_FLT\_STAT.COMTO bit.

The bit field SYS\_COM\_TO\_CFG.COMTODISABLE allows disabling the communication timeout. Disabling of the communication timeout is only allowed for development purposes.

7.9.4.5 CRC error

The BMI7018 checks all messages it receives for a correct CRC. In case the device detects an invalid CRC for the received message a CRC error is generated. The bit FEH\_COM\_FLT\_STAT.CRCERR is set and FEH\_COM\_FLT\_STAT.COMERRCNT is increased. A write to the bit with logic 1 clears the FEH\_COM\_FLT\_STAT.CRCERR bit.

7.9.4.6 Frame error

The BMI7018 checks all messages for a valid frame length. Frames with 64 bit, 80 bit, 96 bit, and 112 bit are accepted. In case the device detects an invalid frame a frame error is generated. The bit FEH\_COM\_FLT\_STAT.FRAMEERR is set and FEH\_COM\_FLT\_STAT.COMERRCNT is increased. A write to the bit with logic 1 clears the FEH\_COM\_FLT\_STAT.FRAMEERR bit.

7.9.4.7 Access error

An access error is detected when a non-existing register is accessed. For the access, it does not matter if it is read or write. Write into read only, or read of write-only registers do not trigger an access error. If an access error occurs for a read request, the device responds with a regular response frame. REGADD[13:0] contains the error indicator 3FFFh. DATA[0] contains the address where the access error was triggered. Bit 15 and bit 14 of DATA[0] are set to 00b. Data padding for access errors is done with 8000h instead of 0000h.

If the access error occurs within a response message to a multiread command, the device provides the readable content until the frame is sent, in which the access error occurs. The frame with the access error contains in DATA[0] the address in which the error occurred. Subsequent frames contain in DATA[0] the address that this frame would use. Access error frames are sent, independent whether the frame would use accessible or non-accessible content, until the requested number of messages is sent. [Figure 53](#) shows the behavior of the BMI7018 in case an access error occurs during a multiread command.

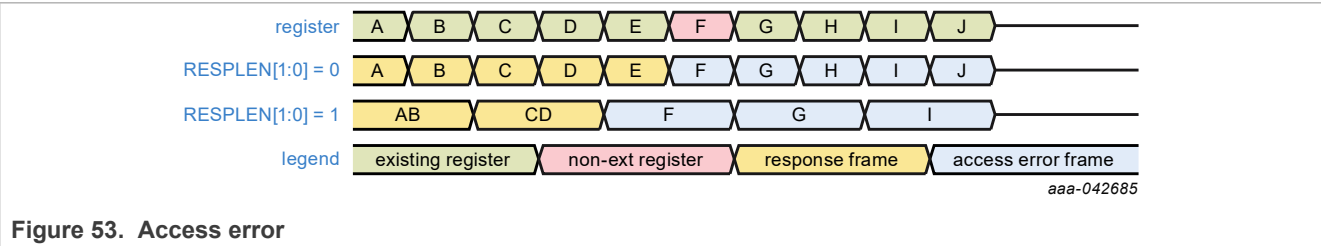


Figure 53. Access error

The register FEH\_ACC\_ERR contains information about the type of the last access error and the register addressed during this access.



**Note:** An access error does not increment the communication error counter.

#### 7.9.4.8 Response of the device to communication errors

When an error in the communication to the BMI7018 is detected (FRAMEERR, CRCERR, RSPLNERR), the message is discarded. The BMI7018 does not send a response to this command.

#### 7.9.5 Microcontroller interface related registers

The most important registers for the microcontroller interface and the related content are shown in [Table 32](#).

**Table 32. Microcontroller interface related registers**

Register	Content
FEH_COM_FLT_EVT_CFG ( <a href="#">Section 12.1.41</a> )	communication faults events
FEH_COM_FLT_POR_CFG ( <a href="#">Section 12.1.37</a> )	reset due to communication faults
FEH_COM_FLT_STAT ( <a href="#">Section 12.1.33</a> )	communication errors
SYS_COM_TO_CFG ( <a href="#">Section 12.1.3</a> )	communication timeout configuration
SYS_COM_CFG ( <a href="#">Section 12.1.2</a> )	communication configuration

## 8 Limiting values

### 8.1 BMI7018 limiting values

**Table 33. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>BAT</sub>	VBAT voltage		-0.3	-	94	V
V <sub>i(CTn)</sub>	Cell terminal input voltage (CTn) (n = 0 to 17)		-0.3	-	(n+1) * 5	V
V <sub>i(CTn)</sub>	Cell terminal input voltage (CTn) (n = 18)		-0.3	-	94	V
V <sub>i(CBn)</sub>	Cell terminal balance input voltage (CBn) (n = 0 to 17)		-0.3	-	(n+1) * 5	V
V <sub>i(CBn)</sub>	Cell terminal balance input voltage (CBn) (n = 18)		-0.3	-	94	V
V <sub>diff(CT)</sub>	Cell terminal input differential voltage		-5	—	10	V
I <sub>i(CTn)</sub>	cell terminal input current	open load detection disabled	-500	—	500	nA
V <sub>i(diff)bal</sub>	balancing input differential voltage		-4.5	—	12.5	V
I <sub>i(bal)</sub>	input current on balancing pins		—	—	330	mA
V <sub>DDA</sub>	VDDA voltage		-0.3	—	1.65	V
V <sub>DDC</sub>	VDDC voltage		-0.3	—	5.5	V
V <sub>DDIO</sub>	VDDIO voltage		-0.3	—	5.5	V
V <sub>AUX</sub>	VAUX voltage		-0.3	—	4	V
V <sub>GPIOx</sub>	GPIOx voltage		-0.3	—	VDDC + 0.5	V

Table 33. Limiting values...continued

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>AINA</sub>	AINA and ALARM <sub>OUT</sub> voltage		-0.3	—	V <sub>DDC</sub> + 0.5	V
V <sub>bus(TPL)</sub>	voltage on TPL communication bus pins	Relative to VSSC	-27	—	40	V
V <sub>i(IMONVDDC)</sub>	input voltage on IMON_VDDC pin		-0.3	—	7	V
V <sub>i(DRIVEVDDC)</sub>	input voltage on DRIVE_VDDC pin		-0.3	—	7	V
<b>Thermal maximum ratings</b>						
T <sub>j</sub>	junction temperature		-40	—	165	°C
T <sub>stg</sub>	storage temperature		-55	—	150	°C
T <sub>reflow(peak)</sub>	peak package reflow temperature	Pin soldering temperature limit is for 30 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause a malfunction or permanent damage to the device.	—	—	260	°C
<b>ESD ratings</b>						
V <sub>ESD1</sub>	electrostatic discharge voltage	At any pin; human body model (HBM): according to AEC-Q100-002 (100 pF, 1.5 kΩ)	-2	—	+2	kV
V <sub>ESD2</sub>	electrostatic discharge voltage	At pin VBAT, CTx, CBx, VDDIO, VDDC, CSN_RXTXLN, RXTXLP, MOSI_RXTXHP, SCLK_RXTXHN, GPIOx, AINA_ALARMOUT, VAUX, ; HBM: according to AEC-Q100-002 (100 pF, 1.5 kΩ); against all GNDs shorted together	-4	—	+4	kV
V <sub>ESD3</sub>	electrostatic discharge voltage	At all pins; charged device model (CDM): according to AEC-Q100-011 (field induced charge; 4 pF)	-500	—	+500	V
V <sub>ESD4</sub>	electrostatic discharge voltage	At corner pins; CDM: according to AEC-Q100-011 (field induced charge; 4 pF)	-750	—	+750	V
V <sub>ESD5</sub>	electrostatic discharge voltage	At pin VBAT, CTx, CBx, VDDIO, VDDC, VSSC, CSN_RXTXLN, RXTXLP, MOSI_RXTXHP, SCLK_RXTXHN, GPIOx, AINA_ALARMOUT, VAUX, VSSA, GNDFLAG; according to IEC 61000-4-2, unpowered (150 pF, 330 Ω) with recommended ESD capacitors as in section application information - with floating ground	-8	—	+8	kV

Table 33. Limiting values...continued  
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>ESD6</sub>	electrostatic discharge voltage	At pin VBAT, CTx, CBx, VDDIO, VDDC, VSSC, CSN_RXTXLN, RXTXLP, MOSI_RXTXHP, SCLK_RXTXHN, GPIOx, AIINA_ALARMOUT, VAUX, VSSA, GNDFLAG; according to ISO-10605, unpowered (150 pF, 330 Ω) with recommended ESD capacitors as in section application information - with ground referenced	-8	—	+8	kV
V <sub>ESD7</sub>	electrostatic discharge voltage	At pin VBAT, CTx, CBx, VDDIO, VDDC, VSSC, CSN_RXTXLN, RXTXLP, MOSI_RXTXHP, SCLK_RXTXHN, GPIOx, AIINA_ALARMOUT, VAUX, VSSA, GNDFLAG; according to ISO-10605, unpowered (150 pF, 2 kΩ) with recommended ESD capacitors as in section application information - with ground referenced	-8	—	+8	kV
V <sub>ESD8</sub>	electrostatic discharge voltage	At pin VBAT, CTx, CBx, VDDIO, VDDC, VSSC, CSN_RXTXLN, RXTXLP, MOSI_RXTXHP, SCLK_RXTXHN, GPIOx, AIINA_ALARMOUT, VAUX, VSSA, GNDFLAG; according to ISO-10605, powered (330 pF, 2 kΩ) with recommended ESD capacitors as in section application information - with ground referenced	-8	—	+8	kV

8.2 ESD structure

The [Figure 54](#) shows the ESD structure of the BMI7018. Values in front of each ESD structure are the guaranteed voltage ratings, not the triggering voltages.

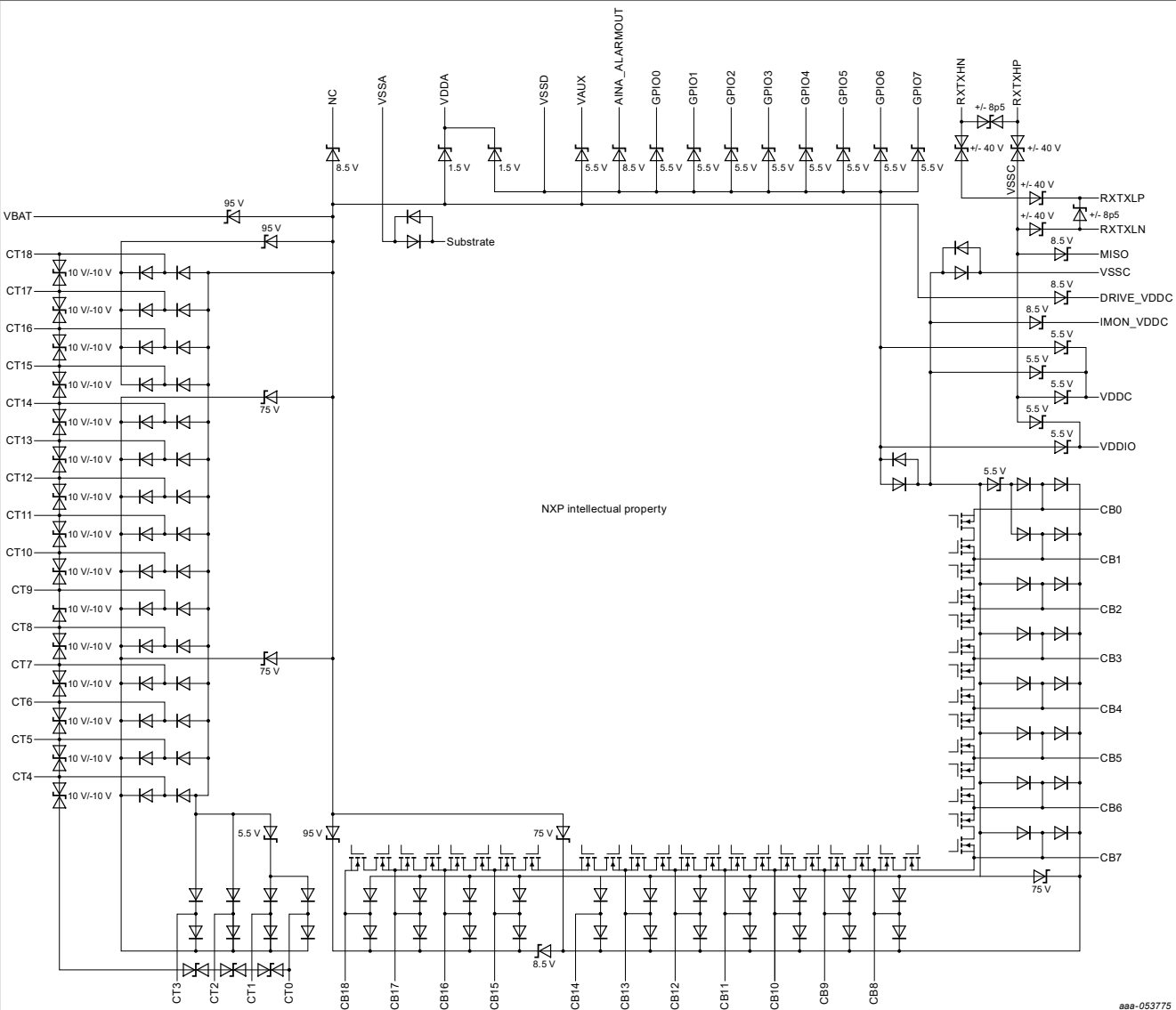


Figure 54. ESD structure

9 Thermal characteristics

Table 34. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Rth <sub>ja</sub>	Junction to ambient natural convection four layer board (2s2p)	Ta = -20 .. 60 °C	—	—	27	K/W
Rth <sub>jc</sub>	Junction to case bottom (exposed pad)	Ta = -20 .. 60 °C	—	—	1	K/W

## 10 Characteristics

### 10.1 BMI7018 Electrical characteristics

**Table 35. Characteristics**

$V_{bat} = 9\text{ V to }90\text{ V}$ ;  $T_a = -20\text{ }^{\circ}\text{C to }60\text{ }^{\circ}\text{C}$ ;  $T_j = -20\text{ }^{\circ}\text{C to }85\text{ }^{\circ}\text{C}$ ; all voltages are defined with respect to ground; positive currents flow into the IC. Typical values are given at  $V_{bat} = 72\text{ V}$ ;  $T_a = 25\text{ }^{\circ}\text{C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>VBAT</b>						
$V_{BAT}$	VBAT operating range		9	—	90	V
$V_{BAT(th)ov}$	VBAT overvoltage threshold		90	—	93	V
$V_{BAT(th)uv}$	VBAT undervoltage threshold		7	8	9	V
$V_{BAT(th)lv}$	VBAT low-voltage (LV) threshold	FP and FPC modes and LP mode with cell balancing	10.5	12	13.5	V
$\Delta V_{max1(VBAT-upperCT)}$	Maximum voltage difference 1 between battery supply voltage and pin CT18 or highest CTn	$V_{bat} = 35\text{ V to maximum supply voltage}$	-2.1	—	2.5	V
$\Delta V_{max2(VBAT-upperCT)}$	Maximum voltage difference between battery supply voltage and pin CT18 or highest CTn	$V_{bat} = 9\text{ V} + 1.5\text{ V to }35\text{ V}$	-1.5	—	2	V
$\Delta V_{bal(VBAT-upperCB)}$	Maximum voltage difference between battery supply voltage and pin CB18 or highest CBn	$T_j = -20\text{ }^{\circ}\text{C to }85\text{ }^{\circ}\text{C}$ , $V_{bat} = 9\text{ V to }81\text{ V}$ , $V_{cell} = -5\text{ V to }5\text{ V}$	-0.4	—	0.4	V
<b>Current consumption</b>						
$I_{BAT(ULP)}$	IBAT current in deep sleep mode	$T_j = -20\text{ }^{\circ}\text{C} \dots 85\text{ }^{\circ}\text{C}$	—	-	19	$\mu\text{A}$
$I_{BAT(LP)}$	IBAT current in sleep mode	$T_j = -20\text{ }^{\circ}\text{C} \dots 85\text{ }^{\circ}\text{C}$	—	-	115	$\mu\text{A}$
$I_{BAT(add)LP}$	Additional IBAT current in sleep mode in sleep mode due to balancing	sleep mode with balancing enabled	—	—	2.9	mA
$I_{BAT(FP)}$	Full Power mode current consumption measuring all cell voltages and auxiliary inputs.	No external load. No cell balancing.	—	—	14.9	mA
$I_{BAT(FPC)2}$	Cyclic mode current consumption measuring all cell voltages, primary auxiliary inputs, and module voltage.	No secondary measurement. No balancing. No external current consumption. No communication.	—	—	12.3	mA
$I_{BATCB(FPC)}$	IBAT additional current in FP or FPC mode when all CB enable	All cell balancing enabled.	—	—	700	$\mu\text{A}$
$\Delta I_{BAT(FP)}$	IC to IC operating current imbalance	$T_a = -20\text{ }^{\circ}\text{C to }60\text{ }^{\circ}\text{C}$ , $V_{bat} = 45\text{ V}$ , $T_a$ and $V_{bat}$ are the same for both ICs, Active mode / all ADCs running / No balancing operation / No communication / No external load	—	—	400	$\mu\text{A}$
<b>Cell voltage measurement accuracy for primary measurement - BOL</b>						
$V_{err(meas)(A)(CTx)}$	Cell voltage measurement error CTx, range A. (LFP cells)	$V_{cell} = 3.3\text{ V}$ , $T_j = 25\text{ }^{\circ}\text{C}$ , $V_{BAT} = 9\text{ V} \dots 81\text{ V}$	-0.8	—	0.8	mV
$V_{err(meas)(B)(CTx)}$	Cell voltage measurement error CTx, range B. (NMC cells)	$V_{cell} = 0\text{ V} \dots 4.5\text{ V}$ , $T_j = -20\text{ }^{\circ}\text{C} \dots 85\text{ }^{\circ}\text{C}$ , $V_{BAT} = 9\text{ V} \dots 81\text{ V}$	-3	—	3	mV
$V_{err(meas)(C)(CTx)}$	Cell voltage measurement error CTx, range C. (full range)	$V_{cell} = -1\text{ V} \dots 5\text{ V}$ , $T_j = -20\text{ }^{\circ}\text{C} \dots 85\text{ }^{\circ}\text{C}$ , $V_{BAT}$ operating range	-5	—	5	mV

Table 35. Characteristics...continued

Vbat = 9 V to 90 V; Ta = -20 °C to 60 °C; Tj = -20 °C to 85 °C; all voltages are defined with respect to ground; positive currents flow into the IC. Typical values are given at Vbat = 72 V; Ta = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Cell voltage measurement accuracy for primary measurement - EOL</b>						
V <sub>err(meas)(F)(CTx)</sub>	Cell voltage measurement error CTx, range F. (NMC cells)	V <sub>cell</sub> =0 V..4.5 V, T <sub>j</sub> =-20°C..85°C, VBAT=9 V..81 V	-5	—	5	mV
V <sub>err(meas)(G)(CTx)</sub>	Cell voltage measurement error CTx, range G. (full range)	V <sub>cell</sub> =-1 V..5 V, T <sub>j</sub> =-20°C..85°C, VBAT= full range	-7	—	7	mV
<b>Cell voltage measurement accuracy for secondary measurement - BOL</b>						
V <sub>err(meas)(A)(CBx)</sub>	Cell voltage measurement error CBx, range A. (LFP cells)	V <sub>cell</sub> =3.3 V, T <sub>j</sub> =25°C, VBAT= 9 V..81 V	-1.7	—	1.7	mV
V <sub>err(meas)(B)(CBx)</sub>	Cell voltage measurement error CBx, range B. (NMC cells)	V <sub>cell</sub> =0 V..4.5 V, T <sub>j</sub> =-20°C..85°C, VBAT= 9 V..81 V	-3	—	3	mV
V <sub>err(meas)(C)(CBx)</sub>	Cell voltage measurement error CBx, range C. (full range)	V <sub>cell</sub> =-1 V..5 V, T <sub>j</sub> =-20°C..85°C, VBAT operating range	-5	—	5	mV
<b>Cell voltage measurement accuracy for secondary measurement - EOL</b>						
V <sub>err(meas)(F)(CBx)</sub>	Cell voltage measurement error CBx, range F. (NMC cells)	V <sub>cell</sub> =0 V..4.5 V, T <sub>j</sub> =-20°C..85°C, VBAT=9 V..81 V	-5	—	5	mV
V <sub>err(meas)(G)(CBx)</sub>	Cell voltage measurement error CBx, range G. (full range)	V <sub>cell</sub> =-1 V..5 V, T <sub>j</sub> =-20°C..85°C, VBAT= full range	-7	—	7	mV
<b>Communication (TPL)</b>						
I <sub>VDDC(TPL)wait</sub>	TPL current on VDDC, device in waiting state	2 RX ON, No TX	—	—	1.4	mA
I <sub>VDDC(TPL)forward</sub>	TPL current on VDDC, device in forward state	1 RX ON, 1 TX ON (TX averaged on bit period)	—	—	11.2	mA
I <sub>VDDC(TPL)respond</sub>	TPL current on VDDC, device in responding state	NO RX, 2 TX ON (TX averaged on bit period)	—	—	21	mA
<b>VDDA</b>						
V <sub>DDA</sub>	VDDA voltage		1.5	1.55	1.6	V
I <sub>lim(VDDA)</sub>	Current limit of VDDA		—	—	12	mA
t <sub>startup(VDDA)</sub>	VDDA startup time	C <sub>load</sub> =100 nF	—	—	50	μs
V <sub>DDA(th)uv</sub>	VDDA undervoltage threshold		1.36	1.4	1.44	V
V <sub>DDA(th)ov</sub>	VDDA overvoltage threshold		1.65	1.7	1.75	V
<b>VAUX</b>						
V <sub>AUX</sub>	VAUX output voltage		3.19	3.3	3.41	V
I <sub>VAUX</sub>	VAUX external current capability		—	—	5	mA
I <sub>lim(VAUX)</sub>	Current limit of VAUX		—	—	12	mA
t <sub>startup(VAUX)</sub>	VAUX startup time	1 KΩ load, 100 nF ext cap	—	—	200	μs
V <sub>AUX(th)uv</sub>	VAUX undervoltage threshold		2.88	3.0	3.12	V
V <sub>AUX(th)ov</sub>	VAUX overvoltage threshold		3.5	3.65	3.8	V
<b>VDDC</b>						
V <sub>DDC</sub>	VDDC output voltage		4.85	5.0	5.15	V
I <sub>VDDC</sub>	External VDDC current drive capability	Ta = -20 °C to 60 °C	—	—	15	mA
t <sub>startup(VDDC)</sub>	Startup time of VDDC	14 Ω sense resistor 5 mA load and 470 nF capacitor	—	—	400	μs

Table 35. Characteristics...continued

$V_{bat} = 9\text{ V to }90\text{ V}$ ;  $T_a = -20\text{ }^{\circ}\text{C to }60\text{ }^{\circ}\text{C}$ ;  $T_j = -20\text{ }^{\circ}\text{C to }85\text{ }^{\circ}\text{C}$ ; all voltages are defined with respect to ground; positive currents flow into the IC. Typical values are given at  $V_{bat} = 72\text{ V}$ ;  $T_a = 25\text{ }^{\circ}\text{C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{out(DRIVE\_VDDC)}$	Driver output current (base current)		-60	—	300	uA
$V_{DDC(th)uv}$	VDDC undervoltage threshold		4.51	4.65	4.79	V
$V_{DDC(th)ov}$	VDDC overvoltage threshold		5.2	5.35	5.5	V
$V_{sense(VDDC)hc}$	Sense voltage of VDDC high current event		167	190	213	mV
$V_{trig(VDDC)oc}$	Trigger voltage of VDDC overcurrent event	for $T_a > +25^{\circ}\text{C}$ , VDDC overcurrent threshold max = 336mV (external NPN transistor thermal protection)	264	300	350	mV
<b>VDDIO</b>						
$V_{DDIO(th)uv}$	VDDIO undervoltage threshold		2.96	3.03	3.1	V
$V_{DDIO(th)ov}$	VDDIO overvoltage threshold		5.25	5.375	5.5	V
<b>Internal temperature measurement</b>						
$T_{j(meas)}$	IC temperature measurement range		-45	—	155	$^{\circ}\text{C}$
$\Delta T_{j(meas)}$	IC temperature measurement error	Range to be measured is $-20\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$	-3	—	3	$^{\circ}\text{C}$
<b>Overtemperature protection</b>						
$T_{sd(th)}$	Shutdown temperature threshold	Of VPRES regulator	160	—	175	$^{\circ}\text{C}$
<b>Mode switching</b>						
$t_{wake(com)}$	Maximum wake-up to communication time	Measured from start of wake-event.	—	—	2.4	ms
$t_{sw(act-sleep)}$	Switching time from Active mode to Sleep mode		—	—	0.3	ms
$t_{sw(act-deepsleep)}$	Switching time from Active mode to deep Sleep mode		—	—	0.3	ms
$t_{sw(act-cyc)}$	Switching time from Active mode to Cyclic mode		—	—	0.3	ms
$t_{wait(cyc-soc)}$	Waiting time between entering in Cyclic mode and start of conversation		5	—	—	ms
$t_{sw(cyc-act)}$	Switching time from Cyclic mode to Active mode		—	—	0.8	ms
$t_{sw(cyc-sleep)}$	Switching time from Cyclic mode to Sleep mode	After completion of the measurement.	—	—	0.3	ms
$t_{sw(sleep-act)}$	Switching time from Sleep mode to Active mode		—	—	2.1	ms
$t_{sw(sleep-cyc)}$	Switching time from Sleep mode to Cyclic mode		—	—	1.6	ms
$t_{startup(deepsleep-act)}$	Start-up time from Deep Sleep mode to Active mode		—	—	2.1	ms
$t_{wake(cyc)res}$	Cyclic mode wake-up time resolution		93	100	107	ms
$\alpha_{wake(cyc)}$	Cyclic mode wake-up time accuracy		-7	—	7	%

Table 35. Characteristics...continued

Vbat = 9 V to 90 V; Ta = -20 °C to 60 °C; Tj = -20 °C to 85 °C; all voltages are defined with respect to ground; positive currents flow into the IC. Typical values are given at Vbat = 72 V; Ta = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t <sub>max(Cwu)</sub>	Maximum Cyclic mode wake-up timer period		6094	6553	7012	s
<b>BIST</b>						
t <sub>check(fr)BIST</sub>	Frame check time for BIST	from setting FEH_MON_BIST_CTRL.STARTBIST until final results available	—	—	500	μs
<b>Measurement resolution</b>						
V <sub>meas(res)VBAT</sub>	Measured voltage resolution		—	3.128	—	mV/LSB
V <sub>meas(res)</sub>	Measured voltage resolution		—	154	—	μV/LSB
T <sub>meas(res)</sub>	Primary and secondary measured temperature resolution		—	32.4	—	mK/LSB
V <sub>meas(res)(supply)</sub>	Supply voltage measurement resolution (VAUX, VDDC)		—	308	—	uV/LSB
V <sub>meas(res)(vdda)</sub>	Supply voltage measurement resolution (VDDA)		—	154	—	uV/LSB
<b>VREF limits</b>						
N <sub>limit(VREF)</sub>	Limits for reference voltages during fault-free operation	PRMM_PER_SECVREF and SECM_PER_PRMVREF	6577h	-	65A9h	LSB
<b>Cell terminal leakage</b>						
I <sub>L(absdyn)</sub>	Dynamic absolute leakage current	absolute cell voltage measurement pin current leakage during measurement sequence	-130	—	130	nA
I <sub>L(difdyn)</sub>	Dynamic differential leakage current	differential cell voltage measurement pin current leakage during measurement sequence	-25	—	25	nA
<b>Cell terminal noise</b>						
V <sub>n(meas)</sub>	Measurement noise voltage	sampling period = 16 scans, T <sub>j</sub> = 85 °C	—	—	300	μVRMS
α <sub>ct(ch)</sub>	Channel crosstalk	based on differential voltage between channel x and x + 1; T <sub>j</sub> = -20°C to 85°C	—	—	-70	dB
<b>Cell terminal open load detection</b>						
R <sub>open(prm)</sub>	Primary open load resistance		6.8	—	13.2	kΩ
R <sub>sw(open)sec</sub>	Secondary cell voltage open-load mechanism switched impedance		13.8	—	26.2	kΩ
M <sub>ratio(open)sec</sub>	Ratio between VBx measurement and actual voltage at VBx pin	CBOL switch closed; VC > 1.5 V	93.6	—	94.1	%
<b>Measurement acquisition</b>						
N <sub>s(PI)</sub>	Number of periodic integrator samples		16	—	511	
N <sub>s(AI)</sub>	Number of application integrator samples		16	—	65534	



Table 35. Characteristics...continued

Vbat = 9 V to 90 V; Ta = -20 °C to 60 °C; Tj = -20 °C to 85 °C; all voltages are defined with respect to ground; positive currents flow into the IC. Typical values are given at Vbat = 72 V; Ta = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Measurement timing</b>						
t <sub>appmeas</sub>	Application measurement time	application result availability after capture command	—	—	265	µs
t <sub>d(prm-start)meas</sub>	Delay time from global primary measurement enable to measurement start		—	—	100	µs
t <sub>d(sec-start)meas</sub>	Delay time from secondary measurement enable to measurement start		—	—	100	µs
t <sub>autopause(prog)</sub>	Programmable autopause time		10	—	160000	µs
t <sub>autopause(acc)</sub>	Autopause timer accuracy		-5	—	5	%
t <sub>autopause(res)</sub>	Autopause time resolution		—	10	—	µs
T <sub>s(meas)</sub>	Measurement sampling period		16.15	17	17.85	µs
t <sub>sync(meas)</sub>	Measurement synchronization time	from any cell to any cell	129.2	136	142.8	µs
<b>VBAT measurement accuracy</b>						
V <sub>I(acc)VBAT</sub>	Measured voltage minimum accuracy	Tj = -20 °C to 85 °C, VBAT ≥ 17 V at pin VBAT (wo Rvbat)	-50	—	50	mV
ΔV <sub>I(meas)VBAT</sub>	Measured Voltage Max Relative Error	Tj = -20 °C to 85 °C, VBAT ≥ 17 V at pin VBAT (wo Rvbat)	—	—	0.3	%
<b>VBAT measurement noise</b>						
V <sub>n(VBAT)(RMS)</sub>	Measurement noise	Sampling period = 16 scan samples, Tj = 85 °C	—	—	10	mVrms
<b>Balancing</b>						
I <sub>bal</sub>	Balancing current	Tj = -20 °C to 85 °C, R <sub>bal</sub> = 10 to 450 Ω, pic current	0	—	360	mA
I <sub>lim(bal)</sub>	Balancing current limit	Tj = -20 °C to 85 °C	360	—	800	mA
R <sub>sw(bal)</sub>	Balancing switch resistance	Tj = -20 °C to 85 °C, V <sub>bat</sub> = 9 V to 81V, 4 to 18 cells	—	—	1.1	Ω
V <sub>th(fault)Bal</sub>	Output fault detection voltage threshold	Tj = -20 °C to +85 °C	0.25	—	0.65	V
I <sub>L(CBx)</sub>	CBx leakage current	Tj = -20...85 °C, 0 < VCBx + 1 - VCBx < 5, ULP mode	-500	—	500	nA
I <sub>L(CBx)</sub>	CBx leakage current	Tj = -20...85 °C, 0 < VCBx + 1 - VCBx < 5, ULP and LP mode, Balancing disabled	-2	—	2	µA
I <sub>L(CBx)3</sub>	CBx input leakage current	Tj = -20 °C...85 °C, -3 < VCBx + 1 - VCBx < 5, All modes, Balancing disabled	-10	—	10	µA
T <sub>th(act)otp</sub>	overtemperature protection activation threshold	threshold for primary temperature measurement to stop balancing	—	3254h	—	LSB
T <sub>th(rel)otp</sub>	overtemperature protection release threshold	threshold for primary temperature measurement to restart balancing	—	3010h	—	LSB

Table 35. Characteristics...continued

$V_{bat} = 9\text{ V to }90\text{ V}$ ;  $T_a = -20\text{ }^{\circ}\text{C to }60\text{ }^{\circ}\text{C}$ ;  $T_j = -20\text{ }^{\circ}\text{C to }85\text{ }^{\circ}\text{C}$ ; all voltages are defined with respect to ground; positive currents flow into the IC. Typical values are given at  $V_{bat} = 72\text{ V}$ ;  $T_a = 25\text{ }^{\circ}\text{C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Balancing timings</b>						
$t_{r(bal)}$	Balancing rise time	$T_j = -20\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ , $R_{bal} = 15\text{ }\Omega$	1	—	100	$\mu\text{s}$
$t_{f(bal)}$	Balancing fall time	$T_j = -20\text{ }^{\circ}\text{C to }85\text{ }^{\circ}\text{C}$ , $R_{bal} = 15\text{ }\Omega$ , from last $bal_{chcfg.chenx}$ bit falling edge or $bal_{globcfg.balen}$ bit falling edge, no fatal fault	1	—	100	$\mu\text{s}$
$t_{d(bal)}$	Balancing delay time	$T_j = -20\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ , $R_{bal} = 15\text{ }\Omega$	—	—	150	$\mu\text{s}$
$t_{gbal(max)}$	Maximum global balancing time		609475.5	655350	701224.5	s
$t_{gbal(res)}$	Global balancing time resolution		—	—	10	s
$t_{gbal(acc)}$	Global balancing time accuracy	$T_j = -20\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$	-7%	—	7%	
$t_{gprebal(max)}$	Maximum global pre-balancing time		609475	655350	701225	s
$t_{gprebal(res)}$	Global pre-balancing time resolution		—	—	10	s
$t_{gprebal(acc)}$	Global pre-balancing time accuracy		-7%	—	7%	
$t_{ibal(max)}$	Maximum individual balancing time		—	—	163830	s
$t_{ibal(res)}$	Individual balancing time resolution		—	—	10	s
$t_{ibal(acc)}$	Individual balancing time accuracy	$T_j = -20\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$	-7% of (programmed period – 10 s)	—	7% of (programmed period – 10 s)	
$\delta_{PWM}$	Pulse width modulation (PWM) duty cycle		0	—	100	%
$\delta_{PWM(res)}$	Pulse width modulation (PWM) duty cycle resolution		$1/2^8$	—	—	%
$f_{PWM(bal)}$	Pulse width modulation (PWM) balancing frequency		—	2	—	Hz
<b>Analog inputs</b>						
$V_{meas(aux)(abs)}$	Auxiliary input measured voltage (absolute value)		0	—	5	V
$V_{meas(ratim)VAUX}$	Auxiliary input measured voltage (ratiometric value)	VAUX voltage used by external circuitry connected to AINx pins	0	—	$VAUX * 0.975$	V
$V_{meas(ratim)VDDC}$	Auxiliary input measured voltage (ratiometric value)	VDDC voltage used by external circuitry connected to AINx pins	0	—	$V_{VDDC} * 0.975$	V
$E_{G(abs)}$	Absolute gain error	$T_j = -20\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$	-0.08	—	0.08	%
$V_{err(offset)(abs)}$	Absolute offset error voltage	$T_j = -20\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$	-3	—	3	mV
$E_{T(meas)ratim}$	Ratiometric measurement total error	$T_j = -20\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$	-0.006 - 0.15% * $V_{AINx}$	—	0.006 + 0.15% * $V_{AINx}$	V
$V_{n(meas)RMS}$	RMS measurement noise voltage	Sampling period = 16 scan samples, $T_j = 85\text{ degC}$	—	—	300	$\mu\text{V}$
$V_{meas(res)(abs)}$	Measured voltage resolution	Absolute measurement (absolute reference voltage)	—	154	—	$\mu\text{V/LSB}$

Table 35. Characteristics...continued

Vbat = 9 V to 90 V; Ta = -20 °C to 60 °C; Tj = -20 °C to 85 °C; all voltages are defined with respect to ground; positive currents flow into the IC. Typical values are given at Vbat = 72 V; Ta = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>meas(res)(ratiom)</sub>	Measured voltage resolution	Ratiometric measurement (VAUX or VDDC)	—	3.05176 x 10 <sup>-3</sup>	—	% / LSB
<b>GPIO</b>						
V <sub>OH(GPIO)</sub>	Output logic high voltage on GPIO pins	I <sub>GPIO</sub> = 1 mA Including routing and all GPIOs / I <sup>2</sup> C driving at the same time.	V <sub>VDDC</sub> - 0.4V	—	V <sub>VDDC</sub>	—
V <sub>OL(GPIO)</sub>	Output logic low voltage on GPIO pins	I <sub>GPIO</sub> = 1 mA Including routing and all GPIOs / I <sup>2</sup> C driving at the same time.	—	—	0.4	V
I <sub>OH(tot)GPIO</sub>	Total HIGH-level output current on GPIO pins		—	—	8	mA
I <sub>OL(tot)GPIO</sub>	Total LOW-level output current on GPIO pins		—	—	20	mA
V <sub>IL(GPIO)</sub>	Input logic low voltage on GPIO pins		—	—	0.8	V
V <sub>IH(GPIO)</sub>	Input logic high voltage on GPIO pins		2.0	—	—	V
V <sub>hys(GPIO)</sub>	Input hysteresis voltage on GPIO pins		0.15	—	1.0	V
V <sub>IL(wake)GPIO</sub>	Input logic low wake-up voltage on GPIO pins		—	—	0.8	V
V <sub>IH(wake)GPIO</sub>	Input logic high wake-up voltage on GPIO pins		2.5	—	—	V
V <sub>hys(wake)GPIO</sub>	Input hysteresis wake-up voltage on GPIO pins		0.03	—	1.2	V
t <sub>deglitch(GPIO)</sub>	Deglitch time on GPIO pins (not for wake up and alarm)		3.81	—	5.6	µs
I <sub>L(GPIO)</sub>	Leakage current on GPIO pins	GPIO0 and GPIO1	—	—	100	nA
I <sub>L(GPIO)</sub>	Leakage current on GPIO pins	GPIO2 to GPIO7, VDDC Active.	—	—	100	nA
<b>GPIO Diagnostics</b>						
R <sub>OL(GPIO)</sub>	GPIO openload diagnostic resistance		6.8	10	13.2	kΩ
<b>Wake pin</b>						
t <sub>deglitch(GPIO0)wake</sub>	Wake-up time of deglitch function on pin GPIO0		50	80	100	µs
<b>ALARM</b>						
t <sub>alarm(deglitch)GPIO1</sub>	Alarm time of deglitch filter on GPIO1 pin		93	—	118.27	µs
t <sub>heartbeat(IH)</sub>	Heartbeat input high time	if ALARMINHBINV = 0, then heartbeat input high time; if ALARMINHBINV = 1, then heartbeat input low time	360	—	640	µs
t <sub>heartbeat(IL)</sub>	Heartbeat input low time	ALARMINHB = T <sub>500u</sub>	360	—	640	µs
t <sub>heartbeat(IL)</sub>	Heartbeat input low time	ALARMINHB = T <sub>1ms</sub>	830	—	1180	µs
t <sub>heartbeat(IL)</sub>	Heartbeat input low time	ALARMINHB = T <sub>10ms</sub>	9240	—	10860	µs
t <sub>heartbeat(IL)</sub>	Heartbeat input low time	ALARMINHB = T <sub>100ms</sub>	93350	—	107630	µs

Table 35. Characteristics...continued

Vbat = 9 V to 90 V; Ta = -20 °C to 60 °C; Tj = -20 °C to 85 °C; all voltages are defined with respect to ground; positive currents flow into the IC. Typical values are given at Vbat = 72 V; Ta = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I <sub>O(source)alarm</sub>	Alarm line output source current	V <sub>VDDIO</sub> = V <sub>VDDC</sub> V <sub>ALARM_OUT</sub> = V <sub>VDDIO</sub> - 0.8 V	2	—	—	mA
I <sub>O(sink)alarm</sub>	Alarm line output sink current	V <sub>ALARM_OUT</sub> = 0.8 V	2	—	—	mA
I <sub>O(source)alarm</sub>	Alarm line output source current	V <sub>VDDIO</sub> = V <sub>VDDC</sub> V <sub>ALARM_OUT</sub> = -0.4 V	1	—	—	mA
I <sub>O(sink)alarm</sub>	Alarm line output sink current	V <sub>VDDIO</sub> = V <sub>VDDC</sub> V <sub>ALARM_OUT</sub> = 0.4 V	1	—	—	mA
t <sub>heartbeat(OH)</sub>	Heartbeat output high time		460	—	540	µs
t <sub>heartbeat(OL)</sub>	Heartbeat output low time	ALARMOUTH = T <sub>500µs</sub>	460	—	540	µs
t <sub>heartbeat(OL)</sub>	Heartbeat output low time	ALARMOUTH = T <sub>1ms</sub>	930	—	1080	µs
t <sub>heartbeat(OL)</sub>	Heartbeat output low time	ALARMOUTH = T <sub>10ms</sub>	9340	—	10760	µs
t <sub>heartbeat(OL)</sub>	Heartbeat output low time	ALARMOUTH = T <sub>100ms</sub>	93450	—	107530	µs
<b>I<sup>2</sup>C-bus interface</b>						
t <sub>IO(I2C-bus)</sub>	I <sup>2</sup> C-bus timeout time		35	—	55	µs
V <sub>IL(I2C-bus)</sub>	I <sup>2</sup> C-bus input logic low voltage		—	—	0.3 * V <sub>VDDIO</sub>	V
V <sub>IH(I2C-bus)</sub>	I <sup>2</sup> C-bus input logic high voltage		0.7 * V <sub>VDDIO</sub>	—	—	V
V <sub>hys(I2C-bus)</sub>	I <sup>2</sup> C-bus input hysteresis voltage		0.05 * V <sub>VDDIO</sub>	—	—	V
I <sub>I(I2C-bus)</sub>	Input current on I <sup>2</sup> C pins	Only with VDDC/VDDIO ON.	-10	—	+10	µA
C <sub>i(I2C-bus)</sub>	Input capacitance on I <sup>2</sup> C pins		—	—	10	pF
V <sub>OL(I2C-bus)</sub>	I <sup>2</sup> C-bus output logic low voltage	I <sub>OL_I2C</sub> = 5 mA, Including routing and all GPIOs / I2C driving at the same time.	—	—	0.4	V
t <sub>f(o)I2C-bus</sub>	I <sup>2</sup> C-bus output fall time from V <sub>IH(min)</sub> to V <sub>IL(max)</sub>		0	—	120	ns
f <sub>SCL</sub>	SCL clock frequency	bit I2C_CFG.CLKSEL = 1 no clock stretching	0	—	100	kHZ
t <sub>HD;STA</sub>	Hold time (repeated) START condition		4.0	—	—	µs
t <sub>LOW</sub>	LOW period of the SCL clock std. mode		4.7	—	—	µs
t <sub>HIGH</sub>	HIGH period of the SCL clock std. mode		4.0	—	—	µs
t <sub>LOW</sub>	LOW period of the SCL clock fast mode		1.3	—	—	µs
t <sub>HIGH</sub>	HIGH period of the SCL clock fast mode		0.6	—	—	µs
t <sub>SU;STA</sub>	Set-up time for a repeated START condition		4.7	—	—	µs
t <sub>SU;DAT</sub>	Data set-up time		250	—	—	ns
t <sub>SU;STO</sub>	Set-up time for STOP condition		4.0	—	—	µs
C <sub>bus</sub>	Capacitive load for each bus line		—	—	100	pF

**Table 35. Characteristics...continued**

$V_{bat} = 9\text{ V to }90\text{ V}$ ;  $T_a = -20\text{ }^{\circ}\text{C to }60\text{ }^{\circ}\text{C}$ ;  $T_j = -20\text{ }^{\circ}\text{C to }85\text{ }^{\circ}\text{C}$ ; all voltages are defined with respect to ground; positive currents flow into the IC. Typical values are given at  $V_{bat} = 72\text{ V}$ ;  $T_a = 25\text{ }^{\circ}\text{C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{VD,DAT}$	Data valid time std. mode		—	—	3.45	$\mu\text{s}$
$t_{VD,ACK}$	Data valid acknowledge time std. mode		—	—	3.45	$\mu\text{s}$
$t_{VD,DAT}$	Data valid time fast mode		—	—	0.9	$\mu\text{s}$
$t_{VD,ACK}$	Data valid acknowledge time fast mode		—	—	0.9	$\mu\text{s}$
<b>Communication timings</b>						
$t_{d(rec-trans)}$	Time between request received by the device and response transmitted		1.3	—	8	$\mu\text{s}$
$t_{d(TPL)}$	Time between two consecutive response message frames transmitted by the product		1.3	—	2.8	$\mu\text{s}$
$t_{to(EOM)}$	Time for end of message timeout	SOM symbol to EOM symbol	250	—	300	$\mu\text{s}$
$t_{d(req)MCU}$	Time between two requests transmitted by MCU		1.3	—	—	$\mu\text{s}$
$t_{d(Fd)}$	Forward delay time	Time required by a message to propagate from one port of the device to the other port of the same device; the delay is measured between SOM to SOM	—	0.5	1.7	$\mu\text{s}$
$t_{d(wake)}$	Time between two consecutive wake-up messages.		3	—	4	ms
$R_{data(TPL)}$	TPL data rate		1.9	—	2.1	Mbit/s
<b>Communication timeout</b>						
$t_{to(com)res}$	Communication time-out resolution		9.5	10	10.5	ms
$t_{to(com)min}$	Minimal communication time-out time		9.5	10	10.5	ms
$t_{to(com)max}$	Maximum communication time-out time		2422.5	2550	2677.5	ms
<b>Communication (TPL)</b>						
$V_{th(sleep-wake)dif}$	Differential receiver threshold voltage in deep Sleep mode or in Sleep mode to wake-up		1.15	—	—	V
$V_{th(full\ power)dif}$	Differential receiver threshold voltage	Active mode rising <sub>edge</sub>	0.48	—	0.68	V
$V_{hys(RX)dif}$	Differential receiver hysteresis voltage		70	—	130	mV
$V_{o(peak)dif}$	Differential peak output voltage	$R_{diff} = 120\text{ }\Omega$ $V_{VDDC} > 4.85\text{ V}$ $V_{VDDC} < 5.15\text{ V}$	1.1	—	2.2	V
$R_{term(act)}$	Termination resistance in Active mode	IC configured in TPL mode and not in sleep states	—	170	—	$\Omega$
$R_{term(sleep)}$	Termination resistance in sleep mode	In SPI mode and in deep sleep and sleep states	20	—	100	k $\Omega$

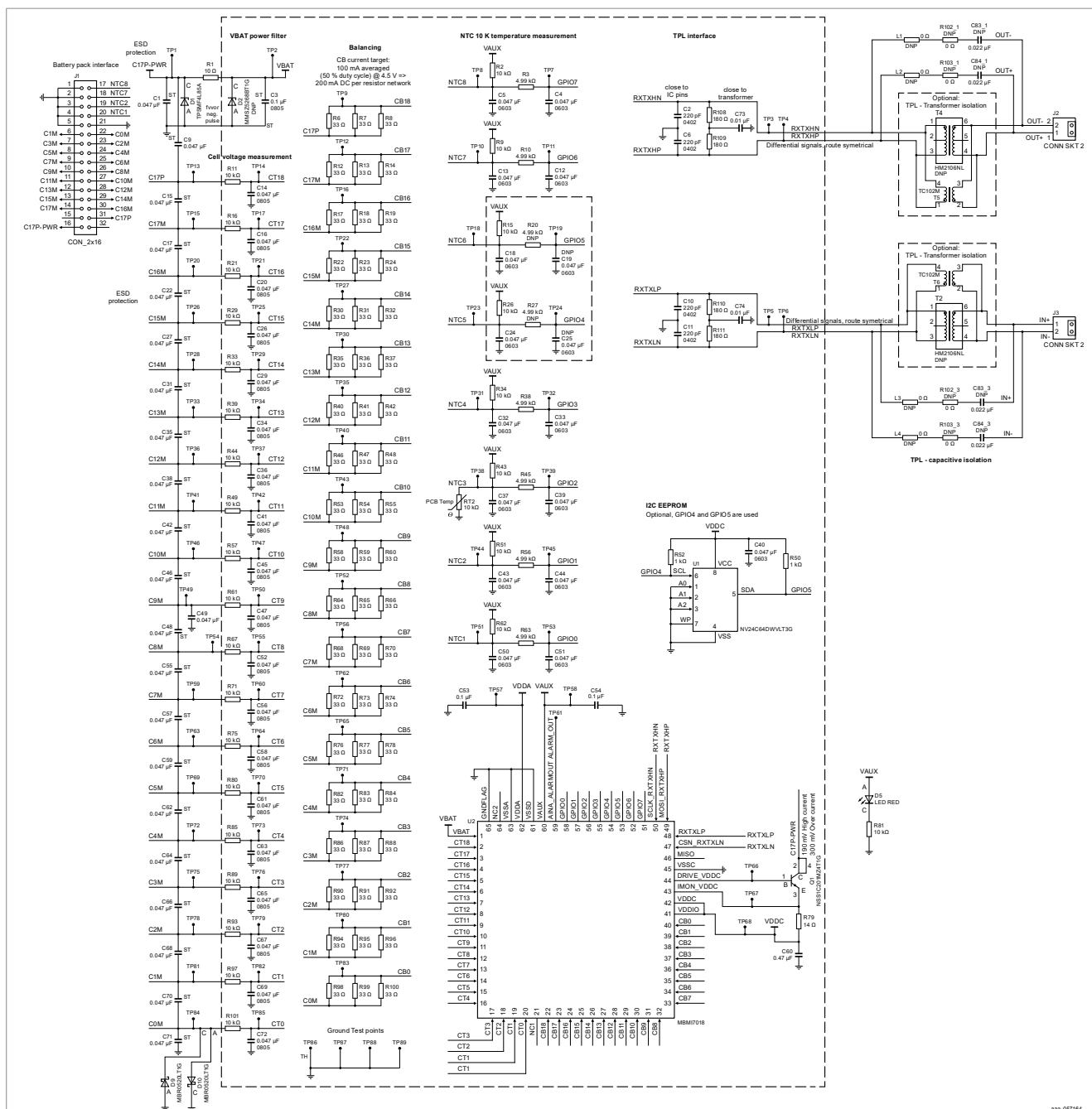
**Table 35. Characteristics...continued**

$V_{bat} = 9\text{ V to }90\text{ V}$ ;  $T_a = -20\text{ }^{\circ}\text{C to }60\text{ }^{\circ}\text{C}$ ;  $T_j = -20\text{ }^{\circ}\text{C to }85\text{ }^{\circ}\text{C}$ ; all voltages are defined with respect to ground; positive currents flow into the IC. Typical values are given at  $V_{bat} = 72\text{ V}$ ;  $T_a = 25\text{ }^{\circ}\text{C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Communication (SPI)</b>						
$V_{IL(SPI)}$	SPI input low voltage on MOSI, CSN, SCLK pins		—	—	0.8	V
$V_{IH(SPI)}$	SPI input high voltage on MOSI, CSN, SCLK pins		2.0	—	VDDIO + 0.3	V
$V_{hys(SPI)}$	SPI input hysteresis voltage on MOSI, CSN, SCLK pins		30	—	600	mV
$V_{IH(wake)CSN}$	SPI input logic high wake-up voltage on CSN pin		2.5	—	—	V
$V_{IL(wake)CSN}$	SPI input logic low wake-up voltage on CSN pin		—	—	0.8	V
$V_{hys(wake)CSN}$	SPI input hysteresis wake-up voltage on CSN pin		30	—	1200	mV
$V_{OL(SPI)}$	SPI output logic low voltage on MISO pin	2 mA	—	—	0.4	V
$V_{OH(SPI)}$	SPI output logic high voltage on MISO pin	-2 mA	VDDIO - 0.4	—	—	V
$f_{SPI}$	SPI output logic high voltage on MISO pin		—	—	4.2	MHz
$t_{en(MISO)}$	MISO enable time		0	—	40	ns
$t_{dis(MISO)}$	MISO disable time		0	—	40	ns
$t_{v(data)MISO}$	MISO data valid after rising edge of SCLK		0	—	45	ns
$t_{d(data)transfer}$	Sequential data transfer delay time		1	—	—	$\mu$ s
$t_{SCLKH}$	SCLK high time		90	—	—	ns
$t_{SCLKL}$	SCLK low time		90	—	—	ns
$t_{FALLSPI}$	SCLK, CSN, and MOSI fall time		—	—	15	ns
$t_{RISESPI}$	SCLK, CSN and MOSI rise time		—	—	15	ns
$t_{SETUPSPI}$	MOSI to SCLK falling edge setup time		20	—	—	ns
$t_{HOLDSPI}$	MOSI to SCLK falling edge hold time		20	—	—	ns
$CSN_{LEAD}$	CSN lead time		100	—	—	ns
$CSN_{LAG}$	CSN lag time		100	—	—	ns
$SCLK_{SBL}$	SCLK stable before CSN low		40	—	—	ns
$SCLK_{SBH}$	SCLK stable after CSN high		40	—	—	ns
$t_{low(wake)}$	Minimum CSN low time before rising edge for wake-up		12	—	—	us

## 11 Application information

Figure 55 provides an application example for the BMI7018 in a typical 18-cell battery application.



**Figure 55. Typical application**

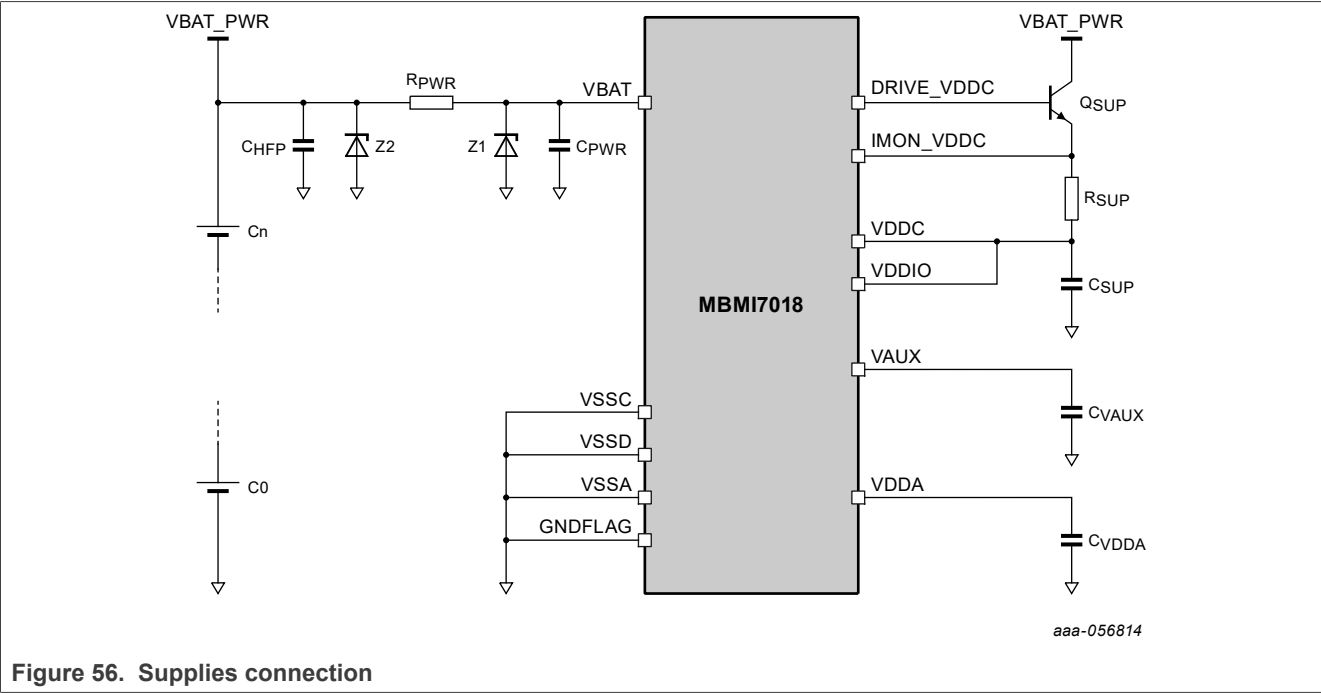
11.1 Typical applications

11.1.1 External components

This section provides information about recommended external components and how to select them.

11.1.1.1 Power supplies

The recommended schematic to supply the BMI7018 and enable voltages is described in [Figure 56](#).



The component values and comments are described in [Table 36](#).

Table 36. Supply components

ID	Value	Units	Comment
C <sub>HFP</sub>	0.047	μF	100 V capacitor; should not be changed to sustain ESD and hotplug.
R <sub>PWR</sub>	10 / 0.1W	Ω	do not exceed to avoid excessive voltage drop between VBAT and CT18; Combined with C <sub>PWR</sub> to filter noise above 160 kHz.
C <sub>PWR</sub>	0.1	μF	100 V capacitor; should not be changed.
Z2			Optional: To sustain negative iso pulses; TPSMF4L85A or equivalent
Z1			Optional: Overvoltage protection; use MMSZ5268BT1G or equivalent.
Q <sub>SUP</sub>			Ballast NPN transistor; PBHV8215Z or equivalent; (Key parameters: V <sub>ceo</sub> min = 120 V, Beta min = 50, I <sub>cbo</sub> < 50 μA).
R <sub>SUP</sub>	14	Ω	Optimal value for VDDC current sourcing and monitoring in TPL applications.
C <sub>SUP</sub>	0.47	μF	25 V capacitor, should not be changed.
C <sub>VAUX</sub>	0.1	μF	25 V capacitor, should not be changed.
C <sub>VDDA</sub>	0.1	μF	25 V capacitor, should not be changed.



11.1.1.2 Cell terminal filters

Figure 57 shows the recommended cell terminal connections first order low-pass filters, cell balancing connections, and ESD protection capacitors.

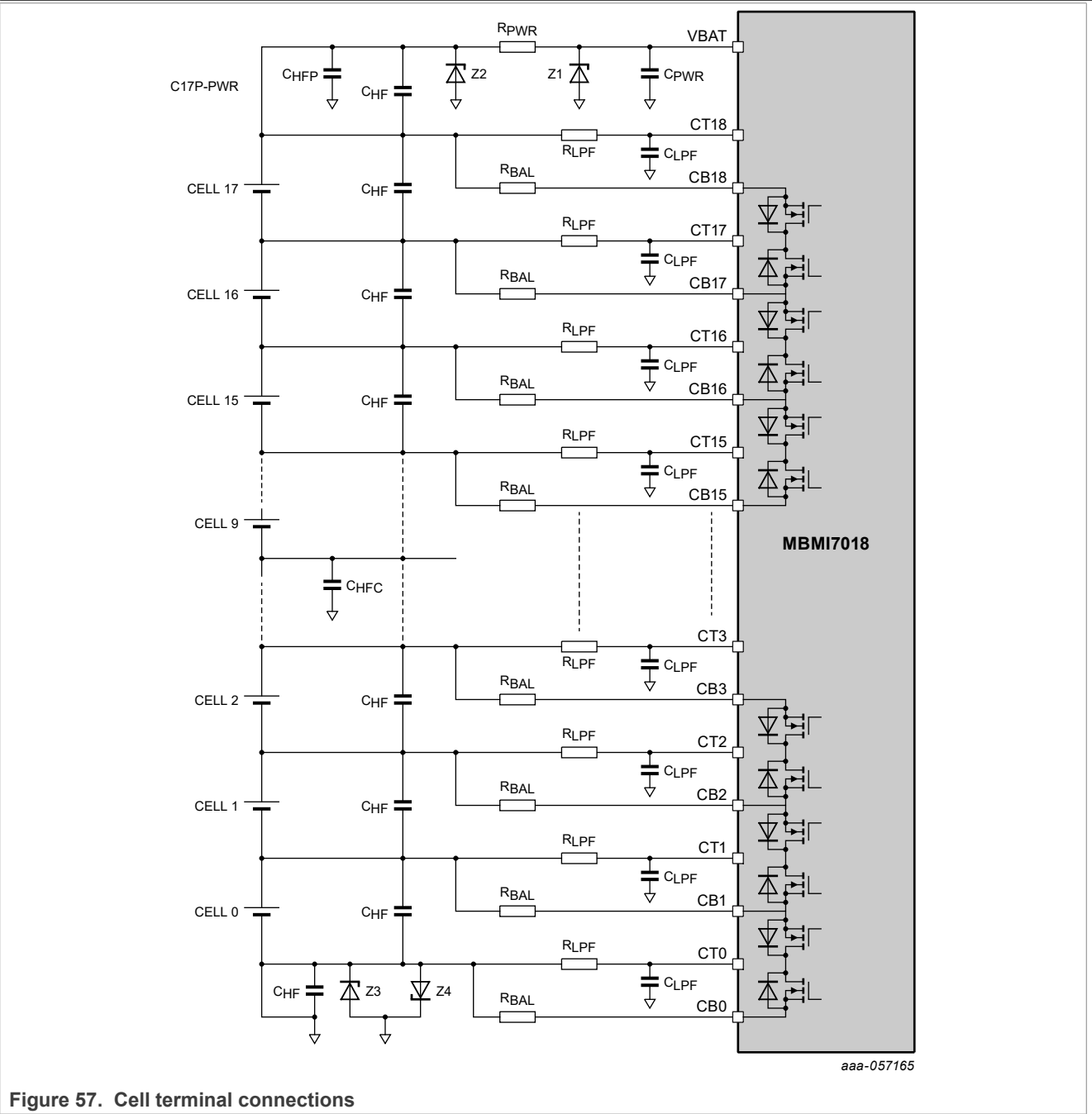


Figure 57. Cell terminal connections

The component values and comments are described in Table 37

Table 37. Cell terminal connection component values

ID	Value	Units	Comments
C <sub>HF</sub>	0.047	μF	25 V capacitor; should not be changed to sustain ESD
C <sub>HFC</sub>	0.047	μF	optional: 100 V common mode capacitor on the middle cell to improve EMC performances
R <sub>LPF</sub>	10	kΩ	Should not be changed; Antialiasing filtering with C <sub>LPF</sub> : fcut : 338 Hz (ten times below 4 kHz internal ADC sampling)
C <sub>LPF</sub>	0.047	μF	100 V capacitor; should not be changed
R <sub>BAL</sub>	X	Ω	Any value is possible if following cell balance current limits are not exceeded: 9 mA > I > 300 mA peak (V <sub>cellmax</sub> / (2 x R <sub>bal</sub> ))
Z3, Z4			optional: Schottky diodes to improve EMC performances - for example, MBR0520LT1G

11.1.1.3 External cell balancing

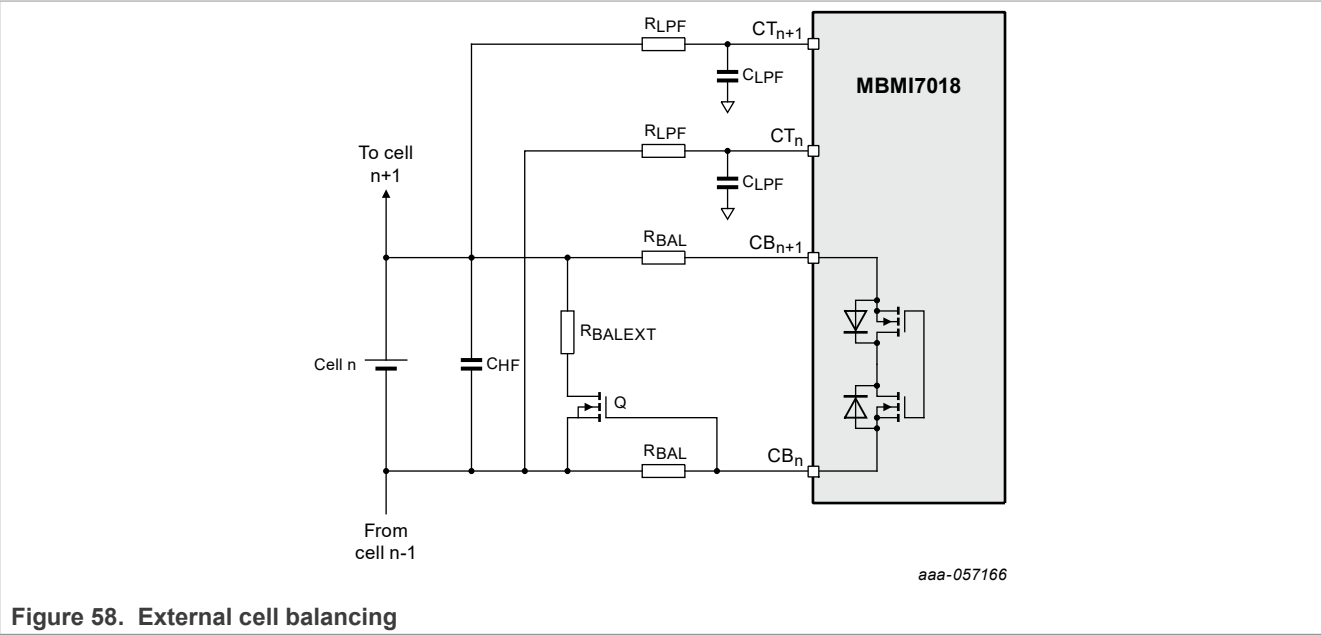
External cell balancing can be implemented with external transistors to increase the total balancing current or shift the power dissipation out of the device toward external cell-balancing resistors. For one cell-balancing channel switched on, the total balancing current will be the sum of the currents through the internal (through 2xR<sub>bal</sub>) and external (through R<sub>balext</sub>) transistors. NMOS, PMOS, and BJT can be used in a similar way.

Figure 58 shows the principle of such implementation with an NMOSFET (Q) as external cell balancing transistor. The NMOSFET is switched on synchronously with the internal cell-balancing switches, when the voltage drop across R<sub>bal</sub> reaches the NMOSFET V<sub>gs</sub> threshold of the NMOSFET.

The maximum V<sub>gs</sub> voltage equals V<sub>cell</sub>/2. Low V<sub>gs</sub> NMOSFET should be selected to ensure a good saturation at the desired current. The selected NMOSFET should be capable for the required cell balancing current, power dissipation, and also capable sustaining negative V<sub>gs</sub> voltage when the adjacent cell-balancing channel is on.

The behavior is fully transparent for the application and does not require any specific software adaptation.

The user is in charge of selecting and validating the external transistors type, characteristics, external balancing resistors, and additional components to protect the transistor against electrical overstresses (for example, hotplug), depending on the user's application requirements.



11.1.1.4 Temperature channels

Figure 59 shows configuration of AINx inputs configured as temperature measurements

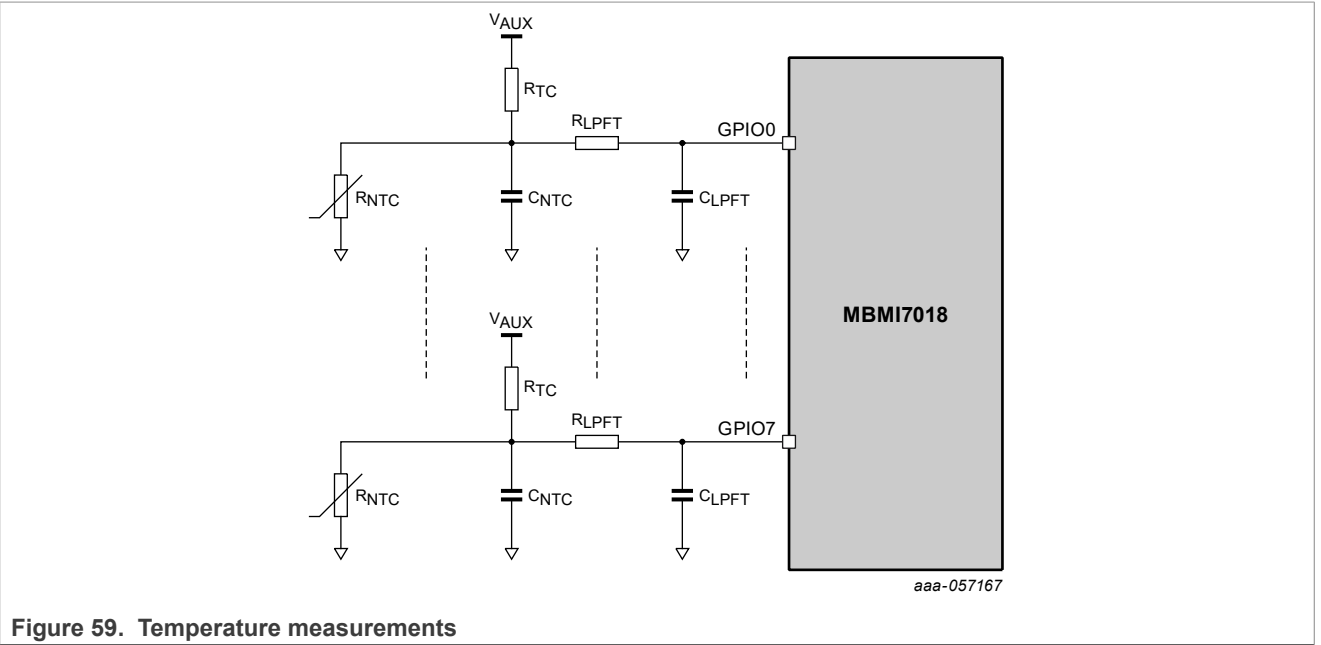


Figure 59. Temperature measurements

Table 38. AINx filter components for temperature measurements

ID	Value	Units	Comments
R <sub>TC</sub>	10	kΩ	Optimal for R <sub>NTC</sub> = 10 kΩ; If changed, see C <sub>LPFT</sub> .
R <sub>NTC</sub>	10	kΩ	Nominal value resistance is given at 25 °C.
C <sub>NTC</sub>	0.047	μF	Optional: ESD protection for off board NTC.
R <sub>LPFT</sub>	5	kΩ	Should not be changed for NTC = 10 kΩ to get F <sub>cut</sub> around 330 Hz with C <sub>LPFT</sub> and keep timing margin for cyclic acquisitions.
C <sub>LPFT</sub>	0.047	μF	Should not be changed for NTC = 10 kΩ.

11.1.1.5 Alarm signal daisy chain

Figure 60 shows the connection of the alarm daisy chain signal between two battery-cell controllers

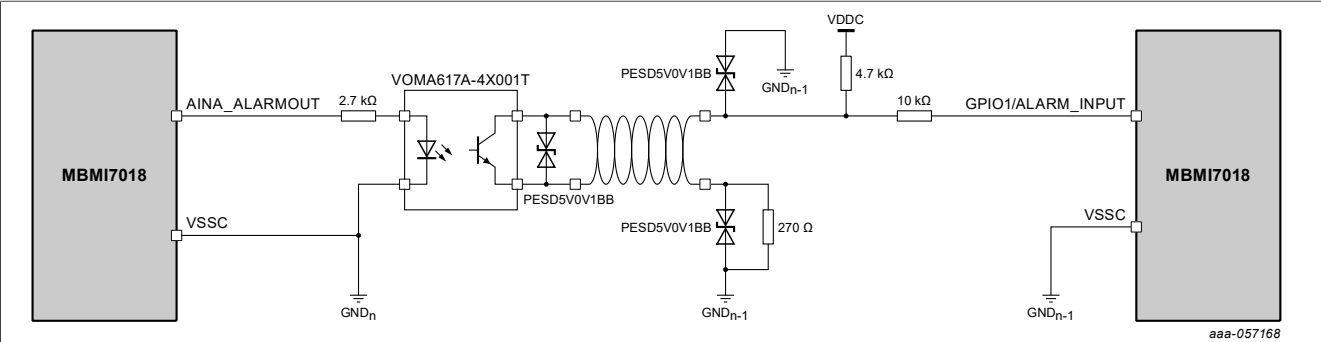


Figure 60. Alarm daisy chain

11.1.1.6 BMI7018 - Isolated communication interface

High-speed differential isolated communication is achieved by using transformers or capacitors.

11.1.1.6.1 BMI7018 distributed applications

11.1.1.6.1.1 Transformer isolation

Figure 61 shows the recommended application schematic with transformer isolation in a distributed system.

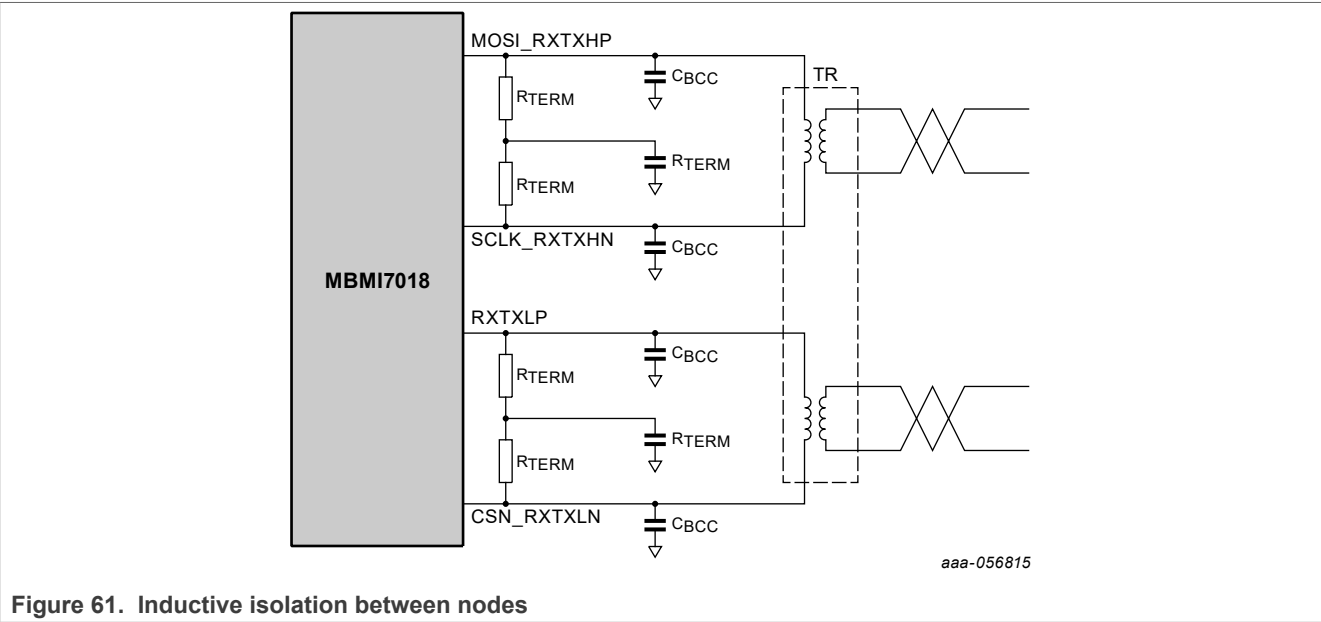


Figure 61. Inductive isolation between nodes

11.1.1.6.1.2 Capacitive isolation

Figure 62 shows the recommended application schematic for capacitive isolation, between nodes, in a distributed system.

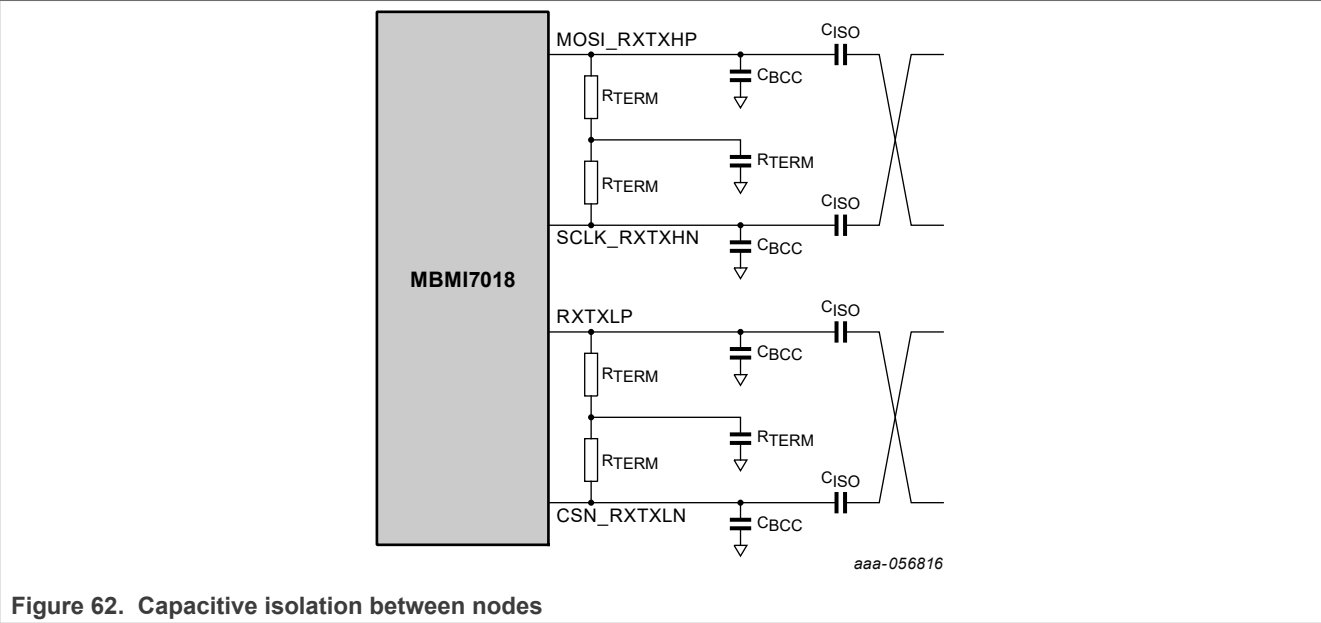


Figure 62. Capacitive isolation between nodes

11.1.1.6.1.3 Component values

Table 39. Component values

ID	Value	Units	Comments
C <sub>BCC</sub>	220	pF	Common mode capacitors
C <sub>ISO</sub>	22	nF	Isolation capacitors
R <sub>TERM</sub>	180	Ω	Split termination resistor
C <sub>TERM</sub>	10	nF	Split termination capacitor
TR	1:1		1 x dual channel 1:1 transformer (i.e., Pulse Electronic HM2118/HM2168) or 2 x single channel transformers (i.e., Pulse Electronic TC102M, HM2119, HM2106/HM2166, TDK P303506-A1-51) - no center taps required - no common mode chokes required - Insertion Loss : -1 dB max - OCL 60 μH min

11.1.1.6.2 BMI7018 centralized applications

11.1.1.6.2.1 Transformer isolation

Figure 63 shows the recommended schematic when using transformers in a centralized application.

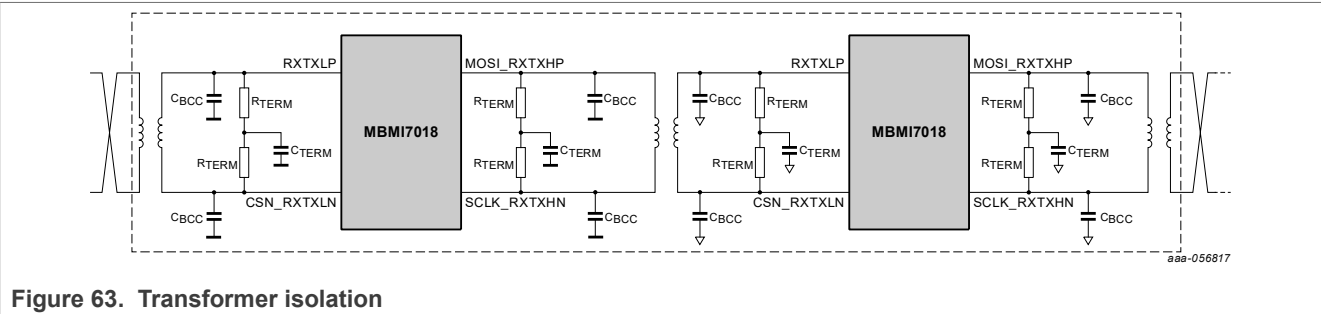


Figure 63. Transformer isolation

### 11.1.1.6.2.2 Capacitive isolation

Figure 64 shows the recommended schematic when using capacitors in a centralized application for onboard and offboard connections.

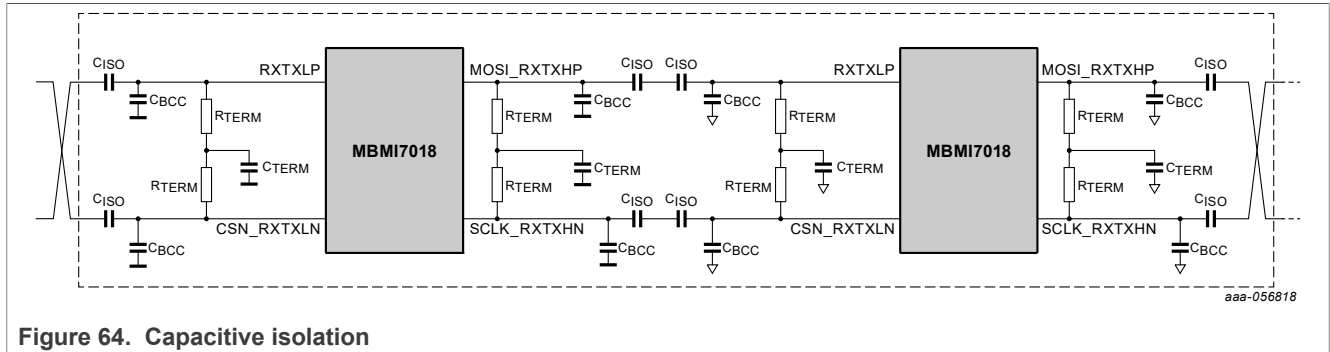


Figure 64. Capacitive isolation

### 11.1.1.6.2.3 Transformer and capacitive isolation

Figure 65 shows the recommended schematic in a centralized application when using capacitors for onboard connections and transformers for offboard connections.

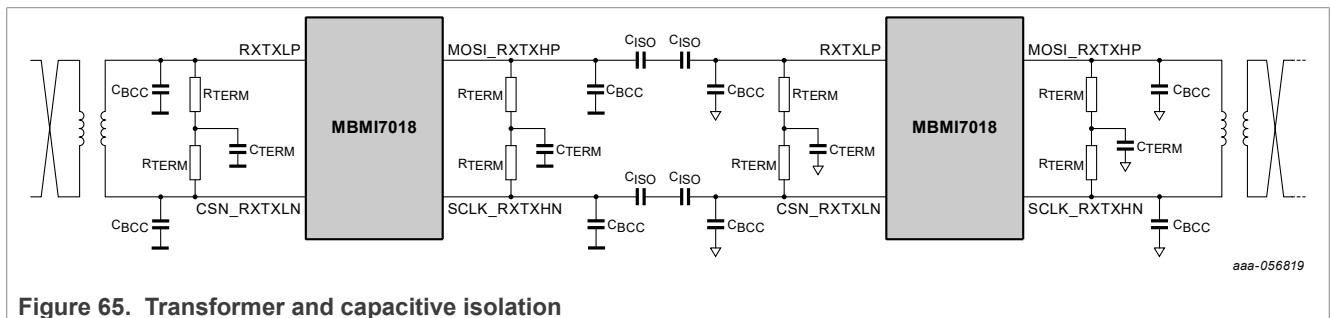


Figure 65. Transformer and capacitive isolation

### 11.1.1.6.2.4 Component values

Table 40. Component values

ID	Value	Units	Comments
CBCC	220	pF	Common mode capacitors
CISO	22	nF	Isolation capacitors
RTERM	180	Ω	Split termination resistor
CTERM	10	nF	Split termination capacitor
TR	1:1		1 x dual-channel 1:1 transformer (i.e., Pulse Electronic HM2118/HM2168) or 2 x single channel transformers (i.e., Pulse Electronic TC102M, HM2119, HM2106/HM2166, TDK P303506-A1-51) - no center taps required - no common mode chokes required - Insertion Loss: -1 dB max - OCL 60 μH min

### 11.1.2 Cell and bus bar connections on CT/CB terminals

The cells are connected to the CT pins starting from the lower position. Unused CT pins remain on the upper CT pins and can be connected to the next lower CT pin without need of external components. Unused CB pins connection follows the same connection strategy as for unused CT pins.

Unused CT pins with complete low pass filter can be connected to the next lower CT pins through a connector.

Bus bars are considered as cells and can be connected to CT pins to allow bus bar voltage measurement through primary measurement chain and to CB pins for secondary measurement. Two cells minimum should separate two bus bars.

Positions for cell connection, bus bars connection, and voltages are summarized in the [Figure 66](#).

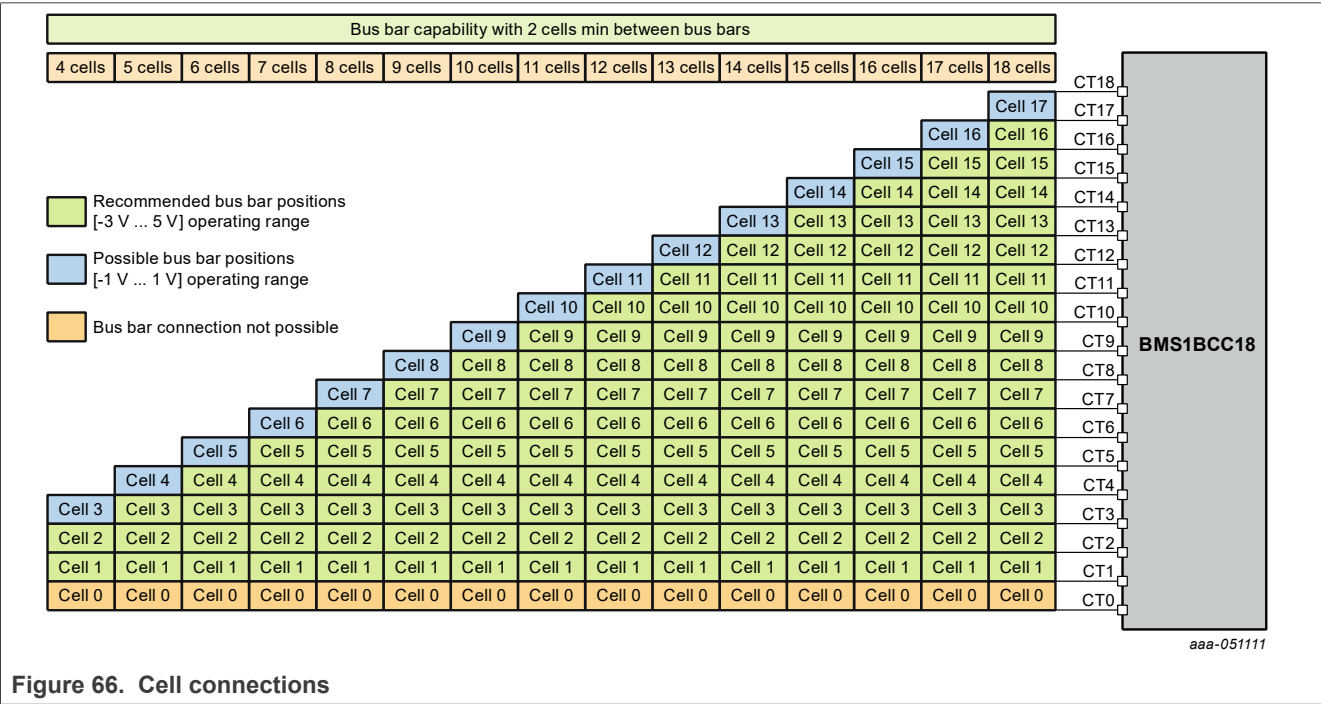


Figure 66. Cell connections

## 12 Register map

Table 41. BMI7018 register map

Start address	End address	Range	Function
00001C00h	00001FFFh	00000400h	<a href="#">secondary measurement</a>
00001800h	00001BFFh	00000400h	<a href="#">primary measurement</a>
00001400h	000017FFh	00000400h	<a href="#">all measurements</a>
00001000h	000013FFh	00000400h	<a href="#">cell balancing registers</a>
00000C00h	00000FFFh	00000400h	<a href="#">I<sup>2</sup>C-bus interface</a>
00000800h	00000BFFh	00000400h	<a href="#">GPIO</a>
00000400h	000007FFh	00000400h	<a href="#">event handling</a>
00000000h	000003FFh	00000400h	<a href="#">system control</a>

### 12.1 Register description

Table 42. Register overview: System\_Control\_Registers

Address	Name	Access	Reset	Description
0h	<a href="#">SYS_CFG_CRC</a>	R	0h	system configuration CRC
1h	<a href="#">SYS_COM_CFG</a>	R/W	200h	communication initialization
2h	<a href="#">SYS_COM_TO_CFG</a>	R/W	1Eh	system communication timeout
3h	<a href="#">SYS_SUPPLY_CFG</a>	R/W	8003h	supply configuration
4h	<a href="#">SYS_MODE</a>	R/W	1400h	system mode
5h	<a href="#">SYS_CYC_WAKEUP_CFG</a>	R/W	0h	interval for cyclic measurements
6h	<a href="#">SYS_TPL_CFG</a>	R/W	10h	TPL configuration
8h	<a href="#">SYS_CLK_SYNC_CTRL</a>	R/W	0h	clock Synchronization
10h	<a href="#">SYS_VERSION</a>	R	320h	device silicon identifier
11h	<a href="#">SYS_UID_LOW</a>	R	0h	unique device ID lower part
12h	<a href="#">SYS_UID_MID</a>	R	0h	unique device ID middle part
13h	<a href="#">SYS_UID_HIGH</a>	R	0h	unique device ID higher part
14h	<a href="#">SYS_PROD_VER</a>	R	200h	software interface related version of the product
80h	<a href="#">SYS_DS_STORAGE0</a>	R/W	0h	deep sleep storage data 0; the value is stored in the ULP domain
81h	<a href="#">SYS_DS_STORAGE1</a>	R/W	0h	deep sleep storage data 1; the value is stored in the ULP domain

Table 43. Register overview: Event\_Handling\_Registers

Address	Name	Access	Reset	Description
400h	<a href="#">FEH_CFG_CRC</a>	R	0h	configuration CRC
401h	<a href="#">FEH_ALARM_CFG</a>	R/W	0h	general alarm configuration
402h	<a href="#">FEH_ALARM_OUT_CFG0</a>	R/W	0h	alarm output source selection
403h	<a href="#">FEH_ALARM_OUT_CFG1</a>	R/W	0h	alarm output source selection
404h	<a href="#">FEH_ALARM_OUT_REASON0</a>	R	0h	alarm output reason
405h	<a href="#">FEH_ALARM_OUT_REASON1</a>	R	0h	alarm output reason
408h	<a href="#">FEH_WAKEUP_CFG0</a>	R/W	0h	wake up source configuration



Table 43. Register overview: Event\_Handling\_Registers...continued

Address	Name	Access	Reset	Description
409h	<a href="#">FEH_WAKEUP_CFG1</a>	R/W	0h	wake up source configuration
40Ah	<a href="#">FEH_WAKEUP_REASON0</a>	R	0h	wake up reason register
40Bh	<a href="#">FEH_WAKEUP_REASON1</a>	R	0h	wake up reason register
410h	<a href="#">FEH_MON_BIST_CTRL</a>	R/W	0h	monitor BIST control register
411h	<a href="#">FEH_MON_BIST_RES</a>	R	FFh	monitor BIST result register; value changes at start-up, if everything is fine to 0000h
41Eh	<a href="#">FEH_ACC_ERR</a>	R	0h	access error status register
41Fh	<a href="#">FEH_GRP_FLT_STAT</a>	R	0h	main system fault status register; this register holds one bit per fault group. For each fault group a separate status register exists. The bit here is cleared if all its sources are cleared.
420h	<a href="#">FEH_SUPPLY_FLT_STAT0</a>	R/W	0h	supply fault status register 0 (these monitors are part of the BIST)
421h	<a href="#">FEH_SUPPLY_FLT_STAT1</a>	R/W	0h	supply fault status register 1 (these monitors are not part of the BIST)
422h	<a href="#">FEH_ANA_FLT_STAT</a>	R/W	0h	analog fault status register
423h	<a href="#">FEH_COM_FLT_STAT</a>	R/W	0h	communication fault status register
424h	<a href="#">FEH_MEAS_FLT_STAT</a>	R/W	0h	other fault status register
428h	<a href="#">FEH_SUPPLY_FLT_POR_CFG0</a>	R/W	0h	supply fault POR selection 0
429h	<a href="#">FEH_SUPPLY_FLT_POR_CFG1</a>	R/W	0h	supply fault POR selection 1
42Ah	reserved	R	0h	analog fault POR selection
42Bh	<a href="#">FEH_COM_FLT_POR_CFG</a>	R/W	8h	communication fault POR enable register
430h	<a href="#">FEH_SUPPLY_FLT_EVT_CFG0</a>	R/W	0h	supply fault event selection register 0
431h	<a href="#">FEH_SUPPLY_FLT_EVT_CFG1</a>	R/W	0h	supply fault event selection register 1
432h	<a href="#">FEH_ANA_FLT_EVT_CFG</a>	R/W	0h	analog fault event enable register
433h	<a href="#">FEH_COM_FLT_EVT_CFG</a>	R/W	0h	communication fault event enable register
434h	<a href="#">FEH_MEAS_FLT_EVT_CFG</a>	R/W	0h	measurement fault event enable register
480h	<a href="#">FEH_POR_REASON</a>	R	0h	power-on reset reason. The value is stored in the ULP domain.

Table 44. Register overview: GPIO\_Registers

Address	Name	Access	Reset	Description
800h	<a href="#">GPIO_CFG0</a>	R/W	0h	GPIO configuration 0
801h	<a href="#">GPIO_CFG1</a>	R/W	0h	GPIO configuration 1
802h	<a href="#">GPIO_OUT</a>	R/W	0h	GPIO output
804h	<a href="#">GPIO_IN</a>	R	0h	GPIO input

Table 45. Register overview: I2C\_Registers

Address	Name	Access	Reset	Description
C00h	<a href="#">I2C_CFG</a>	R/W	0h	I2C configuration
C01h	<a href="#">I2C_CTRL</a>	R/W	0h	I2C control
C02h	<a href="#">I2C_STAT</a>	R	0h	I2C status
C04h	<a href="#">I2C_DATA0</a>	R/W	0h	I2C data register 0
C05h	<a href="#">I2C_DATA1</a>	R/W	0h	I2C data register 1
C06h	<a href="#">I2C_DATA2</a>	R/W	0h	I2C data register 2
C07h	<a href="#">I2C_DATA3</a>	R/W	0h	I2C data register 3
C08h	<a href="#">I2C_DATA4</a>	R/W	0h	I2C data register 4
C09h	<a href="#">I2C_DATA5</a>	R/W	0h	I2C data register 5
C0Ah	<a href="#">I2C_DATA6</a>	R/W	0h	I2C data register 6
C0Bh	<a href="#">I2C_DATA7</a>	R/W	0h	I2C data register 7
C0Ch	<a href="#">I2C_DATA8</a>	R/W	0h	I2C data register 8
C0Dh	<a href="#">I2C_DATA9</a>	R/W	0h	I2C data register 9
C0Eh	<a href="#">I2C_DATA10</a>	R/W	0h	I2C data register 10
C0Fh	<a href="#">I2C_DATA11</a>	R/W	0h	I2C data register 11
C10h	<a href="#">I2C_DATA12</a>	R/W	0h	I2C data register 12
C11h	<a href="#">I2C_DATA13</a>	R/W	0h	I2C data register 13
C12h	<a href="#">I2C_DATA14</a>	R/W	0h	I2C data register 14
C13h	<a href="#">I2C_DATA15</a>	R/W	0h	I2C data register 15
C14h	<a href="#">I2C_DATA16</a>	R/W	0h	I2C data register 16
C15h	<a href="#">I2C_DATA17</a>	R/W	0h	I2C data register 17

Table 46. Register overview: Balancing\_Registers

Address	Name	Access	Reset	Description
1000h	<a href="#">BAL_GLOB_CFG</a>	R/W	0h	The global balancing configuration register is used to configure the balancing modes.
1001h	<a href="#">BAL_GLOB_TO_TMR</a>	R/W	0h	The Global Balancing timeout timer register is used to configure the maximum balancing time for all balancing activities to make sure that in case of fault the balancing switches are switched OFF.
1002h	<a href="#">BAL_CH_CFG0</a>	R/W	0h	balancing channel individual enable channel 0 - 15
1003h	<a href="#">BAL_CH_CFG1</a>	R/W	0h	balancing channel individual enable channel 16 - 17
1004h	<a href="#">BAL_PRE_TMR</a>	R/W	0h	prebalancing timer
1005h	<a href="#">BAL_AUTO_DISCHRG_CTRL</a>	R/W	2152h	emergency discharge enable
1006h	<a href="#">BAL_SWITCH_MON_CFG0</a>	R/W	FFFFh	balancing switch monitoring enable
1007h	<a href="#">BAL_SWITCH_MON_CFG1</a>	R/W	3h	balancing switch monitoring enable
1008h	<a href="#">FULL_PWM_CYCLE_VOLTAGE</a>	R/W	0h	full PWM cycle voltage
1009h	<a href="#">BAL_CH_UV0_STAT0</a>	R	0h	channel undervoltage balancing status channel 0 - 15
100Ah	<a href="#">BAL_CH_UV0_STAT1</a>	R	0h	channel undervoltage balancing status channel 16 - 17
100Bh	<a href="#">BAL_GLOB_UV1_STAT0</a>	R	0h	global undervoltage balancing status channel 0 - 15

Table 46. Register overview: Balancing\_Registers...continued

Address	Name	Access	Reset	Description
100Ch	<a href="#">BAL_GLOB_UV1_STAT1</a>	R	0h	global undervoltage balancing status channel 16 - 17
100Dh	<a href="#">BAL_STAT0</a>	R	0h	logical balancing channel status channel 0 - 15
100Eh	<a href="#">BAL_STAT1</a>	R	0h	logical balancing channel status channel 16 - 17
100Fh	<a href="#">BAL_STAT2</a>	R	0h	balancing status
1010h	<a href="#">BAL_SWITCH_STAT0</a>	R	0h	physical balancing channel status channel 0 - 15
1011h	<a href="#">BAL_SWITCH_STAT1</a>	R	0h	physical balancing channel status channel 16 - 17
1012h	<a href="#">BAL_SWITCH_FLT_STAT0</a>	R	0h	balancing switch fault channel 0 - 15
1013h	<a href="#">BAL_SWITCH_FLT_STAT1</a>	R	0h	balancing switch fault channel 16 - 17
101Fh	<a href="#">BAL_TMR_CH_ALL</a>	W	0h	virtual register, writes in parallel into BAL_TMR_CH0 up to BAL_TMR_CH17
1020h	<a href="#">BAL_TMR_CH0</a>	R/W	0h	balancing timer channel 0
1021h	<a href="#">BAL_TMR_CH1</a>	R/W	0h	balancing timer channel 1
1022h	<a href="#">BAL_TMR_CH2</a>	R/W	0h	balancing timer channel 2
1023h	<a href="#">BAL_TMR_CH3</a>	R/W	0h	balancing timer channel 3
1024h	<a href="#">BAL_TMR_CH4</a>	R/W	0h	balancing timer channel 4
1025h	<a href="#">BAL_TMR_CH5</a>	R/W	0h	balancing timer channel 5
1026h	<a href="#">BAL_TMR_CH6</a>	R/W	0h	balancing timer channel 6
1027h	<a href="#">BAL_TMR_CH7</a>	R/W	0h	balancing timer channel 7
1028h	<a href="#">BAL_TMR_CH8</a>	R/W	0h	balancing timer channel 8
1029h	<a href="#">BAL_TMR_CH9</a>	R/W	0h	balancing timer channel 9
102Ah	<a href="#">BAL_TMR_CH10</a>	R/W	0h	balancing timer channel 10
102Bh	<a href="#">BAL_TMR_CH11</a>	R/W	0h	balancing timer channel 11
102Ch	<a href="#">BAL_TMR_CH12</a>	R/W	0h	balancing timer channel 12
102Dh	<a href="#">BAL_TMR_CH13</a>	R/W	0h	balancing timer channel 13
102Eh	<a href="#">BAL_TMR_CH14</a>	R/W	0h	balancing timer channel 14
102Fh	<a href="#">BAL_TMR_CH15</a>	R/W	0h	balancing timer channel 15
1030h	<a href="#">BAL_TMR_CH16</a>	R/W	0h	balancing timer channel 16
1031h	<a href="#">BAL_TMR_CH17</a>	R/W	0h	balancing timer channel 17
1032h	<a href="#">BAL_PWM_CH_ALL</a>	W	FFh	virtual register, writes in parallel into BAL_PWM_CH0 up to BAL_PWM_CH17
1033h	<a href="#">BAL_PWM_CH0</a>	R/W	FFh	balancing PWM channel 0
1034h	<a href="#">BAL_PWM_CH1</a>	R/W	FFh	balancing PWM channel 1
1035h	<a href="#">BAL_PWM_CH2</a>	R/W	FFh	balancing PWM channel 2
1036h	<a href="#">BAL_PWM_CH3</a>	R/W	FFh	balancing PWM channel 3
1037h	<a href="#">BAL_PWM_CH4</a>	R/W	FFh	balancing PWM channel 4
1038h	<a href="#">BAL_PWM_CH5</a>	R/W	FFh	balancing PWM channel 5
1039h	<a href="#">BAL_PWM_CH6</a>	R/W	FFh	balancing PWM channel 6
103Ah	<a href="#">BAL_PWM_CH7</a>	R/W	FFh	balancing PWM channel 7
103Bh	<a href="#">BAL_PWM_CH8</a>	R/W	FFh	balancing PWM channel 8
103Ch	<a href="#">BAL_PWM_CH9</a>	R/W	FFh	balancing PWM channel 9
103Dh	<a href="#">BAL_PWM_CH10</a>	R/W	FFh	balancing PWM channel 10

Table 46. Register overview: Balancing\_Registers...continued

Address	Name	Access	Reset	Description
103Eh	<a href="#">BAL_PWM_CH11</a>	R/W	FFh	balancing PWM channel 11
103Fh	<a href="#">BAL_PWM_CH12</a>	R/W	FFh	balancing PWM channel 12
1040h	<a href="#">BAL_PWM_CH13</a>	R/W	FFh	balancing PWM channel 13
1041h	<a href="#">BAL_PWM_CH14</a>	R/W	FFh	balancing PWM channel 14
1042h	<a href="#">BAL_PWM_CH15</a>	R/W	FFh	balancing PWM channel 15
1043h	<a href="#">BAL_PWM_CH16</a>	R/W	FFh	balancing PWM channel 16
1044h	<a href="#">BAL_PWM_CH17</a>	R/W	FFh	balancing PWM channel 17

Table 47. Register overview: All\_Measurement\_Registers

Address	Name	Access	Reset	Description
1400h	<a href="#">ALLM_CFG</a>	W	0h	general measurement control
1401h	<a href="#">ALLM_APP_CTRL</a>	W	7C00h	application measurement control
1402h	<a href="#">ALLM_PER_CTRL</a>	W	10h	periodic measurement control
1403h	<a href="#">ALLM_SYNC_CTRL</a>	W	7C00h	synchronous measurement control
1408h	<a href="#">ALLM_VCVB_CFG0</a>	W	0h	cell voltage measurement enable
1409h	<a href="#">ALLM_VCVB_CFG1</a>	W	0h	cell voltage measurement enable

Table 48. Register overview: Primary\_Measurement\_Registers

Address	Name	Access	Reset	Description
1800h	<a href="#">PRMM_CFG</a>	R/W	0h	general measurement control
1801h	<a href="#">PRMM_APP_CTRL</a>	R/W	7C00h	application measurement control
1802h	<a href="#">PRMM_PER_CTRL</a>	R/W	10h	periodic measurement control
1803h	<a href="#">PRMM_SYNC_CTRL</a>	W	0h	synchronous measurement control
1808h	<a href="#">PRMM_VC_CFG0</a>	R/W	0h	cell voltage measurement enable
1809h	<a href="#">PRMM_VC_CFG1</a>	R/W	0h	cell voltage measurement enable
180Ah	<a href="#">PRMM_AIN_CFG</a>	R/W	20h	AINx measurement enables
180Bh	<a href="#">PRMM_AIN_OL_CFG</a>	R/W	0h	AINx open-load detection enable
180Ch	<a href="#">PRMM_VBUF_CFG</a>	R/W	3h	voltage buffer enable
1810h	<a href="#">PRMM_VC_OV_UV_CFG0</a>	R/W	0h	cell voltage overvoltage and undervoltage check enable
1811h	<a href="#">PRMM_VC_OV_UV_CFG1</a>	R/W	0h	cell voltage overvoltage and undervoltage check enable
1812h	<a href="#">PRMM_VC_OV_TH_CFG</a>	R/W	7FFFh	upper comparator limit for VC0 to VC17
1813h	<a href="#">PRMM_VC_UV0_TH_CFG</a>	R/W	0h	lower comparator limit 0 for VC0 to VC17
1814h	<a href="#">PRMM_VC_UV1_TH_CFG</a>	R/W	0h	lower comparator limit 1 for VC0 to VC17
1815h	<a href="#">PRMM_AIN0_OV_TH_CFG</a>	R/W	7FFFh	upper comparator limit for AIN0
1816h	<a href="#">PRMM_AIN1_OV_TH_CFG</a>	R/W	7FFFh	upper comparator limit for AIN1
1817h	<a href="#">PRMM_AIN2_OV_TH_CFG</a>	R/W	7FFFh	upper comparator limit for AIN2
1818h	<a href="#">PRMM_AIN3_OV_TH_CFG</a>	R/W	7FFFh	upper comparator limit for AIN3
1819h	<a href="#">PRMM_AINA_OV_TH_CFG</a>	R/W	7FFFh	upper comparator limit for AINA
181Ah	<a href="#">PRMM_AIN0_UV_TH_CFG</a>	R/W	8001h	lower comparator limit for AIN0

Table 48. Register overview: Primary\_Measurement\_Registers...continued

Address	Name	Access	Reset	Description
181Bh	<a href="#">PRMM_AIN1_UV_TH_CFG</a>	R/W	8001h	lower comparator limit for AIN1
181Ch	<a href="#">PRMM_AIN2_UV_TH_CFG</a>	R/W	8001h	lower comparator limit for AIN2
181Dh	<a href="#">PRMM_AIN3_UV_TH_CFG</a>	R/W	8001h	lower comparator limit for AIN3
181Eh	<a href="#">PRMM_AINA_UV_TH_CFG</a>	R/W	8001h	lower comparator limit for AINA
1820h	<a href="#">PRMM_CAL_CRC</a>	R/W	0h	CRC over calibration data
1821h	<a href="#">PRMM_CFG_CRC</a>	R	0h	CRC over configuration values
1822h	<a href="#">PRMM_VC_OV_FLT_STAT0</a>	R	0h	cell voltage overvoltage status
1823h	<a href="#">PRMM_VC_OV_FLT_STAT1</a>	R	0h	cell voltage overvoltage status
1824h	<a href="#">PRMM_VC_UV0_FLT_STAT0</a>	R	0h	cell voltage undervoltage status regarding limit 0
1825h	<a href="#">PRMM_VC_UV0_FLT_STAT1</a>	R	0h	cell voltage undervoltage status regarding limit 0
1826h	<a href="#">PRMM_VC_UV1_FLT_STAT0</a>	R	0h	cell voltage undervoltage status regarding limit 1
1827h	<a href="#">PRMM_VC_UV1_FLT_STAT1</a>	R	0h	cell voltage under-voltage status regarding limit 1
1828h	<a href="#">PRMM_AIN_OV_FLT_STAT</a>	R	0h	AINx overvoltage status
1829h	<a href="#">PRMM_AIN_UV_FLT_STAT</a>	R	0h	AINx undervoltage status
183Eh	<a href="#">PRMM_MEAS_STAT</a>	R	0h	measurement status
183Fh	<a href="#">PRMM_APP_VC_CNT</a>	R	0h	application measurement VC sample count number
1840h	<a href="#">PRMM_APP_VC0</a>	R	8000h	application measurement result cell 0
1841h	<a href="#">PRMM_APP_VC1</a>	R	8000h	application measurement result cell 1
1842h	<a href="#">PRMM_APP_VC2</a>	R	8000h	application measurement result cell 2
1843h	<a href="#">PRMM_APP_VC3</a>	R	8000h	application measurement result cell 3
1844h	<a href="#">PRMM_APP_VC4</a>	R	8000h	application measurement result cell 4
1845h	<a href="#">PRMM_APP_VC5</a>	R	8000h	application measurement result cell 5
1846h	<a href="#">PRMM_APP_VC6</a>	R	8000h	application measurement result cell 6
1847h	<a href="#">PRMM_APP_VC7</a>	R	8000h	application measurement result cell 7
1848h	<a href="#">PRMM_APP_VC8</a>	R	8000h	application measurement result cell 8
1849h	<a href="#">PRMM_APP_VC9</a>	R	8000h	application measurement result cell 9
184Ah	<a href="#">PRMM_APP_VC10</a>	R	8000h	application measurement result cell 10
184Bh	<a href="#">PRMM_APP_VC11</a>	R	8000h	application measurement result cell 11
184Ch	<a href="#">PRMM_APP_VC12</a>	R	8000h	application measurement result cell 12
184Dh	<a href="#">PRMM_APP_VC13</a>	R	8000h	application measurement result cell 13
184Eh	<a href="#">PRMM_APP_VC14</a>	R	8000h	application measurement result cell 14
184Fh	<a href="#">PRMM_APP_VC15</a>	R	8000h	application measurement result cell 15
1850h	<a href="#">PRMM_APP_VC16</a>	R	8000h	application measurement result cell 16
1851h	<a href="#">PRMM_APP_VC17</a>	R	8000h	application measurement result cell 17
1852h	<a href="#">PRMM_APP_AINA</a>	R	8000h	application measurement result AINA
1853h	<a href="#">PRMM_APP_AIN0</a>	R	8000h	application measurement result AIN0
1854h	<a href="#">PRMM_APP_AIN1</a>	R	8000h	application measurement result AIN1
1855h	<a href="#">PRMM_APP_AIN2</a>	R	8000h	application measurement result AIN2
1856h	<a href="#">PRMM_APP_AIN3</a>	R	8000h	application measurement result AIN3
185Fh	<a href="#">PRMM_PER_NUM</a>	R	0h	measurement period number of the primary periodic results

Table 48. Register overview: Primary\_Measurement\_Registers...continued

Address	Name	Access	Reset	Description
1860h	<a href="#">PRMM_PER_VC0</a>	R	8000h	periodic measurement result cell 0
1861h	<a href="#">PRMM_PER_VC1</a>	R	8000h	periodic measurement result cell 1
1862h	<a href="#">PRMM_PER_VC2</a>	R	8000h	periodic measurement result cell 2
1863h	<a href="#">PRMM_PER_VC3</a>	R	8000h	periodic measurement result cell 3
1864h	<a href="#">PRMM_PER_VC4</a>	R	8000h	periodic measurement result cell 4
1865h	<a href="#">PRMM_PER_VC5</a>	R	8000h	periodic measurement result cell 5
1866h	<a href="#">PRMM_PER_VC6</a>	R	8000h	periodic measurement result cell 6
1867h	<a href="#">PRMM_PER_VC7</a>	R	8000h	periodic measurement result cell 7
1868h	<a href="#">PRMM_PER_VC8</a>	R	8000h	periodic measurement result cell 8
1869h	<a href="#">PRMM_PER_VC9</a>	R	8000h	periodic measurement result cell 9
186Ah	<a href="#">PRMM_PER_VC10</a>	R	8000h	periodic measurement result cell 10
186Bh	<a href="#">PRMM_PER_VC11</a>	R	8000h	periodic measurement result cell 11
186Ch	<a href="#">PRMM_PER_VC12</a>	R	8000h	periodic measurement result cell 12
186Dh	<a href="#">PRMM_PER_VC13</a>	R	8000h	periodic measurement result cell 13
186Eh	<a href="#">PRMM_PER_VC14</a>	R	8000h	periodic measurement result cell 14
186Fh	<a href="#">PRMM_PER_VC15</a>	R	8000h	periodic measurement result cell 15
1870h	<a href="#">PRMM_PER_VC16</a>	R	8000h	periodic measurement result cell 16
1871h	<a href="#">PRMM_PER_VC17</a>	R	8000h	periodic measurement result cell 17
1872h	<a href="#">PRMM_PER_AINA</a>	R	8000h	periodic measurement result AINA
1873h	<a href="#">PRMM_PER_AIN0</a>	R	8000h	periodic measurement result AIN0
1874h	<a href="#">PRMM_PER_AIN1</a>	R	8000h	periodic measurement result AIN1
1875h	<a href="#">PRMM_PER_AIN2</a>	R	8000h	periodic measurement result AIN2
1876h	<a href="#">PRMM_PER_AIN3</a>	R	8000h	periodic measurement result AIN3
1877h	<a href="#">PRMM_PER_PRMTEMP</a>	R	8000h	periodic measurement result primary device temperature
1878h	<a href="#">PRMM_PER_SECVREF</a>	R	8000h	periodic measurement result secondary voltage reference
1879h	<a href="#">PRMM_PER_VAUX</a>	R	8000h	periodic measurement result auxiliary supply voltage
187Ah	<a href="#">PRMM_PER_VDDC</a>	R	8000h	periodic measurement result VDDC
187Fh	<a href="#">PRMM_SYNC_NUM</a>	R	0h	measurement period number of the synchronous results.
1880h	<a href="#">PRMM_SYNC_VC0</a>	R	8000h	synchronous measurement result cell 0
1881h	<a href="#">PRMM_SYNC_VC1</a>	R	8000h	synchronous measurement result cell 1
1882h	<a href="#">PRMM_SYNC_VC2</a>	R	8000h	synchronous measurement result cell 2
1883h	<a href="#">PRMM_SYNC_VC3</a>	R	8000h	synchronous measurement result cell 3
1884h	<a href="#">PRMM_SYNC_VC4</a>	R	8000h	synchronous measurement result cell 4
1885h	<a href="#">PRMM_SYNC_VC5</a>	R	8000h	synchronous measurement result cell 5
1886h	<a href="#">PRMM_SYNC_VC6</a>	R	8000h	synchronous measurement result cell 6
1887h	<a href="#">PRMM_SYNC_VC7</a>	R	8000h	synchronous measurement result cell 7
1888h	<a href="#">PRMM_SYNC_VC8</a>	R	8000h	synchronous measurement result cell 8
1889h	<a href="#">PRMM_SYNC_VC9</a>	R	8000h	synchronous measurement result cell 9
188Ah	<a href="#">PRMM_SYNC_VC10</a>	R	8000h	synchronous measurement result cell 10
188Bh	<a href="#">PRMM_SYNC_VC11</a>	R	8000h	synchronous measurement result cell 11

Table 48. Register overview: Primary\_Measurement\_Registers...continued

Address	Name	Access	Reset	Description
188Ch	<a href="#">PRMM_SYNC_VC12</a>	R	8000h	synchronous measurement result cell 12
188Dh	<a href="#">PRMM_SYNC_VC13</a>	R	8000h	synchronous measurement result cell 13
188Eh	<a href="#">PRMM_SYNC_VC14</a>	R	8000h	synchronous measurement result cell 14
188Fh	<a href="#">PRMM_SYNC_VC15</a>	R	8000h	synchronous measurement result cell 15
1890h	<a href="#">PRMM_SYNC_VC16</a>	R	8000h	synchronous measurement result cell 16
1891h	<a href="#">PRMM_SYNC_VC17</a>	R	8000h	synchronous measurement result cell 17

Table 49. Register overview: Secondary\_Measurement\_Registers

Address	Name	Access	Reset	Description
1C00h	<a href="#">SECM_CFG</a>	R/W	0h	general measurement control
1C01h	<a href="#">SECM_APP_CTRL</a>	W	0h	application measurement control
1C02h	<a href="#">SECM_PER_CTRL</a>	R/W	10h	periodic measurement control
1C03h	<a href="#">SECM_SYNC_CTRL</a>	R/W	7C00h	synchronous measurement control
1C08h	<a href="#">SECM_VB_CFG0</a>	R/W	0h	balance voltage measurement enable
1C09h	<a href="#">SECM_VB_CFG1</a>	R/W	0h	balance voltage measurement enable
1C0Ah	<a href="#">SECM_AIN_CFG</a>	R/W	80h	measurement enables for extra channel
1C0Bh	<a href="#">SECM_AIN_OL_CFG</a>	R/W	0h	AINx open-load detection enable
1C0Ch	<a href="#">SECM_VBUF_CFG</a>	R/W	3h	voltage buffer enable
1C20h	<a href="#">SECM_CAL_CRC</a>	R/W	0h	CRC over calibration data
1C21h	<a href="#">SECM_CFG_CRC</a>	R	0h	CRC over configuration values
1C3Eh	<a href="#">SECM_MEAS_STAT</a>	R	0h	measurement status
1C53h	<a href="#">SECM_APP_AIN4</a>	R	8000h	application measurement result AIN4
1C54h	<a href="#">SECM_APP_AIN5</a>	R	8000h	application measurement result AIN5
1C55h	<a href="#">SECM_APP_AIN6</a>	R	8000h	application measurement result AIN6
1C56h	<a href="#">SECM_APP_AIN7</a>	R	8000h	application measurement result AIN7
1C5Fh	<a href="#">SECM_PER_NUM</a>	R	0h	measurement period number of the secondary periodic results
1C73h	<a href="#">SECM_PER_AIN4</a>	R	8000h	periodic measurement result AIN4
1C74h	<a href="#">SECM_PER_AIN5</a>	R	8000h	periodic measurement result AIN5
1C75h	<a href="#">SECM_PER_AIN6</a>	R	8000h	periodic measurement result AIN6
1C76h	<a href="#">SECM_PER_AIN7</a>	R	8000h	periodic measurement result AIN7
1C77h	<a href="#">SECM_PER_SECTEMP</a>	R	8000h	periodic measurement result secondary device temperature
1C78h	<a href="#">SECM_PER_PRMVREF</a>	R	8000h	periodic measurement result primary voltage reference
1C79h	<a href="#">SECM_PER_VAUX</a>	R	8000h	periodic measurement result auxiliary supply voltage
1C7Ah	<a href="#">SECM_PER_VBAT</a>	R	8000h	periodic measurement result VBAT
1C7Bh	<a href="#">SECM_PER_VDDA</a>	R	8000h	periodic measurement result VDDA
1C7Ch	<a href="#">SECM_PER_VDDC</a>	R	8000h	periodic measurement result VDDC
1C7Eh	<a href="#">SECM_PER_NPNISENSE</a>	R	8000h	periodic measurement result NPN current sensor
1C7Fh	<a href="#">SECM_SYNC_NUM</a>	R	0h	measurement number of the secondary synchronous results
1C80h	<a href="#">SECM_SYNC_VB0</a>	R	8000h	synchronous measurement result from balancing pins cell 0.



Table 49. Register overview: Secondary\_Measurement\_Registers...continued

Address	Name	Access	Reset	Description
1C81h	<a href="#">SECM_SYNC_VB1</a>	R	8000h	synchronous measurement result from balancing pins cell 1
1C82h	<a href="#">SECM_SYNC_VB2</a>	R	8000h	synchronous measurement result from balancing pins cell 2
1C83h	<a href="#">SECM_SYNC_VB3</a>	R	8000h	synchronous measurement result from balancing pins cell 3
1C84h	<a href="#">SECM_SYNC_VB4</a>	R	8000h	synchronous measurement result from balancing pins cell 4
1C85h	<a href="#">SECM_SYNC_VB5</a>	R	8000h	synchronous measurement result from balancing pins cell 5
1C86h	<a href="#">SECM_SYNC_VB6</a>	R	8000h	synchronous measurement result from balancing pins cell 6
1C87h	<a href="#">SECM_SYNC_VB7</a>	R	8000h	synchronous measurement result from balancing pins cell 7
1C88h	<a href="#">SECM_SYNC_VB8</a>	R	8000h	synchronous measurement result from balancing pins cell 8
1C89h	<a href="#">SECM_SYNC_VB9</a>	R	8000h	synchronous measurement result from balancing pins cell 9
1C8Ah	<a href="#">SECM_SYNC_VB10</a>	R	8000h	synchronous measurement result from balancing pins cell 10
1C8Bh	<a href="#">SECM_SYNC_VB11</a>	R	8000h	synchronous measurement result from balancing pins cell 11
1C8Ch	<a href="#">SECM_SYNC_VB12</a>	R	8000h	synchronous measurement result from balancing pins cell 12
1C8Dh	<a href="#">SECM_SYNC_VB13</a>	R	8000h	synchronous measurement result from balancing pins cell 13
1C8Eh	<a href="#">SECM_SYNC_VB14</a>	R	8000h	synchronous measurement result from balancing pins cell 14
1C8Fh	<a href="#">SECM_SYNC_VB15</a>	R	8000h	synchronous measurement result from balancing pins cell 15
1C90h	<a href="#">SECM_SYNC_VB16</a>	R	8000h	synchronous measurement result from balancing pins cell 16
1C91h	<a href="#">SECM_SYNC_VB17</a>	R	8000h	synchronous measurement result from balancing pins cell 17

12.1.1 SYS\_CFG\_CRC register

System configuration CRC

Table 50. SYS\_CFG\_CRC register - system configuration CRC (address 0h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	CRC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 51. SYS\_CFG\_CRC register - system configuration CRC (address 0h)

Bit	Symbol	Access	Value	Description
15:0	CRC	R	0h	<p>This CRC value is recalculated with any write to a covered register and with any read to this register. The updated CRC value is available latest 100 µs after the last write. The CRC value is application specific and must be re-calculated by the MCU. The used polynomial is: <math>D175h (+1) = X^{16} + X^{15} + X^{13} + X^9 + X^7 + X^6 + X^5 + X^3 + X^1 + 1</math>.</p> <p>Following registers are included: SYS_COM_CFG, SYS_COM_TO_CFG, SYS_SUPPLY_CFG, SYS_CYC_WAKEUP_CFG, SYS_TPL_CFG.</p>



### 12.1.2 SYS\_COM\_CFG register

Communication initialization

**Table 52. SYS\_COM\_CFG register - communication initialization (address 1h) bit allocation**

Bit	15	14	13	12	11	10	9	8
Symbol	NUMNODES						BUSFW	CADD
Reset	0	0	0	0	0	0	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	7	6	5	4	3	2	1	0
Symbol	CADD		DADD					
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**Table 53. SYS\_COM\_CFG register - communication initialization (address 1h)**

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:10	NUMNODES	R/W	0h	Number of nodes in the daisy chain. Difference of NUMNODES and DADD defines the wait time for global write commands.
9	BUSFW	R/W		Bus forwarding
			0	DISABLED (read-write) Disabled
			1*	ENABLED (read-write) Enabled if DADD is unequal 00h
8:6	CADD	R/W		Defines the daisy chain address CADD = chain address CADD is only used for responses to a all chain read request.
			000*	RESERVED (read-write) Reserved for future usage
			111	GLOBAL (read-write) Reserved for global write commands
5:0	DADD	R/W		Defines the device address DADD = device address
			00h*	UNENUMERATED (read-write) Device is unenumerated; bus forwarding is disabled.
			3Fh	GLOBAL (read-write) Used for global read and write commands

### 12.1.3 SYS\_COM\_TO\_CFG register

System communication timeout

**Table 54. SYS\_COM\_TO\_CFG register - system communication timeout (address 2h) bit allocation**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	COMTODISABLE								COMTO							
Reset	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 55. SYS\_COM\_TO\_CFG register - system communication timeout (address 2h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:8	COMTODISABLE	R/W		Communication timeout disable. Only intended for software development activities. Must never be used in release software.
			00h*	DEFAULT (read-write) Communication timeout enabled
			5Ah	DISABLED (read-write) Communication timeout disabled
7:0	COMTO	R/W		Communication timeout time <b>COMTO</b> * 10 milliseconds A value of 0 is treated as 10 ms.
			00h	T_MIN (read-write) 10 ms
			01h	T_10m (read-write) 10 ms
			1Eh*	T_300m (read-write) 300 ms
			FFh	T_MAX (read-write) 2550 ms

### 12.1.4 SYS\_SUPPLY\_CFG register

Supply configuration

Table 56. SYS\_SUPPLY\_CFG register - supply configuration (address 3h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	CURMATCH	reserved						
Reset	1	0	0	0	0	0	0	0
Access	R/W	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	reserved					VDDCCYC	VAUXCYC	VAUXACT
Reset	0	0	0	0	0	0	1	1
Access	R	R	R	R	R	R/W	R/W	R/W

Table 57. SYS\_SUPPLY\_CFG register - supply configuration (address 3h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15	CURMATCH	R/W		Enable IC supply current matching in active mode.
			0	DISABLED (read-write) Supply current matching is disabled
			1*	ENABLED (read-write) Supply current matching is enabled
14:3	reserved	R	0h	This read-only field is reserved and always has the value 0.
2	VDDCCYC	R/W		Enable VDDC in cyclic mode.
			0*	DISABLED (read-write) VDDC is disabled in cyclic mode
			1	ENABLED (read-write) VDDC is enabled in cyclic mode
1	VAUXCYC	R/W		Enable VAUX in cyclic mode.
			0	DISABLED (read-write) VAUX is disabled in cyclic mode
			1*	ENABLED (read-write) VAUX is enabled in cyclic mode
0	VAUXACT	R/W		Enable VAUX in active mode.
			0	DISABLED (read-write) VAUX is disabled in active mode

Table 57. SYS\_SUPPLY\_CFG register - supply configuration (address 3h)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
			1*	ENABLED (read-write) VAUX is enabled in active mode

12.1.5 SYS\_MODE register

System mode

Table 58. SYS\_MODE register - system mode (address 4h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved			PREVMODE					reserved			TARGETMODE				
Reset	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	W	W	W	W	W

Table 59. SYS\_MODE register - system mode (address 4h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:13	reserved	R	0h	This read-only field is reserved and always has the value 0.
12:8	PREVMODE	R		Previous mode. <b>Other</b> values as stated are invalid.
			0Ah	SLEEP (read) Sleep mode
			14h*	DEEPSLEEP (read) Deep sleep mode
			1Fh	CYCLIC (read) Cyclic mode
7:5	reserved	R	0h	This read-only field is reserved and always has the value 0.
4:0	TARGETMODE	W	0h	Target mode. The mode transition starts immediately after writing. <b>Other</b> values as stated are ignored.
			0Ah	SLEEP (write) Sleep mode
			14h	DEEPSLEEP (write) Deep sleep mode

12.1.6 SYS\_CYC\_WAKEUP\_CFG register

Interval for cyclic measurements

Table 60. SYS\_CYC\_WAKEUP\_CFG register - interval for cyclic measurements (address 5h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	PERIOD															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 61. SYS\_CYC\_WAKEUP\_CFG register - interval for cyclic measurements (address 5h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:0	PERIOD	R/W		Time between two cyclic wake-up events. <b>PERIOD</b> * 100 milliseconds
			0000h*	DISABLED (read-write) Cyclic wakeup disabled
			0001h	PERIOD (read-write) PERIOD * 100 ms
			FFFFh	PERIOD_MAX (read-write) Maximum period time = 6553500 ms = approximately 1.8 h

### 12.1.7 SYS\_TPL\_CFG register

TPL configuration

Table 62. SYS\_TPL\_CFG register - TPL configuration. (address 6h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	reserved		RESPCFG		TXTERMH	TXTERML	WAKEUPCOMP	
Reset	0	0	0	1	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Table 63. SYS\_TPL\_CFG register - TPL configuration. (address 6h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:6	reserved	R	0h	This read-only field is reserved and always has the value 0.
5:4	RESPCFG	R/W		Response interface
			00	SAME (read-write) Responses are only transmitted on the receiving port.
			01*	BOTH (read-write) Responses are transmitted on both ports if DADD is unequal 00h.
			10	OPPOSITE (read-write) Responses are transmitted on the opposite port of the receiving port.
			11	RESERVED (read-write) Reserved, do not use. For now same as BOTH.
3	TXTERMH	R/W		Termination active while transmit for the higher TPL port. (Pin 49 and pin 50)
			0*	DISABLED (read-write) Disabled; termination is inactive during transmit. Required for normal TPL operation.
			1	ENABLED (read-write) Enabled; termination is active during transmit. Only needed at final daisy-chain node to have equal power consumption.
2	TXTERML	R/W		Termination active while transmit for the lower TPL port. (Pin 47 and pin 48)

Table 63. SYS\_TPL\_CFG register - TPL configuration. (address 6h)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
			0*	DISABLED (read-write) Disabled; termination is inactive during transmit. Required for normal TPL operation.
			1	ENABLED (read-write) Enabled; termination is active during transmit. Only needed at final daisy-chain node to have equal power consumption.
1:0	WAKEUPCOMP	R/W		Defines compatibility for the MC33664 wake-up by the Daisy Chain. Undefined values are treated as HIGHER.
			00*	DEFAULT (read-write) Wake-up signal on both ports is compatible to BMI7018.
			01	LOWER (read-write) Wake-up signal on lower TPL port is compatible to MC33664. The other port is compatible to BMI7018.
			10	HIGHER (read-write) Wake-up signal on higher TPL port is compatible to MC33664. The other port is compatible to BMI7018.

### 12.1.8 SYS\_CLK\_SYNC\_CTRL register

Clock synchronization

Table 64. SYS\_CLK\_SYNC\_CTRL register - clock Synchronization (address 8h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	SYNCCNT															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 65. SYS\_CLK\_SYNC\_CTRL register - clock Synchronization (address 8h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:0	SYNCCNT	R/W		Synchronization counter value: Writing a 0000h resets the counter with no adjustment. For other values it is checked if the internal counter value is higher, in which case the oscillator frequency is decreased. If it is lower the internal oscillator frequency is increased. Reading the value returns the current internal counter value. 1 LSB = 10 $\mu$ s.
			0000h*	RESET (read-write) Counter is reset with no adjustment.
			0001h	ADJUST (read-write) 10 $\mu$ s

### 12.1.9 SYS\_VERSION register

Device silicon identifier

Table 66. SYS\_VERSION register - device silicon identifier (address 10h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	TYPE								FREV				MREV			
Reset	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	1
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 67. SYS\_VERSION register - device silicon identifier (address 10h)

Bit	Symbol	Access	Value	Description
15:8	TYPE	R	3h	Type identifier. Development samples might show a different value.
7:4	FREV	R	9h	Full mask revision ID
3:0	MREV	R	1h	Metal revision ID

### 12.1.10 SYS\_UID\_LOW register

Unique device ID lower part

Table 68. SYS\_UID\_LOW register - unique device ID lower part (address 11h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	LOW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 69. SYS\_UID\_LOW register - unique device ID lower part (address 11h)

Bit	Symbol	Access	Value	Description
15:0	LOW	R	0h	Lower part of unique device ID

### 12.1.11 SYS\_UID\_MID register

Unique device ID middle part

Table 70. SYS\_UID\_MID register - unique device ID middle part (address 12h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	MID															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 71. SYS\_UID\_MID register - unique device ID middle part (address 12h)

Bit	Symbol	Access	Value	Description
15:0	MID	R	0h	Middle part of unique device ID

### 12.1.12 SYS\_UID\_HIGH register

Unique device ID higher part

Table 72. SYS\_UID\_HIGH register - unique device ID higher part (address 13h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	HIGH															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 73. SYS\_UID\_HIGH register - unique device ID higher part (address 13h)

Bit	Symbol	Access	Value	Description
15:0	HIGH	R	0h	Higher part of unique device ID

### 12.1.13 SYS\_PROD\_VER register

Software interface related version of the product

Table 74. SYS\_PROD\_VER register - software interface related version of the product (address 14h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved				MAJOR				MINOR				PATCH			
Reset	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 75. SYS\_PROD\_VER register - software interface related version of the product (address 14h)

Bit	Symbol	Access	Value	Description
15:12	reserved	R	0h	This read-only field is reserved and always has the value 0.
11:8	MAJOR	R	2h	Major Revision: Software interface change, register-map or registers changed. Non-compatible with previous versions. (Auto SAR nomenclature)
7:4	MINOR	R	0h	Minor Revision: Software interface change, for example improvement or extension which is covered by additional registers or transparent to the software. Existing software is compatible but may not use new features. (AutoSAR nomenclature).
3:0	PATCH	R	0h	Patch: Patch with no software interface change. (AutoSAR nomenclature)

### 12.1.14 SYS\_DS\_STORAGE0 register

Deep sleep storage data 0; the value is stored in the ULP domain

Table 76. SYS\_DS\_STORAGE0 register - Deep Sleep Storage Data0. (address 80h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	DATA															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 77. SYS\_DS\_STORAGE0 register - Deep Sleep Storage Data0. (address 80h)

Bit	Symbol	Access	Value	Description
15:0	DATA	R/W	0h	Deep Sleep surviving data; this register has no reset. This register allows to store application data and has no influence on the device.

### 12.1.15 SYS\_DS\_STORAGE1 register

Deep sleep storage data 1; the value is stored in the ULP domain

Table 78. SYS\_DS\_STORAGE1 register - Deep Sleep Storage Data1. (address 81h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	DATA															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 79. SYS\_DS\_STORAGE1 register - Deep Sleep Storage Data1. (address 81h)

Bit	Symbol	Access	Value	Description
15:0	DATA	R/W	0h	Deep Sleep surviving data; this register has no reset. This register allows to store application data and has no influence on the device.

### 12.1.16 FEH\_CFG\_CRC register

#### Configuration CRC

Table 80. FEH\_CFG\_CRC register - configuration CRC (address 400h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	CRC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 81. FEH\_CFG\_CRC register - configuration CRC (address 400h)

Bit	Symbol	Access	Value	Description
15:0	CRC	R	0h	This CRC value is recalculated with any transition into Active mode, with any write to a covered register and with any read to this register. The updated CRC value is available latest 100 $\mu$ s after the last write. The CRC value is application specific and must be re-calculated by the MCU. The used polynomial is: $D175h (+1) = X^{16} + X^{15} + X^{13} + X^9 + X^7 + X^6 + X^5 + X^3 + X^1 + 1$ . Following registers are included: FEH_ALARM_CFG, FEH_ALARM_OUT_CFG0, FEH_ALARM_OUT_CFG1, FEH_WAKEUP_CFG0, FEH_WAKEUP_CFG1, FEH_SUPPLY_FLT_POR_CFG0, FEH_SUPPLY_FLT_POR_CFG1, FEH_COM_FLT_POR_CFG, FEH_SUPPLY_FLT_EVT_CFG0, FEH_SUPPLY_FLT_EVT_CFG1, FEH_ANA_FLT_EVT_CFG, FEH_COM_FLT_EVT_CFG, FEH_MEAS_FLT_EVT_CFG.

### 12.1.17 FEH\_ALARM\_CFG register

#### General alarm configuration

Table 82. FEH\_ALARM\_CFG register - general alarm configuration (address 401h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							ALARM1_NHBINV
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R/W
Bit	7	6	5	4	3	2	1	0



Table 82. FEH\_ALARM\_CFG register - general alarm configuration (address 401h) bit allocation...continued

Symbol	ALARMOUTHB		ALARMOUT		ALARMINHB		ALARMIN	
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 83. FEH\_ALARM\_CFG register - general alarm configuration (address 401h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:9	reserved	R	0h	This read-only field is reserved and always has the value 0.
8	ALARMINHBINV	R/W		Inverted heartbeat input
			0*	DISABLED (read-write) Normal heartbeat (LOW with HIGH pulses) input used
			1	ENABLED (read-write) Inverted heartbeat (HIGH with LOW pulses) input used
7:6	ALARMOUTHB	R/W		Output heartbeat low time setting
			00*	T_500u (read-write) 500 us
			01	T_1ms (read-write) 1 ms
			10	T_10ms (read-write) 10 ms
			11	T_100ms (read-write) 100 ms
5:4	ALARMOUT	R/W		Enable alarm output
			00*	DISABLED (read-write) disabled. Alarm output is high impedance.
			01	HIGH_ACTIVE (read-write) high active
			10	LOW_ACTIVE (read-write) low active
			11	HEARTBEAT (read-write) heartbeat configuration
3:2	ALARMINHB	R/W		Input heartbeat low time setting
			00*	T_500u (read-write) 500 us
			01	T_1ms (read-write) 1 ms
			10	T_10ms (read-write) 10 ms
			11	T_100ms (read-write) 100 ms
1:0	ALARMIN	R/W		Enable alarm input Enabling the alarm input automatically enables the digital receiver for the Alarm input pin.
			00*	DISABLED (read-write) Alarm input is disabled
			01	HIGH_ACTIVE (read-write) Alarm input is enabled, high active
			10	LOW_ACTIVE (read-write) Alarm input is enabled, low active
			11	HEARTBEAT (read-write) Alarm input is enabled, heartbeat configuration

## 12.1.18 FEH\_ALARM\_OUT\_CFG0 register

Alarm output source selection

Table 84. FEH\_ALARM\_OUT\_CFG0 register - alarm output source selection (address 402h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved	SYSFLTEVT	BALRDY	WAKEUPIN	ALARMIN	AIN3UV	AIN3OV	AIN2UV
Reset	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	7	6	5	4	3	2	1	0
Symbol	AIN2OV	AIN1UV	AIN1OV	AIN0UV	AIN0OV	VCUV1	VCUV0	VCOV
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 85. FEH\_ALARM\_OUT\_CFG0 register - alarm output source selection (address 402h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15	reserved	R	0h	This read-only field is reserved and always has the value 0.
14	SYSFLTEVT	R/W		Enable output on alarm output for a detected and selected system fault.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
13	BALRDY	R/W		Enable output on alarm output for cell voltage balancing ready.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
12	WAKEUPIN	R/W		Enable output on detected wakeup input. Enabling this bit automatically enables the digital receiver for the wakeup input pin.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
11	ALARMIN	R/W		Enable output on alarm output for detected alarm input.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
10	AIN3UV	R/W		Enable output on alarm output for AIN3_UV.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
9	AIN3OV	R/W		Enable output on alarm output for AIN3_OV.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
8	AIN2UV	R/W		Enable output on alarm output for AIN2_UV.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
7	AIN2OV	R/W		Enable output on alarm output for AIN2_OV.
			0*	DISABLED (read-write) disabled

Table 85. FEH\_ALARM\_OUT\_CFG0 register - alarm output source selection (address 402h)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
			1	ENABLED (read-write) enabled
6	AIN1UV	R/W		Enable output on alarm output for AIN1_UV.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
5	AIN1OV	R/W		Enable output on alarm output for AIN1_OV.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
4	AIN0UV	R/W		Enable output on alarm output for AIN0_UV.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
3	AIN0OV	R/W		Enable output on alarm output for AIN0_OV.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
2	VCUV1	R/W		Enable output on alarm output for VC_UV1.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
1	VCUV0	R/W		Enable output on alarm output for VC_UV0.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
0	VCOV	R/W		Enable output on alarm output for VC_OV.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled

12.1.19 FEH\_ALARM\_OUT\_CFG1 register

Alarm output source selection

Table 86. FEH\_ALARM\_OUT\_CFG1 register - alarm output source selection (address 403h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							BALPROT
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R/W
Bit	7	6	5	4	3	2	1	0
Symbol	reserved						AINAUV	AINAOV
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R/W	R/W

Table 87. FEH\_ALARM\_OUT\_CFG1 register - alarm output source selection (address 403h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:9	reserved	R	0h	This read-only field is reserved and always has the value 0.
8	BALPROT	R/W		Enable output on alarm output for detected balancing protection
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
7:2	reserved	R	0h	This read-only field is reserved and always has the value 0.
1	AINAUUV	R/W		Enable output on alarm output for AINA_UV.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
0	AINAOV	R/W		Enable output on alarm output for AINA_OV.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled

### 12.1.20 FEH\_ALARM\_OUT\_REASON0 register

Alarm output reason

Table 88. FEH\_ALARM\_OUT\_REASON0 register - alarm output reason (address 404h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved	SYSFLTEVT	BALRDY	WAKEUPIN	ALARMIN	AIN3UV	AIN3OV	AIN2UV
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	AIN2OV	AIN1UV	AIN1OV	AIN0UV	AIN0OV	VCUV1	VCUV0	VCOV
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 89. FEH\_ALARM\_OUT\_REASON0 register - alarm output reason (address 404h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15	reserved	R	0h	This read-only field is reserved and always has the value 0.
14	SYSFLTEVT	R		Detected system fault. Read clears bit.
			0*	NO_ALARM (read) Alarm not caused by detected system fault
			1	ALARM (read) Alarm caused by detected system fault
13	BALRDY	R		Cell voltage balancing ready Read clears bit.
			0*	NO_ALARM (read) Alarm not caused by cell voltage balancing ready
			1	ALARM (read) Alarm caused by cell voltage balancing ready
12	WAKEUPIN	R		Detected wakeup input Read clears bit.
			0*	NO_ALARM (read) Alarm not caused by detected wakeup input

Table 89. FEH\_ALARM\_OUT\_REASON0 register - alarm output reason (address 404h)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
			1	ALARM (read) Alarm caused by detected wakeup input
11	ALARMIN	R		Detected alarm input Read clears bit.
			0*	NO_ALARM (read) Alarm not caused by detected alarm input
			1	ALARM (read) Alarm caused by detected alarm input
10	AIN3UV	R		AIN3_UV Read clears bit.
			0*	NO_ALARM (read) Alarm not caused by AIN3_UV
			1	ALARM (read) Alarm caused by AIN3_UV
9	AIN3OV	R		AIN3_OV Read clears bit.
			0*	NO_ALARM (read) Alarm not caused by AIN3_OV
			1	ALARM (read) Alarm caused by AIN3_OV
8	AIN2UV	R		AIN2_UV Read clears bit.
			0*	NO_ALARM (read) Alarm not caused by AIN2_UV
			1	ALARM (read) Alarm caused by AIN2_UV
7	AIN2OV	R		AIN2_OV Read clears bit.
			0*	NO_ALARM (read) Alarm not caused by AIN2_OV
			1	ALARM (read) Alarm caused by AIN2_OV
6	AIN1UV	R		AIN1_UV Read clears bit.
			0*	NO_ALARM (read) Alarm not caused by AIN1_UV
			1	ALARM (read) Alarm caused by AIN1_UV
5	AIN1OV	R		AIN1_OV Read clears bit.
			0*	NO_ALARM (read) Alarm not caused by AIN1_OV
			1	ALARM (read) Alarm caused by AIN1_OV
4	AIN0UV	R		AIN0_UV Read clears bit.
			0*	NO_ALARM (read) Alarm not caused by AIN0_UV
			1	ALARM (read) Alarm caused by AIN0_UV
3	AIN0OV	R		AIN0_OV Read clears bit.
			0*	NO_ALARM (read) Alarm not caused by AIN0_OV
			1	ALARM (read) Alarm caused by AIN0_OV
2	VCUV1	R		VC_UV1 Read clears bit.
			0*	NO_ALARM (read) Alarm not caused by VC_UV1
			1	ALARM (read) Alarm caused by VC_UV1
1	VCUV0	R		VC_UV0 Read clears bit.
			0*	NO_ALARM (read) Alarm not caused by VC_UV0
			1	ALARM (read) Alarm caused by VC_UV0
0	VCOV	R		VC_OV Read clears bit.
			0*	NO_ALARM (read) Alarm not caused by VC_OV
			1	ALARM (read) Alarm caused by VC_OV

## 12.1.21 FEH\_ALARM\_OUT\_REASON1 register

Alarm output reason

Table 90. FEH\_ALARM\_OUT\_REASON1 register - alarm output reason (address 405h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							BALPROT
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	reserved						AINAUUV	AINAOV
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 91. FEH\_ALARM\_OUT\_REASON1 register - alarm output reason (address 405h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:9	reserved	R	0h	This read-only field is reserved and always has the value 0.
8	BALPROT	R		Balancing protection detection Read clears bit.
			0*	NO_WAKE (read) Alarm not caused by detected Balancing protection
			1	WAKE_UP (read) Alarm caused by detected Balancing protection
7:2	reserved	R	0h	This read-only field is reserved and always has the value 0.
1	AINAUUV	R		AINA_UV Read clears bit.
			0*	NO_WAKE (read) Alarm not caused by AINA_UV
			1	WAKE_UP (read) Alarm caused by AINA_UV
0	AINAOV	R		AINA_OV Read clears bit.
			0*	NO_WAKE (read) Alarm not caused by AINA_OV
			1	WAKE_UP (read) Alarm caused by AINA_OV

## 12.1.22 FEH\_WAKEUP\_CFG0 register

Wake-up source configuration

Table 92. FEH\_WAKEUP\_CFG0 register - wake-up source configuration (address 408h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	TPLWAKEUP	SYSFLTEVT	BALRDY	WAKEUPIN	ALARMIN	AIN3UV	AIN3OV	AIN2UV
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	7	6	5	4	3	2	1	0
Symbol	AIN2OV	AIN1UV	AIN1OV	AIN0UV	AIN0OV	VCUV1	VCUV0	VCOV
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 93. FEH\_WAKEUP\_CFG0 register - wake up source configuration (address 408h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15	TPLWAKEUP	R/W		Wake TPL
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled. Device sends wake-up frames on TPL if wake-up reason was other than communication
14	SYSFLTEVT	R/W		Enable wakeup on a detected system fault.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
13	BALRDY	R/W		Enable wakeup on cell voltage balancing ready.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
12	WAKEUPIN	R/W		Enable wakeup on detected wakeup input. Enabling this bit automatically enables the digital receiver for wake-up input 0.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
11	ALARMIN	R/W		Enable wakeup on detected alarm input
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
10	AIN3UV	R/W		Enable wakeup on AIN3_UV.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
9	AIN3OV	R/W		Enable wakeup on AIN3_OV.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
8	AIN2UV	R/W		Enable wakeup on AIN2_UV.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
7	AIN2OV	R/W		Enable wakeup on AIN2_OV.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
6	AIN1UV	R/W		Enable wakeup on AIN1_UV.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
5	AIN1OV	R/W		Enable wakeup on AIN1_OV.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
4	AIN0UV	R/W		Enable wakeup on AIN0_UV.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
3	AIN0OV	R/W		Enable wakeup on AIN0_OV.

Table 93. FEH\_WAKEUP\_CFG0 register - wake up source configuration (address 408h)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
2	VCUV1	R/W	0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
				Enable wakeup on VC_UV1.
1	VCUV0	R/W	0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
				Enable wakeup on VC_UV0.
0	VCOV	R/W	0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
				Enable wakeup on VC_OV.

### 12.1.23 FEH\_WAKEUP\_CFG1 register

Wake-up source configuration

Table 94. FEH\_WAKEUP\_CFG1 register - wake-up source configuration (address 409h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							BALPROT
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R/W
Bit	7	6	5	4	3	2	1	0
Symbol	reserved						AINAUV	AINAOV
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R/W	R/W

Table 95. FEH\_WAKEUP\_CFG1 register - wake up source configuration (address 409h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:9	reserved	R	0h	This read-only field is reserved and always has the value 0.
8	BALPROT	R/W		Enable wakeup on detected balancing protection
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
7:2	reserved	R	0h	This read-only field is reserved and always has the value 0.
1	AINAUV	R/W		Enable wakeup on AINA_UV.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
0	AINAOV	R/W		Enable wakeup on AINA_OV.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled



12.1.24 FEH\_WAKEUP\_REASON0 register

Wake-up reason register

Table 96. FEH\_WAKEUP\_REASON0 register - wake-up reason register (address 40Ah) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	COMM	SYSFLTEVT	BALRDY	WAKEUPIN	ALARMIN	AIN3UV	AIN3OV	AIN2UV
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	AIN2OV	AIN1UV	AIN1OV	AIN0UV	AIN0OV	VCUV1	VCUV0	VCOV
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 97. FEH\_WAKEUP\_REASON0 register - wake up reason register (address 40Ah)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15	COMM	R		Communication detected Read clears bit.
			0*	NO_WAKE (read) Wakeup not caused by detected communication
			1	WAKE_UP (read) Wakeup caused by detected communication
14	SYSFLTEVT	R		Detected system fault. Read clears bit.
			0*	NO_WAKE (read) Wakeup not caused by detected system fault
			1	WAKE_UP (read) Wakeup caused by detected system fault
13	BALRDY	R		Cell voltage balancing ready Read clears bit.
			0*	NO_WAKE (read) Wakeup not caused by cell voltage balancing ready
			1	WAKE_UP (read) Wakeup caused by cell voltage balancing ready
12	WAKEUPIN	R		Detected wakeup input Read clears bit.
			0*	NO_WAKE (read) Wakeup not caused by detected wakeup input
			1	WAKE_UP (read) Wakeup caused by detected wakeup input
11	ALARMIN	R		Detected alarm input Read clears bit.
			0*	NO_WAKE (read) Wakeup not caused by detected Wakeup input
			1	WAKE_UP (read) Wakeup caused by detected Wakeup input
10	AIN3UV	R		AIN3_UV Read clears bit.
			0*	NO_WAKE (read) Wakeup not caused by AIN3_UV
			1	WAKE_UP (read) Wakeup caused by AIN3_UV
9	AIN3OV	R		AIN3_OV Read clears bit.
			0*	NO_WAKE (read) Wakeup not caused by AIN3_OV
			1	WAKE_UP (read) Wakeup caused by AIN3_OV

Table 97. FEH\_WAKEUP\_REASON0 register - wake up reason register (address 40Ah)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
8	AIN2UV	R		AIN2_UV Read clears bit.
			0*	NO_WAKE (read) Wakeup not caused by AIN2_UV
			1	WAKE_UP (read) Wakeup caused by AIN2_UV
7	AIN2OV	R		AIN2_OV Read clears bit.
			0*	NO_WAKE (read) Wakeup not caused by AIN2_OV
			1	WAKE_UP (read) Wakeup caused by AIN2_OV
6	AIN1UV	R		AIN1_UV Read clears bit.
			0*	NO_WAKE (read) Wakeup not caused by AIN1_UV
			1	WAKE_UP (read) Wakeup caused by AIN1_UV
5	AIN1OV	R		AIN1_OV Read clears bit.
			0*	NO_WAKE (read) Wakeup not caused by AIN1_OV
			1	WAKE_UP (read) Wakeup caused by AIN1_OV
4	AIN0UV	R		AIN0_UV Read clears bit.
			0*	NO_WAKE (read) Wakeup not caused by AIN0_UV
			1	WAKE_UP (read) Wakeup caused by AIN0_UV
3	AIN0OV	R		AIN0_OV Read clears bit.
			0*	NO_WAKE (read) Wakeup not caused by AIN0_OV
			1	WAKE_UP (read) Wakeup caused by AIN0_OV
2	VCUV1	R		VC_UV1 Read clears bit.
			0*	NO_WAKE (read) Wakeup not caused by VC_UV1
			1	WAKE_UP (read) Wakeup caused by VC_UV1
1	VCUV0	R		VC_UV0 Read clears bit.
			0*	NO_WAKE (read) Wakeup not caused by VC_UV0
			1	WAKE_UP (read) Wakeup caused by VC_UV0
0	VCOV	R		VC_OV Read clears bit.
			0*	NO_WAKE (read) Wakeup not caused by VC_OV
			1	WAKE_UP (read) Wakeup caused by VC_OV

## 12.1.25 FEH\_WAKEUP\_REASON1 register

Wake-up reason register

Table 98. FEH\_WAKEUP\_REASON1 register - wake-up reason register (address 40Bh) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							BALPROT
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	reserved						AINAUV	AINAOV
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 99. FEH\_WAKEUP\_REASON1 register - wake up reason register (address 40Bh)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:9	reserved	R	0h	This read-only field is reserved and always has the value 0.
8	BALPROT	R		Balancing protection detection Read clears bit.
			0*	NO_WAKE (read) Wakeup not caused by detected Balancing protection
			1	WAKE_UP (read) Wakeup caused by detected Balancing protection
7:2	reserved	R	0h	This read-only field is reserved and always has the value 0.
1	AINAUV	R		AIN0_UV Read clears bit.
			0*	NO_WAKE (read) Wakeup not caused by AINA_UV
			1	WAKE_UP (read) Wakeup caused by AINA_UV
0	AINAOV	R		AINA_OV Read clears bit.
			0*	NO_WAKE (read) Wakeup not caused by AINA_OV
			1	WAKE_UP (read) Wakeup caused by AINA_OV

12.1.26 FEH\_MON\_BIST\_CTRL register

Monitor BIST control register

Table 100. FEH\_MON\_BIST\_CTRL register - monitor BIST control register (address 410h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	BISTCRC							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	7	6	5	4	3	2	1	0
Symbol	BISTCRC							STARTBIST
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	W

Table 101. FEH\_MON\_BIST\_CTRL register - monitor BIST control register (address 410h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:1	BISTCRC	R/W	0h	CRC of the sequential BIST results. The value is different for the automatic BIST after start-up and a manual started BIST, as more monitors are then included. If the resulting CRC differs from the defined values, the BIST was not executed correctly.
			10B7h	STARTUP (read-write) Value 10B7h represents correct CRC value for start-up BIST
			4E3Dh	MAN_NO_VAUX (read-write) Value 4E3Dh represents the correct CRC value for a manual started BIST if VAUX is not enabled
			7742h	MANUAL (read-write) Value 7742h represents correct CRC value for manual started BIST
0	STARTBIST	W		Start BIST of all supply monitors, including VAUXOV, VAUXUV, VDDCOV and VDDCUV, which are not run at start-up. If the

Table 101. FEH\_MON\_BIST\_CTRL register - monitor BIST control register (address 410h)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
				BIST is executed while measurements are running, some created secondary measurement results might be invalid. Read as zero.
			0*	NO_START (write) Do not start BIST
			0*	STATUS (read) Read as zero.
			1	START (write) Start BIST

## 12.1.27 FEH\_MON\_BIST\_RES register

Monitor BIST result register; value changes at start up, if everything is fine to 0000h

Table 102. FEH\_MON\_BIST\_RES register - Monitor BIST result register (address 411h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved				VDDCUV	VDDCOV	VAUXUV	VAUXOV
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	VPREREFSUV	AFECPUV	AFECPOV	VANAUV	VANAOV	VDDAUUV	VDDAOV	VBATOV
Reset	1	1	1	1	1	1	1	1
Access	R	R	R	R	R	R	R	R

Table 103. FEH\_MON\_BIST\_RES register - Monitor BIST result register (address 411h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:12	reserved	R	0h	This read-only field is reserved and always has the value 0.
11	VDDCUV	R		VDDC Supply under-voltage BIST failed. Not part of start-up BIST, only executed for manual BIST execution.
			0*	PASS (read) BIST passed
			1	FAIL (read) BIST failed
10	VDDCOV	R		VDDC Supply over-voltage BIST failed. Not part of start-up BIST, only executed for manual BIST execution.
			0*	PASS (read) BIST passed
			1	FAIL (read) BIST failed
9	VAUXUV	R		VAUX Supply under-voltage BIST failed. Not part of start-up BIST, only executed for manual BIST execution.
			0*	PASS (read) BIST passed
			1	FAIL (read) BIST failed
8	VAUXOV	R		VAUX Supply over-voltage BIST failed. Not part of start-up BIST, only executed for manual BIST execution.
			0*	PASS (read) BIST passed
			1	FAIL (read) BIST failed
7	VPREREFSUV	R		VPREREFSUV Supply under-voltage BIST failed.

Table 103. FEH\_MON\_BIST\_RES register - Monitor BIST result register (address 411h)....continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
			0	PASS (read) BIST passed
			1*	FAIL (read) BIST failed
				Analog Frontend Charge Pump under-voltage BIST failed.
6	AFECPUV	R	0	PASS (read) BIST passed
			1*	FAIL (read) BIST failed
				Analog Frontend Charge Pump over-voltage BIST failed.
5	AFECPOV	R	0	PASS (read) BIST passed
			1*	FAIL (read) BIST failed
				VANA under-voltage BIST failed.
4	VANAUV	R	0	PASS (read) BIST passed
			1*	FAIL (read) BIST failed
				VANA over-voltage BIST failed.
3	VANAOV	R	0	PASS (read) BIST passed
			1*	FAIL (read) BIST failed
				VDDA Supply under-voltage BIST failed.
2	VDDAUUV	R	0	PASS (read) BIST passed
			1*	FAIL (read) BIST failed
				VDDA Supply over-voltage BIST failed.
1	VDDAOV	R	0	PASS (read) BIST passed
			1*	FAIL (read) BIST failed
				VBAT Supply over-voltage BIST failed.
0	VBATOV	R	0	PASS (read) BIST passed
			1*	FAIL (read) BIST failed

12.1.28 FEH\_ACC\_ERR register

Access error status register

Table 104. FEH\_ACC\_ERR register - access error status register (address 41Eh) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	ERRSTAT	ERRACC	ERRADD					
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	ERRADD							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

**Table 105. FEH\_ACC\_ERR register - access error status register (address 41Eh)**

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15	ERRSTAT	R		Access error status Read clears bit.
			0*	NO_ERROR (read) No error occurred
			1	ERROR (read) Access error has occurred
14	ERRACC	R		Access type of the last access error Read clears bit.
			0*	READ (read) Last error occurred during a read access
			1	WRITE (read) Last error occurred during a write access
13:0	ERRADD	R	0h	Address of the last access which created an access error Read clears bits.

**12.1.29 FEH\_GRP\_FLT\_STAT register**

Main system fault status register; this register holds one bit per fault group. For each fault group a separate status register exists. The bit here is cleared if all its sources are cleared.

**Table 106. FEH\_GRP\_FLT\_STAT register - Main system fault status register (address 41Fh) bit allocation**

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	reserved				MEASFLT	COMFLT	ANAFLT	SUPPLYFLT
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

**Table 107. FEH\_GRP\_FLT\_STAT register - Main system fault status register (address 41Fh)**

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:4	reserved	R	0h	This read-only field is reserved and always has the value 0.
3	MEASFLT	R		Measurement fault status
			0*	NO_ERROR (read) No measurement fault detected
			1	ERROR (read) Measurement fault detected
2	COMFLT	R		Communication fault status
			0*	NO_ERROR (read) No communication fault detected
			1	ERROR (read) Communication fault detected.
1	ANAFLT	R		Analog fault status
			0*	NO_ERROR (read) No analog fault detected
			1	ERROR (read) Analog fault detected
0	SUPPLYFLT	R		Internal/external supply fault status
			0*	NO_ERROR (read) No supply error detected
			1	ERROR (read) Supply error detected

## 12.1.30 FEH\_SUPPLY\_FLT\_STAT0 register

Supply fault status register 0 (these monitors are part of the BIST)

Table 108. FEH\_SUPPLY\_FLT\_STAT0 register - Supply fault status register 0 (address 420h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved				VDDCUV	VDDCOV	VAUXUV	VAUXOV
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R/W	R/W	R/W	R/W
Bit	7	6	5	4	3	2	1	0
Symbol	VPREREFSUV	AFECPUV	AFECPOV	VANAUV	VANAOV	VDDAUV	VDDAOV	VBATOV
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 109. FEH\_SUPPLY\_FLT\_STAT0 register - Supply fault status register 0 (address 420h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:12	reserved	R	0h	This read-only field is reserved and always has the value 0.
11	VDDCUV	R/W		VDDC Supply under-voltage fault. Write 1 clears bit.
			0*	NO_UV (read-write) No VDDC Supply under-voltage detected.
			1	UV (read-write) VDDC Supply under-voltage detected.
10	VDDCOV	R/W		VDDC Supply over-voltage fault. Write 1 clears bit.
			0*	NO_OV (read-write) No VDDC Supply over-voltage detected.
			1	OV (read-write) VDDC Supply over-voltage detected.
9	VAUXUV	R/W		VAUX Supply under-voltage fault. Write 1 clears bit.
			0*	NO_UV (read-write) No VAUX Supply under-voltage detected.
			1	UV (read-write) VAUX Supply under-voltage detected.
8	VAUXOV	R/W		VAUX Supply over-voltage fault. Write 1 clears bit.
			0*	NO_OV (read-write) No VAUX Supply over-voltage detected.
			1	OV (read-write) VAUX Supply over-voltage detected.
7	VPREREFSUV	R/W		VPREREFS Supply under-voltage fault. Write 1 clears bit.
			0*	NO_UV (read-write) No VPREREFS Supply under-voltage detected.
			1	UV (read-write) VPREREFS Supply under-voltage detected.
6	AFECPUV	R/W		AFE Charge Pump under-voltage fault. Write 1 clears bit.
			0*	NO_UV (read-write) No AFE Charge Pump under-voltage detected.
			1	UV (read-write) AFE Charge Pump under-voltage detected.
5	AFECPOV	R/W		AFE Charge Pump over-voltage fault. Write 1 clears bit.
			0*	NO_OV (read-write) No AFE Charge Pump over-voltage detected.

Table 109. FEH\_SUPPLY\_FLT\_STAT0 register - Supply fault status register 0 (address 420h)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
			1	OV (read-write) AFE Charge Pump over-voltage detected.
4	VANAUV	R/W		VANA Supply under-voltage fault. Write 1 clears bit.
			0*	NO_UV (read-write) No VANA Supply under-voltage detected.
			1	UV (read-write) VANA Supply under-voltage detected.
3	VANA OV	R/W		VANA Supply over-voltage fault. Write 1 clears bit.
			0*	NO_OV (read-write) No VANA Supply over-voltage detected.
			1	OV (read-write) VANA Supply over-voltage detected.
2	VDDAUUV	R/W		VDDA Supply under-voltage fault. Write 1 clears bit.
			0*	NO_UV (read-write) No VDDA Supply under-voltage detected.
			1	UV (read-write) VDDA Supply under-voltage detected.
1	VDDA OV	R/W		VDDA Supply over-voltage fault. Write 1 clears bit.
			0*	NO_OV (read-write) No VDDA Supply over-voltage detected.
			1	OV (read-write) VDDA Supply over-voltage detected.
0	VBAT OV	R/W		VBAT Supply over-voltage fault. Write 1 clears bit.
			0*	NO_OV (read-write) No VBAT Supply over-voltage detected.
			1	OV (read-write) VBAT Supply over-voltage detected.

## 12.1.31 FEH\_SUPPLY\_FLT\_STAT1 register

Supply fault status register 1 (these monitors are not part of the BIST)

Table 110. FEH\_SUPPLY\_FLT\_STAT1 register - Supply fault status register 1 (address 421h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	reserved	VPREUV	VPREOV	VDDIOUV	VDDIOOV	VDDCHC	VPRERE FSOV	VBATLV
Reset	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 111. FEH\_SUPPLY\_FLT\_STAT1 register - Supply fault status register 1 (address 421h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:7	reserved	R	0h	This read-only field is reserved and always has the value 0.
6	VPREUV	R/W		VPRE Supply under-voltage fault. Write 1 clears bit.
			0*	NO_UV (read-write) No VPRE Supply under-voltage detected.



Table 111. FEH\_SUPPLY\_FLT\_STAT1 register - Supply fault status register 1 (address 421h)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
5	VPREOV	R/W	1	UV (read-write) VPRE Supply under-voltage detected.
				VPRE Supply over-voltage fault. Write 1 clears bit.
			0*	NO_OV (read-write) No VPRE Supply over-voltage detected.
4	VDDIOUV	R/W	1	OV (read-write) VPRE Supply over-voltage detected.
				VDDIO Supply under-voltage fault. Write 1 clears bit.
			0*	NO_UV (read-write) No VDDIO Supply under-voltage detected.
3	VDDIOOV	R/W	1	UV (read-write) VDDIO Supply under-voltage detected.
				VDDIO Supply over-voltage fault. Write 1 clears bit.
			0*	NO_OV (read-write) No VDDIO Supply over-voltage detected.
2	VDDCHC	R/W	1	OV (read-write) VDDIO Supply over-voltage detected.
				VDDC high-current fault. Write 1 clears bit.
			0*	NO_HC (read-write) No VDDC high-current detected.
1	VPREREFSOV	R/W	1	HC (read-write) VDDC high-current detected.
				VPREREFS Supply over-voltage fault. Write 1 clears bit.
			0*	NO_OV (read-write) No VPREREFS Supply over-voltage detected.
0	VBATLV	R/W	1	OV (read-write) VPREREFS Supply over-voltage detected.
				VBAT Supply low-voltage fault. Write 1 clears bit.
			0*	NO_LV (read-write) No VBAT Supply low-voltage detected.
			1	LV (read-write) VBAT Supply low-voltage detected.

12.1.32 FEH\_ANA\_FLT\_STAT register

Analog fault status register

Table 112. FEH\_ANA\_FLT\_STAT register - analog fault status register (address 422h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	reserved						BALFLT	MONBIST
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R/W	R/W

Table 113. FEH\_ANA\_FLT\_STAT register - analog fault status register (address 422h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:2	reserved	R	0h	This read-only field is reserved and always has the value 0.
1	BALFLT	R/W		Cell balance function fault. Write 1 clears bit.
			0*	NO_FLT (read-write) No cell balancing fault detected
			1	FAULT (read-write) Cell balancing fault detected
0	MONBIST	R/W		Monitor BIST failure fault. Write 1 clears bit.
			0*	NO_FLT (read-write) No monitor BIST failure detected.
			1	FAILURE (read-write) Monitor BIST failure detected.

### 12.1.33 FEH\_COM\_FLT\_STAT register

Communication fault status register

Table 114. FEH\_COM\_FLT\_STAT register - communication fault status register (address 423h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	COMERRCNT							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	7	6	5	4	3	2	1	0
Symbol	reserved			RSPLENERR	COMTO	ERRCNTOF	CRCERR	FRAMEERR
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R/W	R/W	R/W	R/W	R/W

Table 115. FEH\_COM\_FLT\_STAT register - communication fault status register (address 423h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:8	COMERRCNT	R/W		Number of communication errors (frame errors, CRC errors) since last clear, counter saturates at 0xFF. Write with any data unequal 0 clears the counter. The counter value is preserved during Sleep mode. Write 1 clears bits. Write 1 clears bits.
			00h*	NO_ERROR (read-write) No communication error occurred
			01h	CNT (read-write) CNT errors occurred
			FFh	MAX (read-write) Maximum communication error counter = 255 communication errors occurred.
7:5	reserved	R	0h	This read-only field is reserved and always has the value 0.
4	RSPLENERR	R/W		Response length error Write 1 clears bit.
			0*	NO_ERROR (read-write) No response length error occurred
			1	ERROR (read-write) The number of SPI clocks did not fit to the length of a requested response
3	COMTO	R/W		Communication timeout fault status Write 1 clears bit.
			0*	NO_TIMEOUT (read-write) No communication timeout has happened.

Table 115. FEH\_COM\_FLT\_STAT register - communication fault status register (address 423h)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
			1	TIMEMOUT (read-write) Communication timeout has happened.
2	ERRCNTOF	R/W		Communication error counter overflow Write 1 clears bit.
			0*	NO_MAX (read-write) Communication error counter has not reached max value.
			1	MAX (read-write) Communication error counter has reached max value.
1	CRCERR	R/W		Communication CRC error Write 1 clears bit.
			0*	NO_ERROR (read-write) No communication CRC error detected.
			1	ERROR (read-write) Communication CRC error detected.
0	FRAMEERR	R/W		Communication frame error (Wrong number of bits or bit-length error) Write 1 clears bit.
			0*	NO_ERROR (read-write) No communication frame error detected.
			1	ERROR (read-write) Communication frame error detected.

## 12.1.34 FEH\_MEAS\_FLT\_STAT register

Other fault status register

Table 116. FEH\_MEAS\_FLT\_STAT register - other fault status register (address 424h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	reserved					SYNCMEASFLT	SECCALCRCFLT	PRIMCALCRCFLT
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R/W	R/W	R/W

Table 117. FEH\_MEAS\_FLT\_STAT register - other fault status register (address 424h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:3	reserved	R	0h	This read-only field is reserved and always has the value 0.
2	SYNCMEASFLT	R/W		Synchronization fault between the measurement units Write 1 clears bit.
			0*	NO_FLT (read-write) No synchronization fault between the measurement units for a Sync cycle has been detected..
			1	FAULT (read-write) Synchronization fault between the measurement units for a Sync cycle has been detected..
1	SECCALCRCFLT	R/W		A fault in the secondary measurement chain calibration data Write 1 clears bit.

Table 117. FEH\_MEAS\_FLT\_STAT register - other fault status register (address 424h)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
0	PRIMCALCRCFLT	R/W	0*	NO_FLT (read-write) No fault in secondary measurement chain calibration data detected.
			1	FAULT (read-write) A fault in the secondary measurement chain calibration data has been detected.
				A fault in the primary measurement chain calibration data Write 1 clears bit.
			0*	NO_FLT (read-write) No fault in primary measurement chain calibration data detected.
			1	FAULT (read-write) A fault in the primary measurement chain calibration data has been detected.

## 12.1.35 FEH\_SUPPLY\_FLT\_POR\_CFG0 register

Supply fault POR selection 0

Table 118. FEH\_SUPPLY\_FLT\_POR\_CFG0 register - supply fault POR selection 0 (address 428h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved				VDDCUVEN	VDDCOVEN	VAUXUVEN	VAUXOVEN
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R/W	R/W	R/W	R/W
Bit	7	6	5	4	3	2	1	0
Symbol	VPRERE FSUVEN	AFECPUVEN	AFECPOVEN	VANAUVEN	VANAOVEN	VDDAUVEN	VDDAOVEN	VBATOVEN
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 119. FEH\_SUPPLY\_FLT\_POR\_CFG0 register - supply fault POR selection 0 (address 428h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:12	reserved	R	0h	This read-only field is reserved and always has the value 0.
11	VDDCUVEN	R/W		POR on VDDC under-voltage fault.
			0*	NO_POR (read-write) No POR in case of VDDC under-voltage
			1	POR (read-write) VDDC under-voltage error leads to POR
10	VDDCOVEN	R/W		POR on VDDC over-voltage fault.
			0*	NO_POR (read-write) No POR in case of VDDC over-voltage
			1	POR (read-write) VDDC over-voltage error leads to POR
9	VAUXUVEN	R/W		POR on VAUX under-voltage fault.
			0*	NO_POR (read-write) No POR in case of VAUX supply under-voltage
			1	POR (read-write) VAUX supply under-voltage error leads to POR

Table 119. FEH\_SUPPLY\_FLT\_POR\_CFG0 register - supply fault POR selection 0 (address 428h)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
8	VAUXOVEN	R/W		POR on VAUX over-voltage fault.
			0*	NO_POR (read-write) No POR in case of VAUX supply over-voltage
			1	POR (read-write) VAUX supply over-voltage error leads to POR
7	VPREREFSUVEN	R/W		POR on VPREREFS Supply under-voltage fault.
			0*	NO_POR (read-write) No POR in case of VPREREFS supply under-voltage
			1	POR (read-write) VPREREFS supply under-voltage error leads to POR
6	AFECPUVEN	R/W		POR on AFE Charge Pump under-voltage fault.
			0*	NO_POR (read-write) No POR in case of AFE Charge Pump under-voltage
			1	POR (read-write) AFE Charge Pump under-voltage error leads to POR
5	AFECPOVEN	R/W		POR on AFE Charge Pump over-voltage fault.
			0*	NO_POR (read-write) No POR in case of AFE Charge Pump over-voltage
			1	POR (read-write) AFE Charge Pump over-voltage error leads to POR
4	VANAUVEN	R/W		POR on VANA Supply under-voltage fault.
			0*	NO_POR (read-write) No POR in case of VANA supply under-voltage
			1	POR (read-write) VANA supply under-voltage error leads to POR
3	VANAOVEN	R/W		POR on VANA Supply over-voltage fault.
			0*	NO_POR (read-write) No POR in case of VANA supply over-voltage
			1	POR (read-write) VANA supply over-voltage error leads to POR
2	VDDAUVEN	R/W		POR on VDDA Supply under-voltage fault.
			0*	NO_POR (read-write) No POR in case of VDDA supply under-voltage
			1	POR (read-write) VDDA supply under-voltage error leads to POR
1	VDDAOVEN	R/W		POR on VDDA Supply over-voltage fault.
			0*	NO_POR (read-write) No POR in case of VDDA supply over-voltage
			1	POR (read-write) VDDA supply over-voltage error leads to POR
0	VBATOVEN	R/W		POR on VBAT Supply over-voltage fault.
			0*	NO_POR (read-write) No POR in case of VBAT supply over-voltage
			1	POR (read-write) VBAT supply over-voltage error leads to POR

## 12.1.36 FEH\_SUPPLY\_FLT\_POR\_CFG1 register

Supply fault POR selection 1

Table 120. FEH\_SUPPLY\_FLT\_POR\_CFG1 register - supply fault POR selection 1 (address 429h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	reserved	VPREUVEN	VPREOVEN	VDDIOUVEN	VDDIOOVEN	VDDCHCEN	VPREREFSOVEN	VBATLVEN
Reset	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 121. FEH\_SUPPLY\_FLT\_POR\_CFG1 register - supply fault POR selection 1 (address 429h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:7	reserved	R	0h	This read-only field is reserved and always has the value 0.
6	VPREUVEN	R/W		POR on VPRE Supply under-voltage fault.
			0*	NO_POR (read-write) No POR in case of VPRE supply under-voltage
			1	POR (read-write) VPRE supply under-voltage error leads to POR
5	VPREOVEN	R/W		POR on VPRE Supply over-voltage fault.
			0*	NO_POR (read-write) No POR in case of VPRE over-voltage
			1	POR (read-write) VPRE over-voltage error leads to POR
4	VDDIOUVEN	R/W		POR on VDDIO Supply under-voltage fault.
			0*	NO_POR (read-write) No POR in case of VDDIO supply under-voltage
			1	POR (read-write) VDDIO supply under-voltage error leads to POR
3	VDDIOOVEN	R/W		POR on VDDIO Supply over-voltage fault.
			0*	NO_POR (read-write) No POR in case of VDDIO supply over-voltage
			1	POR (read-write) VDDIO supply over-voltage error leads to POR
2	VDDCHCEN	R/W		POR on VDDC high-current fault.
			0*	NO_POR (read-write) No POR in case of VDDC high-current
			1	POR (read-write) VDDC high-current error leads to POR
1	VPREREFSOVEN	R/W		POR on VPREREFS Supply over-voltage fault.
			0*	NO_POR (read-write) No POR in case of VPREREFS over-voltage
			1	POR (read-write) VPREREFS over-voltage error leads to POR

Table 121. FEH\_SUPPLY\_FLT\_POR\_CFG1 register - supply fault POR selection 1 (address 429h)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
0	VBATLVEN	R/W		POR on VBAT Supply low-voltage fault.
			0*	NO_POR (read-write) No POR in case of VBAT supply low-voltage
			1	POR (read-write) VBAT supply low-voltage error leads to POR

### 12.1.37 FEH\_COM\_FLT\_POR\_CFG register

Communication fault POR enable register

Table 122. FEH\_COM\_FLT\_POR\_CFG register - communication fault POR enable register (address 42Bh) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	reserved				COMTOEN	ERRCNT OFEN	reserved	
Reset	0	0	0	0	1	0	0	0
Access	R	R	R	R	R/W	R/W	R	R

Table 123. FEH\_COM\_FLT\_POR\_CFG register - communication fault POR enable register (address 42Bh)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:4	reserved	R	0h	This read-only field is reserved and always has the value 0.
3	COMTOEN	R/W		Create a POR if a communication timeout happens.
			0	PREV_MOD (read-write) Device fallbacks to prev. Mode in case of communication timeout
			1*	POR (read-write) POR in case of communication timeout
2	ERRCNTOFEN	R/W		Communication error counter max value leads to POR
			0*	NO_POR (read-write) Communication error counter has reached max value.
			1	POR (read-write) Communication error counter max value leads to POR
1:0	reserved	R	0h	This read-only field is reserved and always has the value 0.

12.1.38 FEH\_SUPPLY\_FLT\_EVT\_CFG0 register

Supply fault event selection register 0

Table 124. FEH\_SUPPLY\_FLT\_EVT\_CFG0 register - supply fault event selection register 0 (address 430h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved				VDDCUVEN	VDDCOVEN	VAUXUVEN	VAUXOVEN
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R/W	R/W	R/W	R/W
Bit	7	6	5	4	3	2	1	0
Symbol	VPREREFSUVEN	AFECPUVEN	AFECPOVEN	VANAUVEN	VANAOVEN	VDDAUVEN	VDDAOVEN	VBATOVEN
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 125. FEH\_SUPPLY\_FLT\_EVT\_CFG0 register - supply fault event selection register 0 (address 430h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:12	reserved	R	0h	This read-only field is reserved and always has the value 0.
11	VDDCUVEN	R/W		Event on VDDC under-voltage fault.
			0*	NO_EV (read-write) No event on VDDC under-voltage fault.
			1	EVENT (read-write) Event on VDDC under-voltage fault.
10	VDDCOVEN	R/W		Event on VDDC over-voltage fault.
			0*	NO_EV (read-write) No event on VDDC over-voltage fault.
			1	EVENT (read-write) Event on VDDC over-voltage fault.
9	VAUXUVEN	R/W		Event on VAUX under-voltage fault.
			0*	NO_EV (read-write) No event on VAUX under-voltage fault.
			1	EVENT (read-write) Event on VAUX under-voltage fault.
8	VAUXOVEN	R/W		Event on VAUX over-voltage fault.
			0*	NO_EV (read-write) No event on VAUX over-voltage fault.
			1	EVENT (read-write) Event on VAUX over-voltage fault.
7	VPREREFSUVEN	R/W		Event on VPREREFS Supply under-voltage fault.
			0*	NO_EV (read-write) No event on VPREREFS Supply under-voltage fault.
			1	EVENT (read-write) Event on VPREREFS Supply under-voltage fault.
6	AFECPUVEN	R/W		Event on AFE Charge Pump under-voltage fault.
			0*	NO_EV (read-write) No event on AFE Charge Pump under-voltage fault.
			1	EVENT (read-write) Event on AFE Charge Pump under-voltage fault.
5	AFECPOVEN	R/W		Event on AFE Charge Pump over-voltage fault.
			0*	NO_EV (read-write) No event on AFE Charge Pump over-voltage fault.



Table 125. FEH\_SUPPLY\_FLT\_EVT\_CFG0 register - supply fault event selection register 0 (address 430h)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
			1	EVENT (read-write) Event on AFE Charge Pump over-voltage fault.
4	VANAUVEN	R/W		Event on VANA Supply under-voltage fault.
			0*	NO_EV (read-write) No event on VANA Supply under-voltage fault.
			1	EVENT (read-write) Event on VANA Supply under-voltage fault.
3	VANAOVEN	R/W		Event on VANA Supply over-voltage fault.
			0*	NO_EV (read-write) No event on VANA Supply over-voltage fault.
			1	EVENT (read-write) Event on VANA Supply over-voltage fault.
2	VDDAUVEN	R/W		Event on VDDA Supply under-voltage fault.
			0*	NO_EV (read-write) No event on VDDA Supply under-voltage fault.
			1	EVENT (read-write) Event on VDDA Supply under-voltage fault.
1	VDDAOVEN	R/W		Event on VDDA Supply over-voltage fault.
			0*	NO_EV (read-write) No event on VDDA Supply over-voltage fault.
			1	EVENT (read-write) Event on VDDA Supply over-voltage fault.
0	VBATOVEN	R/W		Event on VBAT Supply over-voltage fault.
			0*	NO_EV (read-write) No event on VBAT Supply over-voltage fault.
			1	EVENT (read-write) Event on VBAT Supply over-voltage fault.

## 12.1.39 FEH\_SUPPLY\_FLT\_EVT\_CFG1 register

Supply fault event selection register 1

Table 126. FEH\_SUPPLY\_FLT\_EVT\_CFG1 register - supply fault event selection register 1 (address 431h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	reserved	VPREUVEN	VPREOVEN	VDDIOUVEN	VDDIOOVEN	VDDCHCEN	VPREREFSOVEN	VBATLVEN
Reset	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 127. FEH\_SUPPLY\_FLT\_EVT\_CFG1 register - supply fault event selection register 1 (address 431h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:7	reserved	R	0h	This read-only field is reserved and always has the value 0.
6	VPREUVEN	R/W		Event on VPRE Supply under-voltage fault.
			0*	NO_EV (read-write) No event on VPRE Supply under-voltage fault.
			1	EVENT (read-write) Event on VPRE Supply under-voltage fault.
5	VPREOVEN	R/W		Event on VPRE Supply over-voltage fault.
			0*	NO_EV (read-write) No event on VPRE Supply over-voltage fault.
			1	EVENT (read-write) Event on VPRE Supply over-voltage fault.
4	VDDIOUVEN	R/W		Event on VDDIO Supply under-voltage fault.
			0*	NO_EV (read-write) No event on VDDIO Supply under-voltage fault.
			1	EVENT (read-write) Event on VDDIO Supply under-voltage fault.
3	VDDIOOVEN	R/W		Event on VDDIO Supply over-voltage fault.
			0*	NO_EV (read-write) No event on VDDIO Supply over-voltage fault.
			1	EVENT (read-write) Event on VDDIO Supply over-voltage fault.
2	VDDCHCEN	R/W		Event on VDDC high-current fault.
			0*	NO_EV (read-write) No event on VDDC high-current fault.
			1	EVENT (read-write) Event on VDDC high-current fault.
1	VPREREFSOVEN	R/W		Event on VPREREFS Supply over-voltage fault.
			0*	NO_EV (read-write) No event on VPREREFS Supply over-voltage fault.
			1	EVENT (read-write) Event on VPREREFS Supply over-voltage fault.
0	VBATLVEN	R/W		Event on VBAT Supply low-voltage fault.
			0*	NO_EV (read-write) No event on VBAT Supply low-voltage fault.
			1	EVENT (read-write) Event on VBAT Supply low-voltage fault.

### 12.1.40 FEH\_ANA\_FLT\_EVT\_CFG register

Analog fault event enable register

Table 128. FEH\_ANA\_FLT\_EVT\_CFG register - analog fault event enable register (address 432h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0

**Table 128. FEH\_ANA\_FLT\_EVT\_CFG register - analog fault event enable register (address 432h) bit allocation...***continued*

Symbol	reserved						BALFLTEN	MONBISTEN
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R/W	R/W

**Table 129. FEH\_ANA\_FLT\_EVT\_CFG register - analog fault event enable register (address 432h)**

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:2	reserved	R	0h	This read-only field is reserved and always has the value 0.
1	BALFLTEN	R/W		Event on cell balance function fault.
			0*	NO_EV (read-write) No event on cell balance function fault.
			1	EVENT (read-write) Event on cell balance function fault.
0	MONBISTEN	R/W		Event on Monitor BIST fault.
			0*	NO_EV (read-write) No event on Monitor BIST fault.
			1	EVENT (read-write) Event on Monitor BIST fault.

### 12.1.41 FEH\_COM\_FLT\_EVT\_CFG register

Communication fault event enable register

**Table 130. FEH\_COM\_FLT\_EVT\_CFG register - communication fault event enable register (address 433h) bit allocation**

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	reserved			RSPLEN ERREN	reserved	ERRCNT OFEN	CRCERREN	FRAMEE RREN
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R/W	R	R/W	R/W	R/W

**Table 131. FEH\_COM\_FLT\_EVT\_CFG register - communication fault event enable register (address 433h)**

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:5	reserved	R	0h	This read-only field is reserved and always has the value 0.
4	RSPLENERREN	R/W		Event on number of SPI clocks did not fit to the length of a requested response
			0*	NO_EV (read-write) No event on number of SPI clocks did not fit to the length of a requested response
			1	EVENT (read-write) Event on number of SPI clocks did not fit to the length of a requested response
3	reserved	R	0h	This read-only field is reserved and always has the value 0.

Table 131. FEH\_COM\_FLT\_EVT\_CFG register - communication fault event enable register (address 433h)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
2	ERRCNTOFEN	R/W		Event on communication error counter has reached max value.
			0*	NO_EV (read-write) No event on communication error counter has reached max value.
			1	EVENT (read-write) Event on communication error counter has reached max value.
1	CRCERREN	R/W		Event on communication CRC error detected.
			0*	NO_EV (read-write) No event on communication CRC error detected.
			1	EVENT (read-write) Event on communication CRC error detected.
0	FRAMEERREN	R/W		Event on communication error detected. Wrong number of bits, bit-length error.
			0*	NO_EV (read-write) No event on communication error detected.
			1	EVENT (read-write) Event on communication error detected.

## 12.1.42 FEH\_MEAS\_FLT\_EVT\_CFG register

Measurement fault event enable register

Table 132. FEH\_MEAS\_FLT\_EVT\_CFG register - measurement fault event enable register (address 434h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	reserved					SYNCMEASFLTEN	SECCALCRCFLTEN	PRIMCALCRCFLTEN
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R/W	R/W	R/W

Table 133. FEH\_MEAS\_FLT\_EVT\_CFG register - measurement fault event enable register (address 434h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:3	reserved	R	0h	This read-only field is reserved and always has the value 0.
2	SYNCMEASFLTEN	R/W		Event on synchronization fault between the measurement units for a Sync cycle.
			0*	NO_EV (read-write) No event on synchronization fault.
			1	EVENT (read-write) Event on synchronization fault.
1	SECCALCRCFLTEN	R/W		Event on secondary calibration CRC fault.
			0*	NO_EV (read-write) No event on secondary calibration CRC fault.

Table 133. FEH\_MEAS\_FLT\_EVT\_CFG register - measurement fault event enable register (address 434h)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
			1	EVENT (read-write) Event on secondary calibration CRC fault.
0	PRIMCALCRCFLTEN	R/W		Event on primary calibration CRC fault.
			0*	NO_EV (read-write) No event on primary calibration CRC fault.
			1	EVENT (read-write) Event on primary calibration CRC fault.

### 12.1.43 FEH\_POR\_REASON register

Power-on reset reason. The value is stored in the ULP domain.

Table 134. FEH\_POR\_REASON register - power on reset reason (address 480h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved						SOURCE									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 135. FEH\_POR\_REASON register - power on reset reason (address 480h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:10	reserved	R	0h	This read-only field is reserved and always has the value 0.
9:0	SOURCE	R		Reason for POR. POR sources are binary coded and protected by an EDC. <b>Other</b> values as shown below represent errors in EDC.
			000h*	VDDDLPPERMOV (read) POR caused by VDDDLPPERMOV
			00Fh	VDDDLPUV (read) POR caused by VDDDLPUV
			04Eh	VDDDUV (read) POR caused by VDDDUV
			083h	VBATLV (read) POR caused by VBATLV
			08Ch	VDDIOUV (read) POR caused by VDDIOUV
			0BFh	SWRESET (read) POR caused by software Deep Sleep request
			0C2h	VBATOV (read) POR caused by VBATOV
			0CDh	VDDDOV (read) POR caused by VDDDOV
			105h	VDDCOV (read) POR caused by VDDCOV
			10Ah	VAUXUV (read) POR caused by VAUXUV
			144h	VBATUV (read) POR caused by VBATUV
			14Bh	VDDIOOV (read) POR caused by VDDIOOV
			186h	VDDCUV (read) POR caused by VDDCUV
			189h	VAUXOV (read) POR caused by VAUXOV
			1C7h	VDDCOC (read) POR caused by VDDCOC
			1C8h	VDDCHC (read) POR caused by VDDCHC

Table 135. FEH\_POR\_REASON register - power on reset reason (address 480h)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
			211h	VDDAUV (read) POR caused by VDDAUV
			21Eh	SLEEPOSC (read) POR caused by SLEEPOSC
			222h	VPREUV (read) POR caused by VPREUV
			250h	VDDAOV (read) POR caused by VDDAOV
			25Fh	COMTO (read) POR caused by COMTO
			292h	VPREOV (read) POR caused by VPREOV
			29Dh	SECCLK (read) POR caused by SECCLK
			2A1h	LOGICERR (read) POR caused by LOGICERR
			2D3h	VPREREFSOV (read) POR caused by VPREREFSOV
			2DCh	PRMCLK (read) POR caused by PRMCLK
			2E0h	COMERRORS (read) POR caused by COMERRORS
			314h	VPREREFSUV (read) POR caused by VPREREFSUV
			31Bh	OTEMPSHUTDOWN (read) POR caused by OTEMPSHUT DOWN
			355h	VANAOV (read) POR caused by VANAOV
			397h	AFECPOV (read) POR caused by AFECPOV
			398h	AFECPUV (read) POR caused by AFECPUV
			3D6h	VANAUV (read) POR caused by VANAUV

### 12.1.44 GPIO\_CFG0 register

#### GPIO configuration 0

Table 136. GPIO\_CFG0 register - GPIO configuration 0 (address 800h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	OUTEN7	OUTEN6	OUTEN5	OUTEN4	OUTEN3	OUTEN2	OUTEN1	OUTEN0
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	7	6	5	4	3	2	1	0
Symbol	INPEN7	INPEN6	INPEN5	INPEN4	INPEN3	INPEN2	INPEN1	INPEN0
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 137. GPIO\_CFG0 register - GPIO configuration 0 (address 800h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15	OUTEN7	R/W		Enable the output of the GPIO7.
			0*	DISABLED (read-write) Output is disabled
			1	ENABLED (read-write) Output is enabled. If an analog measurement function is enabled on this GPIO, the GPIO

Table 137. GPIO\_CFG0 register - GPIO configuration 0 (address 800h)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
				output is automatically disabled. This is not reflected in this bit.
14	OUTEN6	R/W		Enable the output of the GPIO6.
			0*	DISABLED (read-write) Output is disabled
			1	ENABLED (read-write) Output is enabled. If an analog measurement function is enabled on this GPIO, the GPIO output is automatically disabled. This is not reflected in this bit.
13	OUTEN5	R/W		Enable the output of the GPIO5.
			0*	DISABLED (read-write) Output is disabled
			1	ENABLED (read-write) Output is enabled. If an analog measurement function is enabled on this GPIO, the GPIO output is automatically disabled. This is not reflected in this bit.
12	OUTEN4	R/W		Enable the output of the GPIO4.
			0*	DISABLED (read-write) Output is disabled
			1	ENABLED (read-write) Output is enabled. If an analog measurement function is enabled on this GPIO, the GPIO output is automatically disabled. This is not reflected in this bit.
11	OUTEN3	R/W		Enable the output of the GPIO3.
			0*	DISABLED (read-write) Output is disabled
			1	ENABLED (read-write) Output is enabled. If an analog measurement function is enabled on this GPIO, the GPIO output is automatically disabled. This is not reflected in this bit.
10	OUTEN2	R/W		Enable the output of the GPIO2.
			0*	DISABLED (read-write) Output is disabled
			1	ENABLED (read-write) Output is enabled. If an analog measurement function is enabled on this GPIO, the GPIO output is automatically disabled. This is not reflected in this bit.
9	OUTEN1	R/W		Enable the output of the GPIO1.
			0*	DISABLED (read-write) Output is disabled
			1	ENABLED (read-write) Output is enabled. If an analog measurement function is enabled on this GPIO, the GPIO output is automatically disabled. This is not reflected in this bit.
8	OUTEN0	R/W		Enable the output of the GPIO0.
			0*	DISABLED (read-write) Output is disabled
			1	ENABLED (read-write) Output is enabled. If an analog measurement function is enabled on this GPIO, the GPIO output is automatically disabled. This is not reflected in this bit.
7	INPEN7	R/W		Enable the input for GPIO7. If a special function requires digital input, the according receiver is enabled automatically. This is not reflected in this bit.
			0*	DISABLED (read-write) Input is disabled

Table 137. GPIO\_CFG0 register - GPIO configuration 0 (address 800h)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
			1	ENABLED (read-write) Input is enabled
6	INPEN6	R/W		Enable the input for GPIO6. If a special function requires digital input, the according receiver is enabled automatically. This is not reflected in this bit.
			0*	DISABLED (read-write) Input is disabled
			1	ENABLED (read-write) Input is enabled
5	INPEN5	R/W		Enable the input for GPIO5. If a special function requires digital input, the according receiver is enabled automatically. This is not reflected in this bit.
			0*	DISABLED (read-write) Input is disabled
			1	ENABLED (read-write) Input is enabled
4	INPEN4	R/W		Enable the input for GPIO4. If a special function requires digital input, the according receiver is enabled automatically. This is not reflected in this bit.
			0*	DISABLED (read-write) Input is disabled
			1	ENABLED (read-write) Input is enabled
3	INPEN3	R/W		Enable the input for GPIO3. If a special function requires digital input, the according receiver is enabled automatically. This is not reflected in this bit.
			0*	DISABLED (read-write) Input is disabled
			1	ENABLED (read-write) Input is enabled
2	INPEN2	R/W		Enable the input for GPIO2. If a special function requires digital input, the according receiver is enabled automatically. This is not reflected in this bit.
			0*	DISABLED (read-write) Input is disabled
			1	ENABLED (read-write) Input is enabled
1	INPEN1	R/W		Enable the input for GPIO1. If a special function requires digital input, the according receiver is enabled automatically. This is not reflected in this bit.
			0*	DISABLED (read-write) Input is disabled
			1	ENABLED (read-write) Input is enabled
0	INPEN0	R/W		Enable the input for GPIO0. If a special function requires digital input, the according receiver is enabled automatically. This is not reflected in this bit.
			0*	DISABLED (read-write) Input is disabled
			1	ENABLED (read-write) Input is enabled

### 12.1.45 GPIO\_CFG1 register

#### GPIO configuration 1

Table 138. GPIO\_CFG1 register - GPIO configuration 1 (address 801h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R



Table 138. GPIO\_CFG1 register - GPIO configuration 1 (address 801h) bit allocation...continued

Bit	7	6	5	4	3	2	1	0
Symbol	ODEN7	ODEN6	ODEN5	ODEN4	ODEN3	ODEN2	ODEN1	ODEN0
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 139. GPIO\_CFG1 register - GPIO configuration 1 (address 801h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:8	reserved	R	0h	This read-only field is reserved and always has the value 0.
7	ODEN7	R/W		Open Drain enable, GPIO7.
			0*	DISABLED (read-write) Open Drain disabled
			1	ENABLED (read-write) Open Drain enabled
6	ODEN6	R/W		Open Drain enable, GPIO6.
			0*	DISABLED (read-write) Open Drain disabled
			1	ENABLED (read-write) Open Drain enabled
5	ODEN5	R/W		Open Drain enable, GPIO5.
			0*	DISABLED (read-write) Open Drain disabled
			1	ENABLED (read-write) Open Drain enabled
4	ODEN4	R/W		Open Drain enable, GPIO4.
			0*	DISABLED (read-write) Open Drain disabled
			1	ENABLED (read-write) Open Drain enabled
3	ODEN3	R/W		Open Drain enable, GPIO3.
			0*	DISABLED (read-write) Open Drain disabled
			1	ENABLED (read-write) Open Drain enabled
2	ODEN2	R/W		Open Drain enable, GPIO2.
			0*	DISABLED (read-write) Open Drain disabled
			1	ENABLED (read-write) Open Drain enabled
1	ODEN1	R/W		Open Drain enable, GPIO1.
			0*	DISABLED (read-write) Open Drain disabled
			1	ENABLED (read-write) Open Drain enabled
0	ODEN0	R/W		Open Drain enable, GPIO0.
			0*	DISABLED (read-write) Open Drain disabled
			1	ENABLED (read-write) Open Drain enabled

12.1.46 GPIO\_OUT register

GPIO output

Table 140. GPIO\_OUT register - GPIO output (address 802h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0

Table 140. GPIO\_OUT register - GPIO output (address 802h) bit allocation...continued

Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 141. GPIO\_OUT register - GPIO output (address 802h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:8	reserved	R	0h	This read-only field is reserved and always has the value 0.
7	OUT7	R/W		Set the output level of the gpio function for GPIO7.
			0*	LOW (read-write) GPIO is low
			1	HIGH (read-write) GPIO is high
6	OUT6	R/W		Set the output level of the gpio function for GPIO6.
			0*	LOW (read-write) GPIO is low
			1	HIGH (read-write) GPIO is high
5	OUT5	R/W		Set the output level of the gpio function for GPIO5.
			0*	LOW (read-write) GPIO is low
			1	HIGH (read-write) GPIO is high
4	OUT4	R/W		Set the output level of the gpio function for GPIO4.
			0*	LOW (read-write) GPIO is low
			1	HIGH (read-write) GPIO is high
3	OUT3	R/W		Set the output level of the gpio function for GPIO3.
			0*	LOW (read-write) GPIO is low
			1	HIGH (read-write) GPIO is high
2	OUT2	R/W		Set the output level of the gpio function for GPIO2.
			0*	LOW (read-write) GPIO is low
			1	HIGH (read-write) GPIO is high
1	OUT1	R/W		Set the output level of the gpio function for GPIO1.
			0*	LOW (read-write) GPIO is low
			1	HIGH (read-write) GPIO is high
0	OUT0	R/W		Set the output level of the gpio function for GPIO0.
			0*	LOW (read-write) GPIO is low
			1	HIGH (read-write) GPIO is high

12.1.47 GPIO\_IN register

GPIO input

Table 142. GPIO\_IN register - GPIO input (address 804h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	HIGHDET7	HIGHDET6	HIGHDET5	HIGHDET4	HIGHDET3	HIGHDET2	HIGHDET1	HIGHDET0
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	IN7	IN6	IN5	IN4	IN3	IN2	IN1	IN0
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 143. GPIO\_IN register - GPIO input (address 804h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15	HIGHDET7	R		High value on GPIO7. Read clears bit.
			0*	NO_HIGH (read) No high level observed
			1	HIGH (read) High level observed.
14	HIGHDET6	R		High value on GPIO6. Read clears bit.
			0*	NO_HIGH (read) No high level observed
			1	HIGH (read) High level observed.
13	HIGHDET5	R		High value on GPIO5. Read clears bit.
			0*	NO_HIGH (read) No high level observed
			1	HIGH (read) High level observed.
12	HIGHDET4	R		High value on GPIO4. Read clears bit.
			0*	NO_HIGH (read) No high level observed
			1	HIGH (read) High level observed.
11	HIGHDET3	R		High value on GPIO3. Read clears bit.
			0*	NO_HIGH (read) No high level observed
			1	HIGH (read) High level observed.
10	HIGHDET2	R		High value on GPIO2. Read clears bit.
			0*	NO_HIGH (read) No high level observed
			1	HIGH (read) High level observed.
9	HIGHDET1	R		High value on GPIO1. Read clears bit.
			0*	NO_HIGH (read) No high level observed
			1	HIGH (read) High level observed.
8	HIGHDET0	R		High value on GPIO0. Read clears bit.
			0*	NO_HIGH (read) No high level observed
			1	HIGH (read) High level observed.
7	IN7	R		Read the level of the gpio function of GPIO7.
			0*	LOW (read) GPIO is low

Table 143. GPIO\_IN register - GPIO input (address 804h)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
			1	HIGH (read) GPIO is high
6	IN6	R		Read the level of the gpio function of GPIO6.
			0*	LOW (read) GPIO is low
			1	HIGH (read) GPIO is high
5	IN5	R		Read the level of the gpio function of GPIO5.
			0*	LOW (read) GPIO is low
			1	HIGH (read) GPIO is high
4	IN4	R		Read the level of the gpio function of GPIO4.
			0*	LOW (read) GPIO is low
			1	HIGH (read) GPIO is high
3	IN3	R		Read the level of the gpio function of GPIO3.
			0*	LOW (read) GPIO is low
			1	HIGH (read) GPIO is high
2	IN2	R		Read the level of the gpio function of GPIO2.
			0*	LOW (read) GPIO is low
			1	HIGH (read) GPIO is high
1	IN1	R		Read the level of the gpio function of GPIO1.
			0*	LOW (read) GPIO is low
			1	HIGH (read) GPIO is high
0	IN0	R		Read the level of the gpio function of GPIO0.
			0*	LOW (read) GPIO is low
			1	HIGH (read) GPIO is high

12.1.48 I2C\_CFG register

I2C configuration

Table 144. I2C\_CFG register - I2C configuration (address C00h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	reserved					CLKSEL		EN
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R/W	R/W	R/W

Table 145. I2C\_CFG register - I2C configuration (address C00h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:3	reserved	R	0h	This read-only field is reserved and always has the value 0.
2:1	CLKSEL	R/W		I <sup>2</sup> C-bus clock selection
			00*	F_100k (read-write) Clock is 100 kHz
			01	F_400k (read-write) Clock is 400 kHz
			10	F_1000k (read-write) Clock is 1000 kHz
			11	RESERVED (read-write) Reserved. Do not use.
0	EN	R/W		Enable I <sup>2</sup> C-bus interface. If the I <sup>2</sup> C-bus interface is disabled while it is active, a stop condition is created and the bus is released. When enabling this bit the GPIO to which the I <sup>2</sup> C-bus lines are connected are switched to the I <sup>2</sup> C-bus function (input receiver active and open-drain output function).
			0*	DISABLED (read-write) Interface disabled
			1	ENABLED (read-write) Interface enabled

### 12.1.49 I2C\_CTRL register

#### I2C control

Table 146. I2C\_CTRL register - I2C control (address C01h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved		RDAFTER					
Reset	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Bit	7	6	5	4	3	2	1	0
Symbol	reserved	STPAFTER	START					
Reset	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 147. I2C\_CTRL register - I2C control (address C01h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:14	reserved	R	0h	This read-only field is reserved and always has the value 0.
13:8	RDAFTER	R/W		Switch to read after <b>RDAFTER</b> bytes. Repeats the start condition after byte <b>RDAFTER</b> .
			00h*	NO_READ (read-write) No switch to read.
			01h	READ_1 (read-write) Switch to read after 1 byte
			24h	READ_36 (read-write) Switch to read after 36 bytes
			25h	RESERVED (read-write) Reserved. Do not use.
7	reserved	R	0h	This read-only field is reserved and always has the value 0.
6	STPAFTER	R/W		Send a stop condition after the last byte.
			0*	NO_STOP (read-write) No stop condition sent after last byte
			1	STOP (read-write) Stop condition sent after last byte

Table 147. I2C\_CTRL register - I2C control (address C01h)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
5:0	START	R/W	0h	Starts the I <sup>2</sup> C-bus transmission and sends <b>START</b> bytes (including Dev. Address to be transmitted/read).
			01h	SEND_1 (read-write) Send one byte
			24h	SEND_36 (read-write) Send 36 bytes
			25h	SEND_MAX (read-write) Send 36 bytes

### 12.1.50 I2C\_STAT register

#### I2C status

Table 148. I2C\_STAT register - I2C status (address C02h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved			LEN				
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	reserved				ARBLOST	NACKRCV	ACTIVE	PENDING
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 149. I2C\_STAT register - I2C status (address C02h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:14	reserved	R	0h	This read-only field is reserved and always has the value 0.
13:8	LEN	R		<b>LEN</b> bytes transferred until NACK received.
			00h*	NACK_0 (read) No bytes transmitted until NACK was received
			01h	NACK_1 (read) 1 byte transmitted until NACK was received
			24h	NACK_36 (read) 36 bytes transmitted until NACK was received
			25h	RESERVED (read) Reserved. Not used.
7:4	reserved	R	0h	This read-only field is reserved and always has the value 0.
3	ARBLOST	R		Wrong data bit
			0*	NO_FLT (read) No wrong data bits detected
			1	FAULT (read) A wrong data bit was detected
2	NACKRCV	R		NACK received
			0*	NO_NACK (read) No NACK was received
			1	NACK (read) A NACK was received
1	ACTIVE	R		I <sup>2</sup> C-bus execution pending
			0*	NO_TRX (read) No transaction is ongoing.

Table 149. I2C\_STAT register - I2C status (address C02h)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
			1	TRX (read) A transaction is ongoing (no STOP condition so far), bus is held with SCL low
0	PENDING	R		I <sup>2</sup> C-bus execution pending
			0*	NO_TRX (read) No transfer is in execution, data registers can be accessed
			1	TRX (read) A transfer is in execution, no access to the data registers is allowed

### 12.1.51 I2C\_DATA0 register

I2C data register 0

Table 150. I2C\_DATA0 register - I2C data register 0 (address C04h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	BYTE1								BYTE0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 151. I2C\_DATA0 register - I2C data register 0 (address C04h)

Bit	Symbol	Access	Value	Description
15:8	BYTE1	R/W	0h	I <sup>2</sup> C-bus data byte 1, i.e., data or subaddress
7:0	BYTE0	R/W	0h	I <sup>2</sup> C-bus data byte 0, i.e., device address

### 12.1.52 I2C\_DATA1 register

I2C data register 1

Table 152. I2C\_DATA1 register - I2C data register 1 (address C05h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	BYTE3								BYTE2							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 153. I2C\_DATA1 register - I2C data register 1 (address C05h)

Bit	Symbol	Access	Value	Description
15:8	BYTE3	R/W	0h	I <sup>2</sup> C-bus data byte 3
7:0	BYTE2	R/W	0h	I <sup>2</sup> C-bus data byte 2

### 12.1.53 I2C\_DATA2 register

I2C data register 2

Table 154. I2C\_DATA2 register - I2C data register 2 (address C06h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	BYTE5								BYTE4							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 155. I2C\_DATA2 register - I2C data register 2 (address C06h)

Bit	Symbol	Access	Value	Description
15:8	BYTE5	R/W	0h	I <sup>2</sup> C-bus data byte 5
7:0	BYTE4	R/W	0h	I <sup>2</sup> C-bus data byte 4

12.1.54 I2C\_DATA3 register

I2C data register 3

Table 156. I2C\_DATA3 register - I2C data register 3 (address C07h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	BYTE7								BYTE6							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 157. I2C\_DATA3 register - I2C data register 3 (address C07h)

Bit	Symbol	Access	Value	Description
15:8	BYTE7	R/W	0h	I <sup>2</sup> C-bus data byte 7
7:0	BYTE6	R/W	0h	I <sup>2</sup> C-bus data byte 6

12.1.55 I2C\_DATA4 register

I2C data register 4

Table 158. I2C\_DATA4 register - I2C data register 4 (address C08h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	BYTE9								BYTE8							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 159. I2C\_DATA4 register - I2C data register 4 (address C08h)

Bit	Symbol	Access	Value	Description
15:8	BYTE9	R/W	0h	I <sup>2</sup> C-bus data byte 9
7:0	BYTE8	R/W	0h	I <sup>2</sup> C-bus data byte 8



12.1.56 I2C\_DATA5 register

I2C data register 5

Table 160. I2C\_DATA5 register - I2C data register 5 (address C09h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	BYTE11								BYTE10							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 161. I2C\_DATA5 register - I2C data register 5 (address C09h)

Bit	Symbol	Access	Value	Description
15:8	BYTE11	R/W	0h	I <sup>2</sup> C-bus data byte 11
7:0	BYTE10	R/W	0h	I <sup>2</sup> C-bus data byte 10

12.1.57 I2C\_DATA6 register

I2C data register 6

Table 162. I2C\_DATA6 register - I2C data register 6 (address C0Ah) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	BYTE13								BYTE12							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 163. I2C\_DATA6 register - I2C data register 6 (address C0Ah)

Bit	Symbol	Access	Value	Description
15:8	BYTE13	R/W	0h	I <sup>2</sup> C-bus data byte 13
7:0	BYTE12	R/W	0h	I <sup>2</sup> C-bus data byte 12

12.1.58 I2C\_DATA7 register

I2C data register 7

Table 164. I2C\_DATA7 register - I2C data register 7 (address C0Bh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	BYTE15								BYTE14							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 165. I2C\_DATA7 register - I2C data register 7 (address C0Bh)

Bit	Symbol	Access	Value	Description
15:8	BYTE15	R/W	0h	I <sup>2</sup> C-bus data byte 15
7:0	BYTE14	R/W	0h	I <sup>2</sup> C-bus data byte 14

12.1.59 I2C\_DATA8 register

I2C data register 8

Table 166. I2C\_DATA8 register - I2C data register 8 (address C0Ch) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	BYTE17								BYTE16							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 167. I2C\_DATA8 register - I2C data register 8 (address C0Ch)

Bit	Symbol	Access	Value	Description
15:8	BYTE17	R/W	0h	I <sup>2</sup> C-bus data byte 17
7:0	BYTE16	R/W	0h	I <sup>2</sup> C-bus data byte 16

12.1.60 I2C\_DATA9 register

I2C data register 9

Table 168. I2C\_DATA9 register - I2C data register 9 (address C0Dh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	BYTE19								BYTE18							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 169. I2C\_DATA9 register - I2C data register 9 (address C0Dh)

Bit	Symbol	Access	Value	Description
15:8	BYTE19	R/W	0h	I <sup>2</sup> C-bus data byte 19
7:0	BYTE18	R/W	0h	I <sup>2</sup> C-bus data byte 18

12.1.61 I2C\_DATA10 register

I2C data register 10

Table 170. I2C\_DATA10 register - I2C data register 10 (address C0Eh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	BYTE21								BYTE20							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 171. I2C\_DATA10 register - I2C data register 10 (address C0Eh)

Bit	Symbol	Access	Value	Description
15:8	BYTE21	R/W	0h	I <sup>2</sup> C-bus data byte 21
7:0	BYTE20	R/W	0h	I <sup>2</sup> C-bus data byte 20

12.1.62 I2C\_DATA11 register

I2C data register 11

Table 172. I2C\_DATA11 register - I2C data register 11 (address C0Fh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	BYTE23								BYTE22							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 173. I2C\_DATA11 register - I2C data register 11 (address C0Fh)

Bit	Symbol	Access	Value	Description
15:8	BYTE23	R/W	0h	I <sup>2</sup> C-bus data byte 23
7:0	BYTE22	R/W	0h	I <sup>2</sup> C-bus data byte 22

12.1.63 I2C\_DATA12 register

I2C data register 12

Table 174. I2C\_DATA12 register - I2C data register 12 (address C10h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	BYTE25								BYTE24							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 175. I2C\_DATA12 register - I2C data register 12 (address C10h)

Bit	Symbol	Access	Value	Description
15:8	BYTE25	R/W	0h	I <sup>2</sup> C-bus data byte 25
7:0	BYTE24	R/W	0h	I <sup>2</sup> C-bus data byte 24

12.1.64 I2C\_DATA13 register

I2C data register 13

Table 176. I2C\_DATA13 register - I2C data register 13 (address C11h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	BYTE27								BYTE26							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 177. I2C\_DATA13 register - I2C data register 13 (address C11h)

Bit	Symbol	Access	Value	Description
15:8	BYTE27	R/W	0h	I <sup>2</sup> C-bus data byte 27
7:0	BYTE26	R/W	0h	I <sup>2</sup> C-bus data byte 26

Table 177. I2C\_DATA13 register - I2C data register 13 (address C11h)...continued

Bit	Symbol	Access	Value	Description
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### 12.1.65 I2C\_DATA14 register

I2C data register 14

Table 178. I2C\_DATA14 register - I2C data register 14 (address C12h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	BYTE29								BYTE28							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 179. I2C\_DATA14 register - I2C data register 14 (address C12h)

Bit	Symbol	Access	Value	Description
15:8	BYTE29	R/W	0h	I <sup>2</sup> C-bus data byte 29
7:0	BYTE28	R/W	0h	I <sup>2</sup> C-bus data byte 28

### 12.1.66 I2C\_DATA15 register

I2C data register 15

Table 180. I2C\_DATA15 register - I2C data register 15 (address C13h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	BYTE31								BYTE30							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 181. I2C\_DATA15 register - I2C data register 15 (address C13h)

Bit	Symbol	Access	Value	Description
15:8	BYTE31	R/W	0h	I <sup>2</sup> C-bus data byte 31
7:0	BYTE30	R/W	0h	I <sup>2</sup> C-bus data byte 30

### 12.1.67 I2C\_DATA16 register

I2C data register 16

Table 182. I2C\_DATA16 register - I2C data register 16 (address C14h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	BYTE33								BYTE32							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 183. I2C\_DATA16 register - I2C data register 16 (address C14h)

Bit	Symbol	Access	Value	Description
15:8	BYTE33	R/W	0h	I <sup>2</sup> C-bus data byte 33
7:0	BYTE32	R/W	0h	I <sup>2</sup> C-bus data byte 32

### 12.1.68 I2C\_DATA17 register

I2C data register 17

Table 184. I2C\_DATA17 register - I2C data register 17 (address C15h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	BYTE35								BYTE34							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 185. I2C\_DATA17 register - I2C data register 17 (address C15h)

Bit	Symbol	Access	Value	Description
15:8	BYTE35	R/W	0h	I <sup>2</sup> C-bus data byte 35
7:0	BYTE34	R/W	0h	I <sup>2</sup> C-bus data byte 34

### 12.1.69 BAL\_GLOB\_CFG register

The global balancing configuration register is used to configure the balancing modes.

Table 186. BAL\_GLOB\_CFG register - Global Balancing Configuration (address 1000h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved					TEMPSRC		
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R/W	R/W	R/W
Bit	7	6	5	4	3	2	1	0
Symbol	reserved		CCMBALEN	TEMPMO DBALEN	GLOBUV1 BALEN	CHUV0 BALEN	TMRBALEN	BALEN
Reset	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Table 187. BAL\_GLOB\_CFG register - Global Balancing Configuration (address 1000h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:11	reserved	R	0h	This read-only field is reserved and always has the value 0.
10:8	TEMPSRC	R/W		Selects the source channel (AINx) for temperature modulated balancing. The MSB is ignored.
			000*	AIN0 (read-write) Selects AIN0 as source for temperature measurement.
			001	AIN1 (read-write) Selects AIN1 as source for temperature measurement.

Table 187. BAL\_GLOB\_CFG register - Global Balancing Configuration (address 1000h)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
			010	AIN2 (read-write) Selects AIN2 as source for temperature measurement.
			011	AIN3 (read-write) Selects AIN3 as source for temperature measurement.
7:6	reserved	R	0h	This read-only field is reserved and always has the value 0.
5	CCMBALEN	R/W		Enables the constant current balancing. When active the product adapts automatically the PWM duty cycle of the activated balancing channels based on their primary periodic measurement results to limit the balancing current variation due to cell voltage variation.
			0*	NOCCM (read-write) Constant Current Balancing is not active.
			1	CCM (read-write) Constant Current Balancing is active.
4	TEMPMODBALEN	R/W		Enables the temperature modulated balancing. After an over-temperature condition the balancing is halted until an under-temperature condition is detected.
			0*	NOTEMPMOD (read-write) Balancing is not temperature modulated.
			1	TEMPMOD (read-write) Balancing is temperature modulated.
3	GLOBUV1BALEN	R/W		Enables the Global undervoltage based balancing feature.
			0*	INDEPENDENT (read-write) Balancing is independent of the global undervoltage threshold.
			1	STOP (read-write) Balancing for all cells stops once the global undervoltage threshold is reached by any cell.
2	CHUV0BALEN	R/W		Enables the voltage based balancing for the individual channel. Balancing stops once each individual channel reaches the under-voltage threshold.
			0*	INDEPENDENT (read-write) Balancing is independent of the cell undervoltage threshold.
			1	STOP (read-write) Balancing for the individual cells stops once the cell undervoltage threshold is reached.
1	TMRBALEN	R/W		Enables the timer based balancing feature. All channel individual counters are stopped if zero.
			0*	INDEPENDENT (read-write) Balancing is independent of the cell balancing timer.
			1	STOP (read-write) Balancing for all cells will be stopped when cell balancing timer expires.
0	BALEN	R/W		Enables the balancing activity. This bit is cleared in case of a balancing timeout or if an enabled global under-voltage condition is reached. All channel individual counters are stopped if zero. The emergency discharge works without setting this bit.
			0*	DISABLED (read-write) Balancing is disabled.
			1	ENABLED (read-write) Balancing is enabled.

### 12.1.70 BAL\_GLOB\_TO\_TMR register

The Global Balancing timeout timer register is used to configure the maximum balancing time for all balancing activities to make sure that in case of fault the balancing switches are switched OFF.

Table 188. BAL\_GLOB\_TO\_TMR register - Global Balancing Timeout (address 1001h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	TOTIME															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 189. BAL\_GLOB\_TO\_TMR register - Global Balancing Timeout (address 1001h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:0	TOTIME	R/W		Balancing timeout value, used for normal balancing. The value of this field represents the current counter value when read. The BAL_GLOB_CFG.BALEN is cleared when zero is reached. The counter saturates at zero. It counts down regardless of the balancing enable state as long as its value is non-zero. <b>TOTIME</b> * 10 seconds
			0000h*	EXPIRED (read-write) Balancing time is expired
			0001h	BALTIME (read-write) Balancing time is set to BALTIME * 10 seconds
			FFFFh	MAX (read-write) Maximum balancing time = 655350 seconds = approximately 182 hours = approximately 7.6 days

12.1.71 BAL\_CH\_CFG0 register

Balancing channel individual enable channel 0 - 15

Table 190. BAL\_CH\_CFG0 register - balancing channel individual enable channel 0 - 15 (address 1002h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	CHEN15	CHEN14	CHEN13	CHEN12	CHEN11	CHEN10	CHEN9	CHEN8
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	7	6	5	4	3	2	1	0
Symbol	CHEN7	CHEN6	CHEN5	CHEN4	CHEN3	CHEN2	CHEN1	CHEN0
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 191. BAL\_CH\_CFG0 register - balancing channel individual enable channel 0 - 15 (address 1002h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15	CHEN15	R/W		Enable balancing for channel 15. The bit is cleared by the device in case of <ul style="list-style-type: none"><li>a detected over-current condition</li><li>a enabled and detected under-voltage condition</li><li>a timeout of the channel timer</li></ul>
			0*	DISABLED (read-write) Balancing for Channel 15 is disabled. The balancing timer for Channel 15 is stopped.

Table 191. BAL\_CH\_CFG0 register - balancing channel individual enable channel 0 - 15 (address 1002h)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
			1	ENABLED (read-write) Balancing for Channel 15 is enabled.
14	CHEN14	R/W		Enable balancing for channel 14. The bit is cleared by the device in case of <ul style="list-style-type: none"> <li>a detected over-current condition</li> <li>a enabled and detected under-voltage condition</li> <li>a timeout of the channel timer</li> </ul>
			0*	DISABLED (read-write) Balancing for Channel 14 is disabled. The balancing timer for Channel 14 is stopped.
			1	ENABLED (read-write) Balancing for Channel 15 is enabled.
13	CHEN13	R/W		Enable balancing for channel 13. The bit is cleared by the device in case of <ul style="list-style-type: none"> <li>a detected over-current condition</li> <li>a enabled and detected under-voltage condition</li> <li>a timeout of the channel timer</li> </ul>
			0*	DISABLED (read-write) Balancing for Channel 13 is disabled. The balancing timer for Channel 13 is stopped.
			1	ENABLED (read-write) Balancing for Channel 13 is enabled.
12	CHEN12	R/W		Enable balancing for channel 12. The bit is cleared by the device in case of <ul style="list-style-type: none"> <li>a detected over-current condition</li> <li>a enabled and detected under-voltage condition</li> <li>a timeout of the channel timer</li> </ul>
			0*	DISABLED (read-write) Balancing for Channel 12 is disabled. The balancing timer for Channel 12 is stopped.
			1	ENABLED (read-write) Balancing for Channel 12 is enabled.
11	CHEN11	R/W		Enable balancing for channel 11. The bit is cleared by the device in case of <ul style="list-style-type: none"> <li>a detected over-current condition</li> <li>a enabled and detected under-voltage condition</li> <li>a timeout of the channel timer</li> </ul>
			0*	DISABLED (read-write) Balancing for Channel 11 is disabled. The balancing timer for Channel 11 is stopped.
			1	ENABLED (read-write) Balancing for Channel 11 is enabled.
10	CHEN10	R/W		Enable balancing for channel 10. The bit is cleared by the device in case of <ul style="list-style-type: none"> <li>a detected over-current condition</li> <li>a enabled and detected under-voltage condition</li> <li>a timeout of the channel timer</li> </ul>
			0*	DISABLED (read-write) Balancing for Channel 10 is disabled. The balancing timer for Channel 10 is stopped.
			1	ENABLED (read-write) Balancing for Channel 10 is enabled.
9	CHEN9	R/W		Enable balancing for channel 9. The bit is cleared by the device in case of <ul style="list-style-type: none"> <li>a detected over-current condition</li> <li>a enabled and detected under-voltage condition</li> <li>a timeout of the channel timer</li> </ul>
			0*	DISABLED (read-write) Balancing for Channel 9 is disabled. The balancing timer for Channel 9 is stopped.



Table 191. BAL\_CH\_CFG0 register - balancing channel individual enable channel 0 - 15 (address 1002h)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
			1	ENABLED (read-write) Balancing for Channel 9 is enabled.
8	CHEN8	R/W		Enable balancing for channel 8. The bit is cleared by the device in case of <ul style="list-style-type: none"> <li>a detected over-current condition</li> <li>a enabled and detected under-voltage condition</li> <li>a timeout of the channel timer</li> </ul>
			0*	DISABLED (read-write) Balancing for Channel 8 is disabled. The balancing timer for Channel 8 is stopped.
			1	ENABLED (read-write) Balancing for Channel 8 is enabled.
7	CHEN7	R/W		Enable balancing for channel 7. The bit is cleared by the device in case of <ul style="list-style-type: none"> <li>a detected over-current condition</li> <li>a enabled and detected under-voltage condition</li> <li>a timeout of the channel timer</li> </ul>
			0*	DISABLED (read-write) Balancing for Channel 7 is disabled. The balancing timer for Channel 7 is stopped.
			1	ENABLED (read-write) Balancing for Channel 7 is enabled.
6	CHEN6	R/W		Enable balancing for channel 6. The bit is cleared by the device in case of <ul style="list-style-type: none"> <li>a detected over-current condition</li> <li>a enabled and detected under-voltage condition</li> <li>a timeout of the channel timer</li> </ul>
			0*	DISABLED (read-write) Balancing for Channel 6 is disabled. The balancing timer for Channel 6 is stopped.
			1	ENABLED (read-write) Balancing for Channel 6 is enabled.
5	CHEN5	R/W		Enable balancing for channel 5. The bit is cleared by the device in case of <ul style="list-style-type: none"> <li>a detected over-current condition</li> <li>a enabled and detected under-voltage condition</li> <li>a timeout of the channel timer</li> </ul>
			0*	DISABLED (read-write) Balancing for Channel 5 is disabled. The balancing timer for Channel 5 is stopped.
			1	ENABLED (read-write) Balancing for Channel 5 is enabled.
4	CHEN4	R/W		Enable balancing for channel 4. The bit is cleared by the device in case of <ul style="list-style-type: none"> <li>a detected over-current condition</li> <li>a enabled and detected under-voltage condition</li> <li>a timeout of the channel timer</li> </ul>
			0*	DISABLED (read-write) Balancing for Channel 4 is disabled. The balancing timer for Channel 4 is stopped.
			1	ENABLED (read-write) Balancing for Channel 4 is enabled.
3	CHEN3	R/W		Enable balancing for channel 3. The bit is cleared by the device in case of <ul style="list-style-type: none"> <li>a detected over-current condition</li> <li>a enabled and detected under-voltage condition</li> <li>a timeout of the channel timer</li> </ul>
			0*	DISABLED (read-write) Balancing for Channel 3 is disabled. The balancing timer for Channel 3 is stopped.

Table 191. BAL\_CH\_CFG0 register - balancing channel individual enable channel 0 - 15 (address 1002h)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
			1	ENABLED (read-write) Balancing for Channel 3 is enabled.
2	CHEN2	R/W		Enable balancing for channel 2. The bit is cleared by the device in case of <ul style="list-style-type: none"> <li>a detected over-current condition</li> <li>a enabled and detected under-voltage condition</li> <li>a timeout of the channel timer</li> </ul>
			0*	DISABLED (read-write) Balancing for Channel 2 is disabled. The balancing timer for Channel 2 is stopped.
			1	ENABLED (read-write) Balancing for Channel 2 is enabled.
1	CHEN1	R/W		Enable balancing for channel 1. The bit is cleared by the device in case of <ul style="list-style-type: none"> <li>a detected over-current condition</li> <li>a enabled and detected under-voltage condition</li> <li>a timeout of the channel timer</li> </ul>
			0*	DISABLED (read-write) Balancing for Channel 1 is disabled. The balancing timer for Channel 1 is stopped.
			1	ENABLED (read-write) Balancing for Channel 1 is enabled.
0	CHEN0	R/W		Enable balancing for channel 0. The bit is cleared by the device in case of <ul style="list-style-type: none"> <li>a detected over-current condition</li> <li>a enabled and detected under-voltage condition</li> <li>a timeout of the channel timer</li> </ul>
			0*	DISABLED (read-write) Balancing for Channel 0 is disabled. The balancing timer for Channel 0 is stopped.
			1	ENABLED (read-write) Balancing for Channel 0 is enabled.

### 12.1.72 BAL\_CH\_CFG1 register

Balancing channel individual enable channel 16 - 17

Table 192. BAL\_CH\_CFG1 register - balancing channel individual enable channel 16 - 17 (address 1003h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	reserved						CHEN17	CHEN16
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R/W	R/W

Table 193. BAL\_CH\_CFG1 register - balancing channel individual enable channel 16 - 17 (address 1003h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:2	reserved	R	0h	This read-only field is reserved and always has the value 0.
1	CHEN17	R/W		Enable balancing for channel 17. The bit is cleared by the device in case of <ul style="list-style-type: none"> <li>a detected over-current condition</li> <li>a enabled and detected under-voltage condition</li> <li>a timeout of the channel timer</li> </ul>
			0*	DISABLED (read-write) Balancing for Channel 17 is disabled. The balancing timer for Channel 17 is stopped.
			1	ENABLED (read-write) Balancing for Channel 17 is enabled.
0	CHEN16	R/W		Enable balancing for channel 16. The bit is cleared by the device in case of <ul style="list-style-type: none"> <li>a detected over-current condition</li> <li>a enabled and detected under-voltage condition</li> <li>a timeout of the channel timer</li> </ul>
			0*	DISABLED (read-write) Balancing for Channel 16 is disabled. The balancing timer for Channel 16 is stopped.
			1	ENABLED (read-write) Balancing for Channel 16 is enabled.

## 12.1.73 BAL\_PRE\_TMR register

prebalancing timer

Table 194. BAL\_PRE\_TMR register - prebalancing timer (address 1004h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	PREBALTIME															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 195. BAL\_PRE\_TMR register - prebalancing timer (address 1004h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:0	PREBALTIME	R/W		Downcounter which runs if BALEN is set. Inhibits the balancing and holds the individual channel timer. The value of this field represents the current counter value when read. The counting saturates at 0 and activates the balancing. The BAL_GLOB_TO_TMR is not influenced by this timer. <b>PREBALTIME</b> * 10 seconds
			0000h*	EXPIRED (read-write) prebalancing time is expired.
			0001h	PREBAL (read-write) prebalancing time is set to PREBAL * 10 seconds
			FFFFh	MAX (read-write) Maximum prebalancing time = 655350 seconds = approximately 182 hours = approximately 7.6 days

## 12.1.74 BAL\_AUTO\_DISCHRG\_CTRL register

Emergency discharge enable

Table 196. BAL\_AUTO\_DISCHRG\_CTRL register - emergency discharge enable (address 1005h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	KEY															
Reset	0	0	1	0	0	0	0	1	0	1	0	1	0	0	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 197. BAL\_AUTO\_DISCHRG\_CTRL register - emergency discharge enable (address 1005h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:0	KEY	R/W		Key for enabling auto discharge. After enabling with <b>DEADh</b> the discharge will continue until disable key <b>2152h</b> is received. <b>Other</b> values will be ignored.
			0001h	OTHERS (read-write) Other values will be ignored.
			2152h*	DISABLED (read-write) Disable key for auto discharge.
			DEADh	ENABLED (read-write) Enable key for auto discharge.

## 12.1.75 BAL\_SWITCH\_MON\_CFG0 register

Balancing switch monitoring enable

Table 198. BAL\_SWITCH\_MON\_CFG0 register - balancing switch monitoring enable (address 1006h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	MONEN15	MONEN14	MONEN13	MONEN12	MONEN11	MONEN10	MONEN9	MONEN8
Reset	1	1	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	7	6	5	4	3	2	1	0
Symbol	MONEN7	MONEN6	MONEN5	MONEN4	MONEN3	MONEN2	MONEN1	MONEN0
Reset	1	1	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 199. BAL\_SWITCH\_MON\_CFG0 register - balancing switch monitoring enable (address 1006h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15	MONEN15	R/W		Enable balancing switch monitoring for channel 15.
			0	DISABLED (read-write) Balancing switch monitoring for Channel 15 is disabled.
			1*	ENABLED (read-write) Balancing switch monitoring for Channel 15 is enabled.
14	MONEN14	R/W		Enable balancing switch monitoring for channel 14.

Table 199. BAL\_SWITCH\_MON\_CFG0 register - balancing switch monitoring enable (address 1006h)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
			0	DISABLED (read-write) Balancing switch monitoring for Channel 14 is disabled.
			1*	ENABLED (read-write) Balancing switch monitoring for Channel 14 is enabled.
13	MONEN13	R/W		Enable balancing switch monitoring for channel 13.
			0	DISABLED (read-write) Balancing switch monitoring for Channel 13 is disabled.
			1*	ENABLED (read-write) Balancing switch monitoring for Channel 13 is enabled.
12	MONEN12	R/W		Enable balancing switch monitoring for channel 12.
			0	DISABLED (read-write) Balancing switch monitoring for Channel 12 is disabled.
			1*	ENABLED (read-write) Balancing switch monitoring for Channel 12 is enabled.
11	MONEN11	R/W		Enable balancing switch monitoring for channel 11.
			0	DISABLED (read-write) Balancing switch monitoring for Channel 11 is disabled.
			1*	ENABLED (read-write) Balancing switch monitoring for Channel 11 is enabled.
10	MONEN10	R/W		Enable balancing switch monitoring for channel 10.
			0	DISABLED (read-write) Balancing switch monitoring for Channel 10 is disabled.
			1*	ENABLED (read-write) Balancing switch monitoring for Channel 10 is enabled.
9	MONEN9	R/W		Enable balancing switch monitoring for channel 9.
			0	DISABLED (read-write) Balancing switch monitoring for Channel 9 is disabled.
			1*	ENABLED (read-write) Balancing switch monitoring for Channel 9 is enabled.
8	MONEN8	R/W		Enable balancing switch monitoring for channel 8.
			0	DISABLED (read-write) Balancing switch monitoring for Channel 8 is disabled.
			1*	ENABLED (read-write) Balancing switch monitoring for Channel 8 is enabled.
7	MONEN7	R/W		Enable balancing switch monitoring for channel 7.
			0	DISABLED (read-write) Balancing switch monitoring for Channel 7 is disabled.
			1*	ENABLED (read-write) Balancing switch monitoring for Channel 7 is enabled.
6	MONEN6	R/W		Enable balancing switch monitoring for channel 6.
			0	DISABLED (read-write) Balancing switch monitoring for Channel 6 is disabled.
			1*	ENABLED (read-write) Balancing switch monitoring for Channel 6 is enabled.
5	MONEN5	R/W		Enable balancing switch monitoring for channel 5.

Table 199. BAL\_SWITCH\_MON\_CFG0 register - balancing switch monitoring enable (address 1006h)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
			0	DISABLED (read-write) Balancing switch monitoring for Channel 5 is disabled.
			1*	ENABLED (read-write) Balancing switch monitoring for Channel 5 is enabled.
4	MONEN4	R/W		Enable balancing switch monitoring for channel 4.
			0	DISABLED (read-write) Balancing switch monitoring for Channel 4 is disabled.
			1*	ENABLED (read-write) Balancing switch monitoring for Channel 4 is enabled.
3	MONEN3	R/W		Enable balancing switch monitoring for channel 3.
			0	DISABLED (read-write) Balancing switch monitoring for Channel 3 is disabled.
			1*	ENABLED (read-write) Balancing switch monitoring for Channel 3 is enabled.
2	MONEN2	R/W		Enable balancing switch monitoring for channel 2.
			0	DISABLED (read-write) Balancing switch monitoring for Channel 2 is disabled.
			1*	ENABLED (read-write) Balancing switch monitoring for Channel 2 is enabled.
1	MONEN1	R/W		Enable balancing switch monitoring for channel 1.
			0	DISABLED (read-write) Balancing switch monitoring for Channel 1 is disabled.
			1*	ENABLED (read-write) Balancing switch monitoring for Channel 1 is enabled.
0	MONEN0	R/W		Enable balancing switch monitoring for channel 0.
			0	DISABLED (read-write) Balancing switch monitoring for Channel 0 is disabled.
			1*	ENABLED (read-write) Balancing switch monitoring for Channel 0 is enabled.

## 12.1.76 BAL\_SWITCH\_MON\_CFG1 register

Balancing switch monitoring enable

Table 200. BAL\_SWITCH\_MON\_CFG1 register - balancing switch monitoring enable (address 1007h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	reserved						MONEN17	MONEN16
Reset	0	0	0	0	0	0	1	1
Access	R	R	R	R	R	R	R/W	R/W

**Table 201. BAL\_SWITCH\_MON\_CFG1 register - balancing switch monitoring enable (address 1007h)**

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:2	reserved	R	0h	This read-only field is reserved and always has the value 0.
1	MONEN17	R/W		Enable balancing switch monitoring for channel 17.
			0	DISABLED (read-write) Balancing switch monitoring for Channel 17 is disabled.
			1*	ENABLED (read-write) Balancing switch monitoring for Channel 17 is enabled.
0	MONEN16	R/W		Enable balancing switch monitoring for channel 16.
			0	DISABLED (read-write) Balancing switch monitoring for Channel 16 is disabled.
			1*	ENABLED (read-write) Balancing switch monitoring for Channel 16 is enabled.

### 12.1.77 FULL\_PWM\_CYCLE\_VOLTAGE register

Full PWM cycle voltage

**Table 202. FULL\_PWM\_CYCLE\_VOLTAGE register - full PWM cycle voltage (address 1008h) bit allocation**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	FULLPWM															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**Table 203. FULL\_PWM\_CYCLE\_VOLTAGE register - full PWM cycle voltage (address 1008h)**

Bit	Symbol	Access	Value	Description
15:0	FULLPWM	R/W	0h	FULL PWM cycle voltage setting to set the cell voltage on which the balancing is operating at the maximum current.( ie : min operating cell voltage in the application) Setting format is the same than cell voltage measurement.

### 12.1.78 BAL\_CH\_UV0\_STAT0 register

Channel undervoltage balancing status channel 0 - 15

**Table 204. BAL\_CH\_UV0\_STAT0 register - channel undervoltage balancing status channel 0 - 15 (address 1009h) bit allocation**

Bit	15	14	13	12	11	10	9	8
Symbol	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

**Table 205. BAL\_CH\_UV0\_STAT0 register - channel under-voltage balancing status channel 0 - 15 (address 1009h)***Legend: \* reset value*

Bit	Symbol	Access	Value	Description
15	CH15	R		Status bit, if a channel under-voltage condition was the reason for disabling individual balancing of channel 15. Read clears bit.
			0*	NOUV (read) Balancing of channel 15 was not disabled due to under-voltage condition.
			1	UV (read) Balancing of channel 15 was disabled due to under-voltage condition.
14	CH14	R		Status bit, if a channel under-voltage condition was the reason for disabling individual balancing of channel 14. Read clears bit.
			0*	NOUV (read) Balancing of channel 14 was not disabled due to under-voltage condition.
			1	UV (read) Balancing of channel 14 was disabled due to under-voltage condition.
13	CH13	R		Status bit, if a channel under-voltage condition was the reason for disabling individual balancing of channel 13. Read clears bit.
			0*	NOUV (read) Balancing of channel 13 was not disabled due to under-voltage condition.
			1	UV (read) Balancing of channel 13 was disabled due to under-voltage condition.
12	CH12	R		Status bit, if a channel under-voltage condition was the reason for disabling individual balancing of channel 12. Read clears bit.
			0*	NOUV (read) Balancing of channel 12 was not disabled due to under-voltage condition.
			1	UV (read) Balancing of channel 12 was disabled due to under-voltage condition.
11	CH11	R		Status bit, if a channel under-voltage condition was the reason for disabling individual balancing of channel 11. Read clears bit.
			0*	NOUV (read) Balancing of channel 11 was not disabled due to under-voltage condition.
			1	UV (read) Balancing of channel 11 was disabled due to under-voltage condition.
10	CH10	R		Status bit, if a channel under-voltage condition was the reason for disabling individual balancing of channel 10. Read clears bit.
			0*	NOUV (read) Balancing of channel 10 was not disabled due to under-voltage condition.
			1	UV (read) Balancing of channel 10 was disabled due to under-voltage condition.
9	CH9	R		Status bit, if a channel under-voltage condition was the reason for disabling individual balancing of channel 9. Read clears bit.
			0*	NOUV (read) Balancing of channel 9 was not disabled due to under-voltage condition.
			1	UV (read) Balancing of channel 9 was disabled due to under-voltage condition.
8	CH8	R		Status bit, if a channel under-voltage condition was the reason for disabling individual balancing of channel 8. Read clears bit.
			0*	NOUV (read) Balancing of channel 8 was not disabled due to under-voltage condition.



**Table 205. BAL\_CH\_UV0\_STAT0 register - channel under-voltage balancing status channel 0 - 15 (address 1009h)...***continued*

Legend: \* reset value

Bit	Symbol	Access	Value	Description
			1	UV (read) Balancing of channel 8 was disabled due to under-voltage condition.
7	CH7	R		Status bit, if a channel under-voltage condition was the reason for disabling individual balancing of channel 7. Read clears bit.
			0*	NOUV (read) Balancing of channel 7 was not disabled due to under-voltage condition.
			1	UV (read) Balancing of channel 7 was disabled due to under-voltage condition.
6	CH6	R		Status bit, if a channel under-voltage condition was the reason for disabling individual balancing of channel 6. Read clears bit.
			0*	NOUV (read) Balancing of channel 6 was not disabled due to under-voltage condition.
			1	UV (read) Balancing of channel 6 was disabled due to under-voltage condition.
5	CH5	R		Status bit, if a channel under-voltage condition was the reason for disabling individual balancing of channel 5. Read clears bit.
			0*	NOUV (read) Balancing of channel 5 was not disabled due to under-voltage condition.
			1	UV (read) Balancing of channel 5 was disabled due to under-voltage condition.
4	CH4	R		Status bit, if a channel under-voltage condition was the reason for disabling individual balancing of channel 4. Read clears bit.
			0*	NOUV (read) Balancing of channel 4 was not disabled due to under-voltage condition.
			1	UV (read) Balancing of channel 4 was disabled due to under-voltage condition.
3	CH3	R		Status bit, if a channel under-voltage condition was the reason for disabling individual balancing of channel 3. Read clears bit.
			0*	NOUV (read) Balancing of channel 3 was not disabled due to under-voltage condition.
			1	UV (read) Balancing of channel 3 was disabled due to under-voltage condition.
2	CH2	R		Status bit, if a channel under-voltage condition was the reason for disabling individual balancing of channel 2. Read clears bit.
			0*	NOUV (read) Balancing of channel 2 was not disabled due to under-voltage condition.
			1	UV (read) Balancing of channel 2 was disabled due to under-voltage condition.
1	CH1	R		Status bit, if a channel under-voltage condition was the reason for disabling individual balancing of channel 1. Read clears bit.
			0*	NOUV (read) Balancing of channel 1 was not disabled due to under-voltage condition.
			1	UV (read) Balancing of channel 1 was disabled due to under-voltage condition.
0	CH0	R		Status bit, if a channel under-voltage condition was the reason for disabling individual balancing of channel 0. Read clears bit.

**Table 205. BAL\_CH\_UV0\_STAT0 register - channel under-voltage balancing status channel 0 - 15 (address 1009h)...***continued*

Legend: \* reset value

Bit	Symbol	Access	Value	Description
			0*	NOUV (read) Balancing of channel 0 was not disabled due to under-voltage condition.
			1	UV (read) Balancing of channel 0 was disabled due to under-voltage condition.

### 12.1.79 BAL\_CH\_UV0\_STAT1 register

Channel undervoltage balancing status channel 16 - 17

**Table 206. BAL\_CH\_UV0\_STAT1 register - channel undervoltage balancing status channel 16 - 17 (address 100Ah) bit allocation**

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	reserved						CH17	CH16
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

**Table 207. BAL\_CH\_UV0\_STAT1 register - channel under-voltage balancing status channel 16 - 17 (address 100Ah)**

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:2	reserved	R	0h	This read-only field is reserved and always has the value 0.
1	CH17	R		Status bit, if a channel under-voltage condition was the reason for disabling individual balancing of channel 17. Read clears bit.
			0*	NOUV (read) Balancing of channel 17 was not disabled due to under-voltage condition.
			1	UV (read) Balancing of channel 17 was disabled due to under-voltage condition.
0	CH16	R		Status bit, if a channel under-voltage condition was the reason for disabling individual balancing of channel 16. Read clears bit.
			0*	NOUV (read) Balancing of channel 16 was not disabled due to under-voltage condition.
			1	UV (read) Balancing of channel 16 was disabled due to under-voltage condition.

## 12.1.80 BAL\_GLOB\_UV1\_STAT0 register

Global undervoltage balancing status channel 0 - 15

Table 208. BAL\_GLOB\_UV1\_STAT0 register - global undervoltage balancing status channel 0 - 15 (address 100Bh) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 209. BAL\_GLOB\_UV1\_STAT0 register - global under-voltage balancing status channel 0 - 15 (address 100Bh)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15	CH15	R		Status bit, if a global under-voltage of channel 15 condition was the reason for disabling the global balancing. Read clears bit.
			0*	NOUV (read) Balancing was not disabled due to global under-voltage condition of channel 15.
			1	UV (read) Balancing was disabled due to global under-voltage condition of channel 15.
14	CH14	R		Status bit, if a global under-voltage of channel 14 condition was the reason for disabling the global balancing. Read clears bit.
			0*	NOUV (read) Balancing was not disabled due to global under-voltage condition of channel 14.
			1	UV (read) Balancing was disabled due to global under-voltage condition of channel 14.
13	CH13	R		Status bit, if a global under-voltage of channel 13 condition was the reason for disabling the global balancing. Read clears bit.
			0*	NOUV (read) Balancing was not disabled due to global under-voltage condition of channel 13.
			1	UV (read) Balancing was disabled due to global under-voltage condition of channel 13.
12	CH12	R		Status bit, if a global under-voltage of channel 12 condition was the reason for disabling the global balancing. Read clears bit.
			0*	NOUV (read) Balancing was not disabled due to global under-voltage condition of channel 12.
			1	UV (read) Balancing was disabled due to global under-voltage condition of channel 12.
11	CH11	R		Status bit, if a global under-voltage of channel 11 condition was the reason for disabling the global balancing. Read clears bit.
			0*	NOUV (read) Balancing was not disabled due to global under-voltage condition of channel 11.
			1	UV (read) Balancing was disabled due to global under-voltage condition of channel 11.

**Table 209. BAL\_GLOB\_UV1\_STAT0 register - global under-voltage balancing status channel 0 - 15 (address 100Bh)...***continued*

Legend: \* reset value

Bit	Symbol	Access	Value	Description
10	CH10	R		Status bit, if a global under-voltage of channel 10 condition was the reason for disabling the global balancing. Read clears bit.
			0*	NOUV (read) Balancing was not disabled due to global under-voltage condition of channel 10.
			1	UV (read) Balancing was disabled due to global under-voltage condition of channel 10.
9	CH9	R		Status bit, if a global under-voltage of channel 9 condition was the reason for disabling the global balancing. Read clears bit.
			0*	NOUV (read) Balancing was not disabled due to global under-voltage condition of channel 9.
			1	UV (read) Balancing was disabled due to global under-voltage condition of channel 9.
8	CH8	R		Status bit, if a global under-voltage of channel 8 condition was the reason for disabling the global balancing. Read clears bit.
			0*	NOUV (read) Balancing was not disabled due to global under-voltage condition of channel 8.
			1	UV (read) Balancing was disabled due to global under-voltage condition of channel 8.
7	CH7	R		Status bit, if a global under-voltage of channel 7 condition was the reason for disabling the global balancing. Read clears bit.
			0*	NOUV (read) Balancing was not disabled due to global under-voltage condition of channel 7.
			1	UV (read) Balancing was disabled due to global under-voltage condition of channel 7.
6	CH6	R		Status bit, if a global under-voltage of channel 6 condition was the reason for disabling the global balancing. Read clears bit.
			0*	NOUV (read) Balancing was not disabled due to global under-voltage condition of channel 6.
			1	UV (read) Balancing was disabled due to global under-voltage condition of channel 6.
5	CH5	R		Status bit, if a global under-voltage of channel 5 condition was the reason for disabling the global balancing. Read clears bit.
			0*	NOUV (read) Balancing was not disabled due to global under-voltage condition of channel 5.
			1	UV (read) Balancing was disabled due to global under-voltage condition of channel 5.
4	CH4	R		Status bit, if a global under-voltage of channel 4 condition was the reason for disabling the global balancing. Read clears bit.
			0*	NOUV (read) Balancing was not disabled due to global under-voltage condition of channel 4.
			1	UV (read) Balancing was disabled due to global under-voltage condition of channel 4.
3	CH3	R		Status bit, if a global under-voltage of channel 3 condition was the reason for disabling the global balancing. Read clears bit.
			0*	NOUV (read) Balancing was not disabled due to global under-voltage condition of channel 3.

**Table 209. BAL\_GLOB\_UV1\_STAT0 register - global under-voltage balancing status channel 0 - 15 (address 100Bh)...***continued*

Legend: \* reset value

Bit	Symbol	Access	Value	Description
			1	UV (read) Balancing was disabled due to global under-voltage condition of channel 3.
2	CH2	R		Status bit, if a global under-voltage of channel 2 condition was the reason for disabling the global balancing. Read clears bit.
			0*	NOUV (read) Balancing was not disabled due to global under-voltage condition of channel 2.
			1	UV (read) Balancing was disabled due to global under-voltage condition of channel 2.
1	CH1	R		Status bit, if a global under-voltage of channel 1 condition was the reason for disabling the global balancing. Read clears bit.
			0*	NOUV (read) Balancing was not disabled due to global under-voltage condition of channel 1.
			1	UV (read) Balancing was disabled due to global under-voltage condition of channel 1.
0	CH0	R		Status bit, if a global under-voltage of channel 0 condition was the reason for disabling the global balancing. Read clears bit.
			0*	NOUV (read) Balancing was not disabled due to global under-voltage condition of channel 0.
			1	UV (read) Balancing was disabled due to global under-voltage condition of channel 0.

### 12.1.81 BAL\_GLOB\_UV1\_STAT1 register

Global undervoltage balancing status channel 16 - 17

**Table 210. BAL\_GLOB\_UV1\_STAT1 register - global undervoltage balancing status channel 16 - 17 (address 100Ch) bit allocation**

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	reserved						CH17	CH16
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

**Table 211. BAL\_GLOB\_UV1\_STAT1 register - global under-voltage balancing status channel 16 - 17 (address 100Ch)**

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:2	reserved	R	0h	This read-only field is reserved and always has the value 0.
1	CH17	R		Status bit, if a global under-voltage of channel 17 condition was the reason for disabling the global balancing. Read clears bit.

**Table 211. BAL\_GLOB\_UV1\_STAT1 register - global under-voltage balancing status channel 16 - 17 (address 100Ch)...***continued*

Legend: \* reset value

Bit	Symbol	Access	Value	Description
0	CH16	R	0*	NOUV (read) Balancing was not disabled due to global under-voltage condition of channel 17.
			1	UV (read) Balancing was disabled due to global under-voltage condition of channel 17.
				Status bit, if a global under-voltage of channel 16 condition was the reason for disabling the global balancing. Read clears bit.
			0*	NOUV (read) Balancing was not disabled due to global under-voltage condition of channel 16.
			1	UV (read) Balancing was disabled due to global under-voltage condition of channel 16.

### 12.1.82 BAL\_STAT0 register

Logical balancing channel status channel 0 - 15

**Table 212. BAL\_STAT0 register - logical balancing channel status channel 0 - 15 (address 100Dh) bit allocation**

Bit	15	14	13	12	11	10	9	8
Symbol	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

**Table 213. BAL\_STAT0 register - logical balancing channel status channel 0 - 15 (address 100Dh)**

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15	CH15	R		Balancing channel 15 status (without PWM and odd/even switching)
			0*	INACTIVE (read) Balancing for channel 15 inactive.
			1	ACTIVE (read) Balancing for channel 15 active.
14	CH14	R		Balancing channel 14 status (without PWM and odd/even switching)
			0*	INACTIVE (read) Balancing for channel 14 inactive.
			1	ACTIVE (read) Balancing for channel 14 active.
13	CH13	R		Balancing channel 13 status (without PWM and odd/even switching)
			0*	INACTIVE (read) Balancing for channel 13 inactive.
			1	ACTIVE (read) Balancing for channel 13 active.
12	CH12	R		Balancing channel 12 status (without PWM and odd/even switching)

Table 213. BAL\_STAT0 register - logical balancing channel status channel 0 - 15 (address 100Dh)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
			0*	INACTIVE (read) Balancing for channel 12 inactive.
			1	ACTIVE (read) Balancing for channel 12 active.
11	CH11	R		Balancing channel 11 status (without PWM and odd/even switching)
			0*	INACTIVE (read) Balancing for channel 11 inactive.
			1	ACTIVE (read) Balancing for channel 11 active.
10	CH10	R		Balancing channel 10 status (without PWM and odd/even switching)
			0*	INACTIVE (read) Balancing for channel 10 inactive.
			1	ACTIVE (read) Balancing for channel 10 active.
9	CH9	R		Balancing channel 9 status (without PWM and odd/even switching)
			0*	INACTIVE (read) Balancing for channel 9 inactive.
			1	ACTIVE (read) Balancing for channel 9 active.
8	CH8	R		Balancing channel 8 status (without PWM and odd/even switching)
			0*	INACTIVE (read) Balancing for channel 8 inactive.
			1	ACTIVE (read) Balancing for channel 8 active.
7	CH7	R		Balancing channel 7 status (without PWM and odd/even switching)
			0*	INACTIVE (read) Balancing for channel 7 inactive.
			1	ACTIVE (read) Balancing for channel 7 active.
6	CH6	R		Balancing channel 6 status (without PWM and odd/even switching)
			0*	INACTIVE (read) Balancing for channel 6 inactive.
			1	ACTIVE (read) Balancing for channel 6 active.
5	CH5	R		Balancing channel 5 status (without PWM and odd/even switching)
			0*	INACTIVE (read) Balancing for channel 5 inactive.
			1	ACTIVE (read) Balancing for channel 5 active.
4	CH4	R		Balancing channel 4 status (without PWM and odd/even switching)
			0*	INACTIVE (read) Balancing for channel 4 inactive.
			1	ACTIVE (read) Balancing for channel 4 active.
3	CH3	R		Balancing channel 3 status (without PWM and odd/even switching)
			0*	INACTIVE (read) Balancing for channel 3 inactive.
			1	ACTIVE (read) Balancing for channel 3 active.
2	CH2	R		Balancing channel 2 status (without PWM and odd/even switching)
			0*	INACTIVE (read) Balancing for channel 2 inactive.
			1	ACTIVE (read) Balancing for channel 2 active.

Table 213. BAL\_STAT0 register - logical balancing channel status channel 0 - 15 (address 100Dh)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
1	CH1	R		Balancing channel 1 status (without PWM and odd/even switching)
			0*	INACTIVE (read) Balancing for channel 1 inactive.
			1	ACTIVE (read) Balancing for channel 1 active.
0	CH0	R		Balancing channel 0 status (without PWM and odd/even switching)
			0*	INACTIVE (read) Balancing for channel 0 inactive.
			1	ACTIVE (read) Balancing for channel 0 active.

### 12.1.83 BAL\_STAT1 register

Logical balancing channel status channel 16 - 17

Table 214. BAL\_STAT1 register - logical balancing channel status channel 16 - 17 (address 100Eh) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	reserved						CH17	CH16
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 215. BAL\_STAT1 register - logical balancing channel status channel 16 - 17 (address 100Eh)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:2	reserved	R	0h	This read-only field is reserved and always has the value 0.
1	CH17	R		Balancing channel 17 status (without PWM and odd/even switching)
			0*	INACTIVE (read) Balancing for channel 17 inactive.
			1	ACTIVE (read) Balancing for channel 17 active.
0	CH16	R		Balancing channel 16 status (without PWM and odd/even switching)
			0*	INACTIVE (read) Balancing for channel 16 inactive.
			1	ACTIVE (read) Balancing for channel 16 active.



## 12.1.84 BAL\_STAT2 register

Balancing status

Table 216. BAL\_STAT2 register - balancing status (address 100Fh) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	BALRDY	BALPRO TFLG	reserved					
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	reserved				BALPROT	AUTODI SCHRG	TEMPBA LINHIBIT	PREBALTMR
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 217. BAL\_STAT2 register - balancing status (address 100Fh)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15	BALRDY	R		The ready bit is set after the cell balancing operation is finished. Reasons for this are that the last BAL_CH_EN.CHx has been cleared by hardware or the BAL_GLOB_CFG.BALEN has been cleared by hardware. With setting of BAL_GLOB_CFG.BALEN this bit is cleared. Read clears bit.
			0*	ONGOING (read) Balancing operation in progress.
			1	FINISHED (read) Balancing operation finished.
14	BALPROTFLG	R		Balancing protection flag. This bit is set when the BALPROT is ACTIVE. Read clears bit.
			0*	NOOCCURENCE (read) Balancing protection was not active.
			1	OCCURRED (read) Balancing protection was active.
13:4	reserved	R	0h	This read-only field is reserved and always has the value 0.
3	BALPROT	R		Balancing protection status
			0*	INACTIVE (read) Balancing protection allows balancing.
			1	ACTIVE (read) Balancing protection inhibits balancing.
2	AUTODISCHRG	R		Auto discharge status
			0*	INACTIVE (read) Auto discharge inactive
			1	ACTIVE (read) Auto discharge active
1	TEMPBALINHIBIT	R		Temperature balancing status
			0*	INACTIVE (read) Temperature based balancing control allows balancing.
			1	ACTIVE (read) Temperature based balancing control inhibits balancing.
0	PREBALTMR	R		preBalancing status
			0*	INACTIVE (read) No prebalancing timer active.
			1	ACTIVE (read) prebalancing timer active (Balancing is inhibited).

12.1.85 BAL\_SWITCH\_STAT0 register

Physical balancing channel status channel 0 - 15

Table 218. BAL\_SWITCH\_STAT0 register - physical balancing channel status channel 0 - 15 (address 1010h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 219. BAL\_SWITCH\_STAT0 register - physical balancing channel status channel 0 - 15 (address 1010h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15	CH15	R		Balancing FET status channel 15 This is the actual status (including odd/even activation and PWM duty cycle) from the switch monitor circuit.
			0*	OPEN (read) Balancing FET is open.
			1	CLOSED (read) Balancing FET is closed.
14	CH14	R		Balancing FET status channel 14 This is the actual status (including odd/even activation and PWM duty cycle) from the switch monitor circuit.
			0*	OPEN (read) Balancing FET is open.
			1	CLOSED (read) Balancing FET is closed.
13	CH13	R		Balancing FET status channel 13 This is the actual status (including odd/even activation and PWM duty cycle) from the switch monitor circuit.
			0*	OPEN (read) Balancing FET is open.
			1	CLOSED (read) Balancing FET is closed.
12	CH12	R		Balancing FET status channel 12 This is the actual status (including odd/even activation and PWM duty cycle) from the switch monitor circuit.
			0*	OPEN (read) Balancing FET is open.
			1	CLOSED (read) Balancing FET is closed.
11	CH11	R		Balancing FET status channel 11 This is the actual status (including odd/even activation and PWM duty cycle) from the switch monitor circuit.
			0*	OPEN (read) Balancing FET is open.
			1	CLOSED (read) Balancing FET is closed.
10	CH10	R		Balancing FET status channel 10 This is the actual status (including odd/even activation and PWM duty cycle) from the switch monitor circuit.
			0*	OPEN (read) Balancing FET is open.

**Table 219. BAL\_SWITCH\_STAT0 register - physical balancing channel status channel 0 - 15 (address 1010h)...***continued*

Legend: \* reset value

Bit	Symbol	Access	Value	Description
			1	CLOSED (read) Balancing FET is closed.
9	CH9	R		Balancing FET status channel 9 This is the actual status (including odd/even activation and PWM duty cycle) from the switch monitor circuit.
			0*	OPEN (read) Balancing FET is open.
			1	CLOSED (read) Balancing FET is closed.
8	CH8	R		Balancing FET status channel 8 This is the actual status (including odd/even activation and PWM duty cycle) from the switch monitor circuit.
			0*	OPEN (read) Balancing FET is open.
			1	CLOSED (read) Balancing FET is closed.
7	CH7	R		Balancing FET status channel 7 This is the actual status (including odd/even activation and PWM duty cycle) from the switch monitor circuit.
			0*	OPEN (read) Balancing FET is open.
			1	CLOSED (read) Balancing FET is closed.
6	CH6	R		Balancing FET status channel 6 This is the actual status (including odd/even activation and PWM duty cycle) from the switch monitor circuit.
			0*	OPEN (read) Balancing FET is open.
			1	CLOSED (read) Balancing FET is closed.
5	CH5	R		Balancing FET status channel 5 This is the actual status (including odd/even activation and PWM duty cycle) from the switch monitor circuit.
			0*	OPEN (read) Balancing FET is open.
			1	CLOSED (read) Balancing FET is closed.
4	CH4	R		Balancing FET status channel 4 This is the actual status (including odd/even activation and PWM duty cycle) from the switch monitor circuit.
			0*	OPEN (read) Balancing FET is open.
			1	CLOSED (read) Balancing FET is closed.
3	CH3	R		Balancing FET status channel 3 This is the actual status (including odd/even activation and PWM duty cycle) from the switch monitor circuit.
			0*	OPEN (read) Balancing FET is open.
			1	CLOSED (read) Balancing FET is closed.
2	CH2	R		Balancing FET status channel 2 This is the actual status (including odd/even activation and PWM duty cycle) from the switch monitor circuit.
			0*	OPEN (read) Balancing FET is open.
			1	CLOSED (read) Balancing FET is closed.
1	CH1	R		Balancing FET status channel 1 This is the actual status (including odd/even activation and PWM duty cycle) from the switch monitor circuit.
			0*	OPEN (read) Balancing FET is open.

**Table 219. BAL\_SWITCH\_STAT0 register - physical balancing channel status channel 0 - 15 (address 1010h)...***continued*

Legend: \* reset value

Bit	Symbol	Access	Value	Description
			1	CLOSED (read) Balancing FET is closed.
0	CH0	R		Balancing FET status channel 0 This is the actual status (including odd/even activation and PWM duty cycle) from the switch monitor circuit.
			0*	OPEN (read) Balancing FET is open.
			1	CLOSED (read) Balancing FET is closed.

### 12.1.86 BAL\_SWITCH\_STAT1 register

Physical balancing channel status channel 16 - 17

**Table 220. BAL\_SWITCH\_STAT1 register - physical balancing channel status channel 16 - 17 (address 1011h) bit allocation**

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	reserved						CH17	CH16
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

**Table 221. BAL\_SWITCH\_STAT1 register - physical balancing channel status channel 16 - 17 (address 1011h)**

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:2	reserved	R	0h	This read-only field is reserved and always has the value 0.
1	CH17	R		Balancing FET status channel 17 This is the actual status (including odd/even activation and PWM duty cycle) from the switch monitor circuit.
			0*	OPEN (read) Balancing FET is open.
			1	CLOSED (read) Balancing FET is closed.
0	CH16	R		Balancing FET status channel 16 This is the actual status (including odd/even activation and PWM duty cycle) from the switch monitor circuit.
			0*	OPEN (read) Balancing FET is open.
			1	CLOSED (read) Balancing FET is closed.

12.1.87 BAL\_SWITCH\_FLT\_STAT0 register

balancing switch fault channel 0 - 15

Table 222. BAL\_SWITCH\_FLT\_STAT0 register - balancing switch fault channel 0 - 15 (address 1012h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 223. BAL\_SWITCH\_FLT\_STAT0 register - balancing switch fault channel 0 - 15 (address 1012h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15	CH15	R		Balancing switch fault channel 15. Physical state of the Balancing circuit has differed from the expected one. This could be due to a broken switch, leakages or over current. Read clears bit.
			0*	NOFLT (read) No fault detected.
			1	FAULT (read) Wrong switch state has been detected.
14	CH14	R		Balancing switch fault channel 14. Physical state of the Balancing circuit has differed from the expected one. This could be due to a broken switch, leakages or over current. Read clears bit.
			0*	NOFLT (read) No fault detected.
			1	FAULT (read) Wrong switch state has been detected.
13	CH13	R		Balancing switch fault channel 13. Physical state of the Balancing circuit has differed from the expected one. This could be due to a broken switch, leakages or over current. Read clears bit.
			0*	NOFLT (read) No fault detected.
			1	FAULT (read) Wrong switch state has been detected.
12	CH12	R		Balancing switch fault channel 12. Physical state of the Balancing circuit has differed from the expected one. This could be due to a broken switch, leakages or over current. Read clears bit.
			0*	NOFLT (read) No fault detected.
			1	FAULT (read) Wrong switch state has been detected.
11	CH11	R		Balancing switch fault channel 11. Physical state of the Balancing circuit has differed from the expected one. This could be due to a broken switch, leakages or over current. Read clears bit.
			0*	NOFLT (read) No fault detected.
			1	FAULT (read) Wrong switch state has been detected.

Table 223. BAL\_SWITCH\_FLT\_STAT0 register - balancing switch fault channel 0 - 15 (address 1012h)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
10	CH10	R		Balancing switch fault channel 10. Physical state of the Balancing circuit has differed from the expected one. This could be due to a broken switch, leakages or over current. Read clears bit.
			0*	NOFLT (read) No fault detected.
			1	FAULT (read) Wrong switch state has been detected.
9	CH9	R		Balancing switch fault channel 9. Physical state of the Balancing circuit has differed from the expected one. This could be due to a broken switch, leakages or over current. Read clears bit.
			0*	NOFLT (read) No fault detected.
			1	FAULT (read) Wrong switch state has been detected.
8	CH8	R		Balancing switch fault channel 8. Physical state of the Balancing circuit has differed from the expected one. This could be due to a broken switch, leakages or over current. Read clears bit.
			0*	NOFLT (read) No fault detected.
			1	FAULT (read) Wrong switch state has been detected.
7	CH7	R		Balancing switch fault channel 7. Physical state of the Balancing circuit has differed from the expected one. This could be due to a broken switch, leakages or over current. Read clears bit.
			0*	NOFLT (read) No fault detected.
			1	FAULT (read) Wrong switch state has been detected.
6	CH6	R		Balancing switch fault channel 6. Physical state of the Balancing circuit has differed from the expected one. This could be due to a broken switch, leakages or over current. Read clears bit.
			0*	NOFLT (read) No fault detected.
			1	FAULT (read) Wrong switch state has been detected.
5	CH5	R		Balancing switch fault channel 5. Physical state of the Balancing circuit has differed from the expected one. This could be due to a broken switch, leakages or over current. Read clears bit.
			0*	NOFLT (read) No fault detected.
			1	FAULT (read) Wrong switch state has been detected.
4	CH4	R		Balancing switch fault channel 4. Physical state of the Balancing circuit has differed from the expected one. This could be due to a broken switch, leakages or over current. Read clears bit.
			0*	NOFLT (read) No fault detected.
			1	FAULT (read) Wrong switch state has been detected.
3	CH3	R		Balancing switch fault channel 3. Physical state of the Balancing circuit has differed from the expected one. This could be due to a broken switch, leakages or over current. Read clears bit.
			0*	NOFLT (read) No fault detected.
			1	FAULT (read) Wrong switch state has been detected.
2	CH2	R		Balancing switch fault channel 2. Physical state of the Balancing circuit has differed from the expected one. This could be due to a broken switch, leakages or over current. Read clears bit.
			0*	NOFLT (read) No fault detected.
			1	FAULT (read) Wrong switch state has been detected.

Table 223. BAL\_SWITCH\_FLT\_STAT0 register - balancing switch fault channel 0 - 15 (address 1012h)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
1	CH1	R		Balancing switch fault channel 1. Physical state of the Balancing circuit has differed from the expected one. This could be due to a broken switch, leakages or over current. Read clears bit.
			0*	NOFLT (read) No fault detected.
			1	FAULT (read) Wrong switch state has been detected.
0	CH0	R		Balancing switch fault channel 0. Physical state of the Balancing circuit has differed from the expected one. This could be due to a broken switch, leakages or over current. Read clears bit.
			0*	NOFLT (read) No fault detected.
			1	FAULT (read) Wrong switch state has been detected.

## 12.1.88 BAL\_SWITCH\_FLT\_STAT1 register

balancing switch fault channel 16 - 17

Table 224. BAL\_SWITCH\_FLT\_STAT1 register - balancing switch fault channel 16 - 17 (address 1013h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	reserved						CH17	CH16
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 225. BAL\_SWITCH\_FLT\_STAT1 register - balancing switch fault channel 16 - 17 (address 1013h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:2	reserved	R	0h	This read-only field is reserved and always has the value 0.
1	CH17	R		Balancing switch fault channel 17. Physical state of the Balancing circuit has differed from the expected one. This could be due to a broken switch, leakages or over current. Read clears bit.
			0*	NOFLT (read) No fault detected.
			1	FAULT (read) Wrong switch state has been detected.
0	CH16	R		Balancing switch fault channel 16. Physical state of the Balancing circuit has differed from the expected one. This could be due to a broken switch, leakages or over current. Read clears bit.
			0*	NOFLT (read) No fault detected.
			1	FAULT (read) Wrong switch state has been detected.

## 12.1.89 BAL\_TMR\_CH\_ALL register

virtual register, writes in parallel into BAL\_TMR\_CH0 up to BAL\_TMR\_CH17

**Table 226. BAL\_TMR\_CH\_ALL register - Virtual register, writes all BAL\_TMR registers (address 101Fh) bit allocation**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved		BALTIME													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

**Table 227. BAL\_TMR\_CH\_ALL register - Virtual register, writes all BAL\_TMR registers (address 101Fh)**

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:14	reserved	W	0h	This read-only field is reserved and always has the value 0.
13:0	BALTIME	W		Sets the balancing time for all channels. <b>BALTIME</b> * 10 seconds
			0000h*	EXPIRED (write) Balancing time is set to 0.
			0001h	BALTIME (write) Balancing time is set to BALTIME * 10 seconds
			3FFFh	MAX (write) Sets maximum balancing time of 163830 seconds = approximately 45.5 hours.

## 12.1.90 BAL\_TMR\_CH0 register

balancing timer channel 0

**Table 228. BAL\_TMR\_CH0 register - balancing timer channel 0 (address 1020h) bit allocation**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved		BALTIME													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**Table 229. BAL\_TMR\_CH0 register - balancing timer channel 0 (address 1020h)**

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:14	reserved	R	0h	This read-only field is reserved and always has the value 0.
13:0	BALTIME	R/W		Balancing time for channel 0. The value of this field represents the current counter value when read. The counting saturates at 0. If the value is zero, the balancing for this channel is stopped. The counting is only active if balancing is enabled, timer based balancing is enabled and the channel enable is set. <b>BALTIME</b> * 10 seconds
			0000h*	EXPIRED (read-write) Balancing time is set to 0.
			0001h	BALTIME (read-write) Balancing time is set to BALTIME * 10 seconds



Table 229. BAL\_TMR\_CH0 register - balancing timer channel 0 (address 1020h)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
			3FFFh	MAX (read-write) Sets maximum balancing time of 163830 seconds = approximately 45.5 hours.

12.1.91 BAL\_TMR\_CH1 register

balancing timer channel 1

Table 230. BAL\_TMR\_CH1 register - balancing timer channel 1 (address 1021h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved		BALTIME													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 231. BAL\_TMR\_CH1 register - balancing timer channel 1 (address 1021h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:14	reserved	R	0h	This read-only field is reserved and always has the value 0.
13:0	BALTIME	R/W		Balancing time for channel 1. The value of this field represents the current counter value when read. The counting saturates at 0. If the value is zero, the balancing for this channel is stopped. The counting is only active if balancing is enabled, timer based balancing is enabled and the channel enable is set. <b>BALTIME</b> * 10 seconds
			0000h*	EXPIRED (read-write) Balancing time is set to 0.
			0001h	BALTIME (read-write) Balancing time is set to BALTIME * 10 seconds
			3FFFh	MAX (read-write) Sets maximum balancing time of 163830 seconds = approximately 45.5 hours.

12.1.92 BAL\_TMR\_CH2 register

balancing timer channel 2

Table 232. BAL\_TMR\_CH2 register - balancing timer channel 2 (address 1022h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved		BALTIME													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 233. BAL\_TMR\_CH2 register - balancing timer channel 2 (address 1022h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:14	reserved	R	0h	This read-only field is reserved and always has the value 0.

Table 233. BAL\_TMR\_CH2 register - balancing timer channel 2 (address 1022h)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
13:0	BALTIME	R/W		Balancing time for channel 2. The value of this field represents the current counter value when read. The counting saturates at 0. If the value is zero, the balancing for this channel is stopped. The counting is only active if balancing is enabled, timer based balancing is enabled and the channel enable is set. <b>BALTIME</b> * 10 seconds
			0000h*	EXPIRED (read-write) Balancing time is set to 0.
			0001h	BALTIME (read-write) Balancing time is set to BALTIME * 10 seconds
			3FFFh	MAX (read-write) Sets maximum balancing time of 163830 seconds = approximately 45.5 hours.

12.1.93 BAL\_TMR\_CH3 register

balancing timer channel 3

Table 234. BAL\_TMR\_CH3 register - balancing timer channel 3 (address 1023h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved		BALTIME													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 235. BAL\_TMR\_CH3 register - balancing timer channel 3 (address 1023h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:14	reserved	R	0h	This read-only field is reserved and always has the value 0.
13:0	BALTIME	R/W		Balancing time for channel 3. The value of this field represents the current counter value when read. The counting saturates at 0. If the value is zero, the balancing for this channel is stopped. The counting is only active if balancing is enabled, timer based balancing is enabled and the channel enable is set. <b>BALTIME</b> * 10 seconds
			0000h*	EXPIRED (read-write) Balancing time is set to 0.
			0001h	BALTIME (read-write) Balancing time is set to BALTIME * 10 seconds
			3FFFh	MAX (read-write) Sets maximum balancing time of 163830 seconds = approximately 45.5 hours.

12.1.94 BAL\_TMR\_CH4 register

balancing timer channel 4

Table 236. BAL\_TMR\_CH4 register - balancing timer channel 4 (address 1024h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved		BALTIME													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 236. BAL\_TMR\_CH4 register - balancing timer channel 4 (address 1024h) bit allocation...continued

Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
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Table 237. BAL\_TMR\_CH4 register - balancing timer channel 4 (address 1024h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:14	reserved	R	0h	This read-only field is reserved and always has the value 0.
13:0	BALTIME	R/W		Balancing time for channel 4. The value of this field represents the current counter value when read. The counting saturates at 0. If the value is zero, the balancing for this channel is stopped. The counting is only active if balancing is enabled, timer based balancing is enabled and the channel enable is set. <b>BALTIME</b> * 10 seconds
			0000h*	EXPIRED (read-write) Balancing time is set to 0.
			0001h	BALTIME (read-write) Balancing time is set to BALTIME * 10 seconds
			3FFFh	MAX (read-write) Sets maximum balancing time of 163830 seconds = approximately 45.5 hours.

### 12.1.95 BAL\_TMR\_CH5 register

balancing timer channel 5

Table 238. BAL\_TMR\_CH5 register - balancing timer channel 5 (address 1025h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved		BALTIME													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 239. BAL\_TMR\_CH5 register - balancing timer channel 5 (address 1025h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:14	reserved	R	0h	This read-only field is reserved and always has the value 0.
13:0	BALTIME	R/W		Balancing time for channel 5. The value of this field represents the current counter value when read. The counting saturates at 0. If the value is zero, the balancing for this channel is stopped. The counting is only active if balancing is enabled, timer based balancing is enabled and the channel enable is set. <b>BALTIME</b> * 10 seconds
			0000h*	EXPIRED (read-write) Balancing time is set to 0.
			0001h	BALTIME (read-write) Balancing time is set to BALTIME * 10 seconds
			3FFFh	MAX (read-write) Sets maximum balancing time of 163830 seconds = approximately 45.5 hours.

### 12.1.96 BAL\_TMR\_CH6 register

balancing timer channel 6

Table 240. BAL\_TMR\_CH6 register - balancing timer channel 6 (address 1026h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved		BALTIME													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 241. BAL\_TMR\_CH6 register - balancing timer channel 6 (address 1026h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:14	reserved	R	0h	This read-only field is reserved and always has the value 0.
13:0	BALTIME	R/W		Balancing time for channel 6. The value of this field represents the current counter value when read. The counting saturates at 0. If the value is zero, the balancing for this channel is stopped. The counting is only active if balancing is enabled, timer based balancing is enabled and the channel enable is set. <b>BALTIME</b> * 10 seconds
			0000h*	EXPIRED (read-write) Balancing time is set to 0.
			0001h	BALTIME (read-write) Balancing time is set to BALTIME * 10 seconds
			3FFFh	MAX (read-write) Sets maximum balancing time of 163830 seconds = approximately 45.5 hours.

12.1.97 BAL\_TMR\_CH7 register

balancing timer channel 7

Table 242. BAL\_TMR\_CH7 register - balancing timer channel 7 (address 1027h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved		BALTIME													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 243. BAL\_TMR\_CH7 register - balancing timer channel 7 (address 1027h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:14	reserved	R	0h	This read-only field is reserved and always has the value 0.
13:0	BALTIME	R/W		Balancing time for channel 7. The value of this field represents the current counter value when read. The counting saturates at 0. If the value is zero, the balancing for this channel is stopped. The counting is only active if balancing is enabled, timer based balancing is enabled and the channel enable is set. <b>BALTIME</b> * 10 seconds
			0000h*	EXPIRED (read-write) Balancing time is set to 0.
			0001h	BALTIME (read-write) Balancing time is set to BALTIME * 10 seconds
			3FFFh	MAX (read-write) Sets maximum balancing time of 163830 seconds = approximately 45.5 hours.

## 12.1.98 BAL\_TMR\_CH8 register

balancing timer channel 8

Table 244. BAL\_TMR\_CH8 register - balancing timer channel 8 (address 1028h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved		BALTIME													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 245. BAL\_TMR\_CH8 register - balancing timer channel 8 (address 1028h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:14	reserved	R	0h	This read-only field is reserved and always has the value 0.
13:0	BALTIME	R/W		Balancing time for channel 8. The value of this field represents the current counter value when read. The counting saturates at 0. If the value is zero, the balancing for this channel is stopped. The counting is only active if balancing is enabled, timer based balancing is enabled and the channel enable is set. <b>BALTIME</b> * 10 seconds
			0000h*	EXPIRED (read-write) Balancing time is set to 0.
			0001h	BALTIME (read-write) Balancing time is set to BALTIME * 10 seconds
			3FFFh	MAX (read-write) Sets maximum balancing time of 163830 seconds = approximately 45.5 hours.

## 12.1.99 BAL\_TMR\_CH9 register

balancing timer channel 9

Table 246. BAL\_TMR\_CH9 register - balancing timer channel 9 (address 1029h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved		BALTIME													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 247. BAL\_TMR\_CH9 register - balancing timer channel 9 (address 1029h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:14	reserved	R	0h	This read-only field is reserved and always has the value 0.
13:0	BALTIME	R/W		Balancing time for channel 9. The value of this field represents the current counter value when read. The counting saturates at 0. If the value is zero, the balancing for this channel is stopped. The counting is only active if balancing is enabled, timer based balancing is enabled and the channel enable is set. <b>BALTIME</b> * 10 seconds
			0000h*	EXPIRED (read-write) Balancing time is set to 0.

Table 247. BAL\_TMR\_CH9 register - balancing timer channel 9 (address 1029h)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
			0001h	BALTIME (read-write) Balancing time is set to BALTIME * 10 seconds
			3FFFh	MAX (read-write) Sets maximum balancing time of 163830 seconds = approximately 45.5 hours.

12.1.100 BAL\_TMR\_CH10 register

balancing timer channel 10

Table 248. BAL\_TMR\_CH10 register - balancing timer channel 10 (address 102Ah) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved		BALTIME													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 249. BAL\_TMR\_CH10 register - balancing timer channel 10 (address 102Ah)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:14	reserved	R	0h	This read-only field is reserved and always has the value 0.
13:0	BALTIME	R/W		Balancing time for channel 10. The value of this field represents the current counter value when read. The counting saturates at 0. If the value is zero, the balancing for this channel is stopped. The counting is only active if balancing is enabled, timer based balancing is enabled and the channel enable is set. <b>BALTIME</b> * 10 seconds
			0000h*	EXPIRED (read-write) Balancing time is set to 0.
			0001h	BALTIME (read-write) Balancing time is set to BALTIME * 10 seconds
			3FFFh	MAX (read-write) Sets maximum balancing time of 163830 seconds = approximately 45.5 hours.

12.1.101 BAL\_TMR\_CH11 register

balancing timer channel 11

Table 250. BAL\_TMR\_CH11 register - balancing timer channel 11 (address 102Bh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved		BALTIME													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 251. BAL\_TMR\_CH11 register - balancing timer channel 11 (address 102Bh)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:14	reserved	R	0h	This read-only field is reserved and always has the value 0.
13:0	BALTIME	R/W		Balancing time for channel 11. The value of this field represents the current counter value when read. The counting saturates at 0. If the value is zero, the balancing for this channel is stopped. The counting is only active if balancing is enabled, timer based balancing is enabled and the channel enable is set. <b>BALTIME</b> * 10 seconds
			0000h*	EXPIRED (read-write) Balancing time is set to 0.
			0001h	BALTIME (read-write) Balancing time is set to BALTIME * 10 seconds
			3FFFh	MAX (read-write) Sets maximum balancing time of 163830 seconds = approximately 45.5 hours.

12.1.102 BAL\_TMR\_CH12 register

balancing timer channel 12

Table 252. BAL\_TMR\_CH12 register - balancing timer channel 12 (address 102Ch) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved		BALTIME													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 253. BAL\_TMR\_CH12 register - balancing timer channel 12 (address 102Ch)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:14	reserved	R	0h	This read-only field is reserved and always has the value 0.
13:0	BALTIME	R/W		Balancing time for channel 12. The value of this field represents the current counter value when read. The counting saturates at 0. If the value is zero, the balancing for this channel is stopped. The counting is only active if balancing is enabled, timer based balancing is enabled and the channel enable is set. <b>BALTIME</b> * 10 seconds
			0000h*	EXPIRED (read-write) Balancing time is set to 0.
			0001h	BALTIME (read-write) Balancing time is set to BALTIME * 10 seconds
			3FFFh	MAX (read-write) Sets maximum balancing time of 163830 seconds = approximately 45.5 hours.

12.1.103 BAL\_TMR\_CH13 register

balancing timer channel 13

Table 254. BAL\_TMR\_CH13 register - balancing timer channel 13 (address 102Dh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved		BALTIME													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 255. BAL\_TMR\_CH13 register - balancing timer channel 13 (address 102Dh)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:14	reserved	R	0h	This read-only field is reserved and always has the value 0.
13:0	BALTIME	R/W		Balancing time for channel 13. The value of this field represents the current counter value when read. The counting saturates at 0. If the value is zero, the balancing for this channel is stopped. The counting is only active if balancing is enabled, timer based balancing is enabled and the channel enable is set. <b>BALTIME</b> * 10 seconds
			0000h*	EXPIRED (read-write) Balancing time is set to 0.
			0001h	BALTIME (read-write) Balancing time is set to BALTIME * 10 seconds
			3FFFh	MAX (read-write) Sets maximum balancing time of 163830 seconds = approximately 45.5 hours.

12.1.104 BAL\_TMR\_CH14 register

balancing timer channel 14

Table 256. BAL\_TMR\_CH14 register - balancing timer channel 14 (address 102Eh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved		BALTIME													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 257. BAL\_TMR\_CH14 register - balancing timer channel 14 (address 102Eh)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:14	reserved	R	0h	This read-only field is reserved and always has the value 0.
13:0	BALTIME	R/W		Balancing time for channel 14. The value of this field represents the current counter value when read. The counting saturates at 0. If the value is zero, the balancing for this channel is stopped. The counting is only active if balancing is enabled, timer based balancing is enabled and the channel enable is set. <b>BALTIME</b> * 10 seconds
			0000h*	EXPIRED (read-write) Balancing time is set to 0.



Table 257. BAL\_TMR\_CH14 register - balancing timer channel 14 (address 102Eh)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
			0001h	BALTIME (read-write) Balancing time is set to BALTIME * 10 seconds
			3FFFh	MAX (read-write) Sets maximum balancing time of 163830 seconds = approximately 45.5 hours.

12.1.105 BAL\_TMR\_CH15 register

balancing timer channel 15

Table 258. BAL\_TMR\_CH15 register - balancing timer channel 15 (address 102Fh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved		BALTIME													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 259. BAL\_TMR\_CH15 register - balancing timer channel 15 (address 102Fh)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:14	reserved	R	0h	This read-only field is reserved and always has the value 0.
13:0	BALTIME	R/W		Balancing time for channel 15. The value of this field represents the current counter value when read. The counting saturates at 0. If the value is zero, the balancing for this channel is stopped. The counting is only active if balancing is enabled, timer based balancing is enabled and the channel enable is set. <b>BALTIME</b> * 10 seconds
			0000h*	PWM0 (read-write) Balancing time is set to 0.
			0001h	PWM1 (read-write) Balancing time is set to BALTIME * 10 seconds
			3FFFh	MAX (read-write) Sets maximum balancing time of 163830 seconds = approximately 45.5 hours.

12.1.106 BAL\_TMR\_CH16 register

balancing timer channel 16

Table 260. BAL\_TMR\_CH16 register - balancing timer channel 16 (address 1030h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved		BALTIME													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 261. BAL\_TMR\_CH16 register - balancing timer channel 16 (address 1030h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:14	reserved	R	0h	This read-only field is reserved and always has the value 0.
13:0	BALTIME	R/W		Balancing time for channel 16. The value of this field represents the current counter value when read. The counting saturates at 0. If the value is zero, the balancing for this channel is stopped. The counting is only active if balancing is enabled, timer based balancing is enabled and the channel enable is set. <b>BALTIME</b> * 10 seconds
			0000h*	EXPIRED (read-write) Balancing time is set to 0.
			0001h	BALTIME (read-write) Balancing time is set to BALTIME * 10 seconds
			3FFFh	MAX (read-write) Sets maximum balancing time of 163830 seconds = approximately 45.5 hours.

12.1.107 BAL\_TMR\_CH17 register

balancing timer channel 17

Table 262. BAL\_TMR\_CH17 register - balancing timer channel 17 (address 1031h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved		BALTIME													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 263. BAL\_TMR\_CH17 register - balancing timer channel 17 (address 1031h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:14	reserved	R	0h	This read-only field is reserved and always has the value 0.
13:0	BALTIME	R/W		Balancing time for channel 17. The value of this field represents the current counter value when read. The counting saturates at 0. If the value is zero, the balancing for this channel is stopped. The counting is only active if balancing is enabled, timer based balancing is enabled and the channel enable is set. <b>BALTIME</b> * 10 seconds
			0000h*	EXPIRED (read-write) Balancing time is set to 0.
			0001h	BALTIME (read-write) Balancing time is set to BALTIME * 10 seconds
			3FFFh	MAX (read-write) Sets maximum balancing time of 163830 seconds = approximately 45.5 hours.

## 12.1.108 BAL\_PWM\_CH\_ALL register

virtual register, writes in parallel into BAL\_PWM\_CH0 up to BAL\_PWM\_CH17

**Table 264. BAL\_PWM\_CH\_ALL register - Virtual register, writes all BAL\_PWM registers (address 1032h) bit allocation**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved								PWM							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Access	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

**Table 265. BAL\_PWM\_CH\_ALL register - Virtual register, writes all BAL\_PWM registers (address 1032h)**

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:8	reserved	W	0h	This read-only field is reserved and always has the value 0.
7:0	PWM	W		Sets the balancing PWM for all channels. <b>PWM</b> * 100/255%
			00h	DISABLED (write) PWM duty cycle set to 0.
			80h	PWM50 (write) PWM duty cycle set to 128/255 *100 % = 50%.
			FFh*	MAX (write) PWM duty cycle set to 100%.

## 12.1.109 BAL\_PWM\_CH0 register

Balancing PWM channel 0

**Table 266. BAL\_PWM\_CH0 register - balancing PWM channel 0 (address 1033h) bit allocation**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved								PWM							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**Table 267. BAL\_PWM\_CH0 register - balancing PWM channel 0 (address 1033h)**

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:8	reserved	R	0h	This read-only field is reserved and always has the value 0.
7:0	PWM	R/W		Balancing PWM for channel 0. <b>PWM</b> * 100/255%
			00h	DISABLED (read-write) PWM duty cycle set to 0.
			80h	PWM50 (read-write) PWM duty cycle set to 128/255 *100 % = 50%.
			FFh*	MAX (read-write) PWM duty cycle set to 100%.

12.1.110 BAL\_PWM\_CH1 register

Balancing PWM channel 1

Table 268. BAL\_PWM\_CH1 register - balancing PWM channel 1 (address 1034h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved								PWM							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 269. BAL\_PWM\_CH1 register - balancing PWM channel 1 (address 1034h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:8	reserved	R	0h	This read-only field is reserved and always has the value 0.
7:0	PWM	R/W		Balancing PWM for channel 1. <b>PWM</b> * 100/255%
			00h	DISABLED (read-write) .
			80h	PWM50 (read-write) PWM duty cycle set to 128/255 *100 %= 50%.
			FFh*	MAX (read-write) PWM duty cycle set to 100%.

12.1.111 BAL\_PWM\_CH2 register

Balancing PWM channel 2

Table 270. BAL\_PWM\_CH2 register - balancing PWM channel 2 (address 1035h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved								PWM							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 271. BAL\_PWM\_CH2 register - balancing PWM channel 2 (address 1035h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:8	reserved	R	0h	This read-only field is reserved and always has the value 0.
7:0	PWM	R/W		Balancing PWM for channel 2. <b>PWM</b> * 100/255%
			00h	DISABLED (read-write) PWM duty cycle set to 0.
			80h	PWM50 (read-write) PWM duty cycle set to 128/255 *100 %= 50%.
			FFh*	MAX (read-write) PWM duty cycle set to 100%.

12.1.112 BAL\_PWM\_CH3 register

Balancing PWM channel 3

Table 272. BAL\_PWM\_CH3 register - balancing PWM channel 3 (address 1036h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved								PWM							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 273. BAL\_PWM\_CH3 register - balancing PWM channel 3 (address 1036h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:8	reserved	R	0h	This read-only field is reserved and always has the value 0.
7:0	PWM	R/W		Balancing PWM for channel 3. <b>PWM</b> * 100/255%
			00h	DISABLED (read-write) PWM duty cycle set to 0.
			80h	PWM50 (read-write) PWM duty cycle set to 128/255 *100 %= 50%.
			FFh*	MAX (read-write) PWM duty cycle set to 100%.

12.1.113 BAL\_PWM\_CH4 register

balancing PWM channel 4

Table 274. BAL\_PWM\_CH4 register - balancing PWM channel 4 (address 1037h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved								PWM							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 275. BAL\_PWM\_CH4 register - balancing PWM channel 4 (address 1037h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:8	reserved	R	0h	This read-only field is reserved and always has the value 0.
7:0	PWM	R/W		Balancing PWM for channel 4. <b>PWM</b> * 100/255%
			00h	DISABLED (read-write) PWM duty cycle set to 0.
			80h	PWM50 (read-write) PWM duty cycle set to 128/255 *100 %= 50%.
			FFh*	MAX (read-write) PWM duty cycle set to 100%.

12.1.114 BAL\_PWM\_CH5 register

Balancing PWM channel 5

Table 276. BAL\_PWM\_CH5 register - balancing PWM channel 5 (address 1038h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved								PWM							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 277. BAL\_PWM\_CH5 register - balancing PWM channel 5 (address 1038h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:8	reserved	R	0h	This read-only field is reserved and always has the value 0.
7:0	PWM	R/W		Balancing PWM for channel 5. <b>PWM</b> * 100/255%
			00h	DISABLED (read-write) PWM duty cycle set to 0.
			80h	PWM50 (read-write) PWM duty cycle set to 128/255 *100 %= 50%.
			FFh*	MAX (read-write) PWM duty cycle set to 100%.

12.1.115 BAL\_PWM\_CH6 register

Balancing PWM channel 6

Table 278. BAL\_PWM\_CH6 register - balancing PWM channel 6 (address 1039h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved								PWM							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 279. BAL\_PWM\_CH6 register - balancing PWM channel 6 (address 1039h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:8	reserved	R	0h	This read-only field is reserved and always has the value 0.
7:0	PWM	R/W		Balancing PWM for channel 6. <b>PWM</b> * 100/255%
			00h	DISABLED (read-write) PWM duty cycle set to 0.
			80h	PWM50 (read-write) PWM duty cycle set to 128/255 *100 %= 50%.
			FFh*	MAX (read-write) PWM duty cycle set to 100%.

12.1.116 BAL\_PWM\_CH7 register

Balancing PWM channel 7

Table 280. BAL\_PWM\_CH7 register - balancing PWM channel 7 (address 103Ah) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved								PWM							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 281. BAL\_PWM\_CH7 register - balancing PWM channel 7 (address 103Ah)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:8	reserved	R	0h	This read-only field is reserved and always has the value 0.
7:0	PWM	R/W		Balancing PWM for channel 7. <b>PWM</b> * 100/255%
			00h	DISABLED (read-write) PWM duty cycle set to 0.
			80h	PWM50 (read-write) PWM duty cycle set to 128/255 *100 %= 50%.
			FFh*	MAX (read-write) PWM duty cycle set to 100%.

12.1.117 BAL\_PWM\_CH8 register

Balancing PWM channel 8

Table 282. BAL\_PWM\_CH8 register - balancing PWM channel 8 (address 103Bh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved								PWM							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 283. BAL\_PWM\_CH8 register - balancing PWM channel 8 (address 103Bh)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:8	reserved	R	0h	This read-only field is reserved and always has the value 0.
7:0	PWM	R/W		Balancing PWM for channel 8. <b>PWM</b> * 100/255%
			00h	DISABLED (read-write) PWM duty cycle set to 0.
			80h	PWM50 (read-write) PWM duty cycle set to 128/255 *100 %= 50%.
			FFh*	MAX (read-write) PWM duty cycle set to 100%.

12.1.118 BAL\_PWM\_CH9 register

Balancing PWM channel 9

Table 284. BAL\_PWM\_CH9 register - balancing PWM channel 9 (address 103Ch) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved								PWM							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 285. BAL\_PWM\_CH9 register - balancing PWM channel 9 (address 103Ch)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:8	reserved	R	0h	This read-only field is reserved and always has the value 0.
7:0	PWM	R/W		Balancing PWM for channel 9. <b>PWM</b> * 100/255%
			00h	DISABLED (read-write) PWM duty cycle set to 0.
			80h	PWM50 (read-write) PWM duty cycle set to 128/255 *100 %= 50%.
			FFh*	MAX (read-write) PWM duty cycle set to 100%.

12.1.119 BAL\_PWM\_CH10 register

Balancing PWM channel 10

Table 286. BAL\_PWM\_CH10 register - balancing PWM channel 10 (address 103Dh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved								PWM							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 287. BAL\_PWM\_CH10 register - balancing PWM channel 10 (address 103Dh)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:8	reserved	R	0h	This read-only field is reserved and always has the value 0.
7:0	PWM	R/W		Balancing PWM for channel 10. <b>PWM</b> * 100/255%
			00h	DISABLED (read-write) PWM duty cycle set to 0.
			80h	PWM50 (read-write) PWM duty cycle set to 128/255 *100 %= 50%.
			FFh*	MAX (read-write) PWM duty cycle set to 100%.



12.1.120 BAL\_PWM\_CH11 register

Balancing PWM channel 11

Table 288. BAL\_PWM\_CH11 register - balancing PWM channel 11 (address 103Eh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved								PWM							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 289. BAL\_PWM\_CH11 register - balancing PWM channel 11 (address 103Eh)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:8	reserved	R	0h	This read-only field is reserved and always has the value 0.
7:0	PWM	R/W		Balancing PWM for channel 11. <b>PWM</b> * 100/255%
			00h	DISABLED (read-write) PWM duty cycle set to 0.
			80h	PWM50 (read-write) PWM duty cycle set to 128/255 *100 %= 50%.
			FFh*	MAX (read-write) PWM duty cycle set to 100%.

12.1.121 BAL\_PWM\_CH12 register

Balancing PWM channel 12

Table 290. BAL\_PWM\_CH12 register - balancing PWM channel 12 (address 103Fh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved								PWM							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 291. BAL\_PWM\_CH12 register - balancing PWM channel 12 (address 103Fh)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:8	reserved	R	0h	This read-only field is reserved and always has the value 0.
7:0	PWM	R/W		Balancing PWM for channel 12 <b>PWM</b> * 100/255%
			00h	DISABLED (read-write) PWM duty cycle set to 0.
			80h	PWM50 (read-write) PWM duty cycle set to 128/255 *100 %= 50%.
			FFh*	MAX (read-write) PWM duty cycle set to 100%.

12.1.122 BAL\_PWM\_CH13 register

Balancing PWM channel 13

Table 292. BAL\_PWM\_CH13 register - balancing PWM channel 13 (address 1040h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved								PWM							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 293. BAL\_PWM\_CH13 register - balancing PWM channel 13 (address 1040h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:8	reserved	R	0h	This read-only field is reserved and always has the value 0.
7:0	PWM	R/W		Balancing PWM for channel 13. <b>PWM</b> * 100/255%
			00h	DISABLED (read-write) PWM duty cycle set to 0.
			80h	PWM50 (read-write) PWM duty cycle set to 128/255 *100 %= 50%.
			FFh*	MAX (read-write) PWM duty cycle set to 100%.

12.1.123 BAL\_PWM\_CH14 register

Balancing PWM channel 14

Table 294. BAL\_PWM\_CH14 register - balancing PWM channel 14 (address 1041h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved								PWM							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 295. BAL\_PWM\_CH14 register - balancing PWM channel 14 (address 1041h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:8	reserved	R	0h	This read-only field is reserved and always has the value 0.
7:0	PWM	R/W		Balancing PWM for channel 14. <b>PWM</b> * 100/255%
			00h	DISABLED (read-write) PWM duty cycle set to 0.
			80h	PWM50 (read-write) PWM duty cycle set to 128/255 *100 %= 50%.
			FFh*	MAX (read-write) PWM duty cycle set to 100%.

12.1.124 BAL\_PWM\_CH15 register

Balancing PWM channel 15

Table 296. BAL\_PWM\_CH15 register - balancing PWM channel 15 (address 1042h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved								PWM							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 297. BAL\_PWM\_CH15 register - balancing PWM channel 15 (address 1042h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:8	reserved	R	0h	This read-only field is reserved and always has the value 0.
7:0	PWM	R/W		Balancing PWM for channel 15. <b>PWM</b> * 100/255%
			00h	DISABLED (read-write) PWM duty cycle set to 0.
			80h	PWM50 (read-write) PWM duty cycle set to 128/255 *100 %= 50%.
			FFh*	MAX (read-write) PWM duty cycle set to 100%.

12.1.125 BAL\_PWM\_CH16 register

Balancing PWM channel 16

Table 298. BAL\_PWM\_CH16 register - balancing PWM channel 16 (address 1043h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved								PWM							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 299. BAL\_PWM\_CH16 register - balancing PWM channel 16 (address 1043h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:8	reserved	R	0h	This read-only field is reserved and always has the value 0.
7:0	PWM	R/W		Balancing PWM for channel 16. <b>PWM</b> * 100/255%
			00h	DISABLED (read-write) PWM duty cycle set to 0.
			80h	PWM50 (read-write) PWM duty cycle set to 128/255 *100 %= 50%.
			FFh*	MAX (read-write) PWM duty cycle set to 100%.

## 12.1.126 BAL\_PWM\_CH17 register

Balancing PWM channel 17

Table 300. BAL\_PWM\_CH17 register - balancing PWM channel 17 (address 1044h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved								PWM							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 301. BAL\_PWM\_CH17 register - balancing PWM channel 17 (address 1044h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:8	reserved	R	0h	This read-only field is reserved and always has the value 0.
7:0	PWM	R/W		Balancing PWM for channel 17. <b>PWM</b> * 100/255%
			00h	DISABLED (read-write) PWM duty cycle set to 0.
			80h	PWM50 (read-write) PWM duty cycle set to 128/255 *100 % = 50%.
			FFh*	MAX (read-write) PWM duty cycle set to 100%.

## 12.1.127 ALLM\_CFG register

General measurement control

Table 302. ALLM\_CFG register - general measurement control (address 1400h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	BALPAUSELEN							
Reset	0	0	0	0	0	0	0	0
Access	W	W	W	W	W	W	W	W
Bit	7	6	5	4	3	2	1	0
Symbol	BALPAUSELEN						BALPAUSECYCMODEN	MEASEN
Reset	0	0	0	0	0	0	0	0
Access	W	W	W	W	W	W	W	W

Table 303. ALLM\_CFG register - general measurement control (address 1400h)

Bit	Symbol	Access	Value	Description
15:2	BALPAUSELEN	W	0h	Writes BALPAUSELEN for primary and secondary measurement.
1	BALPAUSECYCMODEN	W	0h	Writes BALPAUSECYCMODEN for primary and secondary measurement.
0	MEASEN	W	0h	Writes MEASEN for primary and secondary measurement.

## 12.1.128 ALLM\_APP\_CTRL register

Application measurement control

Table 304. ALLM\_APP\_CTRL register - application measurement control (address 1401h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	PAUSEBAL	VCOLNUM					CAPAIN7	CAPAIN6
Reset	0	1	1	1	1	1	0	0
Access	W	W	W	W	W	W	W	W
Bit	7	6	5	4	3	2	1	0
Symbol	CAPAIN5	CAPAIN4	CAPAIN3	CAPAIN2	CAPAIN1	CAPAIN0	CAPAINA	CAPVC
Reset	0	0	0	0	0	0	0	0
Access	W	W	W	W	W	W	W	W

Table 305. ALLM\_APP\_CTRL register - application measurement control (address 1401h)

Bit	Symbol	Access	Value	Description
15	PAUSEBAL	W	0h	Writes PAUSEBAL for primary and secondary measurement.
14:10	VCOLNUM	W	1Fh	Writes VCOLNUM for primary measurement, if CAPVC is set. No influence on secondary measurement.
9	CAPAIN7	W	0h	No influence on primary measurement as long as it is used without the PAUSEBAL bit. Writes CAPAIN7 for secondary measurement.
8	CAPAIN6	W	0h	No influence on primary measurement as long as it is used without the PAUSEBAL bit. Writes CAPAIN6 for secondary measurement.
7	CAPAIN5	W	0h	No influence on primary measurement as long as it is used without the PAUSEBAL bit. Writes CAPAIN5 for secondary measurement.
6	CAPAIN4	W	0h	No influence on primary measurement as long as it is used without the PAUSEBAL bit. Writes CAPAIN4 for secondary measurement.
5	CAPAIN3	W	0h	Writes CAPAIN3 for primary measurement. No influence on secondary measurement as long as it is used without the PAUSEBAL bit.
4	CAPAIN2	W	0h	Writes CAPAIN2 for primary measurement. No influence on secondary measurement as long as it is used without the PAUSEBAL bit.
3	CAPAIN1	W	0h	Writes CAPAIN1 for primary measurement. No influence on secondary measurement as long as it is used without the PAUSEBAL bit.
2	CAPAIN0	W	0h	Writes CAPAIN0 for primary measurement. No influence on secondary measurement as long as it is used without the PAUSEBAL bit.
1	CAPAINA	W	0h	Writes CAPAINA for primary measurement. No influence on secondary measurement as long as it is used without the PAUSEBAL bit.
0	CAPVC	W	0h	Writes CAPVC for primary measurement. No influence on secondary measurement as long as it is used without the PAUSEBAL bit.

## 12.1.129 ALLM\_PER\_CTRL register

periodic measurement control

Table 306. ALLM\_PER\_CTRL register - periodic measurement control (address 1402h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved			PERCTRL	reserved			PERLEN
Reset	0	0	0	0	0	0	0	0
Access	W	W	W	W	W	W	W	W
Bit	7	6	5	4	3	2	1	0
Symbol	PERLEN							
Reset	0	0	0	1	0	0	0	0
Access	W	W	W	W	W	W	W	W

Table 307. ALLM\_PER\_CTRL register - periodic measurement control (address 1402h)

Bit	Symbol	Access	Value	Description
15:13	reserved	W	0h	This read-only field is reserved and always has the value 0.
12	PERCTRL	W	0h	Writes PERCTRL for primary and secondary measurement.
11:9	reserved	W	0h	This read-only field is reserved and always has the value 0.
8:0	PERLEN	W	10h	Writes PERLEN for primary and secondary measurement.

## 12.1.130 ALLM\_SYNC\_CTRL register

Synchronous measurement control

Table 308. ALLM\_SYNC\_CTRL register - synchronous measurement control (address 1403h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	PAUSEBAL	VBOLNUM					reserved	
Reset	0	1	1	1	1	1	0	0
Access	W	W	W	W	W	W	W	W
Bit	7	6	5	4	3	2	1	0
Symbol	reserved						FASTVB	SYNCCYC
Reset	0	0	0	0	0	0	0	0
Access	W	W	W	W	W	W	W	W

Table 309. ALLM\_SYNC\_CTRL register - synchronous measurement control (address 1403h)

Bit	Symbol	Access	Value	Description
15	PAUSEBAL	W	0h	Writes PAUSEBAL for primary and secondary measurement.
14:10	VBOLNUM	W	1Fh	No influence on primary measurement. Writes VBOLNUM for secondary measurement.
9:2	reserved	W	0h	This read-only field is reserved and always has the value 0.
1	FASTVB	W	0h	Dummy fast measurement cycle on primary measurement. Writes FASTVB for secondary measurement.
0	SYNCCYC	W	0h	Writes SYNCCYC for primary and secondary measurement.

## 12.1.131 ALLM\_VCVB\_CFG0 register

Cell voltage measurement enable

Table 310. ALLM\_VCVB\_CFG0 register - cell voltage measurement enable (address 1408h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	VCVB15EN	VCVB14EN	VCVB13EN	VCVB12EN	VCVB11EN	VCVB10EN	VCVB9EN	VCVB8EN
Reset	0	0	0	0	0	0	0	0
Access	W	W	W	W	W	W	W	W
Bit	7	6	5	4	3	2	1	0
Symbol	VCVB7EN	VCVB6EN	VCVB5EN	VCVB4EN	VCVB3EN	VCVB2EN	VCVB1EN	VCVB0EN
Reset	0	0	0	0	0	0	0	0
Access	W	W	W	W	W	W	W	W

Table 311. ALLM\_VCVB\_CFG0 register - cell voltage measurement enable (address 1408h)

Bit	Symbol	Access	Value	Description
15	VCVB15EN	W	0h	Writes VC15EN for primary and VB15EN secondary measurement.
14	VCVB14EN	W	0h	Writes VC14EN for primary and VB14EN secondary measurement.
13	VCVB13EN	W	0h	Writes VC13EN for primary and VB13EN secondary measurement.
12	VCVB12EN	W	0h	Writes VC12EN for primary and VB12EN secondary measurement.
11	VCVB11EN	W	0h	Writes VC11EN for primary and VB11EN secondary measurement.
10	VCVB10EN	W	0h	Writes VC10EN for primary and VB10EN secondary measurement.
9	VCVB9EN	W	0h	Writes VC9EN for primary and VB9EN secondary measurement.
8	VCVB8EN	W	0h	Writes VC8EN for primary and VB8EN secondary measurement.
7	VCVB7EN	W	0h	Writes VC7EN for primary and VB7EN secondary measurement.
6	VCVB6EN	W	0h	Writes VC6EN for primary and VB6EN secondary measurement.
5	VCVB5EN	W	0h	Writes VC5EN for primary and VB5EN secondary measurement.
4	VCVB4EN	W	0h	Writes VC4EN for primary and VB4EN secondary measurement.
3	VCVB3EN	W	0h	Writes VC3EN for primary and VB3EN secondary measurement.
2	VCVB2EN	W	0h	Writes VC2EN for primary and VB2EN secondary measurement.
1	VCVB1EN	W	0h	Writes VC1EN for primary and VB1EN secondary measurement.
0	VCVB0EN	W	0h	Writes VC0EN for primary and VB0EN secondary measurement.

12.1.132 ALLM\_VCVB\_CFG1 register

Cell voltage measurement enable

Table 312. ALLM\_VCVB\_CFG1 register - cell voltage measurement enable (address 1409h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	W	W	W	W	W	W	W	W
Bit	7	6	5	4	3	2	1	0
Symbol	reserved						VCVB17EN	VCVB16EN
Reset	0	0	0	0	0	0	0	0
Access	W	W	W	W	W	W	W	W

Table 313. ALLM\_VCVB\_CFG1 register - cell voltage measurement enable (address 1409h)

Bit	Symbol	Access	Value	Description
15:2	reserved	W	0h	this read-only field is reserved and always has the value 0
1	VCVB17EN	W	0h	writes VC17EN for primary and VB17EN secondary measurement
0	VCVB16EN	W	0h	writes VC16EN for primary and VB16EN secondary measurement

12.1.133 PRMM\_CFG register

General measurement control

Table 314. PRMM\_CFG register - general measurement control (address 1800h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	BALPAUSELEN							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	7	6	5	4	3	2	1	0
Symbol	BALPAUSELEN						BALPAUSEC YCMODEN	MEASEN
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 315. PRMM\_CFG register - general measurement control (address 1800h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:2	BALPAUSELEN	R/W		Pause time of balancing before measurement cycle is executed. An on-going balancing pause operation is not influenced by a change of this value. <b>BALPAUSELEN</b> * 10 µs
			0000h*	NO_PAUSE (read-write) No Pause.



Table 315. PRMM\_CFG register - general measurement control (address 1800h)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
1	BALPAUSECYCM ODEN	R/W	0001h	PAUSE_10u (read-write) Pause = 10 us
			3FFFh	MAX (read-write) Maximum pause = 163830 us = 163 ms
				Enable balancing auto pause. This delays the start of measurements after entering Cyclic mode until the auto pause counter has elapsed.
0	MEASEN	R/W	0*	DISABLED (read-write) Auto pause for balancing is disabled.
			1	ENABLED (read-write) Auto pause for balancing is enabled. Measurements are started when the auto pause counter is elapsed.
				Enable the data acquisition. Setting this bit to zero initiates a result clear and invalidate action (this includes resetting all ready bits). This bit is cleared when entering Sleep mode. Cyclic measurements are always executed, regardless of the value of this bit. Balancing is not stopped automatically (if in Active mode), as it would be permanently inhibited while measurement is active. If balancing shall be paused, do so via the balancing control.
			0*	DISABLED (read-write) Data acquisition disabled
			1	ENABLED (read-write) Data acquisition enabled

## 12.1.134 PRMM\_APP\_CTRL register

Application measurement control

Table 316. PRMM\_APP\_CTRL register - application measurement control (address 1801h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	PAUSEBAL	VCOLNUM					CAPAIN7	CAPAIN6
Reset	0	1	1	1	1	1	0	0
Access	W	R/W	R/W	R/W	R/W	R/W	W	W
Bit	7	6	5	4	3	2	1	0
Symbol	CAPAIN5	CAPAIN4	CAPAIN3	CAPAIN2	CAPAIN1	CAPAIN0	CAPAINA	CAPVC
Reset	0	0	0	0	0	0	0	0
Access	W	W	W	W	W	W	W	W

Table 317. PRMM\_APP\_CTRL register - application measurement control (address 1801h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15	PAUSEBAL	W		Pause the balancing during this capture cycle. If balancing was not paused before, the start of data capture is delayed until the auto pause timer has elapsed. If no CAPxxx is set this bit is ignored.
			0*	NO_PAUSE (write) Continue with balancing.
			1	PAUSE (write) Pause the balancing during this capture cycle.
14:10	VCOLNUM	R/W		VC number for which the open-load detection is enabled.

Table 317. PRMM\_APP\_CTRL register - application measurement control (address 1801h)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
				<b>0 to 17</b> channel for which the open-load detection is enabled. <b>18 to 30</b> reserved (no open-load detection mechanism is enabled). Writing this bitfield is only possible if CAPVC is set as well.
			1Fh*	DISABLED (read-write) Open-load detection is disabled
9	CAPAIN7	W		AIN7 is not part of the primary measurement chain. Still, when used in combination with PAUSEBAL, a pause of the balancing is forced. The allows to keep the primary and secondary measurement chain synchronized.
			0*	NO_CAP (write) Measurements are not captured.
			1	CAP (write) Measurements are captured.
8	CAPAIN6	W		AIN6 is not part of the primary measurement chain. Still, when used in combination with PAUSEBAL, a pause of the balancing is forced. The allows to keep the primary and secondary measurement chain synchronized.
			0*	NO_CAP (write) Measurements are not captured.
			1	CAP (write) Measurements are captured.
7	CAPAIN5	W		AIN5 is not part of the primary measurement chain. Still, when used in combination with PAUSEBAL, a pause of the balancing is forced. The allows to keep the primary and secondary measurement chain synchronized.
			0*	NO_CAP (write) Measurements are not captured.
			1	CAP (write) Measurements are captured.
6	CAPAIN4	W		AIN4 is not part of the primary measurement chain. Still, when used in combination with PAUSEBAL, a pause of the balancing is forced. The allows to keep the primary and secondary measurement chain synchronized.
			0*	NO_CAP (write) Measurements are not captured.
			1	CAP (write) Measurements are captured.
5	CAPAIN3	W		Capture command for AIN3. When used in combination with PAUSEBAL, a pause of the balancing is forced.
			0*	NO_CAP (write) Measurements are not captured.
			1	CAP (write) Measurements are captured.
4	CAPAIN2	W		Capture command for AIN2. When used in combination with PAUSEBAL, a pause of the balancing is forced.
			0*	NO_CAP (write) Measurements are not captured.
			1	CAP (write) Measurements are captured.
3	CAPAIN1	W		Capture command for AIN1. When used in combination with PAUSEBAL, a pause of the balancing is forced.
			0*	NO_CAP (write) Measurements are not captured.
			1	CAP (write) Measurements are captured.
2	CAPAIN0	W		Capture command for AIN0. When used in combination with PAUSEBAL, a pause of the balancing is forced.
			0*	NO_CAP (write) Measurements are not captured.
			1	CAP (write) Measurements are captured.

Table 317. PRMM\_APP\_CTRL register - application measurement control (address 1801h)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
1	CAPAINA	W		Capture command for AINA. When used in combination with PAUSEBAL, a pause of the balancing is forced.
			0*	NO_CAP (write) Measurements are not captured.
			1	CAP (write) Measurements are captured.
0	CAPVC	W		Capture the application measurement values of the cell terminal measurements. The values are now readable via the app_result register. This bit is only available in the primary measurement chain.
			0*	NO_CAP (write) Measurements are not captured.
			1	CAP (write) Measurements are captured.

## 12.1.135 PRMM\_PER\_CTRL register

Periodic measurement control

Table 318. PRMM\_PER\_CTRL register - periodic measurement control (address 1802h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved			PERCTRL	reserved			PERLEN
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R/W	R	R	R	R/W
Bit	7	6	5	4	3	2	1	0
Symbol	PERLEN							
Reset	0	0	0	1	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 319. PRMM\_PER\_CTRL register - periodic measurement control (address 1802h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:13	reserved	R	0h	This read-only field is reserved and always has the value 0.
12	PERCTRL	R/W		Control the periodic result behavior.
			0*	AUTO (read-write) Periodic results are automatically updated
			1	ONCE (read-write) Periodic results are updated once with the last results. (each write updates the results).
11:9	reserved	R	0h	This read-only field is reserved and always has the value 0.
8:0	PERLEN	R/W		Number of measurements for one periodic measurement. The minimum is 16. Writing a value lower than 16 leads to a 16 in the register.
			010h*	PER_16 (read-write) minimum value = 16 measurements per period
			011h	PER_17 (read-write) 17 measurements per period
			1FFh	PER_MAX (read-write) maximum value = 511 measurements per period

12.1.136 PRMM\_SYNC\_CTRL register

Synchronous measurement control

Table 320. PRMM\_SYNC\_CTRL register - synchronous measurement control (address 1803h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	PAUSEBAL	reserved						
Reset	0	0	0	0	0	0	0	0
Access	W	W	W	W	W	W	W	W
Bit	7	6	5	4	3	2	1	0
Symbol	reserved						FASTCYC	SYNCCYC
Reset	0	0	0	0	0	0	0	0
Access	W	W	W	W	W	W	W	W

Table 321. PRMM\_SYNC\_CTRL register - synchronous measurement control (address 1803h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15	PAUSEBAL	W		Pause the balancing during this capture cycle. If balancing was not paused before, the start of data capture is delayed until the auto pause timer has elapsed. If no capture cycle is started this bit is ignored.
			0*	NO_PAUSE (write) Continue with balancing.
			1	PAUSE (write) Pause the balancing during this capture cycle.
14:2	reserved	W	0h	This read-only field is reserved and always has the value 0.
1	FASTCYC	W		Start of a dummy Fast measurement cycle. In this cycle nothing is actually measured and stored. The bit is only implemented to keep the balancing auto pause synchronous between primary and secondary measurement. If set together with SYNCCYC or during an active synchronous measurement cycle, this bit is ignored. Read as zero.
			0*	NO_FAST (write) No new start of a dummy fast measurement cycle.
			0*	STATUS (read) Read as zero.
			1	FAST (write) Start a new dummy fast measurement cycle.
0	SYNCCYC	W		Start a synchronous measurement cycle. In this cycle the CT and CB voltages are measured and stored as matching pairs. If no VC channel is enabled or if set during a running synchronous measurement cycle the set is ignored. Read as zero.
			0*	NO_START (write) No new start a synchronous measurement cycle.
			0*	STATUS (read) Read a zero
			1	START (write) Start a synchronous measurement cycle.

## 12.1.137 PRMM\_VC\_CFG0 register

Cell voltage measurement enable

Table 322. PRMM\_VC\_CFG0 register - cell voltage measurement enable (address 1808h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	VC15EN	VC14EN	VC13EN	VC12EN	VC11EN	VC10EN	VC9EN	VC8EN
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	7	6	5	4	3	2	1	0
Symbol	VC7EN	VC6EN	VC5EN	VC4EN	VC3EN	VC2EN	VC1EN	VC0EN
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 323. PRMM\_VC\_CFG0 register - cell voltage measurement enable (address 1808h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15	VC15EN	R/W		Enable measurement of cell voltage 15. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
14	VC14EN	R/W		Enable measurement of cell voltage 14. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
13	VC13EN	R/W		Enable measurement of cell voltage 13. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
12	VC12EN	R/W		Enable measurement of cell voltage 12. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
11	VC11EN	R/W		Enable measurement of cell voltage 11. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
10	VC10EN	R/W		Enable measurement of cell voltage 10. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
9	VC9EN	R/W		Enable measurement of cell voltage 9. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled

Table 323. PRMM\_VC\_CFG0 register - cell voltage measurement enable (address 1808h)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
8	VC8EN	R/W		Enable measurement of cell voltage 8. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
7	VC7EN	R/W		Enable measurement of cell voltage 7. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
6	VC6EN	R/W		Enable measurement of cell voltage 6. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
5	VC5EN	R/W		Enable measurement of cell voltage 5. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
4	VC4EN	R/W		Enable measurement of cell voltage 4. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
3	VC3EN	R/W		Enable measurement of cell voltage 3. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
2	VC2EN	R/W		Enable measurement of cell voltage 2. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
1	VC1EN	R/W		Enable measurement of cell voltage 1. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
0	VC0EN	R/W		Enable measurement of cell voltage 0. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled

## 12.1.138 PRMM\_VC\_CFG1 register

Cell voltage measurement enable

Table 324. PRMM\_VC\_CFG1 register - cell voltage measurement enable (address 1809h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	reserved						VC17EN	VC16EN
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R/W	R/W

Table 325. PRMM\_VC\_CFG1 register - cell voltage measurement enable (address 1809h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:2	reserved	R	0h	This read-only field is reserved and always has the value 0.
1	VC17EN	R/W		Enable measurement of cell voltage 17. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
0	VC16EN	R/W		Enable measurement of cell voltage 16. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled

## 12.1.139 PRMM\_AIN\_CFG register

AINx measurement enables

Table 326. PRMM\_AIN\_CFG register - AINx measurement enables (address 180Ah) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	RATIOMETRICAIN3		RATIOMETRICAIN2		RATIOMETRICAIN1		RATIOMETRICAIN0	
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	7	6	5	4	3	2	1	0
Symbol	reserved		FLTAPPINV	AINAEN	AIN3EN	AIN2EN	AIN1EN	AIN0EN
Reset	0	0	1	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Table 327. PRMM\_AIN\_CFG register - AINx measurement enables (address 180Ah)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:14	RATIOMETRICAIN3	R/W		Reference selection for AIN3. Changes to these bits during active measurement can lead to undefined results.
			00*	PRMVREF (read-write) Absolute (PRMVREF)
			01	RESERVED (read-write) reserved
			10	VAUX (read-write) Ratiometric (VAUX)
			11	VDDC (read-write) Ratiometric (VDDC)
13:12	RATIOMETRICAIN2	R/W		Reference selection for AIN2. Changes to these bits during active measurement can lead to undefined results.
			00*	PRMVREF (read-write) Absolute (PRMVREF)
			01	RESERVED (read-write) reserved
			10	VAUX (read-write) Ratiometric (VAUX)
			11	VDDC (read-write) Ratiometric (VDDC)
11:10	RATIOMETRICAIN1	R/W		Reference selection for AIN1. Changes to these bits during active measurement can lead to undefined results.
			00*	PRMVREF (read-write) Absolute (PRMVREF)
			01	RESERVED (read-write) reserved
			10	VAUX (read-write) Ratiometric (VAUX)
			11	VDDC (read-write) Ratiometric (VDDC)
9:8	RATIOMETRICAIN0	R/W		Reference selection for AIN0. Changes to these bits during active measurement can lead to undefined results.
			00*	PRMVREF (read-write) Absolute (PRMVREF)
			01	RESERVED (read-write) reserved
			10	VAUX (read-write) Ratiometric (VAUX)
			11	VDDC (read-write) Ratiometric (VDDC)
7:6	reserved	R	0h	This read-only field is reserved and always has the value 0.
5	FLTAPPINV	R/W		Invalidate AINx application results in case of fault.
			0	VALID (read-write) AINx application results are not invalidated in case of a fault
			1*	INVALID (read-write) AINx application results are invalidated when a fault is detected.
4	AINAEN	R/W		Enable measurement of AINA. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
3	AIN3EN	R/W		Enable measurement of AIN3. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled. If a GPIO output function is enabled on this GPIO, the GPIO output is automatically disabled. This is not reflected in the GPIO output enable bit.
2	AIN2EN	R/W		Enable measurement of AIN2. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled



Table 327. PRMM\_AIN\_CFG register - AINx measurement enables (address 180Ah)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
			1	ENABLED (read-write) Measurement enabled. If a GPIO output function is enabled on this GPIO, the GPIO output is automatically disabled. This is not reflected in the GPIO output enable bit.
1	AIN1EN	R/W		Enable measurement of AIN1. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled. If a GPIO output function is enabled on this GPIO, the GPIO output is automatically disabled. This is not reflected in the GPIO output enable bit.
0	AIN0EN	R/W		Enable measurement of AIN0. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled. If a GPIO output function is enabled on this GPIO, the GPIO output is automatically disabled. This is not reflected in the GPIO output enable bit.

## 12.1.140 PRMM\_AIN\_OL\_CFG register

AINx open-load detection enable

Table 328. PRMM\_AIN\_OL\_CFG register - AINx open-load detection enable (address 180Bh) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	reserved			AINAEN	AIN3EN	AIN2EN	AIN1EN	AIN0EN
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R/W	R/W	R/W	R/W	R/W

Table 329. PRMM\_AIN\_OL\_CFG register - AINx open-load detection enable (address 180Bh)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:5	reserved	R	0h	This read-only field is reserved and always has the value 0.
4	AINAEN	R/W		Open-load detection circuit for AINA
			0*	DISABLED (read-write) Disable the open-load detection circuit.
			1	ENABLED (read-write) Enable the open-load detection circuit.
3	AIN3EN	R/W		Open-load detection circuit for AIN3
			0*	DISABLED (read-write) Disable the open-load detection circuit.

Table 329. PRMM\_AIN\_OL\_CFG register - AINx open-load detection enable (address 180Bh)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
			1	ENABLED (read-write) Enable the open-load detection circuit.
2	AIN2EN	R/W		Open-load detection circuit for AIN2
			0*	DISABLED (read-write) Disable the open-load detection circuit.
			1	ENABLED (read-write) Enable the open-load detection circuit.
1	AIN1EN	R/W		Open-load detection circuit for AIN1
			0*	DISABLED (read-write) Disable the open-load detection circuit.
			1	ENABLED (read-write) Enable the open-load detection circuit.
0	AIN0EN	R/W		Open-load detection circuit for AIN0
			0*	DISABLED (read-write) Disable the open-load detection circuit.
			1	ENABLED (read-write) Enable the open-load detection circuit.

12.1.141 PRMM\_VBUF\_CFG register

Voltage buffer enable

Table 330. PRMM\_VBUF\_CFG register - voltage buffer enable (address 180Ch) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	reserved						VDDCEN	VAUXEN
Reset	0	0	0	0	0	0	1	1
Access	R	R	R	R	R	R	R/W	R/W

Table 331. PRMM\_VBUF\_CFG register - voltage buffer enable (address 180Ch)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:2	reserved	R	0h	This read-only field is reserved and always has the value 0.
1	VDDCEN	R/W		Voltage buffer for primary VDDC measurement
			0	DISABLED (read-write) Voltage buffer for primary VDDC measurement is disabled.
			1*	ENABLED (read-write) Voltage buffer for primary VDDC measurement is enabled.
0	VAUXEN	R/W		Voltage buffer for primary VAUX measurement
			0	DISABLED (read-write) Voltage buffer for primary VAUX measurement is disabled.

Table 331. PRMM\_VBUF\_CFG register - voltage buffer enable (address 180Ch)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
			1*	ENABLED (read-write) Voltage buffer for primary VAUX measurement is enabled.

## 12.1.142 PRMM\_VC\_OV\_UV\_CFG0 register

Cell voltage overvoltage and undervoltage check enable

Table 332. PRMM\_VC\_OV\_UV\_CFG0 register - cell voltage over-voltage and under-voltage check enable (address 1810h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	VC15EN	VC14EN	VC13EN	VC12EN	VC11EN	VC10EN	VC9EN	VC8EN
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	7	6	5	4	3	2	1	0
Symbol	VC7EN	VC6EN	VC5EN	VC4EN	VC3EN	VC2EN	VC1EN	VC0EN
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 333. PRMM\_VC\_OV\_UV\_CFG0 register - cell voltage over-voltage and under-voltage check enable (address 1810h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15	VC15EN	R/W		Include VC15 in VC over-voltage and under-voltage checks
			0*	NO_CHECK (read-write) VC15 is not included in VC over-voltage and under-voltage checks.
			1	UV_OV (read-write) VC15 is included in VC over-voltage and under-voltage checks.
14	VC14EN	R/W		Include VC14 in VC over-voltage and under-voltage checks
			0*	NO_CHECK (read-write) VC14 is not included in VC over-voltage and under-voltage checks.
			1	UV_OV (read-write) VC14 is included in VC over-voltage and under-voltage checks.
13	VC13EN	R/W		Include VC13 in VC over-voltage and under-voltage checks
			0*	NO_CHECK (read-write) VC13 is not included in VC over-voltage and under-voltage checks.
			1	UV_OV (read-write) VC13 is included in VC over-voltage and under-voltage checks.
12	VC12EN	R/W		Include VC12 in VC over-voltage and under-voltage checks
			0*	NO_CHECK (read-write) VC12 is not included in VC over-voltage and under-voltage checks.
			1	UV_OV (read-write) VC12 is included in VC over-voltage and under-voltage checks.
11	VC11EN	R/W		Include VC11 in VC over-voltage and under-voltage checks

**Table 333. PRMM\_VC\_OV\_UV\_CFG0 register - cell voltage over-voltage and under-voltage check enable (address 1810h)...***continued*

Legend: \* reset value

Bit	Symbol	Access	Value	Description
			0*	NO_CHECK (read-write) VC11 is not included in VC over-voltage and under-voltage checks.
			1	UV_OV (read-write) VC11 is included in VC over-voltage and under-voltage checks.
10	VC10EN	R/W		Include VC10 in VC over-voltage and under-voltage checks
			0*	NO_CHECK (read-write) VC10 is not included in VC over-voltage and under-voltage checks.
			1	UV_OV (read-write) VC10 is included in VC over-voltage and under-voltage checks.
9	VC9EN	R/W		Include VC9 in VC over-voltage and under-voltage checks
			0*	NO_CHECK (read-write) VC9 is not included in VC over-voltage and under-voltage checks.
			1	UV_OV (read-write) VC9 is included in VC over-voltage and under-voltage checks.
8	VC8EN	R/W		Include VC8 in VC over-voltage and under-voltage checks
			0*	NO_CHECK (read-write) VC8 is not included in VC over-voltage and under-voltage checks.
			1	UV_OV (read-write) VC8 is included in VC over-voltage and under-voltage checks.
7	VC7EN	R/W		Include VC7 in VC over-voltage and under-voltage checks
			0*	NO_CHECK (read-write) VC7 is not included in VC over-voltage and under-voltage checks.
			1	UV_OV (read-write) VC7 is included in VC over-voltage and under-voltage checks.
6	VC6EN	R/W		Include VC6 in VC over-voltage and under-voltage checks
			0*	NO_CHECK (read-write) VC6 is not included in VC over-voltage and under-voltage checks.
			1	UV_OV (read-write) VC6 is included in VC over-voltage and under-voltage checks.
5	VC5EN	R/W		Include VC5 in VC over-voltage and under-voltage checks
			0*	NO_CHECK (read-write) VC5 is not included in VC over-voltage and under-voltage checks.
			1	UV_OV (read-write) VC5 is included in VC over-voltage and under-voltage checks.
4	VC4EN	R/W		Include VC4 in VC over-voltage and under-voltage checks
			0*	NO_CHECK (read-write) VC4 is not included in VC over-voltage and under-voltage checks.
			1	UV_OV (read-write) VC4 is included in VC over-voltage and under-voltage checks.
3	VC3EN	R/W		Include VC3 in VC over-voltage and under-voltage checks
			0*	NO_CHECK (read-write) VC3 is not included in VC over-voltage and under-voltage checks.
			1	UV_OV (read-write) VC3 is included in VC over-voltage and under-voltage checks.
2	VC2EN	R/W		Include VC2 in VC over-voltage and under-voltage checks

**Table 333. PRMM\_VC\_OV\_UV\_CFG0 register - cell voltage over-voltage and under-voltage check enable (address 1810h)...***continued*

Legend: \* reset value

Bit	Symbol	Access	Value	Description
			0*	NO_CHECK (read-write) VC2 is not included in VC over-voltage and under-voltage checks.
			1	UV_OV (read-write) VC2 is included in VC over-voltage and under-voltage checks.
1	VC1EN	R/W		Include VC1 in VC over-voltage and under-voltage checks
			0*	NO_CHECK (read-write) VC1 is not included in VC over-voltage and under-voltage checks.
			1	UV_OV (read-write) VC1 is included in VC over-voltage and under-voltage checks.
0	VC0EN	R/W		Include VC0 in VC over-voltage and under-voltage checks
			0*	NO_CHECK (read-write) VC0 is not included in VC over-voltage and under-voltage checks.
			1	UV_OV (read-write) VC0 is included in VC over-voltage and under-voltage checks.

### 12.1.143 PRMM\_VC\_OV\_UV\_CFG1 register

Cell voltage over-voltage and under-voltage check enable

**Table 334. PRMM\_VC\_OV\_UV\_CFG1 register - cell voltage over-voltage and under-voltage check enable (address 1811h) bit allocation**

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	reserved						VC17EN	VC16EN
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R/W	R/W

**Table 335. PRMM\_VC\_OV\_UV\_CFG1 register - cell voltage over-voltage and under-voltage check enable (address 1811h)**

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:2	reserved	R	0h	This read-only field is reserved and always has the value 0.
1	VC17EN	R/W		Include VC17 in VC over-voltage and under-voltage checks
			0*	NO_CHECK (read-write) VC17 is not included in VC over-voltage and under-voltage checks.
			1	UV_OV (read-write) VC17 is included in VC over-voltage and under-voltage checks.
0	VC16EN	R/W		Include VC16 in VC over-voltage and under-voltage checks
			0*	NO_CHECK (read-write) VC16 is not included in VC over-voltage and under-voltage checks.

**Table 335. PRMM\_VC\_OV\_UV\_CFG1 register - cell voltage over-voltage and under-voltage check enable (address 1811h)...***continued*

Legend: \* reset value

Bit	Symbol	Access	Value	Description
			1	UV_OV (read-write) VC16 is included in VC over-voltage and under-voltage checks.

### 12.1.144 PRMM\_VC\_OV\_TH\_CFG register

Upper comparator limit for VC0 to VC17

**Table 336. PRMM\_VC\_OV\_TH\_CFG register - upper comparator limit for VC0 to VC17 (address 1812h) bit allocation**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	LIMIT															
Reset	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**Table 337. PRMM\_VC\_OV\_TH\_CFG register - upper comparator limit for VC0 to VC17 (address 1812h)**

Bit	Symbol	Access	Value	Description
15:0	LIMIT	R/W	7FFFh	Limit value. If this limit is reached, the OV status is activated.

### 12.1.145 PRMM\_VC\_UV0\_TH\_CFG register

Lower comparator limit 0 for VC0 to VC17

**Table 338. PRMM\_VC\_UV0\_TH\_CFG register - lower comparator limit 0 for VC0 to VC17 (address 1813h) bit allocation**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	LIMIT															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**Table 339. PRMM\_VC\_UV0\_TH\_CFG register - lower comparator limit 0 for VC0 to VC17 (address 1813h)**

Bit	Symbol	Access	Value	Description
15:0	LIMIT	R/W	0h	Limit value. If this limit is reached, the channel individual UV status is activated. Note: This limit is used for the channel individual balancing disable.

## 12.1.146 PRMM\_VC\_UV1\_TH\_CFG register

Lower comparator limit 1 for VC0 to VC17

**Table 340. PRMM\_VC\_UV1\_TH\_CFG register - lower comparator limit 1 for VC0 to VC17 (address 1814h) bit allocation**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	LIMIT															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**Table 341. PRMM\_VC\_UV1\_TH\_CFG register - lower comparator limit 1 for VC0 to VC17 (address 1814h)**

Bit	Symbol	Access	Value	Description
15:0	LIMIT	R/W	0h	Limit value. If this limit is reached, the global UV status is activated. Note: This limit is used for the global balancing disable.

## 12.1.147 PRMM\_AIN0\_OV\_TH\_CFG register

Upper comparator limit for AIN0

**Table 342. PRMM\_AIN0\_OV\_TH\_CFG register - upper comparator limit for AIN0 (address 1815h) bit allocation**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	LIMIT															
Reset	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**Table 343. PRMM\_AIN0\_OV\_TH\_CFG register - upper comparator limit for AIN0 (address 1815h)**

Bit	Symbol	Access	Value	Description
15:0	LIMIT	R/W	7FFFh	Limit value. If this limit is reached, the OV status is activated.

## 12.1.148 PRMM\_AIN1\_OV\_TH\_CFG register

Upper comparator limit for AIN1

**Table 344. PRMM\_AIN1\_OV\_TH\_CFG register - upper comparator limit for AIN1 (address 1816h) bit allocation**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	LIMIT															
Reset	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**Table 345. PRMM\_AIN1\_OV\_TH\_CFG register - upper comparator limit for AIN1 (address 1816h)**

Bit	Symbol	Access	Value	Description
15:0	LIMIT	R/W	7FFFh	Limit value. If this limit is reached, the OV status is activated.

**12.1.149 PRMM\_AIN2\_OV\_TH\_CFG register**

Upper comparator limit for AIN2

**Table 346. PRMM\_AIN2\_OV\_TH\_CFG register - upper comparator limit for AIN2 (address 1817h) bit allocation**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	LIMIT															
Reset	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**Table 347. PRMM\_AIN2\_OV\_TH\_CFG register - upper comparator limit for AIN2 (address 1817h)**

Bit	Symbol	Access	Value	Description
15:0	LIMIT	R/W	7FFFh	Limit value. If this limit is reached, the OV status is activated.

**12.1.150 PRMM\_AIN3\_OV\_TH\_CFG register**

Upper comparator limit for AIN3

**Table 348. PRMM\_AIN3\_OV\_TH\_CFG register - upper comparator limit for AIN3 (address 1818h) bit allocation**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	LIMIT															
Reset	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**Table 349. PRMM\_AIN3\_OV\_TH\_CFG register - upper comparator limit for AIN3 (address 1818h)**

Bit	Symbol	Access	Value	Description
15:0	LIMIT	R/W	7FFFh	Limit value. If this limit is reached, the OV status is activated.

**12.1.151 PRMM\_AINA\_OV\_TH\_CFG register**

Upper comparator limit for AINA

**Table 350. PRMM\_AINA\_OV\_TH\_CFG register - upper comparator limit for AINA (address 1819h) bit allocation**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	LIMIT															
Reset	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**Table 351. PRMM\_AINA\_OV\_TH\_CFG register - upper comparator limit for AINA (address 1819h)**

Bit	Symbol	Access	Value	Description
15:0	LIMIT	R/W	7FFFh	Limit value. If this limit is reached, the OV status is activated.



12.1.152 PRMM\_AIN0\_UV\_TH\_CFG register

Lower comparator limit for AIN0

Table 352. PRMM\_AIN0\_UV\_TH\_CFG register - lower comparator limit for AIN0 (address 181Ah) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	LIMIT															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 353. PRMM\_AIN0\_UV\_TH\_CFG register - lower comparator limit for AIN0 (address 181Ah)

Bit	Symbol	Access	Value	Description
15:0	LIMIT	R/W	8001h	Limit value. If this limit is reached, the UV status is activated.

12.1.153 PRMM\_AIN1\_UV\_TH\_CFG register

Lower comparator limit for AIN1

Table 354. PRMM\_AIN1\_UV\_TH\_CFG register - lower comparator limit for AIN1 (address 181Bh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	LIMIT															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 355. PRMM\_AIN1\_UV\_TH\_CFG register - lower comparator limit for AIN1 (address 181Bh)

Bit	Symbol	Access	Value	Description
15:0	LIMIT	R/W	8001h	Limit value. If this limit is reached, the UV status is activated.

12.1.154 PRMM\_AIN2\_UV\_TH\_CFG register

Lower comparator limit for AIN2

Table 356. PRMM\_AIN2\_UV\_TH\_CFG register - lower comparator limit for AIN2 (address 181Ch) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	LIMIT															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 357. PRMM\_AIN2\_UV\_TH\_CFG register - lower comparator limit for AIN2 (address 181Ch)

Bit	Symbol	Access	Value	Description
15:0	LIMIT	R/W	8001h	Limit value. If this limit is reached, the UV status is activated.

## 12.1.155 PRMM\_AIN3\_UV\_TH\_CFG register

Lower comparator limit for AIN3

**Table 358. PRMM\_AIN3\_UV\_TH\_CFG register - lower comparator limit for AIN3 (address 181Dh) bit allocation**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	LIMIT															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**Table 359. PRMM\_AIN3\_UV\_TH\_CFG register - lower comparator limit for AIN3 (address 181Dh)**

Bit	Symbol	Access	Value	Description
15:0	LIMIT	R/W	8001h	Limit value. If this limit is reached, the UV status is activated.

## 12.1.156 PRMM\_AINA\_UV\_TH\_CFG register

Lower comparator limit for AINA

**Table 360. PRMM\_AINA\_UV\_TH\_CFG register - lower comparator limit for AINA (address 181Eh) bit allocation**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	LIMIT															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**Table 361. PRMM\_AINA\_UV\_TH\_CFG register - lower comparator limit for AINA (address 181Eh)**

Bit	Symbol	Access	Value	Description
15:0	LIMIT	R/W	8001h	Limit value. If this limit is reached, the UV status is activated.

## 12.1.157 PRMM\_CAL\_CRC register

CRC over calibration data

**Table 362. PRMM\_CAL\_CRC register - CRC over calibration data (address 1820h) bit allocation**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	CRC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**Table 363. PRMM\_CAL\_CRC register - CRC over calibration data (address 1820h)**

Bit	Symbol	Access	Value	Description
15:0	CRC	R/W	0h	CRC over calibration data. The CRC calculation runs automatically every time when a synchronous measurement cycle is started and when the calibration data is read from the NVM.

Table 363. PRMM\_CAL\_CRC register - CRC over calibration data (address 1820h)...continued

Bit	Symbol	Access	Value	Description
			BEEFh	CALIBCRC (read-write) The expected value of the calibration CRC.

## 12.1.158 PRMM\_CFG\_CRC register

CRC over configuration values

Table 364. PRMM\_CFG\_CRC register - CRC over configuration values (address 1821h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	CRC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 365. PRMM\_CFG\_CRC register - CRC over configuration values (address 1821h)

Bit	Symbol	Access	Value	Description
15:0	CRC	R	0h	<p>This CRC value is recalculated with any transition into Active mode, with any write to a covered register and with any read to this register. The updated CRC value is available latest 100 µs after the last write. The CRC value is application specific and must be re-calculated by the MCU. The used polynomial is: <math>D175h (+1) = X^{16} + X^{15} + X^{13} + X^9 + X^7 + X^6 + X^5 + X^3 + X^1 + 1</math>.</p> <p>Following registers are included: PRMM_CFG, PRMM_PER_CTRL, PRMM_VC_CFG0, PRMM_VC_CFG1, PRMM_AIN_CFG, PRMM_VBUF_CFG, PRMM_VC_OV_UV_CFG0, PRMM_VC_OV_UV_CFG1, PRMM_VC_OV_TH_CFG, PRMM_VC_UV0_TH_CFG, PRMM_VC_UV1_TH_CFG, PRMM_AIN0_OV_TH_CFG, PRMM_AIN1_OV_TH_CFG, PRMM_AIN2_OV_TH_CFG, PRMM_AIN3_OV_TH_CFG, PRMM_AINA_OV_TH_CFG, PRMM_AIN0_UV_TH_CFG, PRMM_AIN1_UV_TH_CFG, PRMM_AIN2_UV_TH_CFG, PRMM_AIN3_UV_TH_CFG, PRMM_AINA_UV_TH_CFG.</p>

## 12.1.159 PRMM\_VC\_OV\_FLT\_STAT0 register

Cell voltage over-voltage status

Table 366. PRMM\_VC\_OV\_FLT\_STAT0 register - cell voltage over-voltage status (address 1822h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	VC15	VC14	VC13	VC12	VC11	VC10	VC9	VC8
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

**Table 366. PRMM\_VC\_OV\_FLT\_STAT0 register - cell voltage over-voltage status (address 1822h) bit allocation...continued**

Bit	7	6	5	4	3	2	1	0
Symbol	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

**Table 367. PRMM\_VC\_OV\_FLT\_STAT0 register - cell voltage over-voltage status (address 1822h)**

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15	VC15	R		Over-voltage status VC15 Read clears bit.
			0*	NO_OV (read) No over-voltage detected
			1	OV (read) Over-voltage detected
14	VC14	R		Over-voltage status VC14 Read clears bit.
			0*	NO_OV (read) No over-voltage detected
			1	OV (read) Over-voltage detected
13	VC13	R		Over-voltage status VC13 Read clears bit.
			0*	NO_OV (read) No over-voltage detected
			1	OV (read) Over-voltage detected
12	VC12	R		Over-voltage status VC12 Read clears bit.
			0*	NO_OV (read) No over-voltage detected
			1	OV (read) Over-voltage detected
11	VC11	R		Over-voltage status VC11 Read clears bit.
			0*	NO_OV (read) No over-voltage detected
			1	OV (read) Over-voltage detected
10	VC10	R		Over-voltage status VC10 Read clears bit.
			0*	NO_OV (read) No over-voltage detected
			1	OV (read) Over-voltage detected
9	VC9	R		Over-voltage status VC9 Read clears bit.
			0*	NO_OV (read) No over-voltage detected
			1	OV (read) Over-voltage detected
8	VC8	R		Over-voltage status VC8 Read clears bit.
			0*	NO_OV (read) No over-voltage detected
			1	OV (read) Over-voltage detected
7	VC7	R		Over-voltage status VC7 Read clears bit.
			0*	NO_OV (read) No over-voltage detected
			1	OV (read) Over-voltage detected
6	VC6	R		Over-voltage status VC6 Read clears bit.
			0*	NO_OV (read) No over-voltage detected
			1	OV (read) Over-voltage detected
5	VC5	R		Over-voltage status VC5 Read clears bit.
			0*	NO_OV (read) No over-voltage detected

Table 367. PRMM\_VC\_OV\_FLT\_STAT0 register - cell voltage over-voltage status (address 1822h)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
			1	OV (read) Over-voltage detected
4	VC4	R		Over-voltage status VC4 Read clears bit.
			0*	NO_OV (read) No over-voltage detected
			1	OV (read) Over-voltage detected
3	VC3	R		Over-voltage status VC3 Read clears bit.
			0*	NO_OV (read) No over-voltage detected
			1	OV (read) Over-voltage detected
2	VC2	R		Over-voltage status VC2 Read clears bit.
			0*	NO_OV (read) No over-voltage detected
			1	OV (read) Over-voltage detected
1	VC1	R		Over-voltage status VC1 Read clears bit.
			0*	NO_OV (read) No over-voltage detected
			1	OV (read) Over-voltage detected
0	VC0	R		Over-voltage status VC0 Read clears bit.
			0*	NO_OV (read) No over-voltage detected
			1	OV (read) Over-voltage detected

## 12.1.160 PRMM\_VC\_OV\_FLT\_STAT1 register

Cell voltage over-voltage status

Table 368. PRMM\_VC\_OV\_FLT\_STAT1 register - cell voltage over-voltage status (address 1823h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	reserved						VC17	VC16
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 369. PRMM\_VC\_OV\_FLT\_STAT1 register - cell voltage over-voltage status (address 1823h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:2	reserved	R	0h	This read-only field is reserved and always has the value 0.
1	VC17	R		Over-voltage status VC17 Read clears bit.
			0*	NO_OV (read) No over-voltage detected
			1	OV (read) Over-voltage detected
0	VC16	R		Over-voltage status VC16 Read clears bit.

Table 369. PRMM\_VC\_OV\_FLT\_STAT1 register - cell voltage over-voltage status (address 1823h)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
			0*	NO_OV (read) No over-voltage detected
			1	OV (read) Over-voltage detected

## 12.1.161 PRMM\_VC\_UV0\_FLT\_STAT0 register

Cell voltage under-voltage status regarding limit 0

Table 370. PRMM\_VC\_UV0\_FLT\_STAT0 register - cell voltage under-voltage status regarding limit 0 (address 1824h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	VC15	VC14	VC13	VC12	VC11	VC10	VC9	VC8
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 371. PRMM\_VC\_UV0\_FLT\_STAT0 register - cell voltage under-voltage status regarding limit 0 (address 1824h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15	VC15	R		Under-voltage status VC15 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
14	VC14	R		Under-voltage status VC14 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
13	VC13	R		Under-voltage status VC13 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
12	VC12	R		Under-voltage status VC12 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
11	VC11	R		Under-voltage status VC11 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
10	VC10	R		Under-voltage status VC10 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
9	VC9	R		Under-voltage status VC9 Read clears bit.

**Table 371. PRMM\_VC\_UV0\_FLT\_STAT0 register - cell voltage under-voltage status regarding limit 0 (address 1824h)...***continued*

Legend: \* reset value

Bit	Symbol	Access	Value	Description
8	VC8	R	0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
				Under-voltage status VC8 Read clears bit.
7	VC7	R	0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
				Under-voltage status VC7 Read clears bit.
6	VC6	R	0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
				Under-voltage status VC6 Read clears bit.
5	VC5	R	0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
				Under-voltage status VC5 Read clears bit.
4	VC4	R	0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
				Under-voltage status VC4 Read clears bit.
3	VC3	R	0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
				Under-voltage status VC3 Read clears bit.
2	VC2	R	0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
				Under-voltage status VC2 Read clears bit.
1	VC1	R	0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
				Under-voltage status VC1 Read clears bit.
0	VC0	R	0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
				Under-voltage status VC0 Read clears bit.

### 12.1.162 PRMM\_VC\_UV0\_FLT\_STAT1 register

Cell voltage under-voltage status regarding limit 0

**Table 372. PRMM\_VC\_UV0\_FLT\_STAT1 register - cell voltage under-voltage status regarding limit 0 (address 1825h) bit allocation**

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 372. PRMM\_VC\_UV0\_FLT\_STAT1 register - cell voltage under-voltage status regarding limit 0 (address 1825h) bit allocation...continued

Bit	7	6	5	4	3	2	1	0
Symbol	reserved						VC17	VC16
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 373. PRMM\_VC\_UV0\_FLT\_STAT1 register - cell voltage under-voltage status regarding limit 0 (address 1825h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:2	reserved	R	0h	This read-only field is reserved and always has the value 0.
1	VC17	R		Under-voltage status VC17 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
0	VC16	R		Under-voltage status VC16 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected

12.1.163 PRMM\_VC\_UV1\_FLT\_STAT0 register

Cell voltage under-voltage status regarding limit 1

Table 374. PRMM\_VC\_UV1\_FLT\_STAT0 register - cell voltage under-voltage status regarding limit 1 (address 1826h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	VC15	VC14	VC13	VC12	VC11	VC10	VC9	VC8
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 375. PRMM\_VC\_UV1\_FLT\_STAT0 register - cell voltage under-voltage status regarding limit 1 (address 1826h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15	VC15	R		Under-voltage status VC15 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
14	VC14	R		Under-voltage status VC14 Read clears bit.
			0*	NO_UV (read) No under-voltage detected



**Table 375. PRMM\_VC\_UV1\_FLT\_STAT0 register - cell voltage under-voltage status regarding limit 1 (address 1826h)...***continued*

Legend: \* reset value

Bit	Symbol	Access	Value	Description
			1	UV (read) Under-voltage detected
13	VC13	R		Under-voltage status VC13 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
12	VC12	R		Under-voltage status VC12 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
11	VC11	R		Under-voltage status VC11 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
10	VC10	R		Under-voltage status VC10 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
9	VC9	R		Under-voltage status VC9 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
8	VC8	R		Under-voltage status VC8 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
7	VC7	R		Under-voltage status VC7 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
6	VC6	R		Under-voltage status VC6 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
5	VC5	R		Under-voltage status VC5 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
4	VC4	R		Under-voltage status VC4 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
3	VC3	R		Under-voltage status VC3 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
2	VC2	R		Under-voltage status VC2 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
1	VC1	R		Under-voltage status VC1 Read clears bit.

**Table 375. PRMM\_VC\_UV1\_FLT\_STAT0 register - cell voltage under-voltage status regarding limit 1 (address 1826h)...***continued*

Legend: \* reset value

Bit	Symbol	Access	Value	Description
0	VC0	R	0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
				Under-voltage status VC0 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected

### 12.1.164 PRMM\_VC\_UV1\_FLT\_STAT1 register

Cell voltage under-voltage status regarding limit 1

**Table 376. PRMM\_VC\_UV1\_FLT\_STAT1 register - cell voltage under-voltage status regarding limit 1 (address 1827h) bit allocation**

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	reserved						VC17	VC16
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

**Table 377. PRMM\_VC\_UV1\_FLT\_STAT1 register - cell voltage under-voltage status regarding limit 1 (address 1827h)**

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:2	reserved	R	0h	This read-only field is reserved and always has the value 0.
1	VC17	R		Under-voltage status VC17 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
0	VC16	R		Under-voltage status VC16 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected

### 12.1.165 PRMM\_AIN\_OV\_FLT\_STAT register

AINx over-voltage status

**Table 378. PRMM\_AIN\_OV\_FLT\_STAT register - AINx over-voltage status (address 1828h) bit allocation**

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0

Table 378. PRMM\_AIN\_OV\_FLT\_STAT register - AINx over-voltage status (address 1828h) bit allocation...continued

Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	reserved			AINA	AIN3	AIN2	AIN1	AIN0
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 379. PRMM\_AIN\_OV\_FLT\_STAT register - AINx over-voltage status (address 1828h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:5	reserved	R	0h	This read-only field is reserved and always has the value 0.
4	AINA	R		Over-voltage status AINA Read clears bit.
			0*	NO_OV (read) No over-voltage detected
			1	OV (read) Over-voltage detected
3	AIN3	R		Over-voltage status AIN3 Read clears bit.
			0*	NO_OV (read) No over-voltage detected
			1	OV (read) Over-voltage detected
2	AIN2	R		Over-voltage status AIN2 Read clears bit.
			0*	NO_OV (read) No over-voltage detected
			1	OV (read) Over-voltage detected
1	AIN1	R		Over-voltage status AIN1 Read clears bit.
			0*	NO_OV (read) No over-voltage detected
			1	OV (read) Over-voltage detected
0	AIN0	R		Over-voltage status AIN0 Read clears bit.
			0*	NO_OV (read) No over-voltage detected
			1	OV (read) Over-voltage detected

## 12.1.166 PRMM\_AIN\_UV\_FLT\_STAT register

AINx under-voltage status

Table 380. PRMM\_AIN\_UV\_FLT\_STAT register - AINx under-voltage status (address 1829h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	reserved			AINA	AIN3	AIN2	AIN1	AIN0
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 381. PRMM\_AIN\_UV\_FLT\_STAT register - AINx under-voltage status (address 1829h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:5	reserved	R	0h	This read-only field is reserved and always has the value 0.
4	AINA	R		Under-voltage status AINA Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
3	AIN3	R		Under-voltage status AIN3 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
2	AIN2	R		Under-voltage status AIN2 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
1	AIN1	R		Under-voltage status AIN1 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
0	AIN0	R		Under-voltage status AIN0 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected

## 12.1.167 PRMM\_MEAS\_STAT register

Measurement status

Table 382. PRMM\_MEAS\_STAT register - measurement status (address 183Eh) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	MEASFLT	COMFLT	ANAFLT	SUPPLYFLT	reserved		SYNCRDY	PERRDY
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	reserved		APPRDYAIN3	APPRDYAIN2	APPRDYAIN1	APPRDYAIN0	APPRDYAINA	APPRDYVC
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 383. PRMM\_MEAS\_STAT register - measurement status (address 183Eh)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15	MEASFLT	R		Measurement fault status
			0*	NO_FLT (read) No measurement fault detected
			1	FAULT (read) Measurement fault detected
14	COMFLT	R		Communication fault status
			0*	NO_FLT (read) No communication fault detected
			1	FAULT (read) Communication fault detected.

Table 383. PRMM\_MEAS\_STAT register - measurement status (address 183Eh)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
13	ANAFLT	R		Analog fault status
			0*	NO_FLT (read) No analog fault detected
			1	FAULT (read) Analog fault detected
12	SUPPLYFLT	R		Internal/external supply fault status
			0*	NO_FLT (read) No supply error detected
			1	FAULT (read) Supply error detected
11:10	reserved	R	0h	This read-only field is reserved and always has the value 0.
9	SYNCRDY	R		Synchronous measurement data is ready for readout, the bit is cleared by a read into the safety result range.
			0*	NO_DATA (read) No data available
			1	DATA (read) Sample data available.
8	PERRDY	R		New periodic result data has been created (depending on the periodic update mode, they might need to be requested), the bit is cleared by a read to any register in the range PRMM_PER_VC0 to (PRMM_PER_VDDC + 1) if PRMM_PER_CTRL.PERCTRL is set to AUTO. If PRMM_PER_CTRL.PERCTRL is set to ONCE, a write to PRMM_PER_CTRL.PERCTRL == ONCE clears it.
			0*	NO_DATA (read) No data available
			1	DATA (read) Sample data available.
7:6	reserved	R	0h	This read-only field is reserved and always has the value 0.
5	APPRDYAIN3	R		A new AIN3 application result can be requested / captured.
			0*	NO_DATA (read) No data available (<16 sample)
			1	DATA (read) Data can be captured (>=16 samples are captured).
4	APPRDYAIN2	R		A new AIN2 application result can be requested / captured.
			0*	NO_DATA (read) No data available (<16 sample)
			1	DATA (read) Data can be captured (>=16 samples are captured).
3	APPRDYAIN1	R		A new AIN1 application result can be requested / captured.
			0*	NO_DATA (read) No data available (<16 sample)
			1	DATA (read) Data can be captured (>=16 samples are captured).
2	APPRDYAIN0	R		A new AIN0 application result can be requested / captured.
			0*	NO_DATA (read) No data available (<16 sample)
			1	DATA (read) Data can be captured (>=16 samples are captured).
1	APPRDYAINA	R		A new AINA application result can be requested / captured.
			0*	NO_DATA (read) No data available (<16 sample)
			1	DATA (read) Data can be captured (>=16 samples are captured).
0	APPRDYVC	R		A new VC application result can be requested / captured.
			0*	NO_DATA (read) No data available (<16 sample)

Table 383. PRMM\_MEAS\_STAT register - measurement status (address 183Eh)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
			1	DATA (read) Data can be captured (>=16 samples are captured).

## 12.1.168 PRMM\_APP\_VC\_CNT register

Application measurement VC sample count number

Table 384. PRMM\_APP\_VC\_CNT register - application measurement VC sample count number (address 183Fh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	NUM															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 385. PRMM\_APP\_VC\_CNT register - application measurement VC sample count number (address 183Fh)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:0	NUM	R		Number of samples used for Application result. Read clears bits.
			0000h*	LOW (read) Zero or insufficient samples, VC Application results are invalid.
			FFFFh	OVERRUN (read) Sample counter overrun, VC Application results are invalid.

## 12.1.169 PRMM\_APP\_VC0 register

Application measurement result cell 0

Table 386. PRMM\_APP\_VC0 register - application measurement result cell 0 (address 1840h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 387. PRMM\_APP\_VC0 register - application measurement result cell 0 (address 1840h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 0 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.170 PRMM\_APP\_VC1 register

Application measurement result cell 1

Table 388. PRMM\_APP\_VC1 register - application measurement result cell 1 (address 1841h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 389. PRMM\_APP\_VC1 register - application measurement result cell 1 (address 1841h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 1 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.171 PRMM\_APP\_VC2 register

Application measurement result cell 2

Table 390. PRMM\_APP\_VC2 register - application measurement result cell 2 (address 1842h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 391. PRMM\_APP\_VC2 register - application measurement result cell 2 (address 1842h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 2 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.172 PRMM\_APP\_VC3 register

Application measurement result cell 3

Table 392. PRMM\_APP\_VC3 register - application measurement result cell 3 (address 1843h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 393. PRMM\_APP\_VC3 register - application measurement result cell 3 (address 1843h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 3 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.173 PRMM\_APP\_VC4 register

Application measurement result cell 4

Table 394. PRMM\_APP\_VC4 register - application measurement result cell 4 (address 1844h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 395. PRMM\_APP\_VC4 register - application measurement result cell 4 (address 1844h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 4 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.174 PRMM\_APP\_VC5 register

Application measurement result cell 5

Table 396. PRMM\_APP\_VC5 register - application measurement result cell 5 (address 1845h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 397. PRMM\_APP\_VC5 register - application measurement result cell 5 (address 1845h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 5 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.175 PRMM\_APP\_VC6 register

Application measurement result cell 6

Table 398. PRMM\_APP\_VC6 register - application measurement result cell 6 (address 1846h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R



Table 399. PRMM\_APP\_VC6 register - application measurement result cell 6 (address 1846h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 6 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.176 PRMM\_APP\_VC7 register

Application measurement result cell 7

Table 400. PRMM\_APP\_VC7 register - application measurement result cell 7 (address 1847h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 401. PRMM\_APP\_VC7 register - application measurement result cell 7 (address 1847h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 7 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.177 PRMM\_APP\_VC8 register

Application measurement result cell 8

Table 402. PRMM\_APP\_VC8 register - application measurement result cell 8 (address 1848h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 403. PRMM\_APP\_VC8 register - application measurement result cell 8 (address 1848h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 8 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.178 PRMM\_APP\_VC9 register

Application measurement result cell 9

Table 404. PRMM\_APP\_VC9 register - application measurement result cell 9 (address 1849h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 405. PRMM\_APP\_VC9 register - application measurement result cell 9 (address 1849h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 9 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

12.1.179 PRMM\_APP\_VC10 register

Application measurement result cell 10

Table 406. PRMM\_APP\_VC10 register - application measurement result cell 10 (address 184Ah) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 407. PRMM\_APP\_VC10 register - application measurement result cell 10 (address 184Ah)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 10 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

12.1.180 PRMM\_APP\_VC11 register

Application measurement result cell 11

Table 408. PRMM\_APP\_VC11 register - application measurement result cell 11 (address 184Bh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 409. PRMM\_APP\_VC11 register - application measurement result cell 11 (address 184Bh)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 11 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

12.1.181 PRMM\_APP\_VC12 register

Application measurement result cell 12

Table 410. PRMM\_APP\_VC12 register - application measurement result cell 12 (address 184Ch) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															

**Table 410. PRMM\_APP\_VC12 register - application measurement result cell 12 (address 184Ch) bit allocation...***continued*

Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

**Table 411. PRMM\_APP\_VC12 register - application measurement result cell 12 (address 184Ch)**

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 12 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

**12.1.182 PRMM\_APP\_VC13 register**

Application measurement result cell 13

**Table 412. PRMM\_APP\_VC13 register - application measurement result cell 13 (address 184Dh) bit allocation**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

**Table 413. PRMM\_APP\_VC13 register - application measurement result cell 13 (address 184Dh)**

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 13 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

**12.1.183 PRMM\_APP\_VC14 register**

Application measurement result cell 14

**Table 414. PRMM\_APP\_VC14 register - application measurement result cell 14 (address 184Eh) bit allocation**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

**Table 415. PRMM\_APP\_VC14 register - application measurement result cell 14 (address 184Eh)**

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 14 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.184 PRMM\_APP\_VC15 register

Application measurement result cell 15

Table 416. PRMM\_APP\_VC15 register - application measurement result cell 15 (address 184Fh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 417. PRMM\_APP\_VC15 register - application measurement result cell 15 (address 184Fh)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 15 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.185 PRMM\_APP\_VC16 register

Application measurement result cell 16

Table 418. PRMM\_APP\_VC16 register - application measurement result cell 16 (address 1850h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 419. PRMM\_APP\_VC16 register - application measurement result cell 16 (address 1850h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 16 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.186 PRMM\_APP\_VC17 register

Application measurement result cell 17

Table 420. PRMM\_APP\_VC17 register - application measurement result cell 17 (address 1851h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 421. PRMM\_APP\_VC17 register - application measurement result cell 17 (address 1851h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 17 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.187 PRMM\_APP\_AINA register

Application measurement result AINA

Table 422. PRMM\_APP\_AINA register - application measurement result AINA (address 1852h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 423. PRMM\_APP\_AINA register - application measurement result AINA (address 1852h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of AINA at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.188 PRMM\_APP\_AIN0 register

Application measurement result AIN0

Table 424. PRMM\_APP\_AIN0 register - application measurement result AIN0 (address 1853h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 425. PRMM\_APP\_AIN0 register - application measurement result AIN0 (address 1853h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of AIN0 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.189 PRMM\_APP\_AIN1 register

Application measurement result AIN1

Table 426. PRMM\_APP\_AIN1 register - application measurement result AIN1 (address 1854h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 427. PRMM\_APP\_AIN1 register - application measurement result AIN1 (address 1854h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of AIN1 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.190 PRMM\_APP\_AIN2 register

Application measurement result AIN2

Table 428. PRMM\_APP\_AIN2 register - application measurement result AIN2 (address 1855h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 429. PRMM\_APP\_AIN2 register - application measurement result AIN2 (address 1855h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of AIN2 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.191 PRMM\_APP\_AIN3 register

Application measurement result AIN3

Table 430. PRMM\_APP\_AIN3 register - application measurement result AIN3 (address 1856h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 431. PRMM\_APP\_AIN3 register - application measurement result AIN3 (address 1856h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of AIN3 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.192 PRMM\_PER\_NUM register

Measurement period number of the primary periodic results

Table 432. PRMM\_PER\_NUM register - measurement period number of the primary periodic results (address 185Fh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	NUM															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

**Table 433. PRMM\_PER\_NUM register - measurement period number of the primary periodic results (address 185Fh)**

Bit	Symbol	Access	Value	Description
15:0	NUM	R	0h	Number of the periodic cycle in which the primary periodic results have been created. The value is incremented for each periodic cycle executed. The counting wraps at its limit.

**12.1.193 PRMM\_PER\_VC0 register**

Periodic measurement result cell 0

**Table 434. PRMM\_PER\_VC0 register - periodic measurement result cell 0 (address 1860h) bit allocation**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

**Table 435. PRMM\_PER\_VC0 register - periodic measurement result cell 0 (address 1860h)**

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 0 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

**12.1.194 PRMM\_PER\_VC1 register**

Periodic measurement result cell 1

**Table 436. PRMM\_PER\_VC1 register - periodic measurement result cell 1 (address 1861h) bit allocation**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

**Table 437. PRMM\_PER\_VC1 register - periodic measurement result cell 1 (address 1861h)**

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 1 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

**12.1.195 PRMM\_PER\_VC2 register**

Periodic measurement result cell 2

**Table 438. PRMM\_PER\_VC2 register - periodic measurement result cell 2 (address 1862h) bit allocation**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 439. PRMM\_PER\_VC2 register - periodic measurement result cell 2 (address 1862h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 2 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.196 PRMM\_PER\_VC3 register

Periodic measurement result cell 3

Table 440. PRMM\_PER\_VC3 register - periodic measurement result cell 3 (address 1863h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 441. PRMM\_PER\_VC3 register - periodic measurement result cell 3 (address 1863h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 3 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.197 PRMM\_PER\_VC4 register

Periodic measurement result cell 4

Table 442. PRMM\_PER\_VC4 register - periodic measurement result cell 4 (address 1864h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 443. PRMM\_PER\_VC4 register - periodic measurement result cell 4 (address 1864h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 4 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.198 PRMM\_PER\_VC5 register

Periodic measurement result cell 5

Table 444. PRMM\_PER\_VC5 register - periodic measurement result cell 5 (address 1865h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R



Table 445. PRMM\_PER\_VC5 register - periodic measurement result cell 5 (address 1865h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 5 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.199 PRMM\_PER\_VC6 register

Periodic measurement result cell 6

Table 446. PRMM\_PER\_VC6 register - periodic measurement result cell 6 (address 1866h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 447. PRMM\_PER\_VC6 register - periodic measurement result cell 6 (address 1866h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 6 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.200 PRMM\_PER\_VC7 register

Periodic measurement result cell 7

Table 448. PRMM\_PER\_VC7 register - periodic measurement result cell 7 (address 1867h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 449. PRMM\_PER\_VC7 register - periodic measurement result cell 7 (address 1867h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 7 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.201 PRMM\_PER\_VC8 register

Periodic measurement result cell 8

Table 450. PRMM\_PER\_VC8 register - periodic measurement result cell 8 (address 1868h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 451. PRMM\_PER\_VC8 register - periodic measurement result cell 8 (address 1868h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 8 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.202 PRMM\_PER\_VC9 register

Periodic measurement result cell 9

Table 452. PRMM\_PER\_VC9 register - periodic measurement result cell 9 (address 1869h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 453. PRMM\_PER\_VC9 register - periodic measurement result cell 9 (address 1869h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 9 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.203 PRMM\_PER\_VC10 register

Periodic measurement result cell 10

Table 454. PRMM\_PER\_VC10 register - periodic measurement result cell 10 (address 186Ah) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 455. PRMM\_PER\_VC10 register - periodic measurement result cell 10 (address 186Ah)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 10 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.204 PRMM\_PER\_VC11 register

Periodic measurement result cell 11

Table 456. PRMM\_PER\_VC11 register - periodic measurement result cell 11 (address 186Bh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 457. PRMM\_PER\_VC11 register - periodic measurement result cell 11 (address 186Bh)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 11 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.205 PRMM\_PER\_VC12 register

Periodic measurement result cell 12

Table 458. PRMM\_PER\_VC12 register - periodic measurement result cell 12 (address 186Ch) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 459. PRMM\_PER\_VC12 register - periodic measurement result cell 12 (address 186Ch)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 12 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.206 PRMM\_PER\_VC13 register

Periodic measurement result cell 13

Table 460. PRMM\_PER\_VC13 register - periodic measurement result cell 13 (address 186Dh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 461. PRMM\_PER\_VC13 register - periodic measurement result cell 13 (address 186Dh)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 13 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.207 PRMM\_PER\_VC14 register

Periodic measurement result cell 14

Table 462. PRMM\_PER\_VC14 register - periodic measurement result cell 14 (address 186Eh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 463. PRMM\_PER\_VC14 register - periodic measurement result cell 14 (address 186Eh)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 14 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.208 PRMM\_PER\_VC15 register

Periodic measurement result cell 15

Table 464. PRMM\_PER\_VC15 register - periodic measurement result cell 15 (address 186Fh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 465. PRMM\_PER\_VC15 register - periodic measurement result cell 15 (address 186Fh)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 15 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.209 PRMM\_PER\_VC16 register

Periodic measurement result cell 16

Table 466. PRMM\_PER\_VC16 register - periodic measurement result cell 16 (address 1870h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 467. PRMM\_PER\_VC16 register - periodic measurement result cell 16 (address 1870h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 16 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.210 PRMM\_PER\_VC17 register

Periodic measurement result cell 17

Table 468. PRMM\_PER\_VC17 register - periodic measurement result cell 17 (address 1871h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 469. PRMM\_PER\_VC17 register - periodic measurement result cell 17 (address 1871h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 17 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.211 PRMM\_PER\_AINA register

Periodic measurement result AINA

Table 470. PRMM\_PER\_AINA register - periodic measurement result AINA (address 1872h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 471. PRMM\_PER\_AINA register - periodic measurement result AINA (address 1872h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of AINA of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.212 PRMM\_PER\_AIN0 register

Periodic measurement result AIN0

Table 472. PRMM\_PER\_AIN0 register - periodic measurement result AIN0 (address 1873h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 473. PRMM\_PER\_AIN0 register - periodic measurement result AIN0 (address 1873h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of AIN0 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.213 PRMM\_PER\_AIN1 register

Periodic measurement result AIN1

Table 474. PRMM\_PER\_AIN1 register - periodic measurement result AIN1 (address 1874h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 475. PRMM\_PER\_AIN1 register - periodic measurement result AIN1 (address 1874h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of AIN1 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.214 PRMM\_PER\_AIN2 register

Periodic measurement result AIN2

Table 476. PRMM\_PER\_AIN2 register - periodic measurement result AIN2 (address 1875h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 477. PRMM\_PER\_AIN2 register - periodic measurement result AIN2 (address 1875h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of AIN2 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.215 PRMM\_PER\_AIN3 register

Periodic measurement result AIN3

Table 478. PRMM\_PER\_AIN3 register - periodic measurement result AIN3 (address 1876h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 479. PRMM\_PER\_AIN3 register - periodic measurement result AIN3 (address 1876h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of AIN3 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.216 PRMM\_PER\_PRMTEMP register

Periodic measurement result primary device temperature

Table 480. PRMM\_PER\_PRMTEMP register - periodic measurement result primary device temperature (address 1877h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

**Table 481. PRMM\_PER\_PRMTMP register - periodic measurement result primary device temperature (address 1877h)**

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured value of primary temperature sensor of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

**12.1.217 PRMM\_PER\_SECVREF register**

Periodic measurement result secondary voltage reference

**Table 482. PRMM\_PER\_SECVREF register - periodic measurement result secondary voltage reference (address 1878h) bit allocation**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

**Table 483. PRMM\_PER\_SECVREF register - periodic measurement result secondary voltage reference (address 1878h)**

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of secondary reference voltage of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

**12.1.218 PRMM\_PER\_VAUX register**

Periodic measurement result auxiliary supply voltage

**Table 484. PRMM\_PER\_VAUX register - periodic measurement result auxiliary supply voltage (address 1879h) bit allocation**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

**Table 485. PRMM\_PER\_VAUX register - periodic measurement result auxiliary supply voltage (address 1879h)**

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of VAUX of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.219 PRMM\_PER\_VDDC register

Periodic measurement result VDDC

Table 486. PRMM\_PER\_VDDC register - periodic measurement result VDDC (address 187Ah) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 487. PRMM\_PER\_VDDC register - periodic measurement result VDDC (address 187Ah)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of VDDC of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.220 PRMM\_SYNC\_NUM register

Measurement period number of the synchronous results.

Table 488. PRMM\_SYNC\_NUM register - measurement period number of the synchronous results. (address 187Fh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	NUM															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 489. PRMM\_SYNC\_NUM register - measurement period number of the synchronous results. (address 187Fh)

Bit	Symbol	Access	Value	Description
15:0	NUM	R	0h	Number of the synchronous cycle in which the synchronous results have been created. The value is incremented for each synchronous cycle executed. The counting wraps at its limit.

## 12.1.221 PRMM\_SYNC\_VC0 register

Synchronous measurement result cell 0

Table 490. PRMM\_SYNC\_VC0 register - synchronous measurement result cell 0 (address 1880h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R



Table 491. PRMM\_SYNC\_VC0 register - synchronous measurement result cell 0 (address 1880h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 0 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.222 PRMM\_SYNC\_VC1 register

Synchronous measurement result cell 1

Table 492. PRMM\_SYNC\_VC1 register - synchronous measurement result cell 1 (address 1881h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 493. PRMM\_SYNC\_VC1 register - synchronous measurement result cell 1 (address 1881h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 1 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.223 PRMM\_SYNC\_VC2 register

Synchronous measurement result cell 2

Table 494. PRMM\_SYNC\_VC2 register - synchronous measurement result cell 2 (address 1882h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 495. PRMM\_SYNC\_VC2 register - synchronous measurement result cell 2 (address 1882h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 2 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.224 PRMM\_SYNC\_VC3 register

Synchronous measurement result cell 3

Table 496. PRMM\_SYNC\_VC3 register - synchronous measurement result cell 3 (address 1883h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															

Table 496. PRMM\_SYNC\_VC3 register - synchronous measurement result cell 3 (address 1883h) bit allocation...continued

Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 497. PRMM\_SYNC\_VC3 register - synchronous measurement result cell 3 (address 1883h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 3 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.225 PRMM\_SYNC\_VC4 register

Synchronous measurement result cell 4

Table 498. PRMM\_SYNC\_VC4 register - synchronous measurement result cell 4 (address 1884h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 499. PRMM\_SYNC\_VC4 register - synchronous measurement result cell 4 (address 1884h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 4 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.226 PRMM\_SYNC\_VC5 register

Synchronous measurement result cell 5

Table 500. PRMM\_SYNC\_VC5 register - synchronous measurement result cell 5 (address 1885h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 501. PRMM\_SYNC\_VC5 register - synchronous measurement result cell 5 (address 1885h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 5 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.227 PRMM\_SYNC\_VC6 register

Synchronous measurement result cell 6

Table 502. PRMM\_SYNC\_VC6 register - synchronous measurement result cell 6 (address 1886h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 503. PRMM\_SYNC\_VC6 register - synchronous measurement result cell 6 (address 1886h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 6 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.228 PRMM\_SYNC\_VC7 register

Synchronous measurement result cell 7

Table 504. PRMM\_SYNC\_VC7 register - synchronous measurement result cell 7 (address 1887h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 505. PRMM\_SYNC\_VC7 register - synchronous measurement result cell 7 (address 1887h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 7 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.229 PRMM\_SYNC\_VC8 register

Synchronous measurement result cell 8

Table 506. PRMM\_SYNC\_VC8 register - synchronous measurement result cell 8 (address 1888h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 507. PRMM\_SYNC\_VC8 register - synchronous measurement result cell 8 (address 1888h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 8 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.230 PRMM\_SYNC\_VC9 register

Synchronous measurement result cell 9

Table 508. PRMM\_SYNC\_VC9 register - synchronous measurement result cell 9 (address 1889h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 509. PRMM\_SYNC\_VC9 register - synchronous measurement result cell 9 (address 1889h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 9 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.231 PRMM\_SYNC\_VC10 register

Synchronous measurement result cell 10

Table 510. PRMM\_SYNC\_VC10 register - synchronous measurement result cell 10 (address 188Ah) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 511. PRMM\_SYNC\_VC10 register - synchronous measurement result cell 10 (address 188Ah)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 10 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.232 PRMM\_SYNC\_VC11 register

Synchronous measurement result cell 11

Table 512. PRMM\_SYNC\_VC11 register - synchronous measurement result cell 11 (address 188Bh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															

Table 512. PRMM\_SYNC\_VC11 register - synchronous measurement result cell 11 (address 188Bh) bit allocation...continued

Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 513. PRMM\_SYNC\_VC11 register - synchronous measurement result cell 11 (address 188Bh)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 11 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.233 PRMM\_SYNC\_VC12 register

Synchronous measurement result cell 12

Table 514. PRMM\_SYNC\_VC12 register - synchronous measurement result cell 12 (address 188Ch) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 515. PRMM\_SYNC\_VC12 register - synchronous measurement result cell 12 (address 188Ch)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 12 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.234 PRMM\_SYNC\_VC13 register

Synchronous measurement result cell 13

Table 516. PRMM\_SYNC\_VC13 register - synchronous measurement result cell 13 (address 188Dh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 517. PRMM\_SYNC\_VC13 register - synchronous measurement result cell 13 (address 188Dh)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 13 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.235 PRMM\_SYNC\_VC14 register

Synchronous measurement result cell 14

Table 518. PRMM\_SYNC\_VC14 register - synchronous measurement result cell 14 (address 188Eh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 519. PRMM\_SYNC\_VC14 register - synchronous measurement result cell 14 (address 188Eh)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 14 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.236 PRMM\_SYNC\_VC15 register

Synchronous measurement result cell 15

Table 520. PRMM\_SYNC\_VC15 register - synchronous measurement result cell 15 (address 188Fh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 521. PRMM\_SYNC\_VC15 register - synchronous measurement result cell 15 (address 188Fh)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 15 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.237 PRMM\_SYNC\_VC16 register

Synchronous measurement result cell 16

Table 522. PRMM\_SYNC\_VC16 register - synchronous measurement result cell 16 (address 1890h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 523. PRMM\_SYNC\_VC16 register - synchronous measurement result cell 16 (address 1890h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 16 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.238 PRMM\_SYNC\_VC17 register

Synchronous measurement result cell 17

Table 524. PRMM\_SYNC\_VC17 register - synchronous measurement result cell 17 (address 1891h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 525. PRMM\_SYNC\_VC17 register - synchronous measurement result cell 17 (address 1891h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 17 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.239 SECM\_CFG register

General measurement control

Table 526. SECM\_CFG register - general measurement control (address 1C00h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	BALPAUSELEN							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	7	6	5	4	3	2	1	0
Symbol	BALPAUSELEN						BALPAUSEC YCMODEN	MEASEN
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 527. SECM\_CFG register - general measurement control (address 1C00h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:2	BALPAUSELEN	R/W		Pause time of balancing before measurement cycle is executed. An on-going balancing pause operation is not influenced by a change of this value. <b>BALPAUSELEN</b> * 10 $\mu$ s
			0000h*	NO_PAUSE (read-write) No Pause.
			0001h	PAUSE_10u (read-write) Pause = 10 $\mu$ s

Table 527. SECM\_CFG register - general measurement control (address 1C00h)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
			3FFFh	MAX (read-write) Maximum pause = 163830 us = 163 ms
1	BALPAUSECYCM ODEN	R/W		Enable balancing auto pause. This delays the start of measurements after entering Cyclic mode until the auto pause counter has elapsed. This field has no effect in secondary measurement.
			0*	DISABLED (read-write) auto pause for balancing is disabled.
			1	ENABLED (read-write) auto pause for balancing is enabled. Measurements are started when the auto pause counter is elapsed.
0	MEASEN	R/W		Enable the data acquisition. Setting this bit to zero initiates a result clear and invalidate action (this includes resetting all ready bits). This bit is cleared when entering Sleep mode. Cyclic measurements are always executed, regardless of the value of this bit. Balancing is not stopped automatically (if in Active mode), as it would be permanently inhibited while measurement is active. If balancing shall be paused, do so via the balancing control.
			0*	DISABLED (read-write) Data acquisition disabled
			1	ENABLED (read-write) Data acquisition enabled

## 12.1.240 SECM\_APP\_CTRL register

Application measurement control

Table 528. SECM\_APP\_CTRL register - application measurement control (address 1C01h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	PAUSEBAL	reserved					CAPAIN7	CAPAIN6
Reset	0	0	0	0	0	0	0	0
Access	W	W	W	W	W	W	W	W
Bit	7	6	5	4	3	2	1	0
Symbol	CAPAIN5	CAPAIN4	CAPAIN3	CAPAIN2	CAPAIN1	CAPAIN0	CAPAINA	CAPVC
Reset	0	0	0	0	0	0	0	0
Access	W	W	W	W	W	W	W	W

Table 529. SECM\_APP\_CTRL register - application measurement control (address 1C01h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15	PAUSEBAL	W		Pause the balancing during this capture cycle. If balancing was not paused before, the start of data capture is delayed until the auto pause timer has elapsed. This field has no effect in secondary measurement.
			0*	NO_PAUSE (write) Continue with balancing.
			1	PAUSE (write) Pause the balancing during this capture cycle.
14:10	reserved	W	0h	This read-only field is reserved and always has the value 0.



Table 529. SECM\_APP\_CTRL register - application measurement control (address 1C01h)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
9	CAPAIN7	W		Capture command for AIN7. When used in combination with PAUSEBAL, a pause of the balancing is forced.
			0*	NO_CAP (write) Measurements are not captured.
			1	CAP (write) Measurements are captured.
8	CAPAIN6	W		Capture command for AIN6. When used in combination with PAUSEBAL, a pause of the balancing is forced.
			0*	NO_CAP (write) Measurements are not captured.
			1	CAP (write) Measurements are captured.
7	CAPAIN5	W		Capture command for AIN5. When used in combination with PAUSEBAL, a pause of the balancing is forced.
			0*	NO_CAP (write) Measurements are not captured.
			1	CAP (write) Measurements are captured.
6	CAPAIN4	W		Capture command for AIN4. When used in combination with PAUSEBAL, a pause of the balancing is forced.
			0*	NO_CAP (write) Measurements are not captured.
			1	CAP (write) Measurements are captured.
5	CAPAIN3	W		AIN3 is not part of the secondary measurement chain. Still, when used in combination with PAUSEBAL, a pause of the balancing is forced. The allows to keep the primary and secondary measurement chain synchronized.
			0*	NO_CAP (write) Measurements are not captured.
			1	CAP (write) Measurements are captured.
4	CAPAIN2	W		AIN2 is not part of the secondary measurement chain. Still, when used in combination with PAUSEBAL, a pause of the balancing is forced. The allows to keep the primary and secondary measurement chain synchronized.
			0*	NO_CAP (write) Measurements are not captured.
			1	CAP (write) Measurements are captured.
3	CAPAIN1	W		AIN1 is not part of the secondary measurement chain. Still, when used in combination with PAUSEBAL, a pause of the balancing is forced. The allows to keep the primary and secondary measurement chain synchronized.
			0*	NO_CAP (write) Measurements are not captured.
			1	CAP (write) Measurements are captured.
2	CAPAIN0	W		AIN0 is not part of the secondary measurement chain. Still, when used in combination with PAUSEBAL, a pause of the balancing is forced. The allows to keep the primary and secondary measurement chain synchronized.
			0*	NO_CAP (write) Measurements are not captured.
			1	CAP (write) Measurements are captured.
1	CAPAINA	W		AINA is not part of the secondary measurement chain. Still, when used in combination with PAUSEBAL, a pause of the balancing is forced. The allows to keep the primary and secondary measurement chain synchronized.
			0*	NO_CAP (write) Measurements are not captured.

**Table 529. SECM\_APP\_CTRL register - application measurement control (address 1C01h)...continued**

Legend: \* reset value

Bit	Symbol	Access	Value	Description
			1	CAP (write) Measurements are captured.
0	CAPVC	W		Trigger the balancing auto pause if set in combination with the PAUSEBAL bit. Needed to keep primary and secondary measurement synchron when used via the ALLM access. In primary: Capture the application measurement value of the cell terminal measurements.
			0*	NO_CAP (write) Measurements are not captured.
			1	CAP (write) Measurements are captured.

**12.1.241 SECM\_PER\_CTRL register**

Periodic measurement control

**Table 530. SECM\_PER\_CTRL register - periodic measurement control (address 1C02h) bit allocation**

Bit	15	14	13	12	11	10	9	8
Symbol	reserved			PERCTRL	reserved			PERLEN
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R/W	R	R	R	R/W
Bit	7	6	5	4	3	2	1	0
Symbol	PERLEN							
Reset	0	0	0	1	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

**Table 531. SECM\_PER\_CTRL register - periodic measurement control (address 1C02h)**

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:13	reserved	R	0h	This read-only field is reserved and always has the value 0.
12	PERCTRL	R/W		Control the periodic result behavior.
			0*	AUTO (read-write) Periodic results are automatically updated
			1	ONCE (read-write) Periodic results are updated once with the last results. (each write updates the results).
11:9	reserved	R	0h	This read-only field is reserved and always has the value 0.
8:0	PERLEN	R/W		Number of measurements for one periodic measurement. The minimum is 16. Writing a value lower than 16 leads to a 16 in the register.
			010h*	PER_16 (read-write) minimum value = 16 measurements per period
			011h	PER_17 (read-write) 17 measurements per period
			1FFh	PER_MAX (read-write) maximum value = 511 measurements per period

12.1.242 SECM\_SYNC\_CTRL register

Synchronous measurement control

Table 532. SECM\_SYNC\_CTRL register - synchronous measurement control (address 1C03h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	PAUSEBAL	VBOLNUM					reserved	
Reset	0	1	1	1	1	1	0	0
Access	W	R/W	R/W	R/W	R/W	R/W	W	W
Bit	7	6	5	4	3	2	1	0
Symbol	reserved						FASTVB	SYNCCYC
Reset	0	0	0	0	0	0	0	0
Access	W	W	W	W	W	W	W	W

Table 533. SECM\_SYNC\_CTRL register - synchronous measurement control (address 1C03h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15	PAUSEBAL	W		Pause the balancing during this capture cycle. If balancing was not paused before, the start of data capture is delayed until the auto pause timer has elapsed. If no capture cycle is started this bit is ignored.
			0*	NO_PAUSE (write) Continue with balancing.
			1	PAUSE (write) Pause the balancing during this capture cycle.
14:10	VBOLNUM	R/W		VB number for which the open load detection is enabled. <b>0 to 17</b> channel for which the open load detection is enabled. <b>18 to 29</b> reserved (no open load detection mechanism is enabled) <b>30</b> the open load detection is enabled for the currently measured channel.
			1Fh*	DISABLED (read-write) Open-load detection is disabled
9:2	reserved	W	0h	This read-only field is reserved and always has the value 0.
1	FASTVB	W		Start a fast VB measurement cycle. The fast VB measurement is a measurement of the VBx voltages. The fast VB measurement is initiated by setting the bit SECM_SYNC_CTRL.FASTVB. ADC2B measures each enabled VBx voltage for $28 \times x \times t_{s(meas)}$ . Read as zero.
			0*	NO_FAST (write) No new start of a fast VB measurement cycle.
			0*	STATUS (read) Read as zero.
			1	FAST (write) Start a new fast VB measurement cycle.
0	SYNCCYC	W		Start a synchronous measurement cycle. In this cycle the CT and CB voltages are measured and stored as matching pairs. If no VB channel is enabled or if set during a running synchronous measurement cycle or a running Fast VB cycle, the set is ignored. Read as zero.
			0*	NO_START (write) No new start a synchronous measurement cycle.

Table 533. SECM\_SYNC\_CTRL register - synchronous measurement control (address 1C03h)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
			0*	STATUS (read) Read as zero.
			1	START (write) Start a synchronous measurement cycle.

12.1.243 SECM\_VB\_CFG0 register

Balance voltage measurement enable

Table 534. SECM\_VB\_CFG0 register - balance voltage measurement enable (address 1C08h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	VB15EN	VB14EN	VB13EN	VB12EN	VB11EN	VB10EN	VB9EN	VB8EN
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	7	6	5	4	3	2	1	0
Symbol	VB7EN	VB6EN	VB5EN	VB4EN	VB3EN	VB2EN	VB1EN	VB0EN
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 535. SECM\_VB\_CFG0 register - balance voltage measurement enable (address 1C08h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15	VB15EN	R/W		Enable measurement of balance voltage 15. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
14	VB14EN	R/W		Enable measurement of balance voltage 14. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
13	VB13EN	R/W		Enable measurement of balance voltage 13. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
12	VB12EN	R/W		Enable measurement of balance voltage 12. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
11	VB11EN	R/W		Enable measurement of balance voltage 11. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
10	VB10EN	R/W		Enable measurement of balance voltage 10. Changes to this bit during active measurement can lead to undefined results.

Table 535. SECM\_VB\_CFG0 register - balance voltage measurement enable (address 1C08h)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
9	VB9EN	R/W	0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
				Enable measurement of balance voltage 9. Changes to this bit during active measurement can lead to undefined results.
8	VB8EN	R/W	0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
				Enable measurement of balance voltage 8. Changes to this bit during active measurement can lead to undefined results.
7	VB7EN	R/W	0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
				Enable measurement of balance voltage 7. Changes to this bit during active measurement can lead to undefined results.
6	VB6EN	R/W	0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
				Enable measurement of balance voltage 6. Changes to this bit during active measurement can lead to undefined results.
5	VB5EN	R/W	0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
				Enable measurement of balance voltage 5. Changes to this bit during active measurement can lead to undefined results.
4	VB4EN	R/W	0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
				Enable measurement of balance voltage 4. Changes to this bit during active measurement can lead to undefined results.
3	VB3EN	R/W	0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
				Enable measurement of balance voltage 3. Changes to this bit during active measurement can lead to undefined results.
2	VB2EN	R/W	0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
				Enable measurement of balance voltage 2. Changes to this bit during active measurement can lead to undefined results.
1	VB1EN	R/W	0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
				Enable measurement of balance voltage 1. Changes to this bit during active measurement can lead to undefined results.
0	VB0EN	R/W	0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
				Enable measurement of balance voltage 0. Changes to this bit during active measurement can lead to undefined results.

## 12.1.244 SECM\_VB\_CFG1 register

Balance voltage measurement enable

Table 536. SECM\_VB\_CFG1 register - balance voltage measurement enable (address 1C09h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	reserved						VB17EN	VB16EN
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R/W	R/W

Table 537. SECM\_VB\_CFG1 register - balance voltage measurement enable (address 1C09h)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:2	reserved	R	0h	This read-only field is reserved and always has the value 0.
1	VB17EN	R/W		Enable measurement of balance voltage 17. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
0	VB16EN	R/W		Enable measurement of balance voltage 16. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled

## 12.1.245 SECM\_AIN\_CFG register

Measurement enables for extra channel

Table 538. SECM\_AIN\_CFG register - measurement enables for extra channel (address 1C0Ah) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	RATIOMETRICAIN7		RATIOMETRICAIN6		RATIOMETRICAIN5		RATIOMETRICAIN4	
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	7	6	5	4	3	2	1	0
Symbol	FLTAPPINV	reserved			AIN7EN	AIN6EN	AIN5EN	AIN4EN
Reset	1	0	0	0	0	0	0	0
Access	R/W	R	R	R	R/W	R/W	R/W	R/W

Table 539. SECM\_AIN\_CFG register - measurement enables for extra channel (address 1C0Ah)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:14	RATIOMETRICAIN7	R/W		Reference selection for AIN7. Changes to these bits during active measurement can lead to undefined results.
			00*	SECVREF (read-write) Absolute (SECVREF)
			01	RESERVED (read-write) reserved
			10	VAUX (read-write) Ratiometric (VAUX)
			11	VDDC (read-write) Ratiometric (VDDC)
13:12	RATIOMETRICAIN6	R/W		Reference selection for AIN6. Changes to these bits during active measurement can lead to undefined results.
			00*	SECVREF (read-write) Absolute (SECVREF)
			01	RESERVED (read-write) reserved
			10	VAUX (read-write) Ratiometric (VAUX)
			11	VDDC (read-write) Ratiometric (VDDC)
11:10	RATIOMETRICAIN5	R/W		Reference selection for AIN5. Changes to these bits during active measurement can lead to undefined results.
			00*	SECVREF (read-write) Absolute (SECVREF)
			01	RESERVED (read-write) reserved
			10	VAUX (read-write) Ratiometric (VAUX)
			11	VDDC (read-write) Ratiometric (VDDC)
9:8	RATIOMETRICAIN4	R/W		Reference selection for AIN4. Changes to these bits during active measurement can lead to undefined results.
			00*	SECVREF (read-write) Absolute (SECVREF)
			01	RESERVED (read-write) reserved
			10	VAUX (read-write) Ratiometric (VAUX)
			11	VDDC (read-write) Ratiometric (VDDC)
7	FLTAPPINV	R/W		Invalidate AINx application results in case of fault.
			0	VALID (read-write) AINx application results are not invalidated in case of a fault
			1*	INVALID (read-write) AINx application results are invalidated when a fault is detected.
6:4	reserved	R	0h	This read-only field is reserved and always has the value 0.
3	AIN7EN	R/W		Enable measurement of AIN7. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled. If a GPIO output function is enabled on this GPIO, the GPIO output is automatically disabled. This is not reflected in the GPIO output enable bit.
2	AIN6EN	R/W		Enable measurement of AIN6. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled. If a GPIO output function is enabled on this GPIO, the GPIO output is automatically disabled. This is not reflected in the GPIO output enable bit.

**Table 539. SECM\_AIN\_CFG register - measurement enables for extra channel (address 1C0Ah)...***continued*

Legend: \* reset value

Bit	Symbol	Access	Value	Description
1	AIN5EN	R/W		Enable measurement of AIN5. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled. If a GPIO output function is enabled on this GPIO, the GPIO output is automatically disabled. This is not reflected in the GPIO output enable bit.
0	AIN4EN	R/W		Enable measurement of AIN4. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled. If a GPIO output function is enabled on this GPIO, the GPIO output is automatically disabled. This is not reflected in the GPIO output enable bit.

**12.1.246 SECM\_AIN\_OL\_CFG register**

AINx open-load detection enable

**Table 540. SECM\_AIN\_OL\_CFG register - AINx open-load detection enable (address 1C0Bh) bit allocation**

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	reserved				AIN7EN	AIN6EN	AIN5EN	AIN4EN
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R/W	R/W	R/W	R/W

**Table 541. SECM\_AIN\_OL\_CFG register - AINx open-load detection enable (address 1C0Bh)**

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:4	reserved	R	0h	This read-only field is reserved and always has the value 0.
3	AIN7EN	R/W		open-load detection circuit for AIN7
			0*	DISABLED (read-write) Disable the open-load detection circuit.
			1	ENABLED (read-write) Enable the open-load detection circuit.
2	AIN6EN	R/W		open-load detection circuit for AIN6
			0*	DISABLED (read-write) Disable the open-load detection circuit.
			1	ENABLED (read-write) Enable the open-load detection circuit.
1	AIN5EN	R/W		open-load detection circuit for AIN5



Table 541. SECM\_AIN\_OL\_CFG register - AINx open-load detection enable (address 1C0Bh)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
			0*	DISABLED (read-write) Disable the open-load detection circuit.
			1	ENABLED (read-write) Enable the open-load detection circuit.
0	AIN4EN	R/W		open-load detection circuit for AIN4
			0*	DISABLED (read-write) Disable the open-load detection circuit.
			1	ENABLED (read-write) Enable the open-load detection circuit.

## 12.1.247 SECM\_VBUF\_CFG register

Voltage buffer enable

Table 542. SECM\_VBUF\_CFG register - voltage buffer enable (address 1C0Ch) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	reserved						VDDCEN	VAUXEN
Reset	0	0	0	0	0	0	1	1
Access	R	R	R	R	R	R	R/W	R/W

Table 543. SECM\_VBUF\_CFG register - voltage buffer enable (address 1C0Ch)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15:2	reserved	R	0h	This read-only field is reserved and always has the value 0.
1	VDDCEN	R/W		Enable the voltage buffer for secondary VDDC measurement.
			0	DISABLED (read-write) Voltage buffer for VDDC is disabled.
			1*	ENABLED (read-write) Voltage buffer for VDDC is enabled.
0	VAUXEN	R/W		Enable the voltage buffer for secondary VAUX measurement.
			0	DISABLED (read-write) Voltage buffer for VAUX is disabled.
			1*	ENABLED (read-write) Voltage buffer for VAUX is enabled.

## 12.1.248 SECM\_CAL\_CRC register

CRC over calibration data

Table 544. SECM\_CAL\_CRC register - CRC over calibration data (address 1C20h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	CRC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 544. SECM\_CAL\_CRC register - CRC over calibration data (address 1C20h) bit allocation...continued

Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
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Table 545. SECM\_CAL\_CRC register - CRC over calibration data (address 1C20h)

Bit	Symbol	Access	Value	Description
15:0	CRC	R/W	0h	CRC over calibration data. The CRC calculation runs automatically every time when a synchronous measurement cycle is started and when the calibration data is read from the NVM.
			BEEFh	CALIBCRC (read-write) The expected value of the calibration CRC.

### 12.1.249 SECM\_CFG\_CRC register

CRC over configuration values

Table 546. SECM\_CFG\_CRC register - CRC over configuration values (address 1C21h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	CRC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 547. SECM\_CFG\_CRC register - CRC over configuration values (address 1C21h)

Bit	Symbol	Access	Value	Description
15:0	CRC	R	0h	This CRC value is recalculated with any transition into Active mode, with any write to a covered register and with any read to this register. The updated CRC value is available latest 100 $\mu$ s after the last write. The CRC value is application specific and must be re-calculated by the MCU. The used polynomial is: $D175h (+1) = X^{16} + X^{15} + X^{13} + X^9 + X^7 + X^6 + X^5 + X^3 + X^1 + 1$ . Following registers are included: SECM_CFG, SECM_PER_CTRL, SECM_VB_CFG0, SECM_VB_CFG1, SECM_AIN_CFG, SECM_VBUF_CFG.

### 12.1.250 SECM\_MEAS\_STAT register

Measurement status

Table 548. SECM\_MEAS\_STAT register - measurement status (address 1C3Eh) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	MEASFLT	COMFLT	ANAFLT	SUPPLYFLT	reserved	FASTVBRDY	SYNCRDY	PERRDY
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	reserved				APPRDYAIN7	APPRDYAIN6	APPRDYAIN5	APPRDYAIN4
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 549. SECM\_MEAS\_STAT register - measurement status (address 1C3Eh)

Legend: \* reset value

Bit	Symbol	Access	Value	Description
15	MEASFLT	R		Measurement fault status
			0*	NO_FLT (read) No measurement fault detected
			1	FAULT (read) Measurement fault detected
14	COMFLT	R		Communication fault status
			0*	NO_FLT (read) No communication fault detected
			1	FAULT (read) Communication fault detected.
13	ANAFLT	R		Analog fault status
			0*	NO_FLT (read) No analog fault detected
			1	FAULT (read) Analog fault detected
12	SUPPLYFLT	R		Internal/external supply fault status
			0*	NO_FLT (read) No supply error detected
			1	FAULT (read) Supply error detected
11	reserved	R	0h	This read-only field is reserved and always has the value 0.
10	FASTVBRDY	R		Fast VB measurement data is ready for readout, the bit is cleared by a read to any register in the range SECM_SYNC_VB0 to SECM_SYNC_VB17 or if a synchronous measurement cycle is completed.
			0*	NO_DATA (read) No data available
			1	DATA (read) Sample data available.
9	SYNCRDY	R		Synchronous measurement data is ready for readout, the bit is cleared by a read to any register in the range SECM_SYNC_VB0 to SECM_SYNC_VB17 or if a fast VB measurement cycle is completed.
			0*	NO_DATA (read) No data available
			1	DATA (read) Sample data available.
8	PERRDY	R		New periodic result data has been created (depending on the periodic update mode, they might need to be requested), the bit is cleared by a read to any register in the range SECM_PER_AIN4 to SECM_PER_NPNISENSE if SECM_PER_CTRL.PERCTRL is set to AUTO. If SECM_PER_CTRL.PERCTRL is set to ONCE, a write to SECM_PER_CTRL.PERCTRL == ONCE clears it.
			0*	NO_DATA (read) No data available
			1	DATA (read) Sample data available.
7:4	reserved	R	0h	This read-only field is reserved and always has the value 0.
3	APPRDYAIN7	R		A new AIN7 application result can be requested / captured.
			0*	NO_DATA (read) No data available (<16 sample)
			1	DATA (read) Data can be captured (>=16 samples are captured).
2	APPRDYAIN6	R		A new AIN6 application result can be requested / captured.
			0*	NO_DATA (read) No data available (<16 sample)
			1	DATA (read) Data can be captured (>=16 samples are captured).
1	APPRDYAIN5	R		A new AIN5 application result can be requested / captured.

Table 549. SECM\_MEAS\_STAT register - measurement status (address 1C3Eh)...continued

Legend: \* reset value

Bit	Symbol	Access	Value	Description
0	APPRDYAIN4	R	0*	NO_DATA (read) No data available (<16 sample)
			1	DATA (read) Data can be captured (>=16 samples are captured).
				A new AIN4 application result can be requested / captured.
			0*	NO_DATA (read) No data available (<16 sample)
			1	DATA (read) Data can be captured (>=16 samples are captured).

12.1.251 SECM\_APP\_AIN4 register

Application measurement result AIN4

Table 550. SECM\_APP\_AIN4 register - application measurement result AIN4 (address 1C53h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 551. SECM\_APP\_AIN4 register - application measurement result AIN4 (address 1C53h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of AIN4 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.252 SECM\_APP\_AIN5 register

Application measurement result AIN5

Table 552. SECM\_APP\_AIN5 register - application measurement result AIN5 (address 1C54h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 553. SECM\_APP\_AIN5 register - application measurement result AIN5 (address 1C54h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of AIN5 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.253 SECM\_APP\_AIN6 register

Application measurement result AIN6

Table 554. SECM\_APP\_AIN6 register - application measurement result AIN6 (address 1C55h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 555. SECM\_APP\_AIN6 register - application measurement result AIN6 (address 1C55h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of AIN6 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.254 SECM\_APP\_AIN7 register

Application measurement result AIN7

Table 556. SECM\_APP\_AIN7 register - application measurement result AIN7 (address 1C56h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 557. SECM\_APP\_AIN7 register - application measurement result AIN7 (address 1C56h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of AIN7 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

### 12.1.255 SECM\_PER\_NUM register

Measurement period number of the secondary periodic results

Table 558. SECM\_PER\_NUM register - measurement period number of the secondary periodic results (address 1C5Fh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	NUM															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 559. SECM\_PER\_NUM register - measurement period number of the secondary periodic results (address 1C5Fh)

Bit	Symbol	Access	Value	Description
15:0	NUM	R	0h	Number of the periodic cycle in which the secondary periodic results have been created. The value is incremented for each periodic cycle executed. The counting wraps at its limit.

### 12.1.256 SECM\_PER\_AIN4 register

Periodic measurement result AIN4

Table 560. SECM\_PER\_AIN4 register - periodic measurement result AIN4 (address 1C73h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 561. SECM\_PER\_AIN4 register - periodic measurement result AIN4 (address 1C73h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of AIN4 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

### 12.1.257 SECM\_PER\_AIN5 register

Periodic measurement result AIN5

Table 562. SECM\_PER\_AIN5 register - periodic measurement result AIN5 (address 1C74h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 563. SECM\_PER\_AIN5 register - periodic measurement result AIN5 (address 1C74h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of AIN5 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.258 SECM\_PER\_AIN6 register

Periodic measurement result AIN6

Table 564. SECM\_PER\_AIN6 register - periodic measurement result AIN6 (address 1C75h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 565. SECM\_PER\_AIN6 register - periodic measurement result AIN6 (address 1C75h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of AIN6 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.259 SECM\_PER\_AIN7 register

Periodic measurement result AIN7

Table 566. SECM\_PER\_AIN7 register - periodic measurement result AIN7 (address 1C76h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 567. SECM\_PER\_AIN7 register - periodic measurement result AIN7 (address 1C76h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of AIN7 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.260 SECM\_PER\_SECTEMP register

Periodic measurement result secondary device temperature

Table 568. SECM\_PER\_SECTEMP register - periodic measurement result secondary device temperature (address 1C77h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

**Table 569. SECM\_PER\_SECTEMP register - periodic measurement result secondary device temperature (address 1C77h)**

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured temperature of secondary temperature sensor of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

**12.1.261 SECM\_PER\_PRMVREF register**

Periodic measurement result primary voltage reference

**Table 570. SECM\_PER\_PRMVREF register - periodic measurement result primary voltage reference (address 1C78h) bit allocation**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

**Table 571. SECM\_PER\_PRMVREF register - periodic measurement result primary voltage reference (address 1C78h)**

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of the primary voltage reference of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

**12.1.262 SECM\_PER\_VAUX register**

Periodic measurement result auxiliary supply voltage

**Table 572. SECM\_PER\_VAUX register - periodic measurement result auxiliary supply voltage (address 1C79h) bit allocation**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

**Table 573. SECM\_PER\_VAUX register - periodic measurement result auxiliary supply voltage (address 1C79h)**

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of VAUX of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).



## 12.1.263 SECM\_PER\_VBAT register

Periodic measurement result VBAT

Table 574. SECM\_PER\_VBAT register - periodic measurement result VBAT (address 1C7Ah) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 575. SECM\_PER\_VBAT register - periodic measurement result VBAT (address 1C7Ah)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of VBAT of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.264 SECM\_PER\_VDDA register

Periodic measurement result VDDA

Table 576. SECM\_PER\_VDDA register - periodic measurement result VDDA (address 1C7Bh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 577. SECM\_PER\_VDDA register - periodic measurement result VDDA (address 1C7Bh)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of VDDA of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.265 SECM\_PER\_VDDC register

Periodic measurement result VDDC

Table 578. SECM\_PER\_VDDC register - periodic measurement result VDDC (address 1C7Ch) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 579. SECM\_PER\_VDDC register - periodic measurement result VDDC (address 1C7Ch)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of VDDC of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.266 SECM\_PER\_NPNISENSE register

Periodic measurement result NPN current sensor

Table 580. SECM\_PER\_NPNISENSE register - periodic measurement result NPN current sensor (address 1C7Eh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 581. SECM\_PER\_NPNISENSE register - periodic measurement result NPN current sensor (address 1C7Eh)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of NPN current sensor of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

## 12.1.267 SECM\_SYNC\_NUM register

Measurement number of the secondary synchronous results

Table 582. SECM\_SYNC\_NUM register - measurement number of the secondary synchronous results (address 1C7Fh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	NUM															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 583. SECM\_SYNC\_NUM register - measurement number of the secondary synchronous results (address 1C7Fh)

Bit	Symbol	Access	Value	Description
15:0	NUM	R	0h	Number of the synchronous cycle in which the secondary results have been created. The value is incremented for each synchronous cycle executed. The counting wraps at its limit. The value is not incremented for FASTVB cycle.

## 12.1.268 SECM\_SYNC\_VB0 register

Synchronous measurement result from balancing pins cell 0.

Table 584. SECM\_SYNC\_VB0 register - synchronous measurement result from balancing pins cell 0. (address 1C80h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

**Table 585. SECM\_SYNC\_VB0 register - synchronous measurement result from balancing pins cell 0. (address 1C80h)**

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 0 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

**12.1.269 SECM\_SYNC\_VB1 register**

Synchronous measurement result from balancing pins cell 1

**Table 586. SECM\_SYNC\_VB1 register - synchronous measurement result from balancing pins cell 1 (address 1C81h) bit allocation**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

**Table 587. SECM\_SYNC\_VB1 register - synchronous measurement result from balancing pins cell 1 (address 1C81h)**

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 1 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

**12.1.270 SECM\_SYNC\_VB2 register**

Synchronous measurement result from balancing pins cell 2

**Table 588. SECM\_SYNC\_VB2 register - synchronous measurement result from balancing pins cell 2 (address 1C82h) bit allocation**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

**Table 589. SECM\_SYNC\_VB2 register - synchronous measurement result from balancing pins cell 2 (address 1C82h)**

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 2 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

**12.1.271 SECM\_SYNC\_VB3 register**

Synchronous measurement result from balancing pins cell 3

**Table 590. SECM\_SYNC\_VB3 register - synchronous measurement result from balancing pins cell 3 (address 1C83h) bit allocation**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

**Table 591. SECM\_SYNC\_VB3 register - synchronous measurement result from balancing pins cell 3 (address 1C83h)**

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 3 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

**12.1.272 SECM\_SYNC\_VB4 register**

Synchronous measurement result from balancing pins cell 4

**Table 592. SECM\_SYNC\_VB4 register - synchronous measurement result from balancing pins cell 4 (address 1C84h) bit allocation**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

**Table 593. SECM\_SYNC\_VB4 register - synchronous measurement result from balancing pins cell 4 (address 1C84h)**

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 4 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

**12.1.273 SECM\_SYNC\_VB5 register**

Synchronous measurement result from balancing pins cell 5

**Table 594. SECM\_SYNC\_VB5 register - synchronous measurement result from balancing pins cell 5 (address 1C85h) bit allocation**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

**Table 595. SECM\_SYNC\_VB5 register - synchronous measurement result from balancing pins cell 5 (address 1C85h)**

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 5 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

**12.1.274 SECM\_SYNC\_VB6 register**

Synchronous measurement result from balancing pins cell 6

**Table 596. SECM\_SYNC\_VB6 register - synchronous measurement result from balancing pins cell 6 (address 1C86h) bit allocation**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

**Table 597. SECM\_SYNC\_VB6 register - synchronous measurement result from balancing pins cell 6 (address 1C86h)**

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 6 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

**12.1.275 SECM\_SYNC\_VB7 register**

Synchronous measurement result from balancing pins cell 7

**Table 598. SECM\_SYNC\_VB7 register - synchronous measurement result from balancing pins cell 7 (address 1C87h) bit allocation**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

**Table 599. SECM\_SYNC\_VB7 register - synchronous measurement result from balancing pins cell 7 (address 1C87h)**

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 7 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

**12.1.276 SECM\_SYNC\_VB8 register**

Synchronous measurement result from balancing pins cell 8

**Table 600. SECM\_SYNC\_VB8 register - synchronous measurement result from balancing pins cell 8 (address 1C88h) bit allocation**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

**Table 601. SECM\_SYNC\_VB8 register - synchronous measurement result from balancing pins cell 8 (address 1C88h)**

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 8 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

### 12.1.277 SECM\_SYNC\_VB9 register

Synchronous measurement result from balancing pins cell 9

**Table 602. SECM\_SYNC\_VB9 register - synchronous measurement result from balancing pins cell 9 (address 1C89h) bit allocation**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

**Table 603. SECM\_SYNC\_VB9 register - synchronous measurement result from balancing pins cell 9 (address 1C89h)**

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 9 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

### 12.1.278 SECM\_SYNC\_VB10 register

Synchronous measurement result from balancing pins cell 10

**Table 604. SECM\_SYNC\_VB10 register - synchronous measurement result from balancing pins cell 10 (address 1C8Ah) bit allocation**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

**Table 605. SECM\_SYNC\_VB10 register - synchronous measurement result from balancing pins cell 10 (address 1C8Ah)**

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 10 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

**12.1.279 SECM\_SYNC\_VB11 register**

Synchronous measurement result from balancing pins cell 11

**Table 606. SECM\_SYNC\_VB11 register - synchronous measurement result from balancing pins cell 11 (address 1C8Bh) bit allocation**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

**Table 607. SECM\_SYNC\_VB11 register - synchronous measurement result from balancing pins cell 11 (address 1C8Bh)**

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 11 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

**12.1.280 SECM\_SYNC\_VB12 register**

Synchronous measurement result from balancing pins cell 12

**Table 608. SECM\_SYNC\_VB12 register - synchronous measurement result from balancing pins cell 12 (address 1C8Ch) bit allocation**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

**Table 609. SECM\_SYNC\_VB12 register - synchronous measurement result from balancing pins cell 12 (address 1C8Ch)**

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 12 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

**12.1.281 SECM\_SYNC\_VB13 register**

Synchronous measurement result from balancing pins cell 13

**Table 610. SECM\_SYNC\_VB13 register - synchronous measurement result from balancing pins cell 13 (address 1C8Dh) bit allocation**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

**Table 611. SECM\_SYNC\_VB13 register - synchronous measurement result from balancing pins cell 13 (address 1C8Dh)**

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 13 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

**12.1.282 SECM\_SYNC\_VB14 register**

Synchronous measurement result from balancing pins cell 14

**Table 612. SECM\_SYNC\_VB14 register - synchronous measurement result from balancing pins cell 14 (address 1C8Eh) bit allocation**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

**Table 613. SECM\_SYNC\_VB14 register - synchronous measurement result from balancing pins cell 14 (address 1C8Eh)**

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 14 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

**12.1.283 SECM\_SYNC\_VB15 register**

Synchronous measurement result from balancing pins cell 15

**Table 614. SECM\_SYNC\_VB15 register - synchronous measurement result from balancing pins cell 15 (address 1C8Fh) bit allocation**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R



**Table 615. SECM\_SYNC\_VB15 register - synchronous measurement result from balancing pins cell 15 (address 1C8Fh)**

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 15 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

**12.1.284 SECM\_SYNC\_VB16 register**

Synchronous measurement result from balancing pins cell 16

**Table 616. SECM\_SYNC\_VB16 register - synchronous measurement result from balancing pins cell 16 (address 1C90h) bit allocation**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

**Table 617. SECM\_SYNC\_VB16 register - synchronous measurement result from balancing pins cell 16 (address 1C90h)**

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 16 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

**12.1.285 SECM\_SYNC\_VB17 register**

Synchronous measurement result from balancing pins cell 17

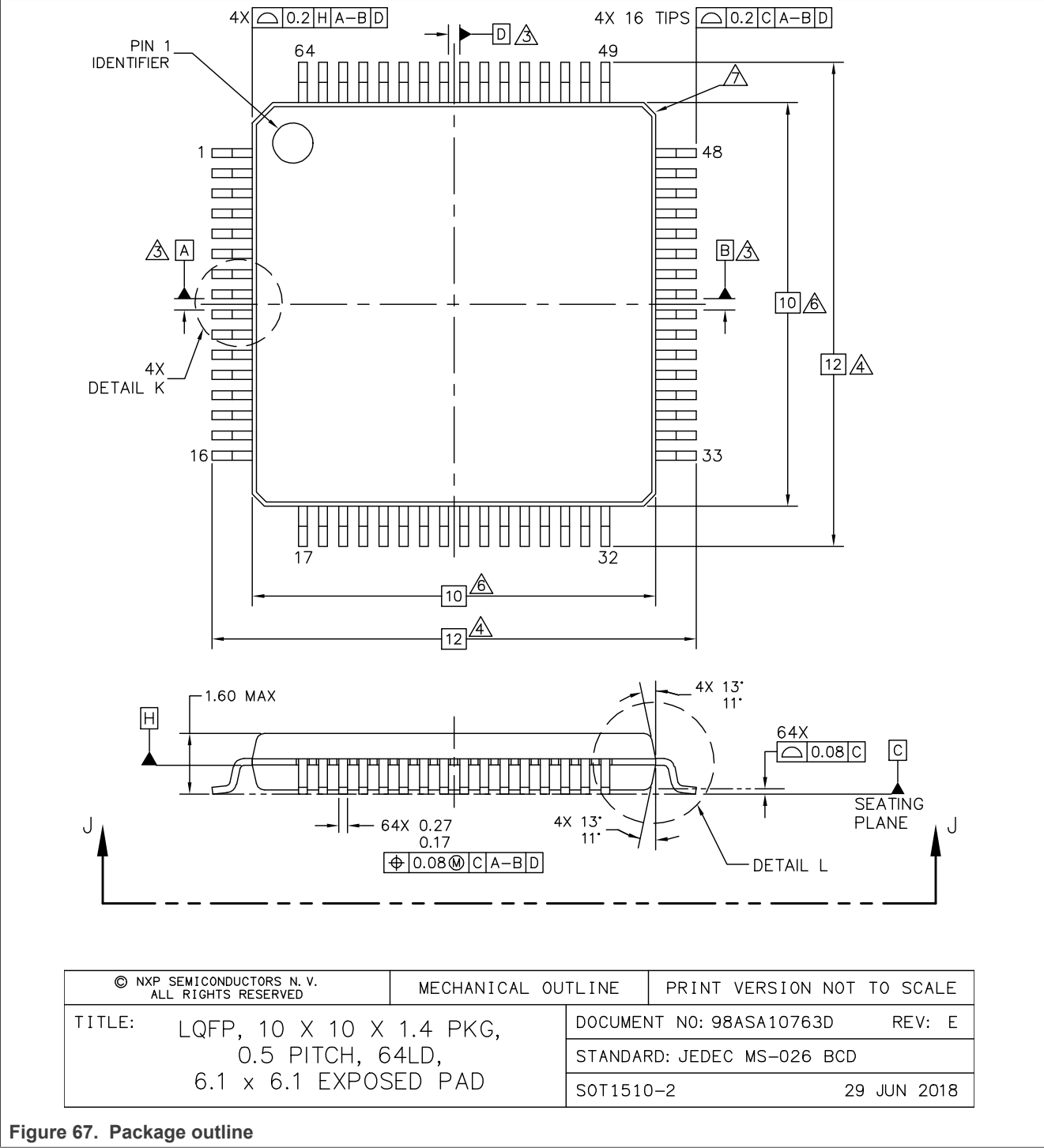
**Table 618. SECM\_SYNC\_VB17 register - synchronous measurement result from balancing pins cell 17 (address 1C91h) bit allocation**

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

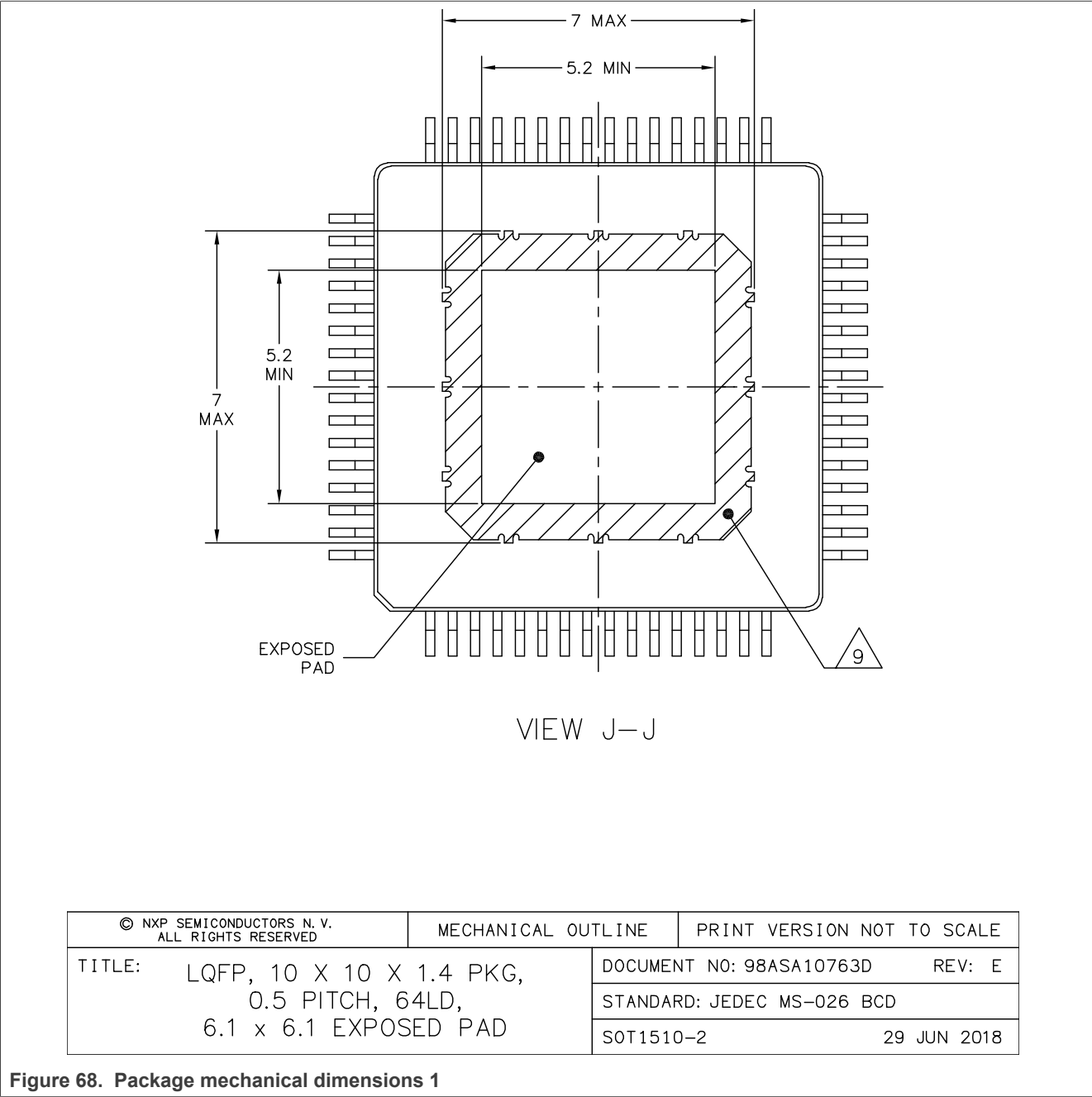
**Table 619. SECM\_SYNC\_VB17 register - synchronous measurement result from balancing pins cell 17 (address 1C91h)**

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 17 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

13 Package outline



13.1 Package mechanical dimensions



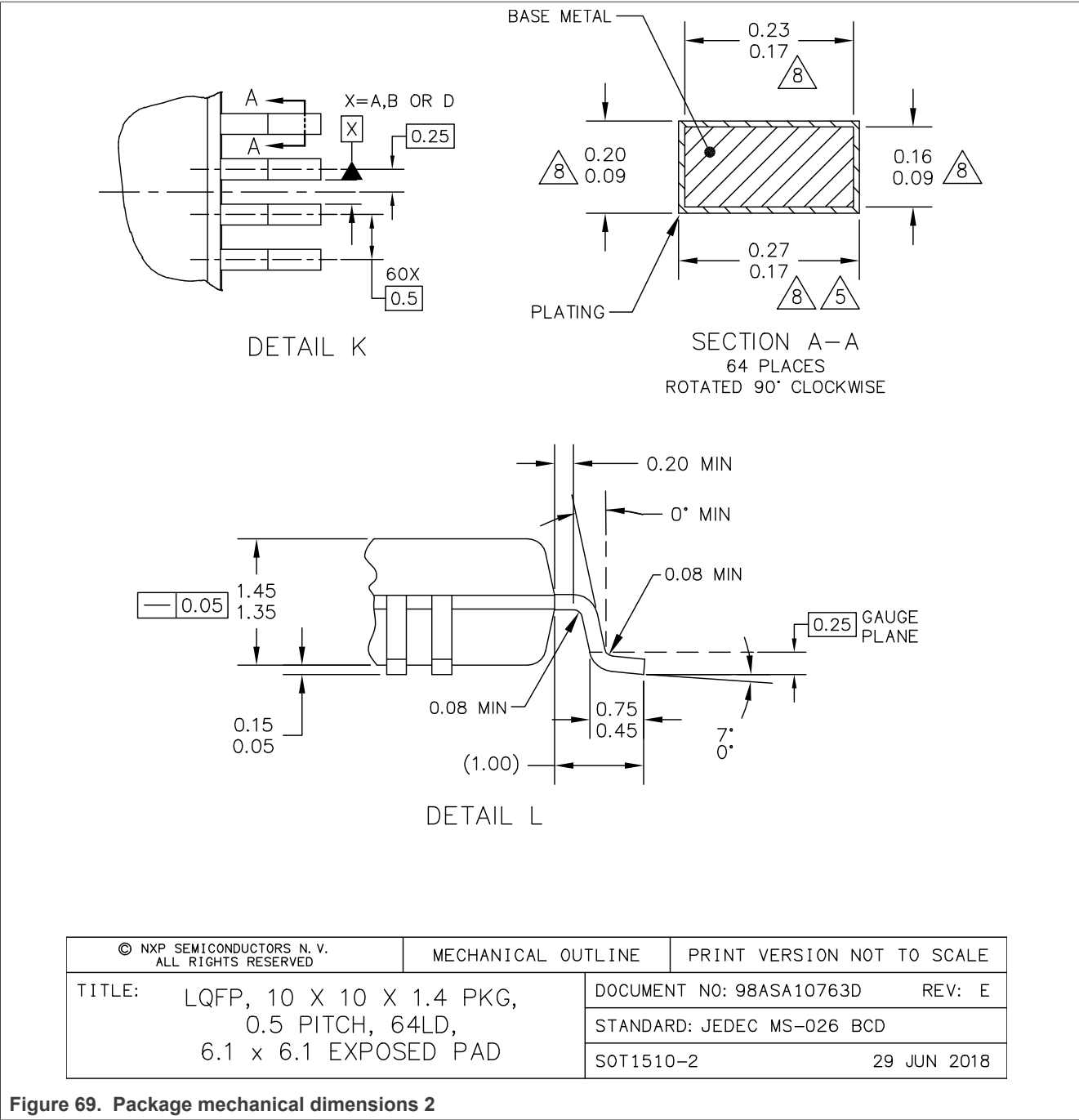


Figure 69. Package mechanical dimensions 2

NOTES:

- 1. DIMENSIONS ARE IN MILLIMETERS.
- 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
- 3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
- 4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
- 5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM DIMENSION BY MORE THAN 0.08 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 MM.
- 6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. DIMENSIONS ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
- 7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
- 8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 MM AND 0.25 MM FROM THE LEAD TIP.
- 9. HATCHED AREA REPRESENTS POSSIBLE MOLD FLASH ON EXPOSED PAD.
- 10. KEEP OUT ZONE REPRESENTS AREA ON PCB THAT MUST NOT HAVE ANY EXPOSED METAL (EG. TRACE/VIA) FOR PCB ROUTING DUE TO THE POSSIBILITY OF SHORTING TO TIE BAR/EXPOSED PAD.

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TITLE: LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, 64LD, 6.1 x 6.1 EXPOSED PAD	DOCUMENT NO: 98ASA10763D		REV: E
	STANDARD: JEDEC MS-026 BCD		
	SOT1510-2		29 JUN 2018

Figure 70. Package mechanical dimensions 3

## 14 Revision history

Table 620. Revision history

Document ID	Release date	Description
BMI7018 v.1.0	23 Sep 2024	• Initial version

Legal information

Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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