

BGU7062N2

Analog high linearity low noise variable gain amplifier

Rev. 1 — 8 July 2013

Product data sheet

1. Product profile

1.1 General description

The BGU7062N2 is a fully integrated analog-controlled variable gain amplifier module. Its low noise and high linearity performance makes it ideal for sensitive receivers in cellular base station applications. The BGU7062N2 is designed for the 1710 MHz to 1785 MHz frequency range. It has a gain control range of more than 35 dB. At maximum gain the noise figure is 0.77 dB. The gain is analog-controlled having maximum gain at 0 V and minimum gain at 3.3 V. The LNA can be bypassed extending the dynamic range. The BGU7062N2 is internally matched to 50 ohm, meaning no external matching is required, enabling ease of use. It is housed in a 16 pins 8 mm × 8 mm × 1.3 mm leadless HLQFN16R package SOT1301.

1.2 Features and benefits

- Input and output internally matched to 50 Ω
- Low noise figure of 0.77 dB
- High IP_{3i} of 1 dBm
- High P_{i(1dB)} of -12.3 dBm
- Bypass mode of LNA giving high dynamic gain range
- Gain control range of 0 dB to 35 dB
- Single 5 V supply
- Single analog gain control of 0 V to 3.3 V
- Unconditionally stable up to 12.75 GHz
- Moisture sensitivity level 3
- ESD protection at all pins

1.3 Applications

- Cellular base stations, remote radio heads
- 3G, LTE infrastructure
- Low noise applications with variable gain and high linearity requirements
- Active antenna



1.4 Quick reference data

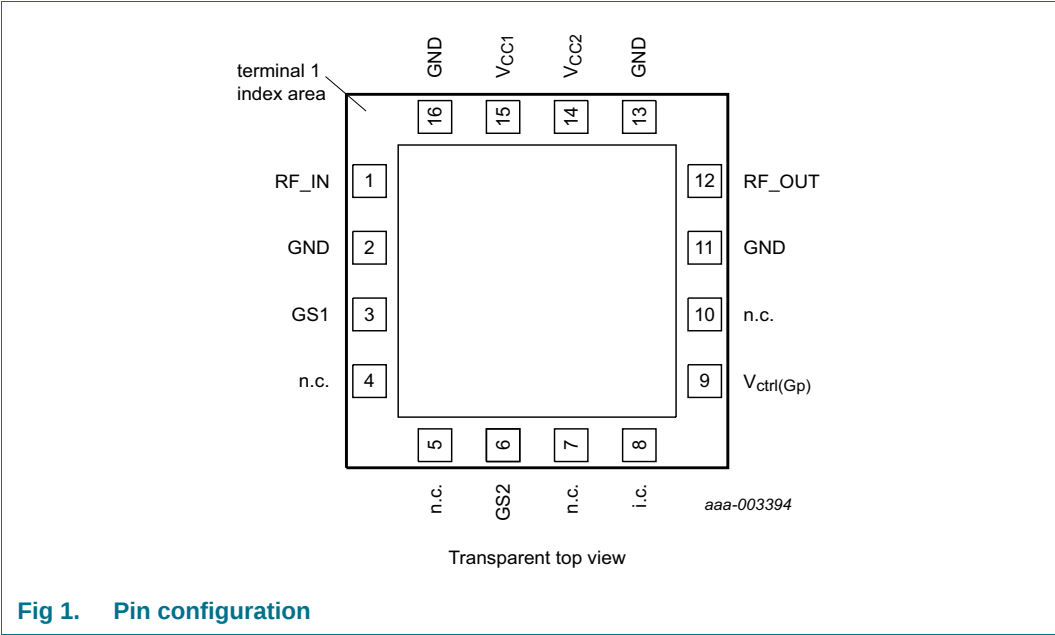
Table 1. Quick reference data
 $V_{CC1} = 5\text{ V}$; $V_{CC2} = 5\text{ V}$; $f = 1750\text{ MHz}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; input and output $50\text{ }\Omega$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{CC(tot)}$	total supply current	high gain mode	[1] 190	215	250	mA
		low gain mode	[2] 165	185	215	mA
NF	noise figure	$V_{ctrl(Gp)} = 0\text{ V}$ (maximum power gain)	[1] -	0.77	-	dB
		$G_p = 35\text{ dB}$	[1] -	0.94	1.1	dB
$IP3_i$	input third-order intercept point	$G_p = 35\text{ dB}$; 2-tone; tone-spacing = 1.0 MHz	[1] 0	1.0	-	dBm
$P_{i(1dB)}$	input power at 1 dB gain compression	$G_p = 35\text{ dB}$	[1] -14	-12.3	-	dBm

- [1] high gain mode: GS1 = LOW; GS2 = HIGH (see Table 9)
[2] low gain mode: GS1 = HIGH; GS2 = LOW (see Table 9)

2. Pinning information

2.1 Pinning



2.2 Pin description

Symbol	Pin	Description
RF_IN	1	RF input
GND	2, 11, 13, 16	ground
GS1	3	gain switch control 1
n.c.	4, 5, 7, 10	not connected, internally open

Table 2. Pin description ...continued

Symbol	Pin	Description
GS2	6	gain switch control 2
i.c.	8	internally connected to ground
V _{ctrl(Gp)}	9	power gain control voltage
RF_OUT	12	RF output
V _{CC2}	14	supply voltage 2
V _{CC1}	15	supply voltage 1

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BGU7062N2	HLQFN16R	plastic thermal enhanced low profile quad flat package; no leads; 16 terminals; body 8 × 8 × 1.3 mm	SOT1301-1

4. Functional diagram

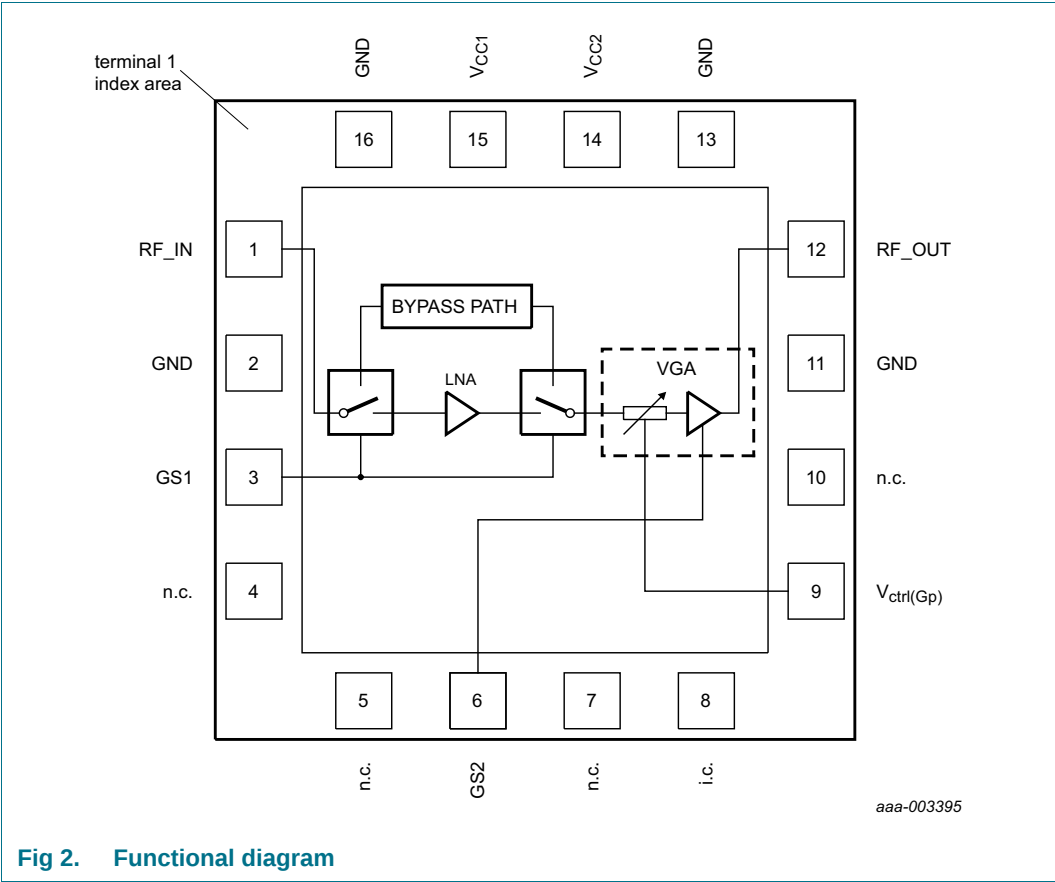


Fig 2. Functional diagram

5. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		0	6	V
V _{ctrl(Gp)}	power gain control voltage		−1	+3.6	V
V _{I(GS1)}	input voltage on pin GS1		−1	+3.6	V
V _{I(GS2)}	input voltage on pin GS2		−1	+3.6	V
P _{I(RF)CW}	continuous waveform RF input power	high gain mode; V _{ctrl(Gp)} = 0 V; 1710 MHz ≤ f ≤ 1785 MHz [1]	-	10	dBm
		low gain mode; V _{ctrl(Gp)} = 0 V; 1710 MHz ≤ f ≤ 1785 MHz [2]	-	15	dBm
T _j	junction temperature		-	150	°C
T _{stg}	storage temperature		−40	+150	°C
V _{ESD}	electrostatic discharge voltage	Human Body Model (HBM); according to ANSI/ESDA-JEDEC JS-001-2010-Device Testing, Human Body Model	-	±2	kV
		Charged Device Model (CDM); according to JEDEC standard 22-C101	-	±750	V

[1] high gain mode: GS1 = LOW; GS2 = HIGH (see [Table 9](#))

[2] low gain mode: GS1 = HIGH; GS2 = LOW (see [Table 9](#))

6. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC1}	supply voltage 1		4.75	5	5.25	V
V _{CC2}	supply voltage 2		4.75	5	5.25	V
V _{ctrl(Gp)}	power gain control voltage		0	-	3.3	V
V _{I(GS1)}	input voltage on pin GS1		0	-	3.3	V
V _{I(GS2)}	input voltage on pin GS2		0	-	3.3	V
Z ₀	characteristic impedance		-	50	-	Ω
T _{case}	case temperature		−40	-	+85	°C

7. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
R _{th(j-case)}	thermal resistance from junction to case		[1] 42	K/W

[1] The case temperature is measured at the ground solder pad.

8. Characteristics

Table 7. Characteristics high gain mode

GS1 = LOW; GS2 = HIGH (see [Table 9](#)); $V_{CC1} = 5\text{ V}$; $V_{CC2} = 5\text{ V}$; $f = 1750\text{ MHz}$; $T_{amb} = 25\text{ °C}$; input and output $50\text{ }\Omega$; unless otherwise specified. All RF parameters have been characterized at the device RF input and RF output terminals.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{CC(tot)}$	total supply current		190	215	250	mA
$G_{p(min)}$	minimum power gain	$V_{ctrl(Gp)} = 3.3\text{ V}$	-	13.3	-	dB
$G_{p(max)}$	maximum power gain	$V_{ctrl(Gp)} = 0\text{ V}$	-	37.2	-	dB
$G_{p(flat)}$	power gain flatness	$1710\text{ MHz} \leq f \leq 1785\text{ MHz}$; $18\text{ dB} \leq G_p \leq 35\text{ dB}$	-	0.3	-	dB
NF	noise figure	$V_{ctrl(Gp)} = 0\text{ V}$ (maximum power gain)	-	0.77	-	dB
		$G_p = 35\text{ dB}$	-	0.94	1.1	dB
		$G_p = 18\text{ dB}$	-	5.95	-	dB
IP3 _i	input third-order intercept point	2-tone; tone-spacing = 1.0 MHz				
		$G_p = 35\text{ dB}$	0	1.0	-	dBm
		$G_p = 30\text{ dB}$	-	3.6	-	dBm
		$G_p = 29\text{ dB}$	-	4.0	-	dBm
		$G_p = 18\text{ dB}$	-	4.6	-	dBm
P _{I(1dB)}	input power at 1 dB gain compression	$G_p = 35\text{ dB}$	-14	-12.3	-	dBm
		$G_p = 30\text{ dB}$	-	-7.2	-	dBm
		$G_p = 29\text{ dB}$	-	-6.8	-	dBm
		$G_p = 18\text{ dB}$	-	-6.1	-	dBm
RL _{in}	input return loss	$V_{ctrl(Gp)} = 0\text{ V}$ (maximum power gain)	-	24.9	-	dB
		$G_p = 35\text{ dB}$	-	23.5	-	dB
RL _{out}	output return loss	$V_{ctrl(Gp)} = 0\text{ V}$ (maximum power gain)	-	17.5	-	dB
K	Rollett stability factor	$0\text{ GHz} \leq f \leq 12.75\text{ GHz}$	1	-	-	

Table 8. Characteristics low gain mode

GS1 = HIGH; GS2 = LOW (see [Table 9](#)); $V_{CC1} = 5\text{ V}$; $V_{CC2} = 5\text{ V}$; $f = 1750\text{ MHz}$; $T_{amb} = 25\text{ °C}$; input and output $50\text{ }\Omega$; unless otherwise specified. All RF parameters have been characterized at the device RF input and RF output terminals.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{CC(tot)}$	total supply current		165	185	215	mA
$G_{p(min)}$	minimum power gain	$V_{ctrl(Gp)} = 3.3\text{ V}$	-	-6.5	-	dB
$G_{p(max)}$	maximum power gain	$V_{ctrl(Gp)} = 0\text{ V}$	-	18.0	-	dB
$G_{p(flat)}$	power gain flatness	$1710\text{ MHz} \leq f \leq 1785\text{ MHz}$; $3\text{ dB} \leq G_p \leq 17\text{ dB}$	-	0.2	-	dB
NF	noise figure	$G_p = 17\text{ dB}$	-	10.5	-	dB
		$G_p = 3\text{ dB}$	-	22.1	-	dB
IP3 _i	input third-order intercept point	2-tone; tone-spacing = 1.0 MHz			-	
		$G_p = 17\text{ dB}$	-	20.9	-	dBm
		$G_p = 12\text{ dB}$	-	25.1	-	dBm
		$G_p = 11\text{ dB}$	-	25.9	-	dBm
		$G_p = 3\text{ dB}$	-	30.0	-	dBm

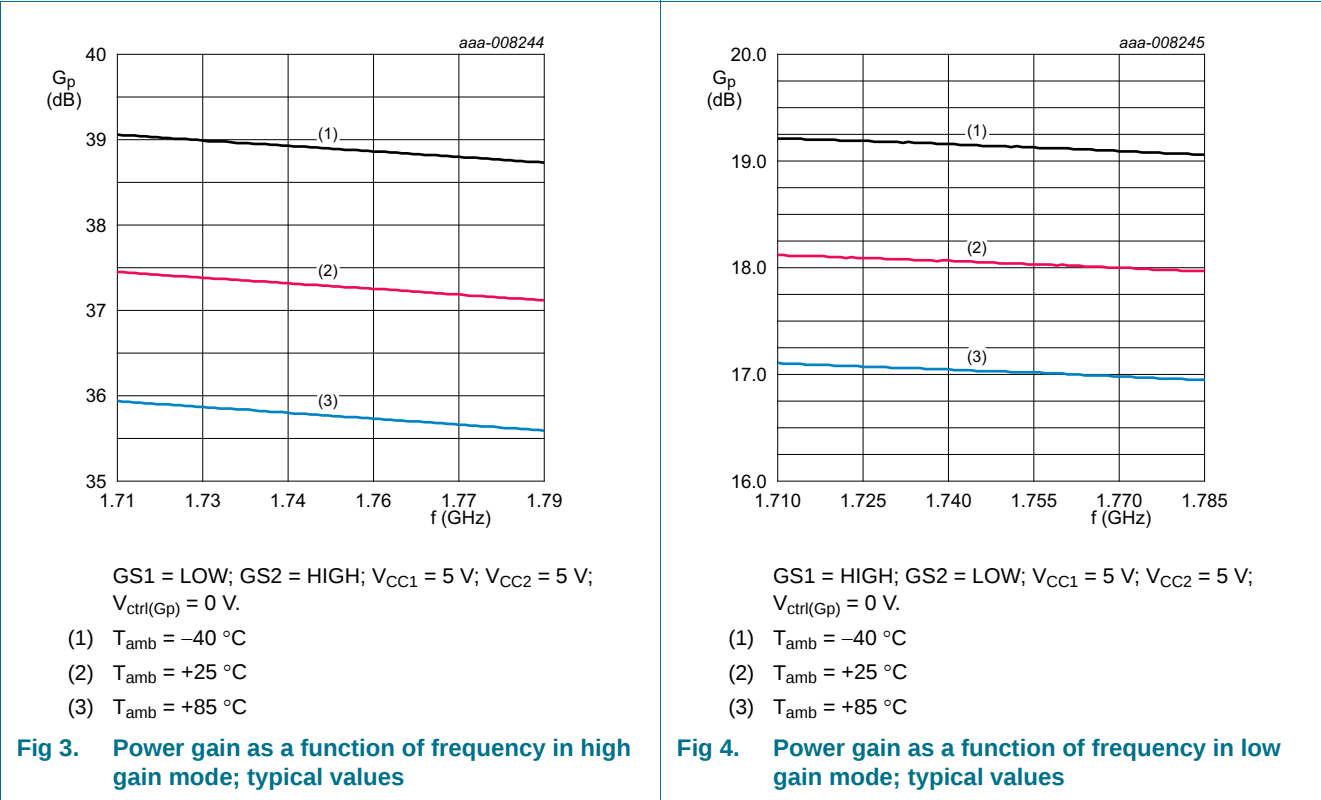
Table 8. Characteristics low gain mode ...continued
GS1 = HIGH; GS2 = LOW (see Table 9); V_{CC1} = 5 V; V_{CC2} = 5 V; f = 1750 MHz; T_{amb} = 25 °C; input and output 50 Ω; unless otherwise specified. All RF parameters have been characterized at the device RF input and RF output terminals.

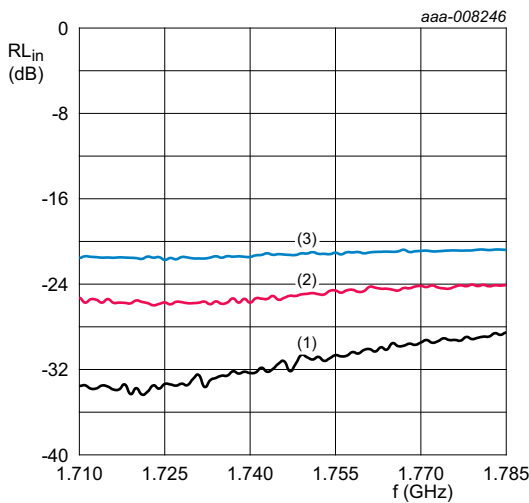
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P _{I(1dB)}	input power at 1 dB gain compression	G _p = 17 dB	-	5.8	-	dBm
		G _p = 12 dB	-	9.9	-	dBm
		G _p = 11 dB	-	10.3	-	dBm
		G _p = 3 dB	-	10.9	-	dBm
RL _{in}	input return loss	V _{ctrl(Gp)} = 0 V (maximum power gain)	-	19.3	-	dB
		G _p = 17 dB	-	22	-	dB
RL _{out}	output return loss	V _{ctrl(Gp)} = 0 V (maximum power gain)	-	17.3	-	dB
K	Rollett stability factor	0 GHz ≤ f ≤ 12.75 GHz	1	-	-	

Table 9. Gain switch truth table
V_{CC1} = 5 V; V_{CC2} = 5 V; -40 °C ≤ T_{amb} ≤ +85 °C

Gain mode	GS1		GS2	
	logic	V _{GS1}	logic	V _{GS2}
high gain mode	LOW	0 V to 0.5 V	HIGH	2 V to 3.3 V
low gain mode	HIGH	2 V to 3.3 V	LOW	0 V to 0.5 V

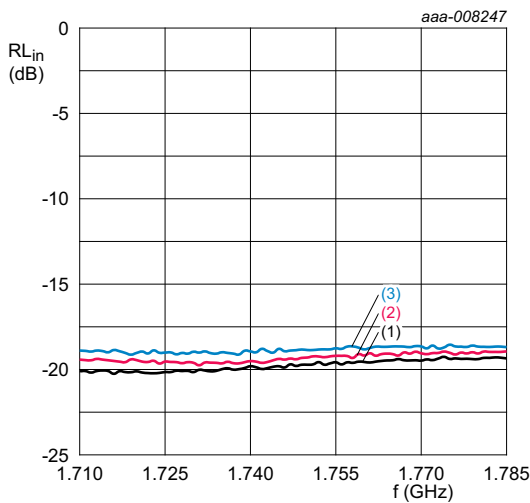
8.1 Graphs





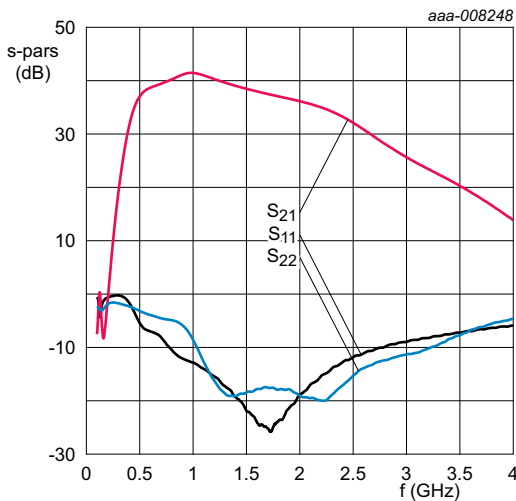
GS1 = LOW; GS2 = HIGH; $V_{CC1} = 5\text{ V}$; $V_{CC2} = 5\text{ V}$;
 $V_{ctrl(Gp)} = 0\text{ V}$.
(1) $T_{amb} = -40\text{ }^{\circ}\text{C}$
(2) $T_{amb} = +25\text{ }^{\circ}\text{C}$
(3) $T_{amb} = +85\text{ }^{\circ}\text{C}$

Fig 5. Input return loss as a function of frequency in high gain mode; typical values



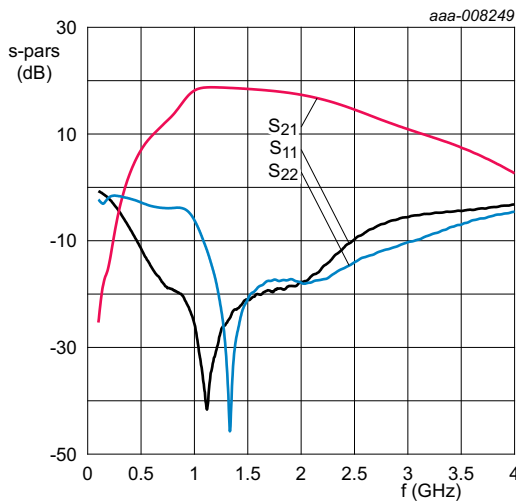
GS1 = HIGH; GS2 = LOW; $V_{CC1} = 5\text{ V}$; $V_{CC2} = 5\text{ V}$;
 $V_{ctrl(Gp)} = 0\text{ V}$.
(1) $T_{amb} = -40\text{ }^{\circ}\text{C}$
(2) $T_{amb} = +25\text{ }^{\circ}\text{C}$
(3) $T_{amb} = +85\text{ }^{\circ}\text{C}$

Fig 6. Input return loss as a function of frequency in low gain mode; typical values



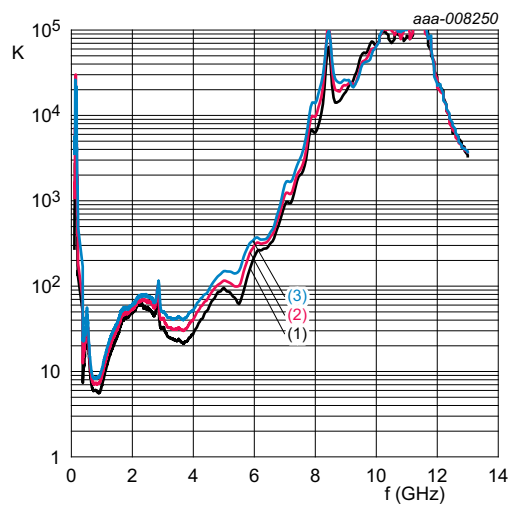
GS1 = LOW; GS2 = HIGH; $V_{CC1} = 5\text{ V}$; $V_{CC2} = 5\text{ V}$;
 $V_{ctrl(Gp)} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

Fig 7. S-parameters as a function of frequency in high gain mode; typical values



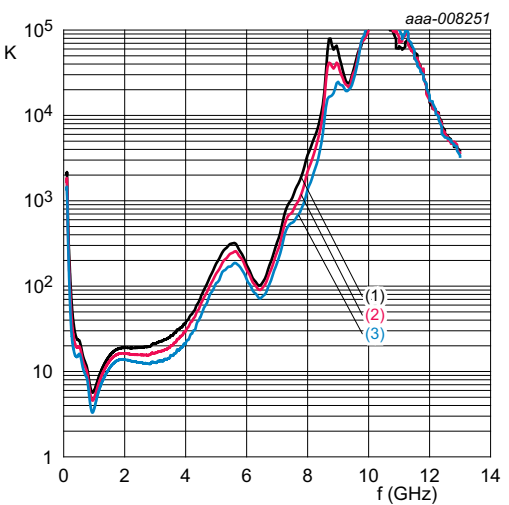
GS1 = HIGH; GS2 = LOW; $V_{CC1} = 5\text{ V}$; $V_{CC2} = 5\text{ V}$;
 $V_{ctrl(Gp)} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

Fig 8. S-parameters as a function of frequency in low gain mode; typical values



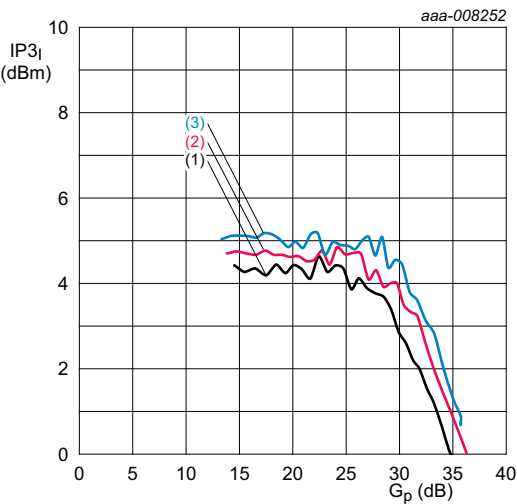
GS1 = LOW; GS2 = HIGH; $V_{CC1} = 5\text{ V}$; $V_{CC2} = 5\text{ V}$; $V_{ctrl}(G_p) = 0\text{ V}$.
(1) $T_{amb} = -40\text{ }^{\circ}\text{C}$
(2) $T_{amb} = +25\text{ }^{\circ}\text{C}$
(3) $T_{amb} = +85\text{ }^{\circ}\text{C}$

Fig 9. Rollet stability factor as a function of frequency in high gain mode; typical values



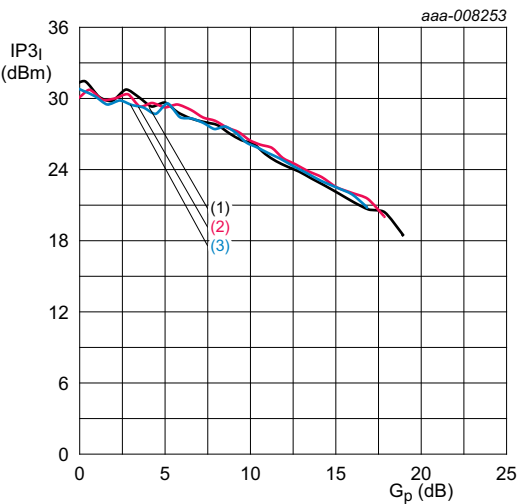
GS1 = HIGH; GS2 = LOW; $V_{CC1} = 5\text{ V}$; $V_{CC2} = 5\text{ V}$; $V_{ctrl}(G_p) = 0\text{ V}$.
(1) $T_{amb} = -40\text{ }^{\circ}\text{C}$
(2) $T_{amb} = +25\text{ }^{\circ}\text{C}$
(3) $T_{amb} = +85\text{ }^{\circ}\text{C}$

Fig 10. Rollet stability factor as a function of frequency in low gain mode; typical values



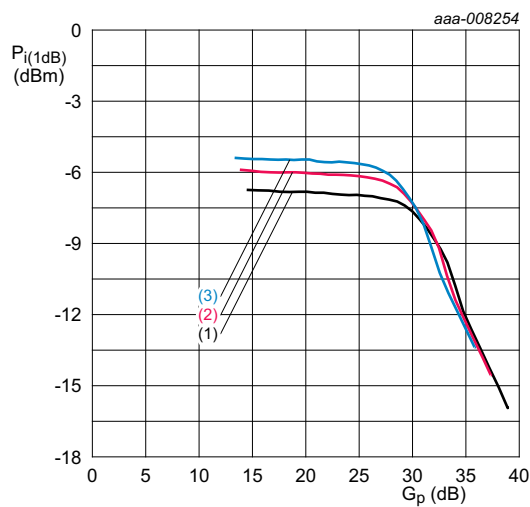
GS1 = LOW; GS2 = HIGH; $V_{CC1} = 5\text{ V}$; $V_{CC2} = 5\text{ V}$; $f = 1750\text{ MHz}$.
(1) $T_{amb} = -40\text{ }^{\circ}\text{C}$
(2) $T_{amb} = +25\text{ }^{\circ}\text{C}$
(3) $T_{amb} = +85\text{ }^{\circ}\text{C}$

Fig 11. Input third-order intercept point as a function of power gain in high gain mode; typical values



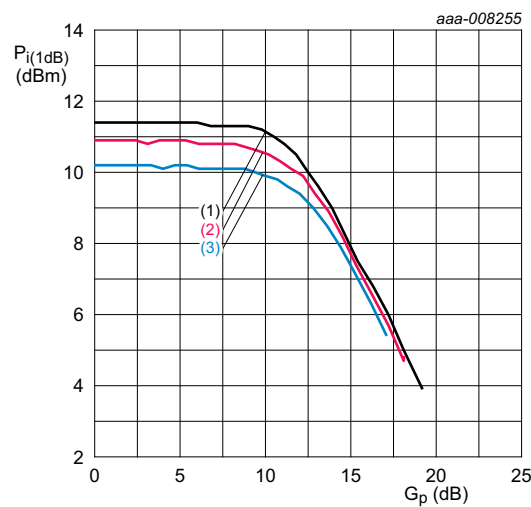
GS1 = HIGH; GS2 = LOW; $V_{CC1} = 5\text{ V}$; $V_{CC2} = 5\text{ V}$; $f = 1750\text{ MHz}$.
(1) $T_{amb} = -40\text{ }^{\circ}\text{C}$
(2) $T_{amb} = +25\text{ }^{\circ}\text{C}$
(3) $T_{amb} = +85\text{ }^{\circ}\text{C}$

Fig 12. Input third-order intercept point as a function of power gain in low gain mode; typical values



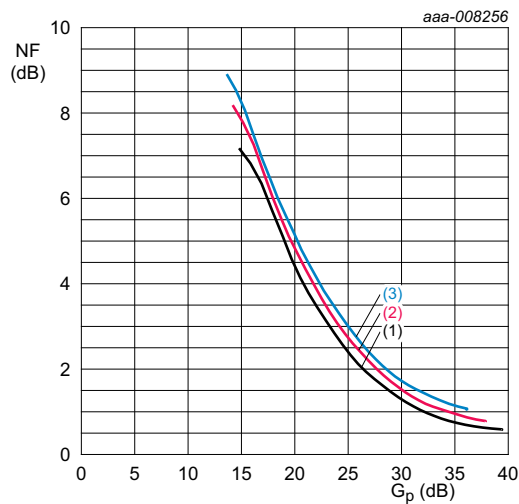
GS1 = LOW; GS2 = HIGH; $V_{CC1} = 5\text{ V}$; $V_{CC2} = 5\text{ V}$; $f = 1750\text{ MHz}$.
(1) $T_{amb} = -40^\circ\text{C}$
(2) $T_{amb} = +25^\circ\text{C}$
(3) $T_{amb} = +85^\circ\text{C}$

Fig 13. Input power at 1 dB gain compression as a function of power gain in high gain mode; typical values



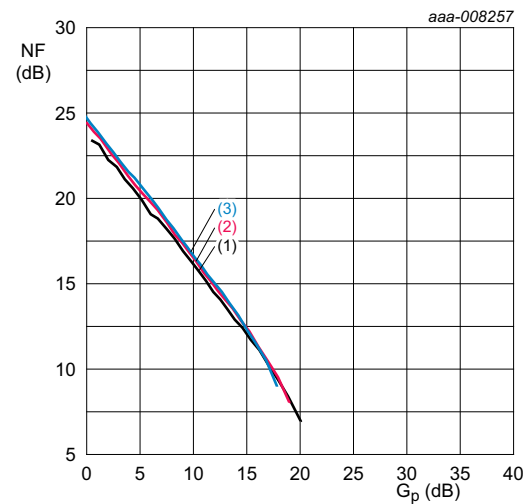
GS1 = HIGH; GS2 = LOW; $V_{CC1} = 5\text{ V}$; $V_{CC2} = 5\text{ V}$; $f = 1750\text{ MHz}$.
(1) $T_{amb} = -40^\circ\text{C}$
(2) $T_{amb} = +25^\circ\text{C}$
(3) $T_{amb} = +85^\circ\text{C}$

Fig 14. Input power at 1 dB gain compression as a function of power gain in low gain mode; typical values



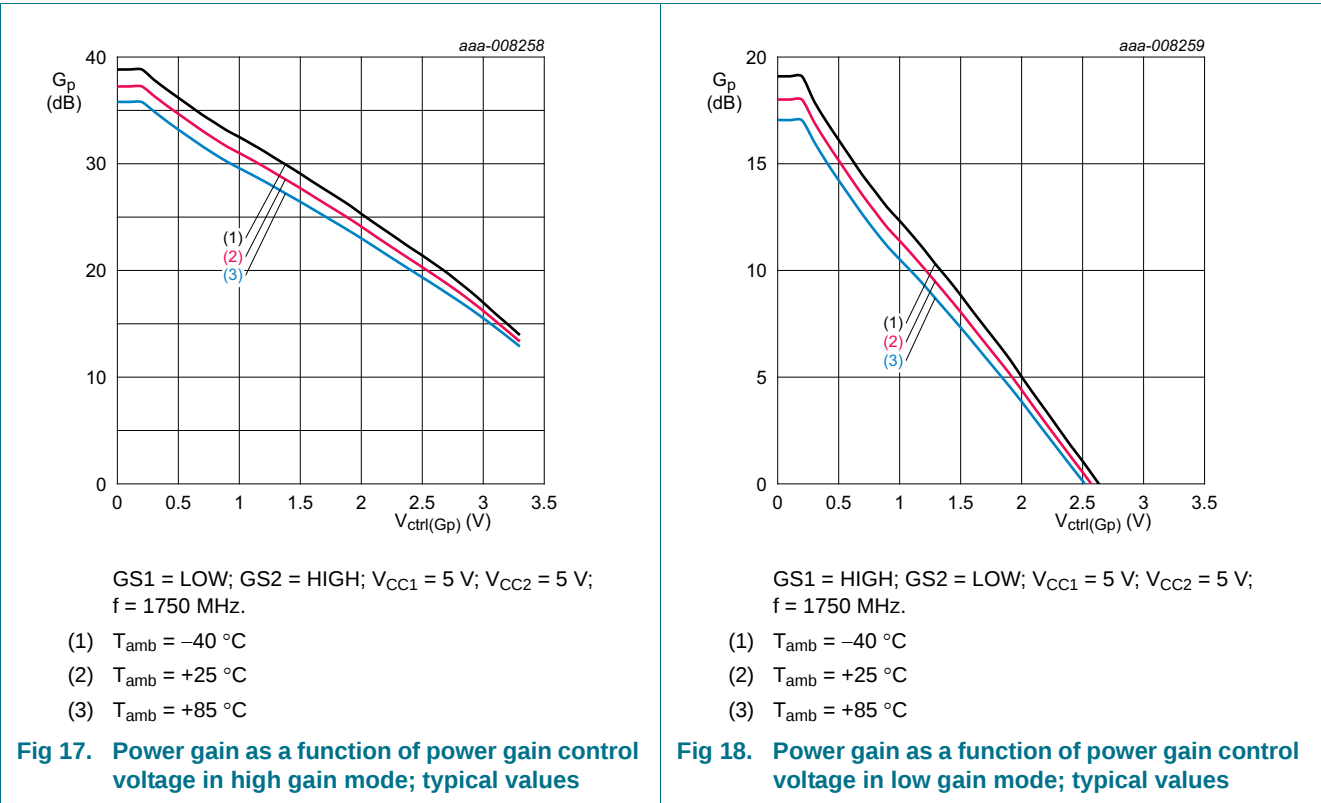
GS1 = LOW; GS2 = HIGH; $V_{CC1} = 5\text{ V}$; $V_{CC2} = 5\text{ V}$; $f = 1750\text{ MHz}$.
(1) $T_{amb} = -40^\circ\text{C}$
(2) $T_{amb} = +25^\circ\text{C}$
(3) $T_{amb} = +85^\circ\text{C}$

Fig 15. Noise figure as a function of power gain in high gain mode; typical values



GS1 = HIGH; GS2 = LOW; $V_{CC1} = 5\text{ V}$; $V_{CC2} = 5\text{ V}$; $f = 1750\text{ MHz}$.
(1) $T_{amb} = -40^\circ\text{C}$
(2) $T_{amb} = +25^\circ\text{C}$
(3) $T_{amb} = +85^\circ\text{C}$

Fig 16. Noise figure as a function of power gain in low gain mode; typical values

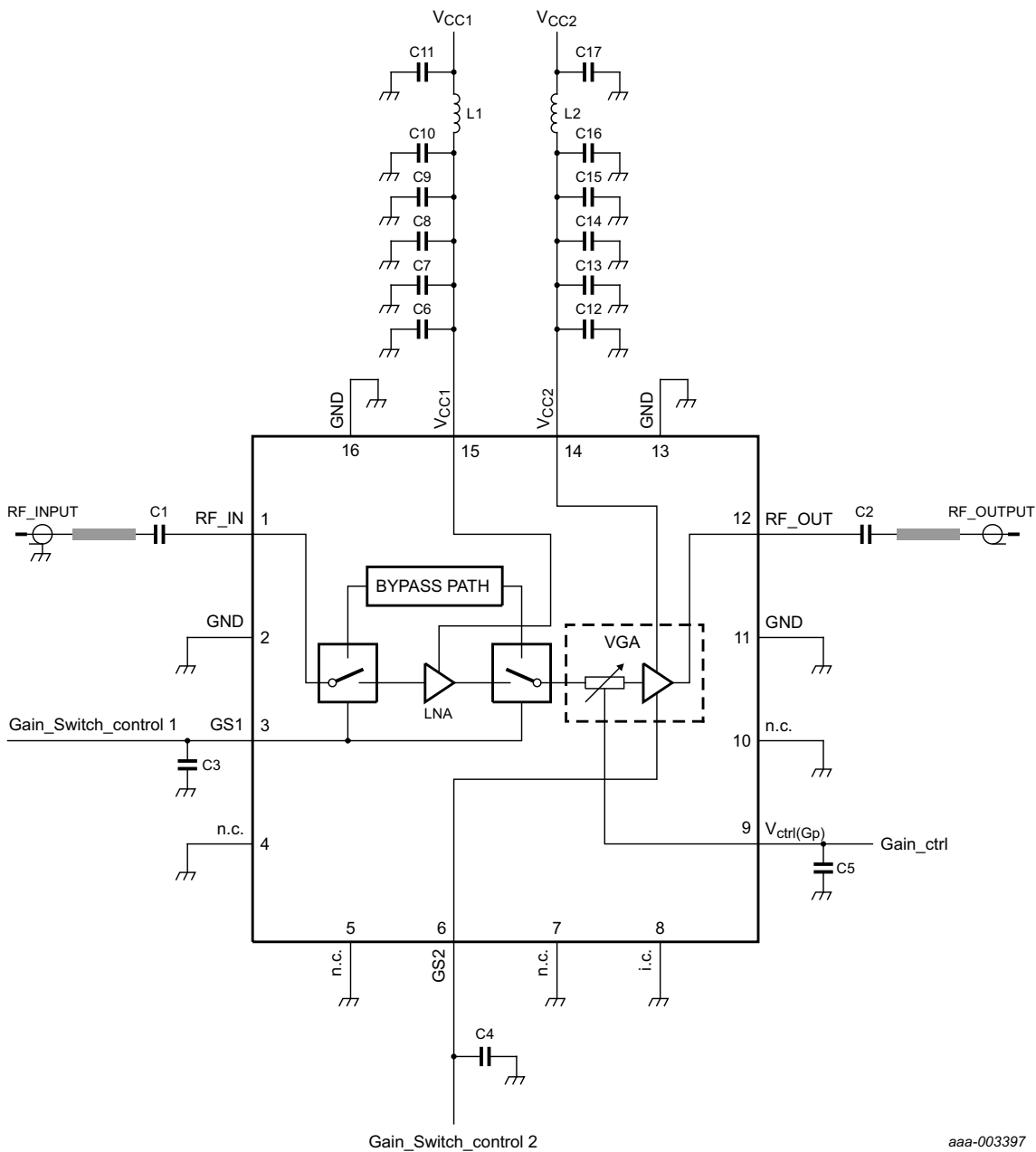


9. Application information

Table 10. List of components
For application circuit see [Figure 19](#).

Component	Description	Value	Remarks
C1, C2	capacitor	1 nF	[1] 0402
C3, C4, C5, C6, C12	capacitor	100 pF	[1] 0402
C7, C8, C9, C10,	capacitor	optional	
C11, C17	capacitor	100 nF	[1] 0402
C13, C14, C15, C16	capacitor	optional	
L1, L2	inductor	10 nH	[2] 0402

[1] Murata GRM1555 series.
[2] Murata LQG15 series.



See [Table 10](#) for a list of components.

Fig 19. Schematic layout for application circuit

10. Package outline

HLQFN16R: plastic thermal enhanced low profile quad flat package; no leads; 16 terminals; body 8 x 8 x 1.3 mm SOT1301-1

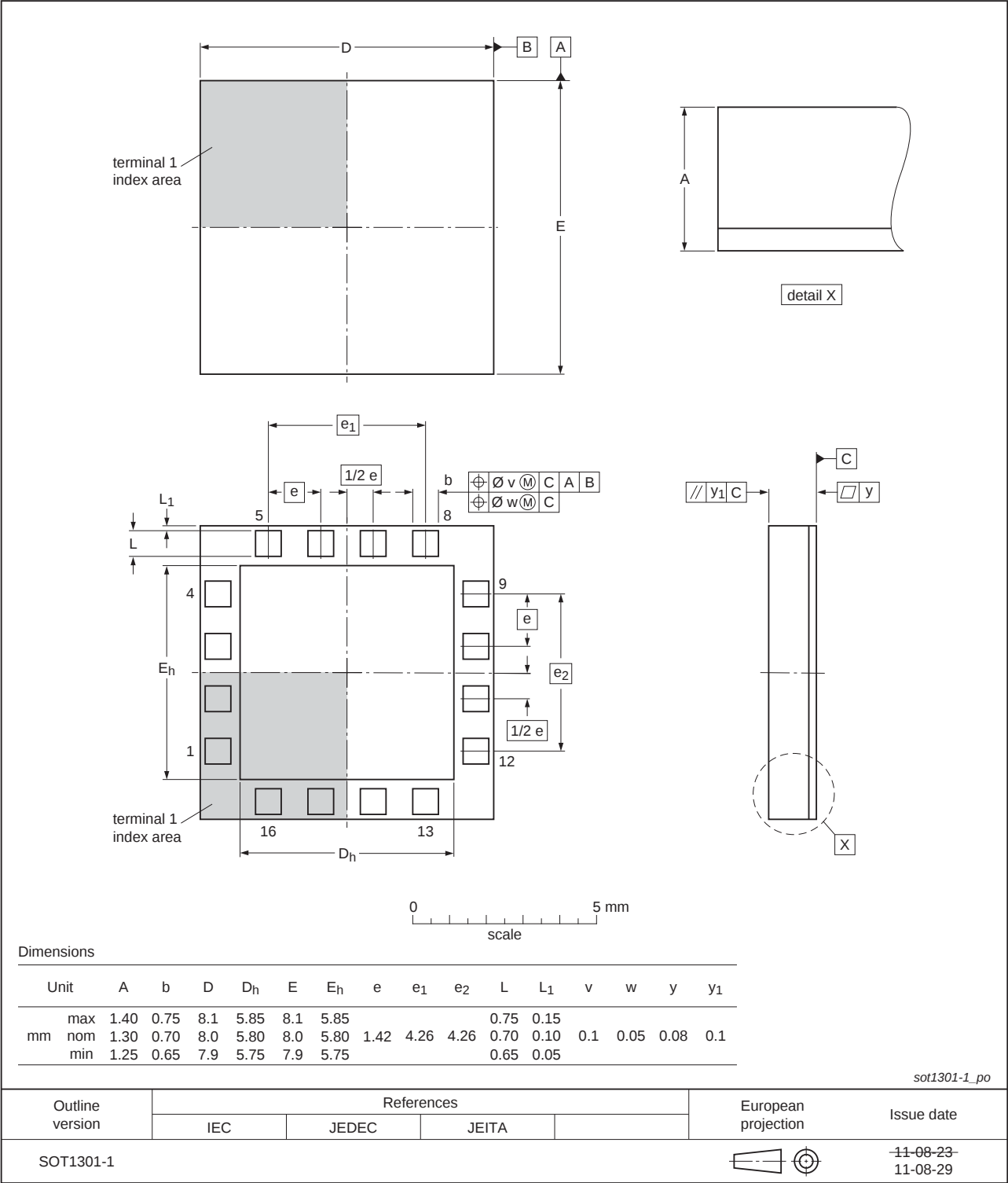


Fig 20. Package outline SOT1301-1 (HLQFN16R)

11. Abbreviations

Table 11. Abbreviations

Acronym	Description
3G	3rd Generation
ESD	ElectroStatic Discharge
LNA	Low Noise Amplifier
LTE	Long Term Evolution

12. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BGU7062N2 v.1	20130708	Product data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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